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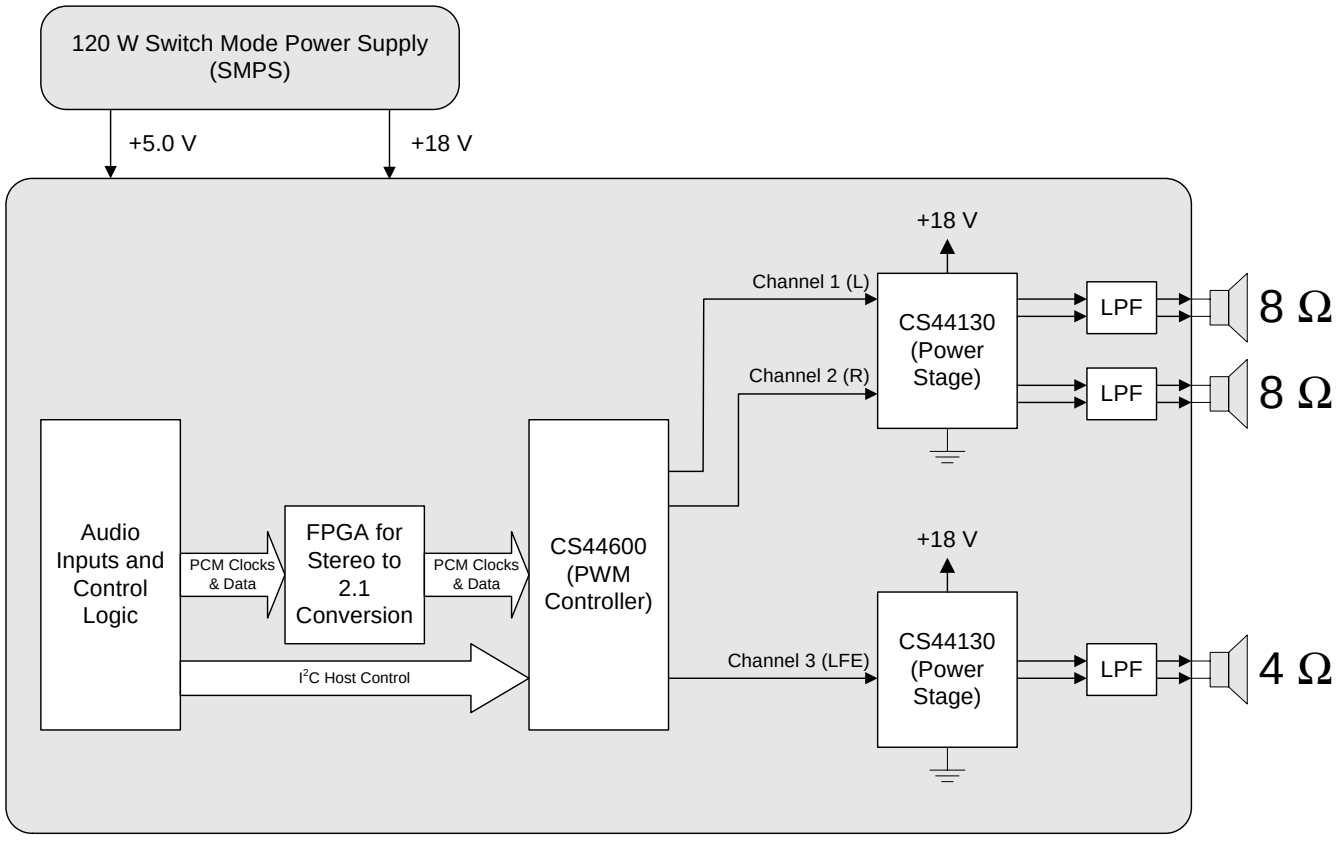
CRD44130-FB

20 W x 2 + 40 W x 1 PWM Amplifier Reference Design

Features

- Two Full-Bridge Channels, 20 W each (@ 10% THD+N)
- One Parallel Full-Bridge Channel, 40 W (@ 10% THD+N)
- < 0.3% THD+N at 12 W
- Thermally Enhanced QFN Package Requires No Heat Sink
- Accepts Analog Audio or S/PDIF Digital Audio Inputs
- Onboard FPGA Converts Stereo Inputs to Properly Filtered 2.1 Outputs
- CS44600 Spread Spectrum Modulation Reduces EMI Emissions
- Thermal, Over-Current, and Under-Voltage Protection
- > 85% Amplifier Efficiency
- Can be operated as a Stand-Alone Board through On-Board Controls or with Windows® Compatible Graphical User Interface
- Demonstrates Recommended Layout and Grounding Arrangements



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General Description

The CRD44130-FB PWM amplifier demonstrates the CS44600 and CS44130 Cirrus Logic's multi-channel all-digital PWM controller and power stage. This reference design implements a multi-channel amplifier that delivers 20 W per channel into 8 Ω loads and 40 W into a 4 Ω load using a single +18 V supply (at 10% THD+N). The CRD44130-FB comes equipped with a 120 W Switch Mode Power Supply (SMPS) for quick demonstration. The CS44130 can operate with power supply levels up to 21 V, delivering up to 32 W into 8 Ω at 10% THD+N or 57 W into 4 Ω when configured as a parallel full-bridge. Additional thermal enhancements may be necessary for continuous power output at voltages greater than +18 V.

As shown in the block diagram on the front page, the CS44600 IC takes three stereo digital audio PCM inputs and converts them to PWM outputs. This 64-pin LQFP PWM controller provides an integrated sample rate converter, volume up/down, speaker load compensation, peak limiting to prevent amplifier clipping, and AM frequency interference elimination. The CRD44130-FB makes use of only 3 of the CS44600's 6 PWM outputs.

This reference design showcases the CS44130, an integrated power stage back-end for digital amplifiers. There are a total of two CS44130's on the CRD44130 board, one configured for full-bridge operation and another for parallel full-bridge. The CS44130 incorporates internal protection circuitry for over-current, under-voltage, and thermal error conditions.

The inductor/capacitor 2nd order low-pass filter (LPF) removes high-frequency components from the output signal effectively converting it from digital to analog.

For complete ordering information, please refer to "Ordering Information" on page 39.

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TABLE OF CONTENTS

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LIST OF FIGURES

LIST OF TABLES

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1. SYSTEM OVERVIEW

The CRD44130-FB reference design is an excellent means for evaluating the CS44130 dual full-bridge power stage. This design includes analog and digital input capability, an FPGA for stereo to 2.1 conversion, a digital Class-D PWM modulator, one stereo full-bridge power stage, and one parallel full-bridge power stage- all on a two-layer board.

The CRD44130-FB schematic set is shown in Figures 5 through 10 and the board layout is shown in Figures 11 through 13.

1.1 CS44600 PWM Modulator

A complete description of the CS44600 is included in the CS44600 product data sheet, located at http://www.cirrus.com.

The CS44600 converts linear PCM data to pulse width modulated (PWM) output. It uses a crystal-based sample rate converter (SRC) to eliminate serial audio interface jitter and maintain a constant PWM switching rate of 384 kHz, resulting in high-quality sound output.

PCM data and clocks are input from either the CS8416 (S/PDIF Receiver) or CS5341 (Stereo ADC).

1.2 CS44130 Power Stage

A complete description of the CS44130 is included in the CS44130 product data sheet, located at http://www.cirrus.com.

The CS44130 is a high-voltage PWM amplifier power stage. It integrates four half-bridge drivers and fault protection. For the CRD44130-FB, one of the CS44130 parts is configured with full-bridge outputs and one is configured with a single parallel full-bridge output. Care should be taken to not connect the black speaker connectors to ground as these outputs are driven.

1.3 Stereo to 2.1 Conversion

The CRD44130-FB includes an FPGA programmed to convert stereo PCM audio data to 2.1 audio. The 2.1 conversion capability is enabled and disabled by pressing push-button S1, and is indicated by LED D14.

When 2.1 is enabled, the J1 speaker outputs will produce midrange and high-frequency audio content for left and right channels. The J2 speaker output will produce low-frequency mono content with a crossover frequency of 120 Hz for use with a subwoofer. Figure 14 on page 28 shows the system frequency response with 2.1 enabled.

When 2.1 is disabled, the J1 speaker outputs will produce full-range audio content for left and right channels, and the J2 speaker output will produce full-range audio content for the left channel only. Figure 15 on page 29 and Figure 16 on page 30 show the system frequency response with 2.1 disabled.

1.4 CS8416 Digital Audio Receiver

The operation of the CS8416 receiver and a discussion of the digital audio interface are described in the CS8416 data sheet, located at http://www.cirrus.com.

The CS8416 converts the S/PDIF data stream into PCM data, which is then supplied to the CS44600. The CS8416 operates in master mode with RMCK = 256*Fs. The digital interface format is set to Left-Justified (24-bit).

D17 (RERR) indicates a S/PDIF receiver error, such as loss of lock or a non-PCM data input.

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S/PDIF input is applied through J11 or J8 (both J11 and J8 cannot be driven simultaneously). When valid S/PDIF data is not applied through J11 or J8, the board will switch to use of the analog inputs through J9 and J10.

1.5 CS5341 Analog-to-Digital Converter

The operation of the CS5341 ADC is described in the CS5341 data sheet, located at http://www.cirrus.com.

The CS5341 converts analog audio into PCM data for the CRD44130-FB. The CS5341 operates in slave mode, and the digital interface format is set to Left-Justified (24-bit).

Analog input is applied through J9 and J10 and is activated only if valid S/PDIF data is not applied through J11 or J8. See Figure 5 on page 15 for analog and digital audio input schematics.

When analog inputs are used, full scale output is achieved when the analog input level is 2.0 Vrms.

1.6 Power Stage Output Filter

The CRD44130-FB includes a 2^{nd} order low-pass filter to remove high-frequency content from the PWM output of each CS44130 device. The output filters for the left and right speaker outputs present at J1 are optimized for 8 Ω speaker loads. The output filter for the low-frequency (LFE) speaker output present at J2 is optimized for 4 Ω loads.

1.7 Power Supply

The CRD44130-FB uses a 120 W Switch Mode Power Supply (SMPS). The supply provides a regulated +18 V for the CS44130 power stages and +5 V for the digital logic.

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2. BOARD CONTROL

The CRD44130 can be used either in Software Mode or Stand-Alone Mode. In Software Mode, the board is connected to a computer via a standard 9-pin RS-232 or a USB Cable. In this mode, all settings on the board are controlled by a Graphic User Interface. In Stand-Alone Mode, the board is controlled by on-board hardware controls including push-buttons, volume knobs, and jumpers.

2.1 Graphic User Interface (GUI) Control

The CRD44130-FB is shipped with a Microsoft Windows-based GUI that allows control over the CS8416 and CS44130 registers. The software can also be downloaded from the Cirrus website at http://www.cirrus.com. Interface to the CRD44130-FB control port is provided using either a RS-232 serial cable or USB cable.

Once the CRD44130-FB is connected to the host PC, and power is connected to the board, FlexLoader.exe is loaded from the directory into which it was installed. Once loaded, all registers are set to their default reset state. The GUI File menu provides the ability to save and restore (load) register settings in the form of script files. Sample script files are provided for basic functionality. The GUI serial port interface is set up by default for 115.2 Kbps operation on COM1. To change these settings, edit the “CRD44130-FB Communications” section of the flexconfig.ini file or change the system communications setting in the Windows control panel.

For more information regarding the GUI interface including operation, version release, and troubleshooting advice, please refer to the flexloader.chm help file located in the Flexloader install directory.

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2.1.1 CS44600 Dialog Tab

The CS44600 Dialog tab provides high-level control over the CS44600's registers. Controls are provided to enable the power stages, control the volume, enable and adjust the limiter function, and configure the GUI for various user preferences.

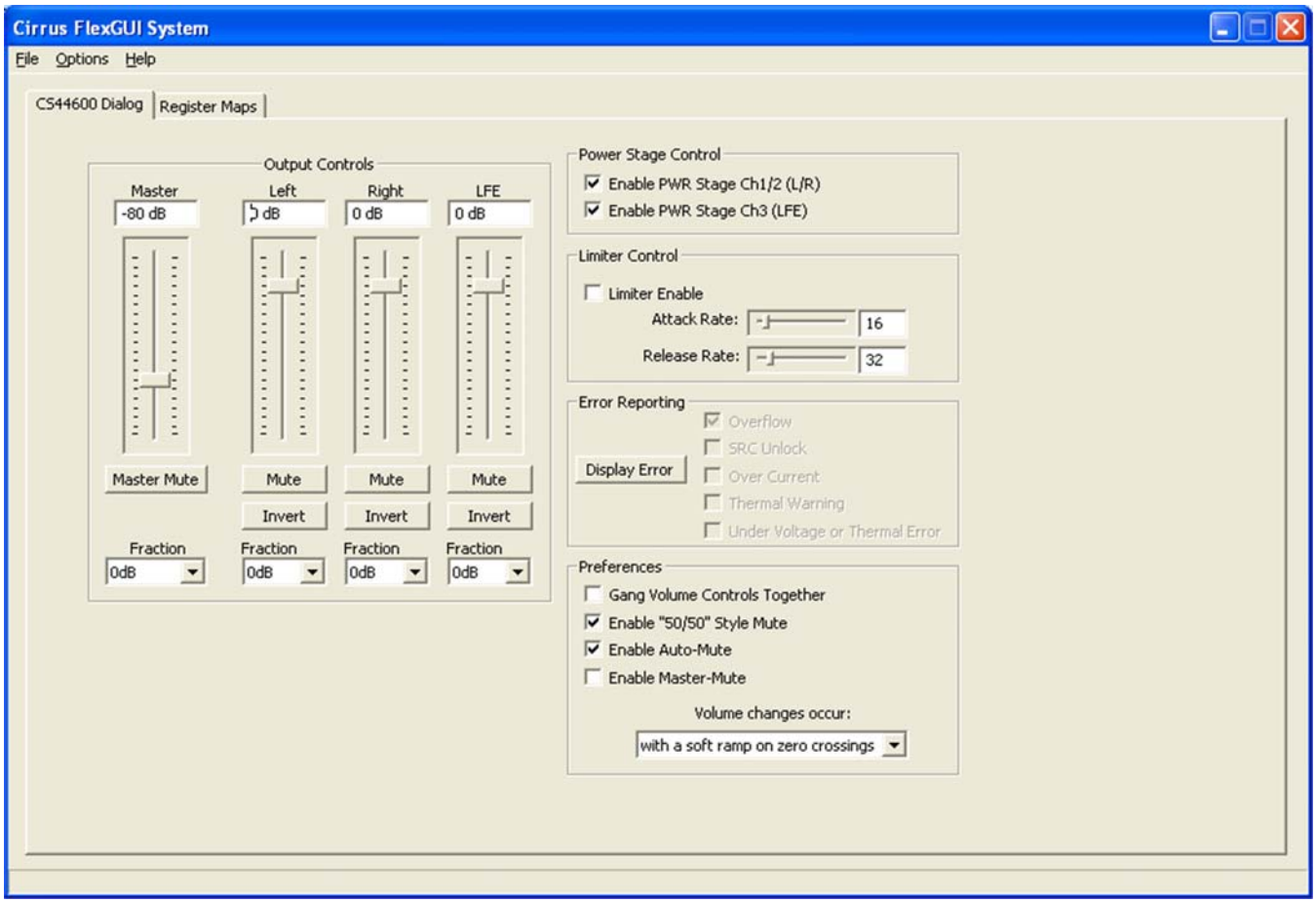

Figure 1. CRD44130-FB Dialog Tab

2.1.2 Advanced Register Debug Tab

The Advanced Register Debug tab provides low-level control over the CS44600 and CS8416 individual register settings. Each device is displayed on a separate tab. Register values can be modified bitwise or bytewise. For bitwise, click the appropriate push-button for the desired bit. For bytewise, the desired hex value can be typed directly into the register address box in the register map.

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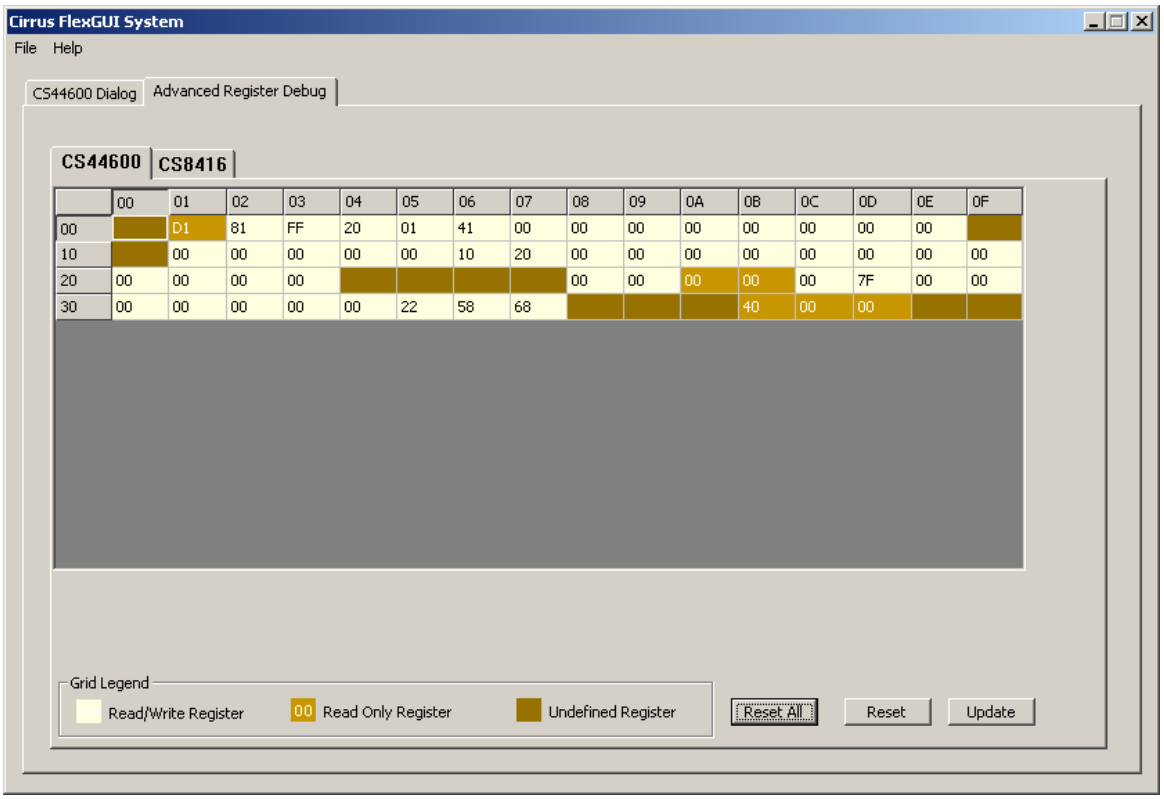

Figure 2. CS44600 Advanced Register Debug Tab

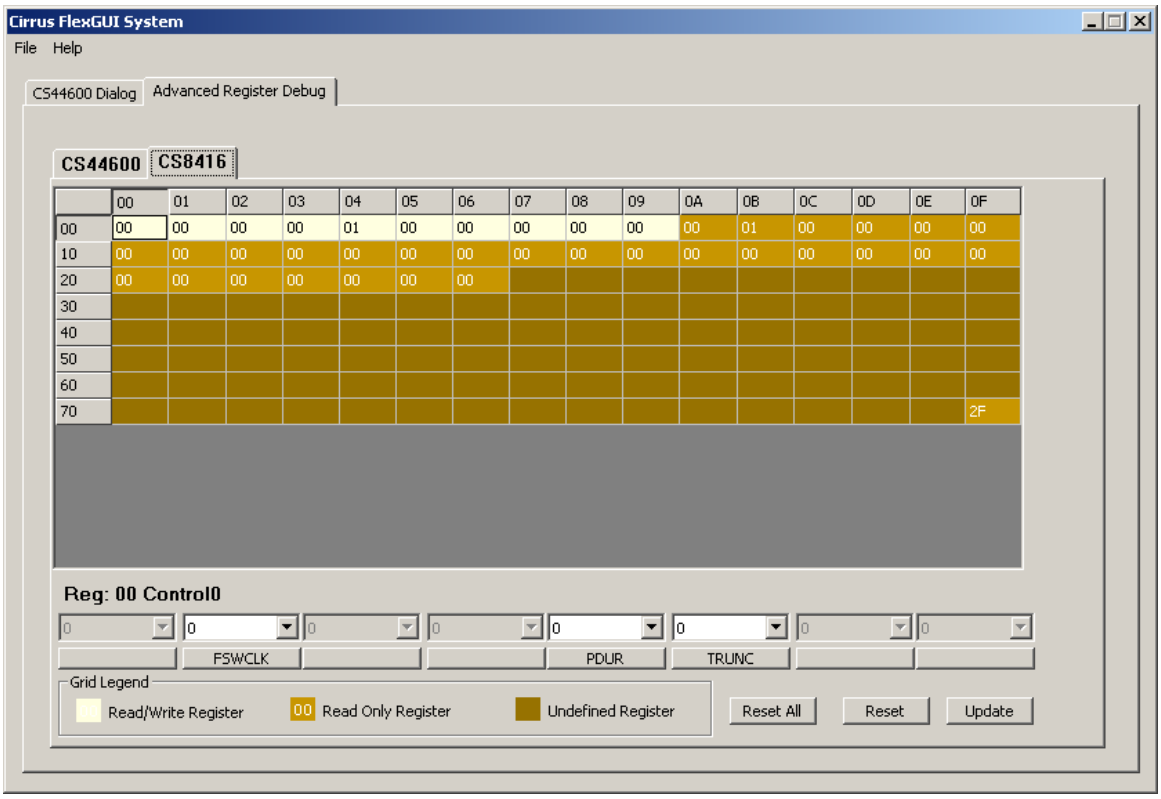

Figure 3. CS8416 Advanced Register Debug Tab

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2.2 Hardware Board Control

The CRD44130-FB provides labeled push-buttons to control mute, Left/Right Channel enable/disable, LFE enable/disable, 2.1 enable/disable, 0 dB gain, and a variable volume control knob. LED's provide user feedback for current board settings.

Volume is controlled by either R35 or J4. If a shunt is placed on J4, the CS44600 master volume register will be forced to 0 dB and volume control R35 will have no effect. If the shunt is removed from J4, R35 will control the CS44600 master volume register, which can be varied from -127 dB to +24 dB in 1 dB increments.

See Table 1 on page 10 for push-button descriptions

.

Push-Button	LED	Label	Description	
			LED On	LED Off
S1	D14	2.1 Enable/Disable	J1 speaker outputs provide midrange and high-frequency Left and Right channel audio content. J2 provides mono, low-frequency audio content (see Figure 14 for filter response).	J1 speaker outputs provide full-range Left and Right channel audio content. J2 provides full-range, Left channel audio content.
S2	D13	Mute/Unmute	All speaker outputs are muted. PWM outputs are 50% duty cycle.	Speaker outputs are not muted.
S3	D16	L/R On/Off	CS44130 power stage U1 is enabled.	CS44130 power stage U1 is held in reset. Left and right channels on J1 will not output audio.
S4	D19	LFE On/Off	CS44130 power stage U2 is enabled.	CS44130 power stage U2 is held in reset. Subwoofer channel on J2 will not output audio.

Table 1. Push-Button Descriptions

2.3 Board Error Handling

2.3.1 Software Mode

If an error condition occurs while the board is operating in Software Mode, the interrupts will not be serviced by the micro-controller as they are in Stand-Alone Mode. If a thermal warning event occurs, it will be ignored, and the board will continue to work as specified by the GUI controls. An over-current, under-voltage, or thermal error condition will cause the CS44130 devices to reset themselves in an attempt to clear the error. If the devices cannot clear the error within a fixed amount of time (approximately 0.5 seconds), they will shut off permanently and will require the user to toggle their reset signals via the power stage enable check-boxes on the GUI. Clicking on the "Display Error" push-button on the GUI allows the user to determine which of the error conditions, if any, is present at any given time.

2.3.2 Stand-Alone Mode

The CS44130 provides signals indicating thermal warning, thermal error, over-current, and under-voltage. A thermal warning will cause the CS44600 to attenuate the audio signal in an attempt to remove the thermal warning condition, after which it will gradually restore the volume to the original setting. An over-current, under-voltage, or thermal error condition will cause the CS44130 devices to reset themselves in an attempt to clear the error. If the devices cannot clear the error within a fixed amount of time (approximately 0.5 seconds), they will shut off permanently and will require the user to toggle their reset signals through push-buttons S3 and S4.

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2.4 Board Connections

2.4.1 Audio Inputs

The CRD44130-FB provides stereo analog and digital inputs. The Analog inputs are J9 (left input) and J10 (right input). When analog inputs are used, full scale output is achieved when the analog input level is 2.0 Vrms. S/PDIF digital input can be either the optical receiver J8 or the RCA connector J11. When a valid PCM S/PDIF digital audio signal is present on J8 or J11 (cannot be present on both simultaneously), the CRD44130-FB outputs the program material present on that digital input. When a valid PCM S/PDIF digital audio signal is not present on either J8 or J11 (or both are mistakenly driven simultaneously), the CRD44130-FB outputs the program material present on its analog inputs. Due to the timing constraints of the FPGA, digital audio inputs must be limited to a sample rates of 32-96 kHz.

2.4.2 Speaker Outputs

The CRD44130-FB provides speaker-level left, right, and low-frequency speaker outputs. Left and right channel output connections are made through speaker terminal J1; and the low-frequency speaker output connection is made through speaker terminal J2. Refer to Figure 4 for speaker connection details.

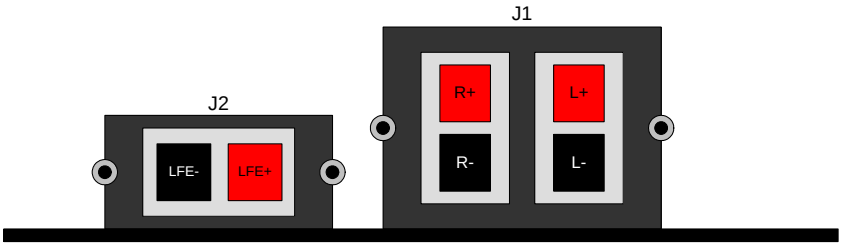

Figure 4. Speaker Output Connections

When LED D14 is lit, this indicates that 2.1 is enabled. This means that the left, right, and low-frequency channels will be filtered according to the frequency response shown in Figure 14. In this mode, the low-frequency channel will be the filtered sum of the left and right channels. When 2.1 is disabled (by pressing push-button S1), the board provides no filtering and the low-frequency output produces full bandwidth left-channel audio.

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3. POWER SUPPLY

3.1 Power Supply Ratings

The required power supply current rating can be estimated as follows. The 12 W (full-bridge) and 24 W (parallel full-bridge) is used as the reference output power per channel because this represents the typical full-scale output with no clipping. Assume the efficiency, η, is approximately 85% (this accounts for power-to-supply control electronics and overhead), then for 12 W x 2 channels + 24 W x 1 channel:

$$P_{Total} = \frac{P_{Out}}{\eta} = \frac{48W}{0.85} \cong 56.5W$$

$$P_{Supply} = \frac{P_{Total}}{2} = \frac{56.5W}{2} = 28.25W$$

Consequently, the supply current is:

$$I_{Supply} = \frac{P_{Supply}}{V_{Supply}} = \frac{28.25W}{18V} \cong 1.57A$$

The factor of 2 in the denominator of P_{Supply} arises from the fact that for typical consumer applications in digital televisions, the power supply should be capable of providing ½ the total requirement for all channels operating at full power. This design guide is still quite conservative, and it provides more than adequate headroom in real applications.

3.2 Power Supply Decoupling

Proper power supply decoupling is one key to maximizing the performance of a Class-D amplifier. Because the design uses an open loop output stage, noise on the power supply rail will be coupled to the output. Referring to Figure 11 on page 21, the top side of the CRD44130-FB PWM amplifier board, good decoupling practice is shown. Notice that the 0.1 µF ceramic capacitors are as close as physically possible to the power pins of the CS44130. The ground side of the capacitors is connected directly to top side ground plane, which is also used by the power supply return pins. This keeps the high-frequency current loop small to minimize power supply variations and EMI. 330 µF electrolytic capacitors are also located in close proximity to the power supply pins to supply the current locally for each channel. These are not required to be expensive low ESR capacitors. General-purpose electrolytic capacitors that are specified to handle the ripple current can be used.

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4. ELECTROMAGNETIC INTERFERENCE (EMI)

This reference design from Cirrus Logic is a board-level solution which is meant to control emissions by minimizing and suppressing them at the source, in contrast to containing them in an enclosure. Utilizing spread spectrum modulation techniques to reduce the overall switching energy, along with a low internal modulator clock frequency of 24.576 MHz, greatly reduces the radiated emissions. These features allow the use of very inexpensive components for coupling the high-frequency noise-to-chassis ground. No common mode chokes, inductors, or power line filters were required.

The EMI requirements for an amplifier have added dimensions beyond those imposed on power supplies. Audio amplifiers are usually located in close proximity to radio receivers, particularly AM receivers which are notoriously sensitive to interference. Amplifiers also need to operate with speaker leads of unpredictable length and construction which make it possible for any high-frequency currents that appear on the outputs to generate nuisance emissions.

4.1 Suppression of EMI at the Source

Several techniques are used in the circuit design and board layout of the CRD44130-FB to minimize high-frequency fields in the immediate vicinity of the high power components. Specific techniques include the following:

- As was mentioned in Section 3.2, effective power supply decoupling of high-frequency currents and minimizing the loop area of the decoupling loop is one aspect of minimizing EMI.
- Each output of the CS44130 includes “snubbing” components. For example, the PWM outputs of U1 and U2 include snubber components R7, R8, and R9 (20 Ω); and C32, C34, and C36 (330 pF). These components serve to damp ringing on the switching outputs in the 30-50 MHz range. The snubbing components should be as close as practical to the output pins to maximize their effectiveness. Again, refer to Figure 11 for the preferred component layout.
- A separate ground plane with a capacitively coupled electrical connection to the chassis and which surrounds the speaker output connector should be implemented. This allows the speaker outputs to be AC coupled to the chassis just before they exit the chassis from the speaker connector. Again, refer to Figure 11 for the preferred component layout.
- Make use of source termination resistors on all digital signals whose traces are longer than approximately 25 mm (1 inch).

It is extremely critical that the layout of the power amplifier section of the Cirrus Logic CRD44130-FB reference design be copied as exactly as possible to assure best RF/EMI performance.

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5. ERRATA

To avoid over-current errors, the volume control on the CRD44130-FB Rev. B is limited to -2 dBFS.

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6. CRD44130-FB SCHEMATICS

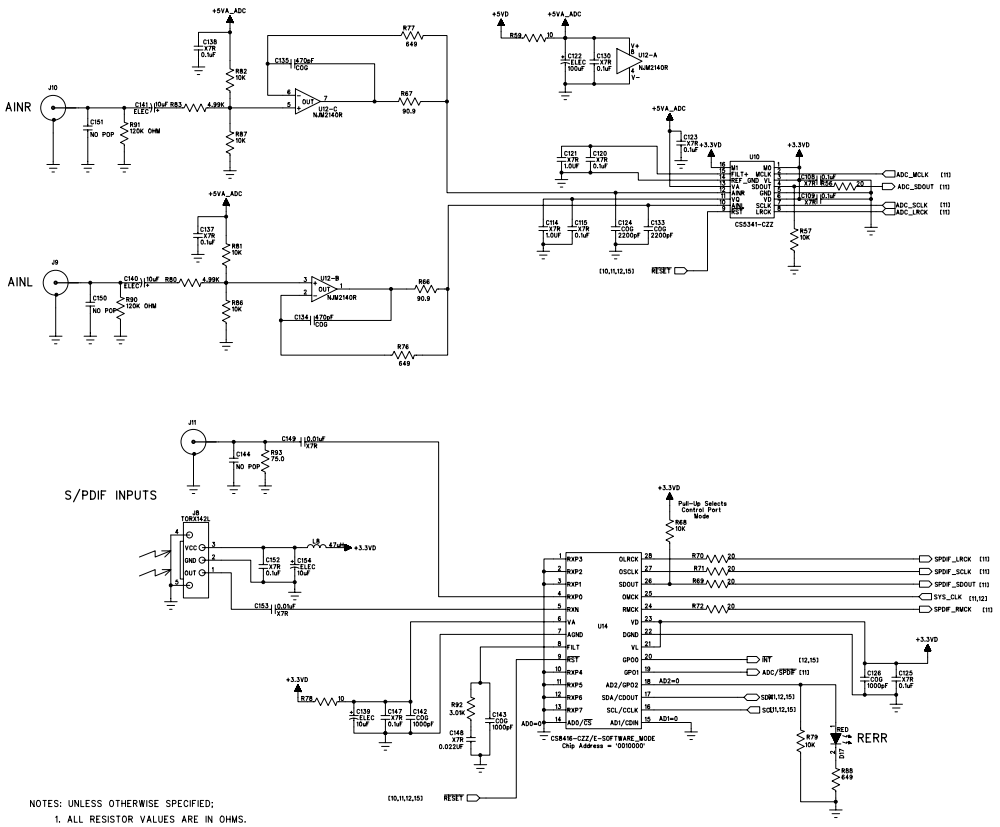

Figure 5. Audio Inputs

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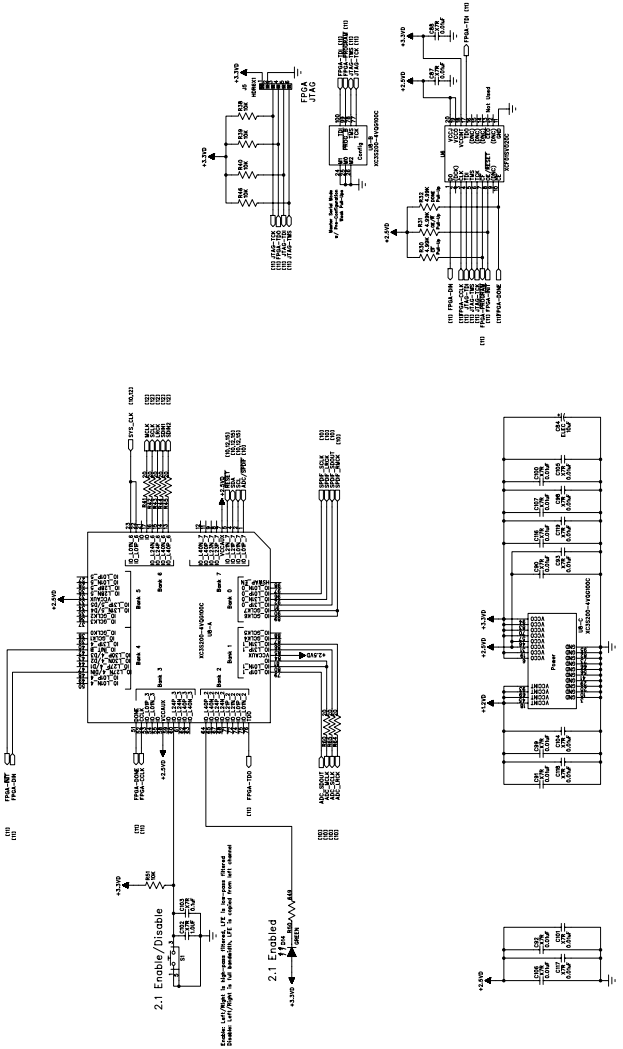

Figure 6. FPGA

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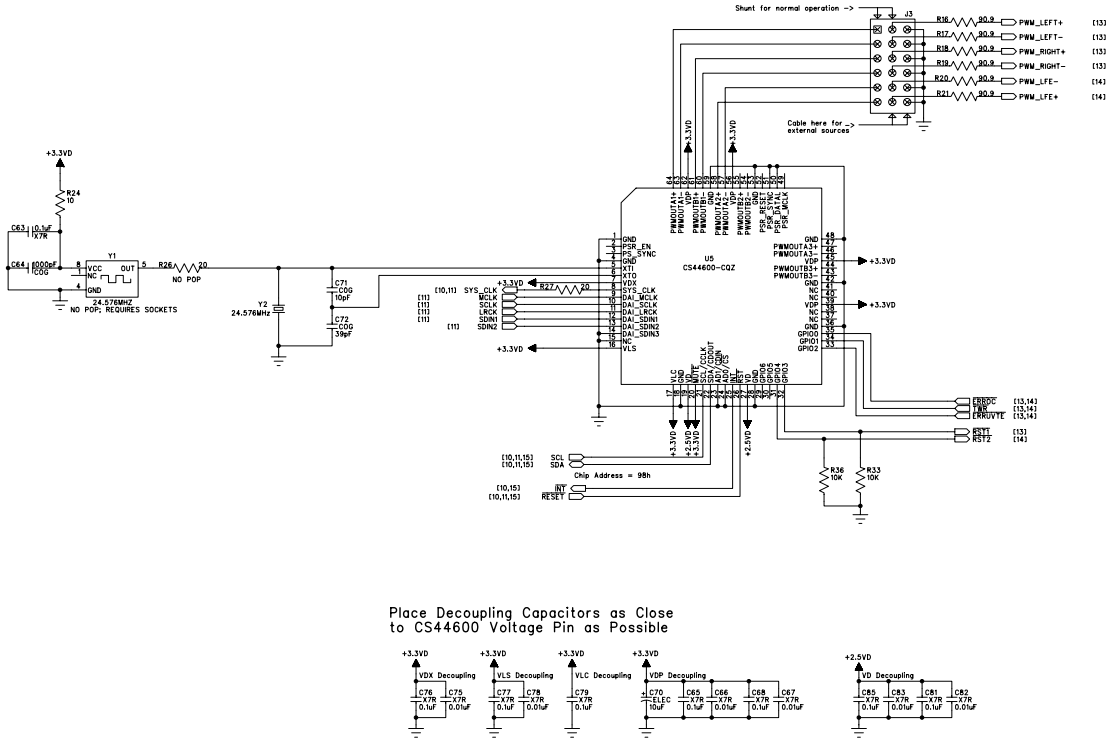

Place Decoupling Capacitors as Close to CS44600 Voltage Pin as Possible

Figure 7. CS44600

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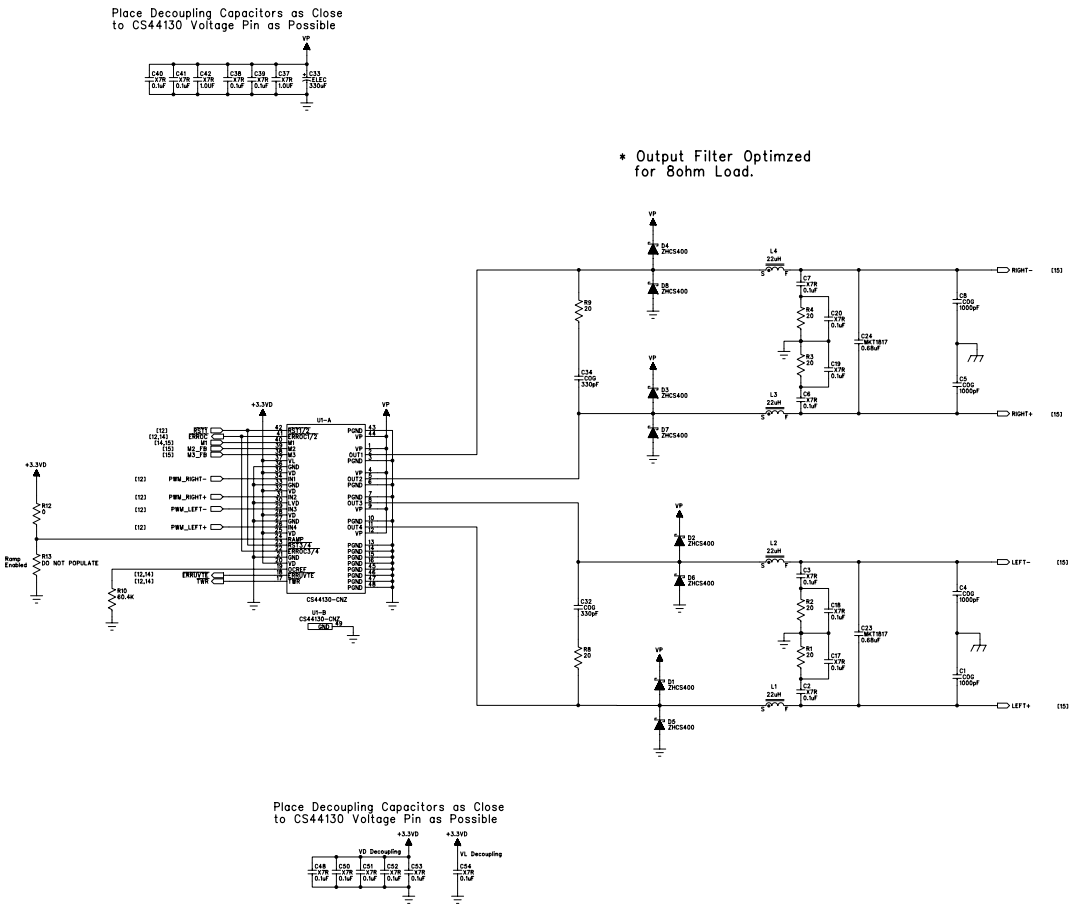

Figure 8. CS44130, Left/Right Channel Outputs

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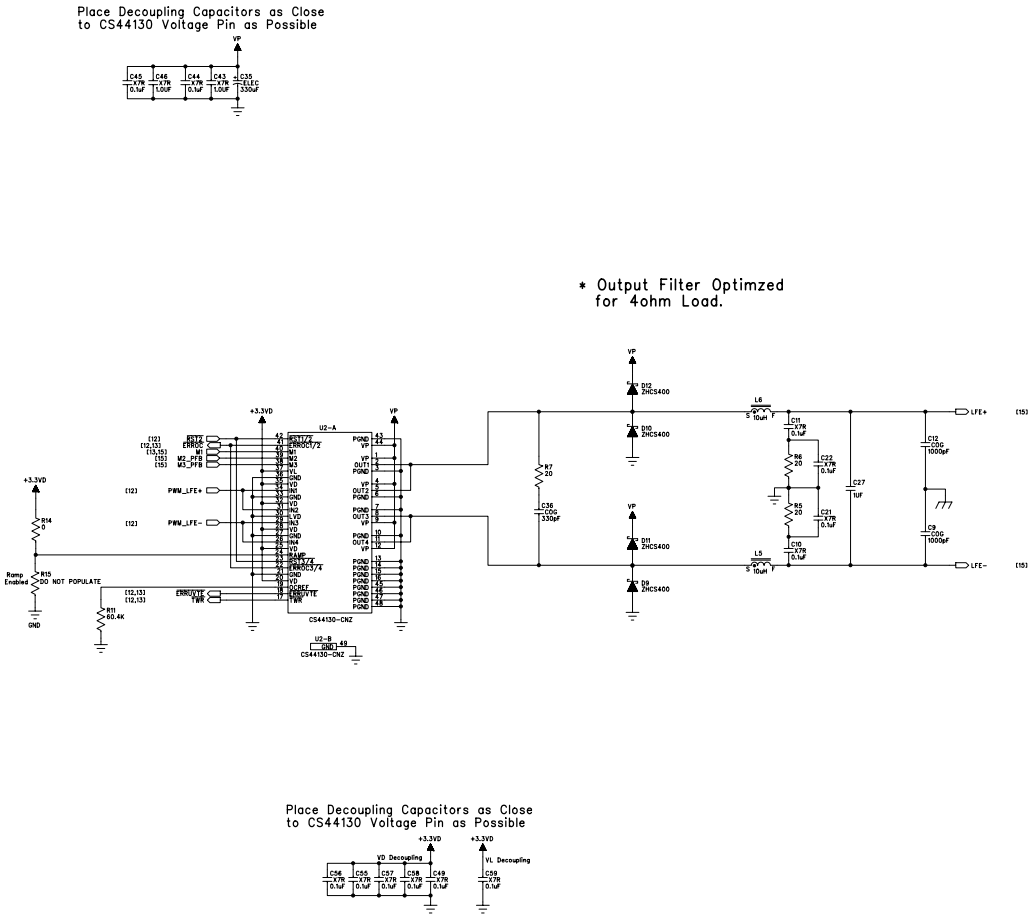

Figure 9. CS44130, LFE Channel Output

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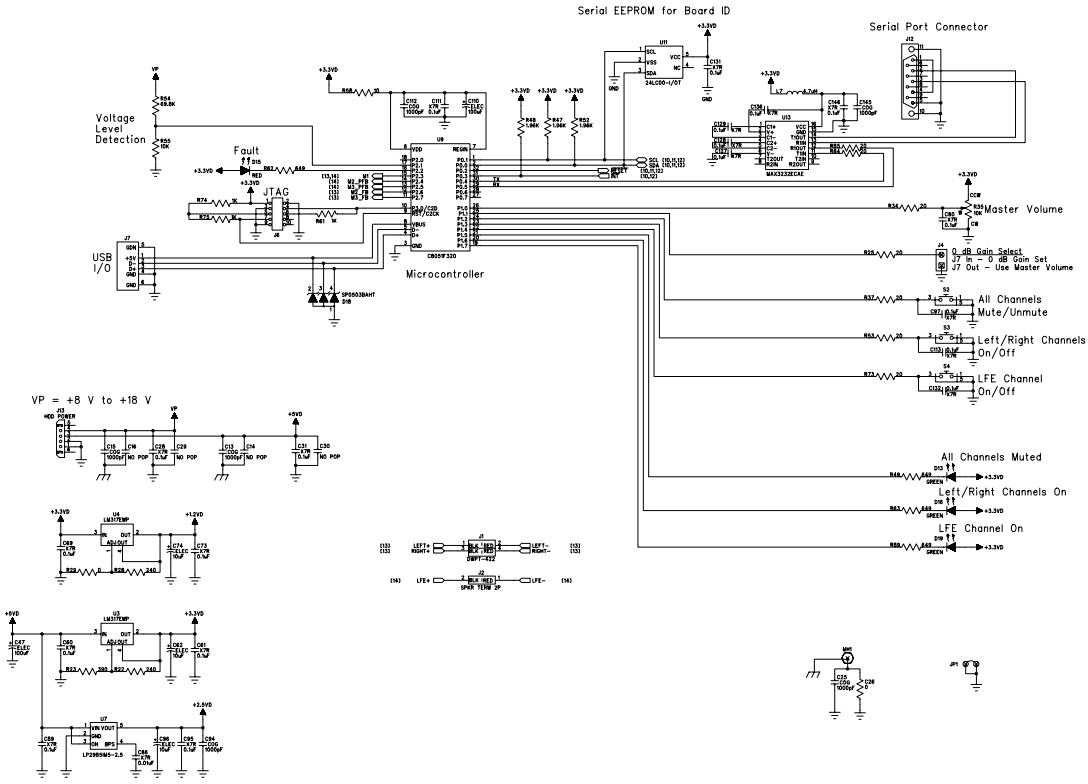

Figure 10. Micro-Controller and Power

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7. CRD44130-FB LAYOUT

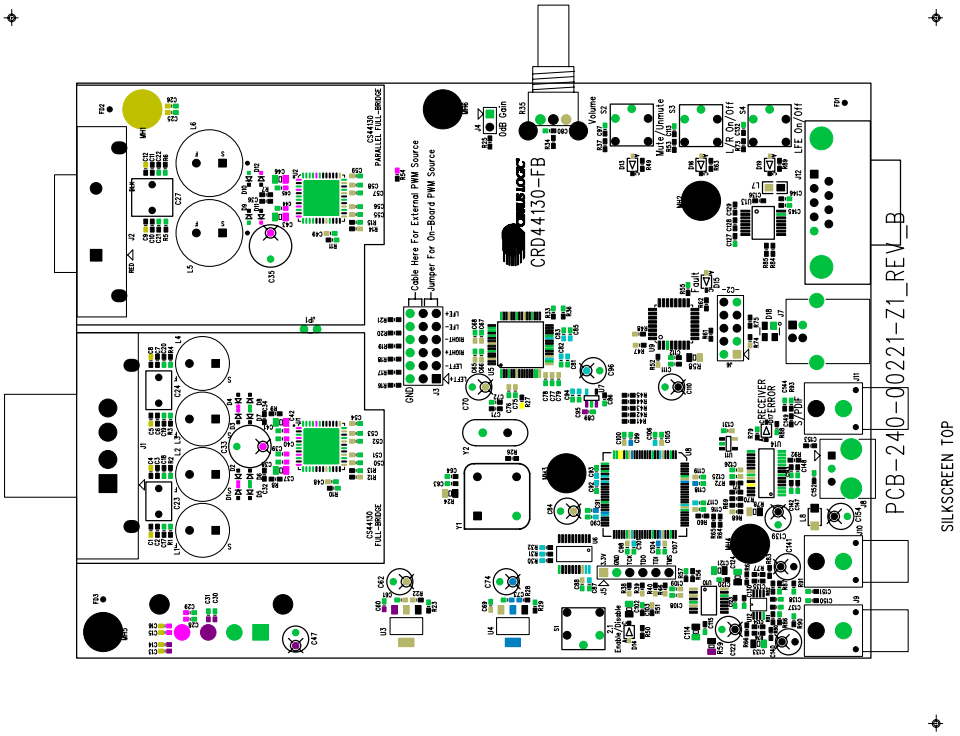

Figure 11. Silk Screen Top

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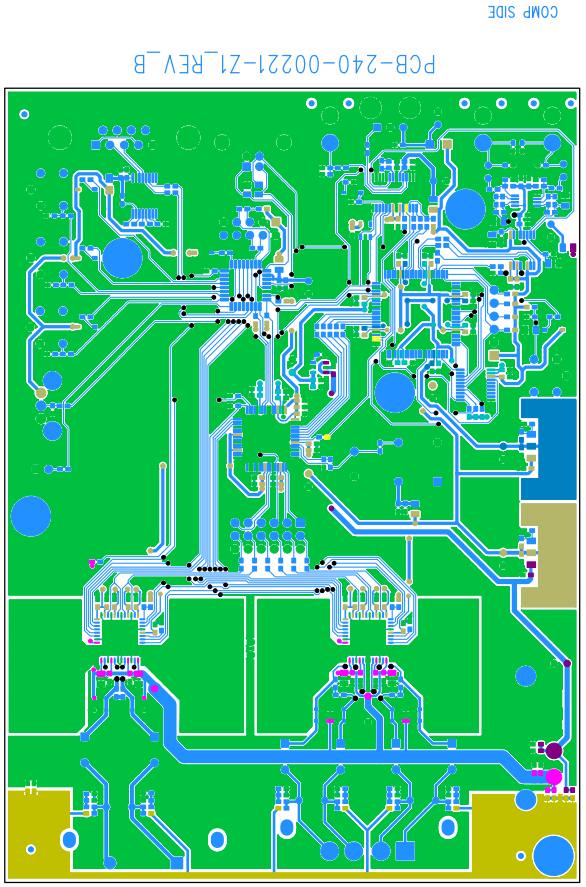

Figure 12. Top Layer

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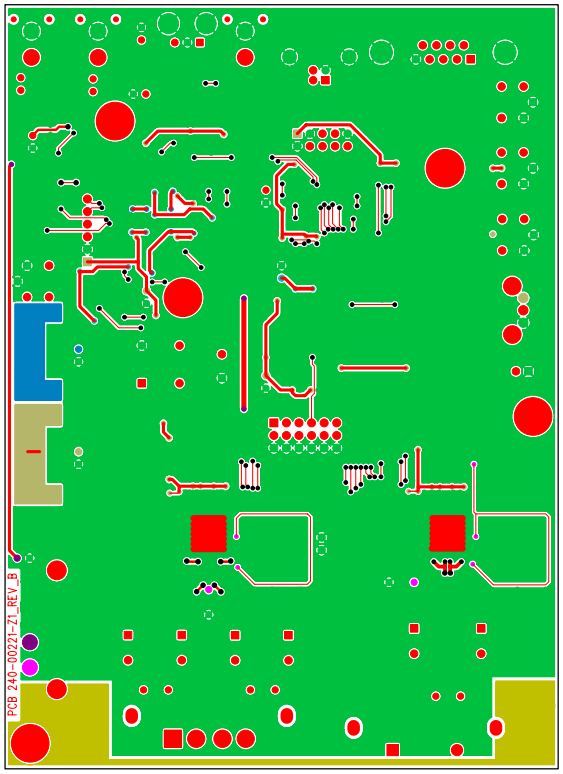

Figure 13. Bottom Layer

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8. CRD44130-FB BILL OF MATERIALS

Item	Description	Qty	Reference Designator	MFG	MFG P/N
1	CAP 1000pF 5% 50V C0G NPb 0603	16	C1 C4 C5 C8 C9 C12 C13 C15 C25 C64 C94 C112 C126 C142 C143 C145	PANASONIC	ECJ1VC1H102J
2	CAP 0.1uF 10% 25V X7R 0603	69	C2 C3 C6 C7 C10 C11 C17 C18 C19 C20 C21 C22 C28 C31 C38 C39 C40 C41 C44 C45 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C63 C65 C68 C69 C73 C76 C77 C79 C80 C81 C85 C89 C95 C97 C103 C108 C109 C111 C113 C115 C120 C123 C125 C127 C128 C129 C130 C131 C132 C136 C137 C138 C146 C147 C152	KEMET	C0603C104K3RAC
3	NO POP CAP 0603	7	C14 C16 C29 C30 C144 C150 C151	NO POP	NP-CAP-0603
4	CAP 0.68uF 5% 63V POLY RAD	2	C23 C24	ROEDERSTEIN	MKT 1817-468-064
5	CAP 1uF 5% 50V MTL FLM RAD	1	C27	PANASONIC	ECQV1H105JL
6	CAP 330PF 5% 50V C0G 0603	3	C32 C34 C36	KEMET	C0603C331J5GAC
7	CAP 330uF 20% 25V ELEC RAD	2	C33 C35	PANASONIC	ECA1EM331B
8	CAP 1uF 10% 25V X7R 0805	7	C37 C42 C43 C46 C102 C114 C121	TDK	C2012X7R1E105K
9	CAP 100uF 20% 10V ELEC RAD 5X11	3	C47 C110 C122	PANASONIC	ECA1AM101
10	CAP 10uF 20% 50V ELEC RAD	9	C62 C70 C74 C84 C96 C139 C140 C141 C154	PANASONIC	ECA1HM100I
11	CAP 0.01uF 10% 25V X7R 0603	27	C66 C67 C75 C78 C82 C83 C86 C87 C88 C90 C91 C92 C93 C98 C99 C100 C101 C104 C105 C106 C107 C116 C117 C118 C119 C149 C153	KEMET	C0603C103K3RAC
12	CAP 10pF 0.5pF 50V C0G 0603	1	C71	PANASONIC	ECJ1VC1H100D
13	CAP 39pF 5% 50V C0G 0603	1	C72	KEMET	C0603C390J5GAC
14	CAP 2200pF 5% 50V C0G 0805	2	C124 C133	KEMET	C0805C222J5GAC
15	CAP 470pF 5% 50V C0G 0603	2	C134 C135	KEMET	C0603C471J5GAC
16	CAP 0.022uF 5% 50V X7R NPb 0603	1	C148	KEMET	C0603C223J5RAC
17	DIODE SCHTKY 40V 6.75A SOD323	12	D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12	ZETEX	ZHCS400
18	"LED CLR GRN, 2.1V 1mA .16MCD, SMD"	4	D13 D14 D16 D19	CHICAGO MINIATURE	CMD28-21VGC/TR8/T1
19	LED CLR SUP RED 1.7V 1mA 1.6MCD SMD	2	D15 D17	CHICAGO MINIATURE	CMD28-21SRC/TR8/T1

Table 2. Bill of Materials

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Item	Description	Qty	Reference Designator	MFG	MFG P/N
20	DIODE ARRAY 5V (TVS) ESD SOT143	1	D18	LITTLE FUSE	SP0503BAHT
21	CON 2x2 SPKR TERMINAL WITH BACK COV	1	J1	DRAGON CITY INDUSTRIES	PT-422P-03
22	CON 2X1 SPKR TERM RA TH	1	J2	DRAGON CITY INDUSTRIES	PT-223
23	"HDR 6x3 ML .1"" 062BD S GLD TH"	1	J3	SAMTEC	TSW-106-07-G-T
24	"HDR 2x1 ML .1"" CTR 062BD ST GLD TH"	1	J4	SAMTEC	TSW-102-07-G-S
25	HDR 6x1 ML ST 2.54MM GLD TH	1	J5	SAMTEC	TSW-106-07-G-S
26	"HDR 5x2 MLE .1"" CTR S GLD"	1	J6	SAMTEC	TSW-105-07-G-D
27	CON RA USB BLK	1	J7	AMP	787780-1
28	OPT RCVR 192kHz 25Mb/s 3.3V 5M	1	J8	TOSHIBA	TORX142L
29	JACK RCA RA-BLK PHONO GLD TABS	3	J9 J10 J11	A/D ELECTRON-ICS	ARJ-2018-NIL-1-NIL
30	"CON DSUB 9P FML .318"" W W/ BDLCK RA"	1	J12	AMP	747844-6
31	"HDR 4X1 ML .200"" TIN PWR RA TH"	1	J13	MOLEX	531130410
32	"WIRE, JUMPER 2P, 0.1"" CTR, BRASS"	1	JP1	COMPONENTS CORPORATION	TP-101-10
33	IND 22uH 3.5A 15% 413 DIA TH	4	L1 L2 L3 L4	TRANSTEK MAGNETICS	TMP50612CT
34	IND 10uH 7A 10% 400 DIA TH	2	L5 L6	TRANSTEK MAGNETICS	TMP50626CT
35	IND 4.7uH 30mA@10MHz 10% 0805	1	L7	TDK	MLF2012A4R7K
36	IND 47uH 10% 1210	1	L8	PANASONIC	ELJFA470KF
37	"SPCR, STANDOFF 4-40 THR, 0.875""L"	6	MH1 MH2 MH3 MH4 MH5 MH6	KEYSTONE	1809
38	RES 20 OHM 1/10W 5% 0603 FILM	30	R1 R2 R3 R4 R5 R6 R7 R8 R9 R25 R27 R34 R37 R41 R42 R43 R44 R45 R53 R56 R60 R64 R65 R69 R70 R71 R72 R73 R84 R85	DALE	CRCW0603200J
39	RES 120k OHM 1/10W 5% 0603 FILM	4	R10 R11 R90 R91	DALE	CRCW0603124J
40	NO POP RES 0603	0	R12 R14	NO POP	NP-RES-0603
41	RES 0 OHM 1/10W 5% 0603 FILM	4	R13 R15 C26 R29	DALE	CRCW0603000Z

Table 2. Bill of Materials (Continued)

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Item	Description	Qty	Reference Designator	MFG	MFG P/N
42	RES 90.9 OHM 1/10W 1% 0603 FILM	8	R16 R17 R18 R19 R20 R21 R66 R67	DALE	CRCW060390R9F
43	RES 240 OHM 1/10W 5% 0603 FILM	2	R22 R28	DALE	CRCW0603241J
44	RES 390 OHM 1/10W 5% 0603 FILM	1	R23	DALE	CRCW0603391J
45	RES 10 OHM 1/8W 5% 0805 FILM	4	R24 R58 R59 R78	DALE	CRCW0805100J
46	RES 20 OHM 1/10W 5% 0603 FILM	0	R26	DALE	CRCW0603200J
47	RES 4.99k OHM 1/10W 1% 0603 FILM	5	R30 R31 R32 R80 R83	DALE	CRCW06034991F
48	RES 10k OHM 1/10W 1% 0603 FILM	15	R33 R36 R38 R39 R40 R46 R51 R55 R57 R68 R79 R81 R82 R86 R87	DALE	CRCW06031002F
49	"POT, 10k LNR TAPER, 9MM ROTARY VERT"	1	R35	PANASONIC	EVUE2JFK4B14
50	RES 1.96k OHM 1/10W 1% 0603 FILM	3	R47 R48 R52	DALE	CRCW06031961F
51	RES 649 OHM 1/10W 1% 0603 FILM	8	R49 R50 R62 R63 R76 R77 R88 R89	DALE	CRCW06036490F
52	RES 69.8k OHM 1/10W 1% 0603 FILM	1	R54	DALE	CRCW06036982F
53	RES 1k OHM 1/10W 5% 0603 FILM	3	R61 R74 R75	DALE	CRCW0603102J
54	RES 3.01k OHM 1/10W 1% 0603 FILM	1	R92	DALE	CRCW06033011F
55	RES 75 OHM 1/10W 1% 0603 FILM	1	R93	DALE	CRCW060375R0F
56	SWT 0/1 TACT W/ESD	4	S1 S2 S3 S4	C&K	PTS645TL50
57	IC CRUS QUAD HALF DIG AMP NPb QFN48	2	U1 U2	CIRRUS LOGIC	CS44130-CNZ/A0
58	"IC LNR, 3TERM V REG ADJ SOT-223"	2	U3 U4	NATIONAL SEMICONDUC-TOR	LM317EMP
59	IC CRUS 6CH DIG AMP CTRL NPb LQFP64	1	U5	CIRRUS LOGIC	CS44600-CQZ/B
60	IC DIG IN-SYS PROG PROM TSSOP20	1	U6	XILINX	XCF01SVO20C
61	IC LNR VREG PWR 150MA 2.5V SOT23-5	1	U7	NATIONAL SEMICONDUC-TOR	LP2985IM5-2.5
62	IC DIG SPARTAN 3 NPb FPGA100	1	U8	XILINX	XC3S200-4VQG100C
63	IC PGM USB 16kB FLASH MCU LQFP32	1	U9	CYGNAL	C8051F320

Table 2. Bill of Materials (Continued)

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Item	Description	Qty	Reference Designator	MFG	MFG P/N
64	IC CRUS 105dB 192kHz M-BIT AUD ADC	1	U10	CIRRUS LOGIC	CS5341-CZZ/E
65	IC PGM 128 BIT SER EEPROM SOT23-5	1	U11	MICROCHIP	24LC00-I/OT
66	IC LNR DUAL OP AMP LOW V RRO VSP8	1	U12	NJR	NJM2140R
67	IC LNR 3-5V RS232 DVR/RCVR SSOP16	1	U13	MAXIM	MAX3232ECAE
68	IC CRUS DIG AUD RCVR NPb TSSOP28	1	U14	CIRRUS LOGIC	CS8416-CZZ/E
69	OSC 24.576MHz 50PPM 5V HALF DIP8	0	Y1	CAL CRYSTAL	CX21AH-24.576MHZ
70	XTL 24.576MHZ HC-49S 30ppm 20pF	1	Y2	ECS	ECS-245.7-20-4
71	"SCREW 4-40X5/16"" PH STEEL"	6	XMH1 XMH2 XMH3 XMH4 XMH5 XMH6	BUILDING FAS-TENERS	PMS 440 0031 PH
72	SCHEM CRD44130-FB AMP	REF		CIRRUS LOGIC	600-00221-01
73	PCB CRD44130-FB	1		CIRRUS LOGIC	240-00221-Z1
74	ASSY DWG PWA CRD44130-FB	REF		CIRRUS LOGIC	603-00221-01
75	"SKT 1P .100""L .041""DIA GLD"	4	XY1 (4 PINS)	AUGAT	8134-HC-5P2
76	KNOB CONVENTIONAL PUSH-ON	1	XR35	SELCO PROD-UCTS	DCN-150006
77	KNOB COVER PUSH-ON 15MM W/ LINE	1	XXR35	SELCO PROD-UCTS	C151
78	INSULATOR .312 x .145 FOR HC49U/US	1	XY2	ECS	700-9001

Table 2. Bill of Materials (Continued)

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9. TYPICAL PERFORMANCE PLOTS

These performance plots were taken with the CRD44130-FB powered from the described +18 V SMPS power supply.

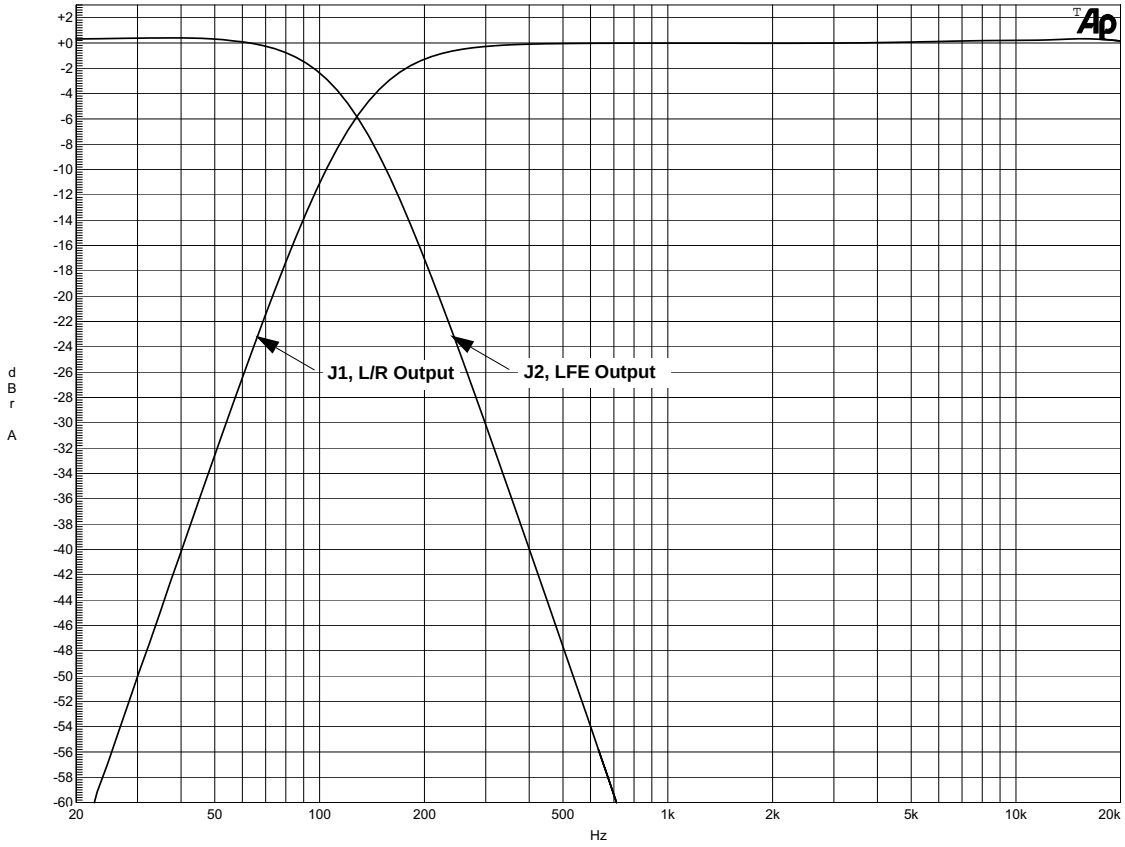

Figure 14. Frequency Response (2.1 Enabled)

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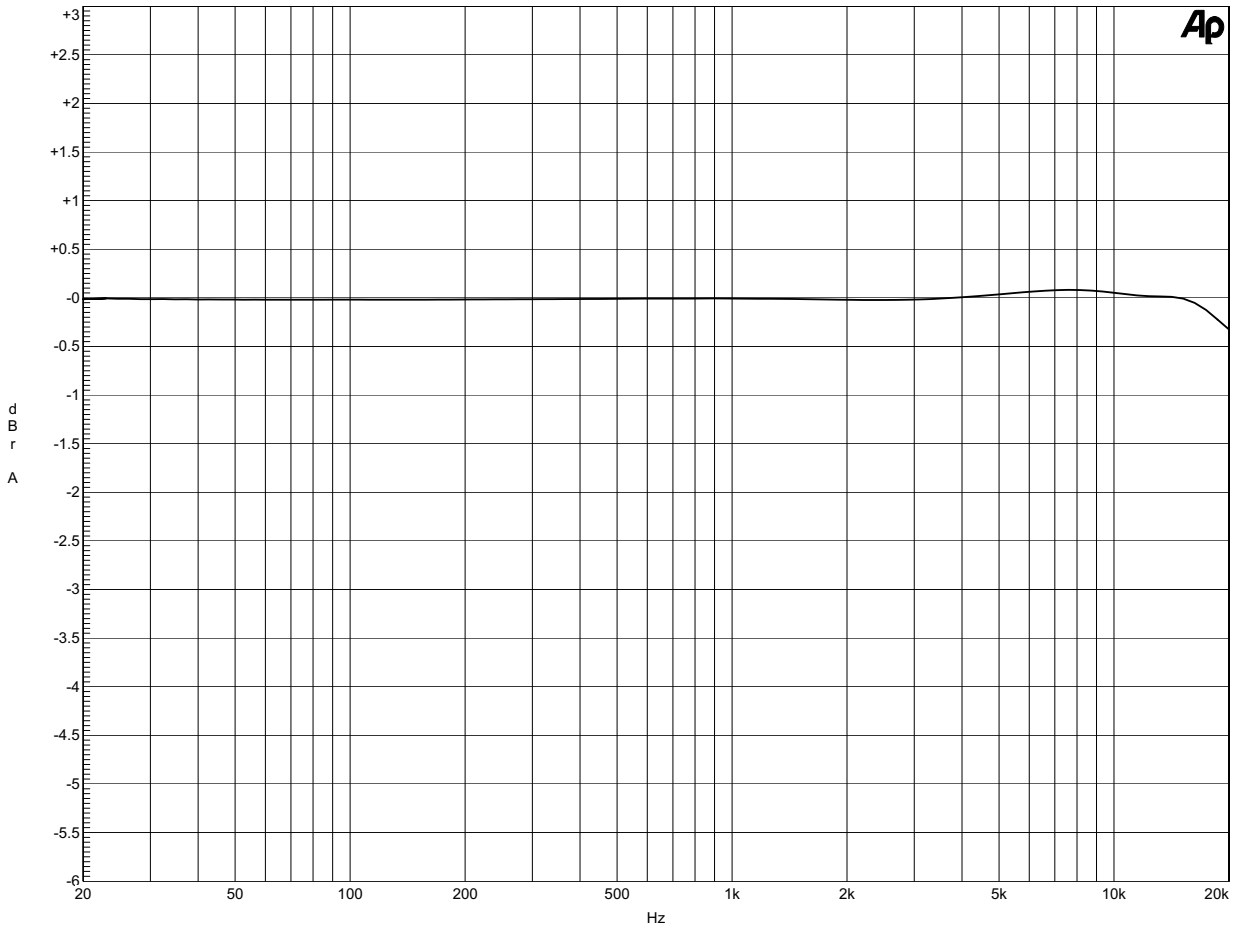

Figure 15. Frequency Response - J1, L/R Output (2.1 Disabled)

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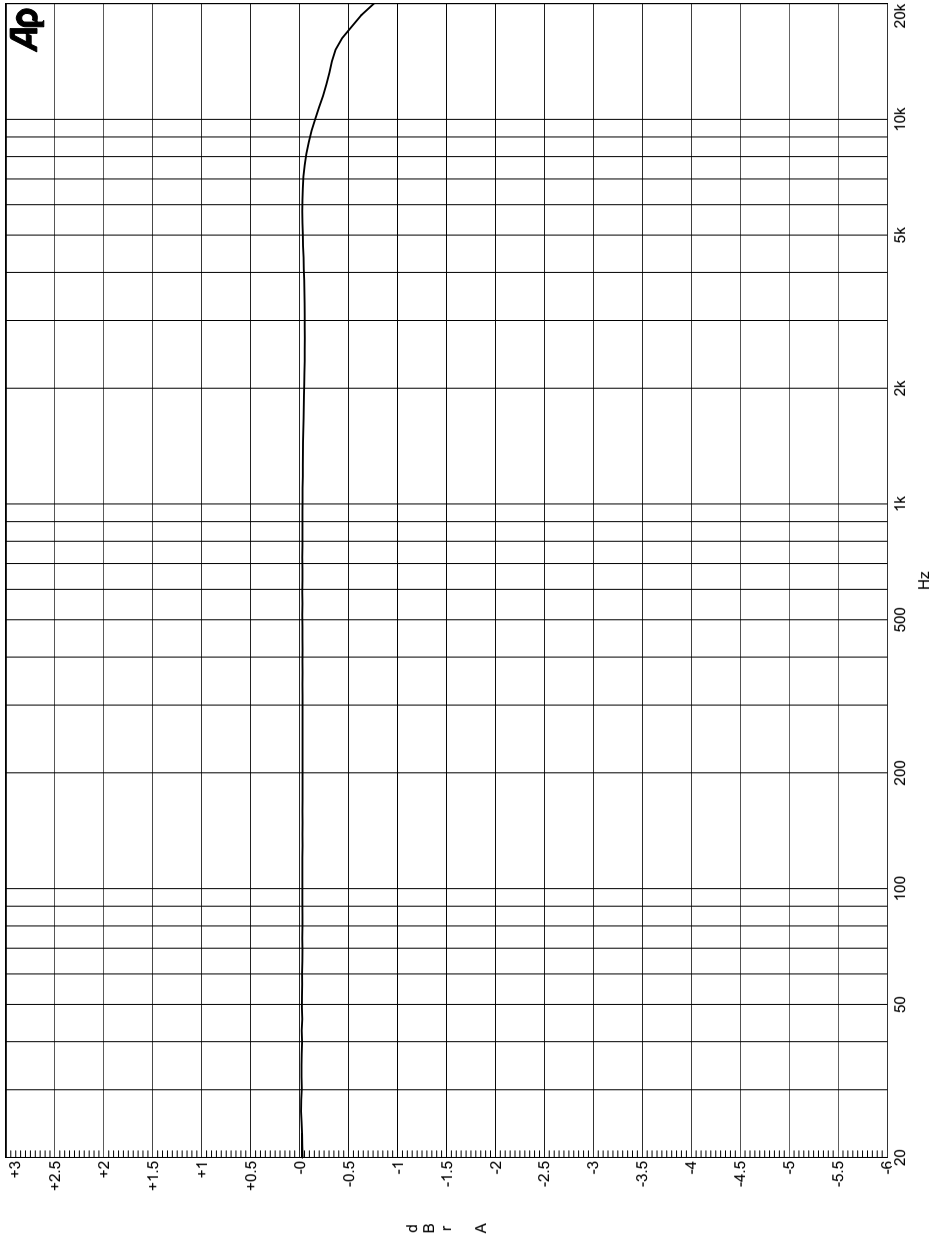

Figure 16. Frequency Response - J2, LFE Output (2.1 Disabled)

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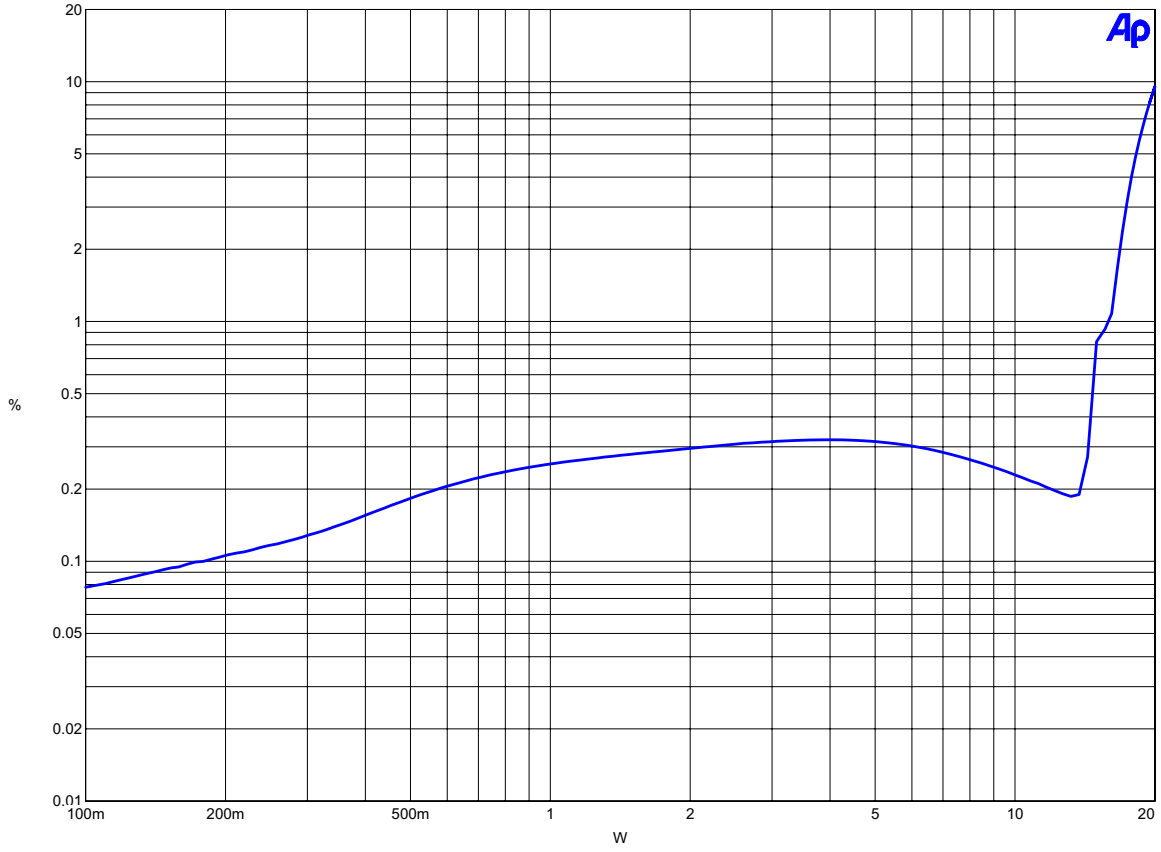

Figure 17. THD+N vs. Power at 1 kHz- J1, L/R Outputs (2.1 Disabled)

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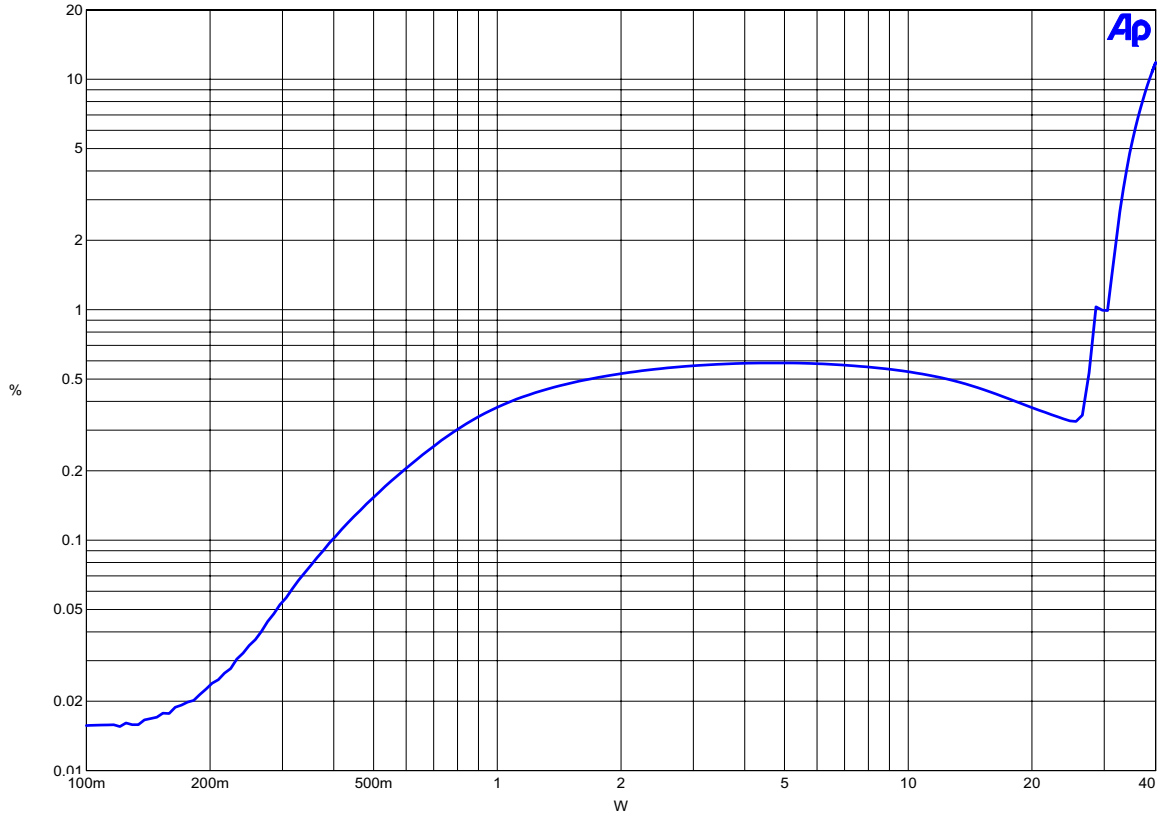

Figure 18. THD+N vs. Power at 1 kHz - J2, LFE Output (2.1 Disabled)

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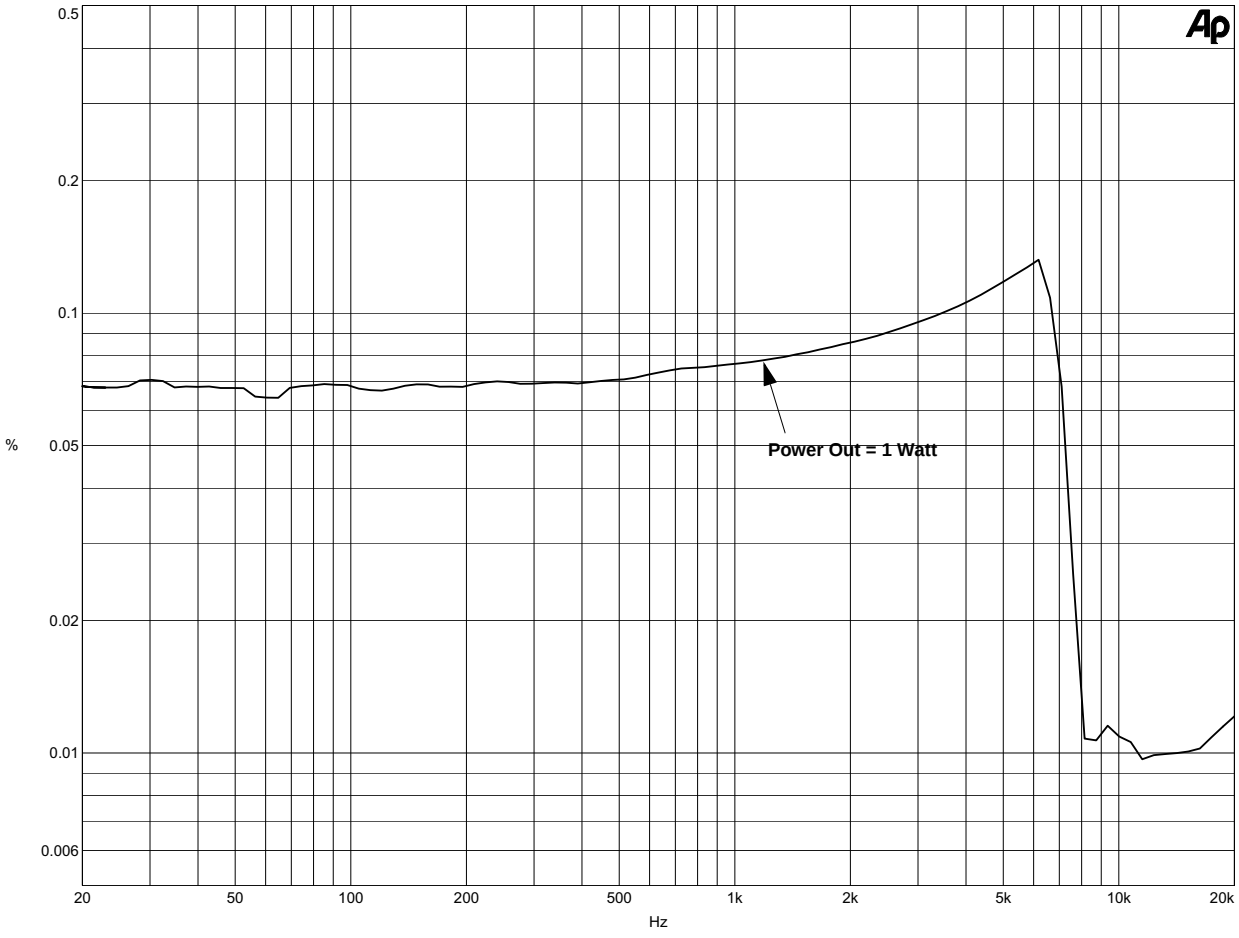

Figure 19. THD+N vs. Frequency, J1, L/R Outputs (2.1 Disabled)

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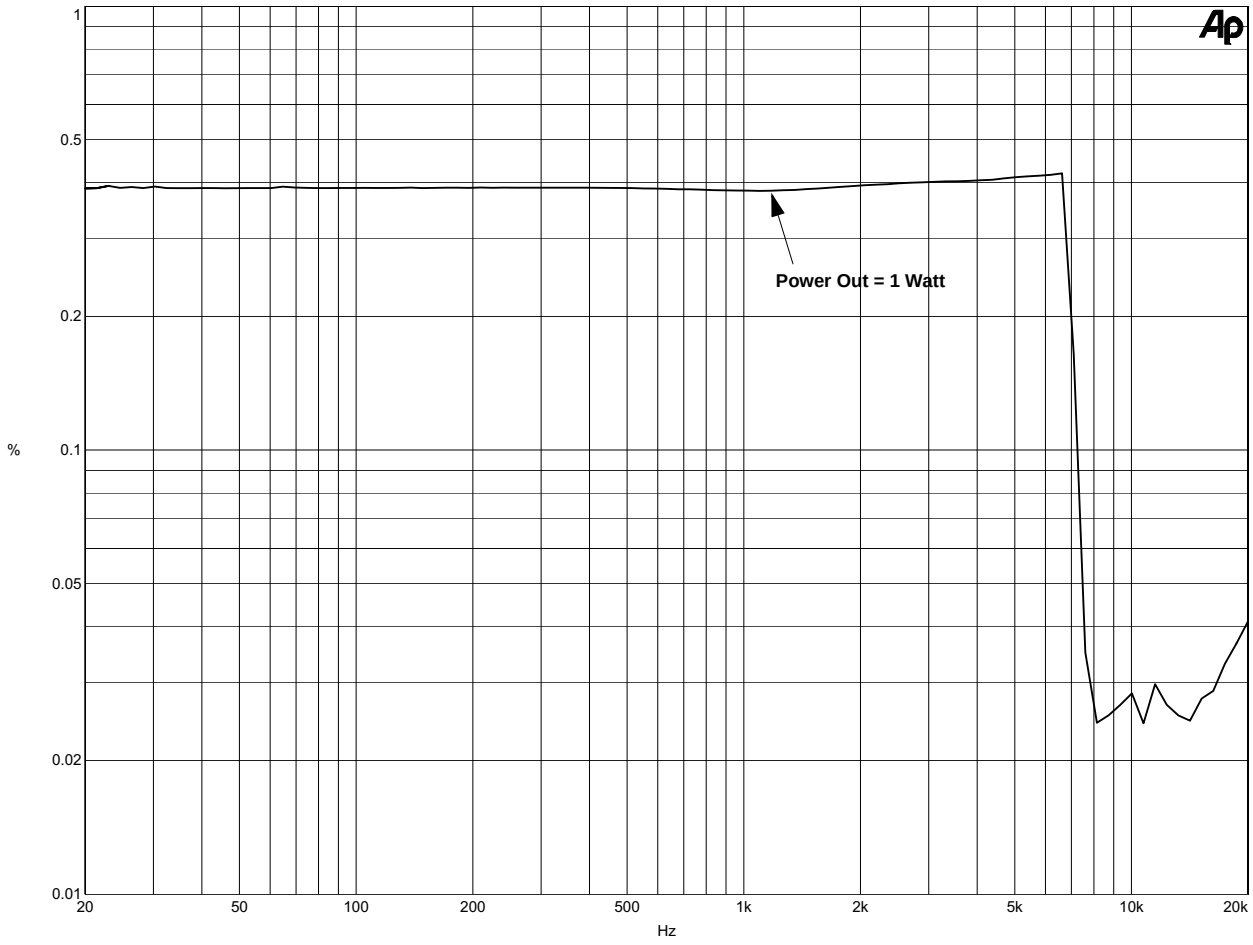

Figure 20. THD+N vs. Frequency - J2, LFE Output (2.1 Disabled)

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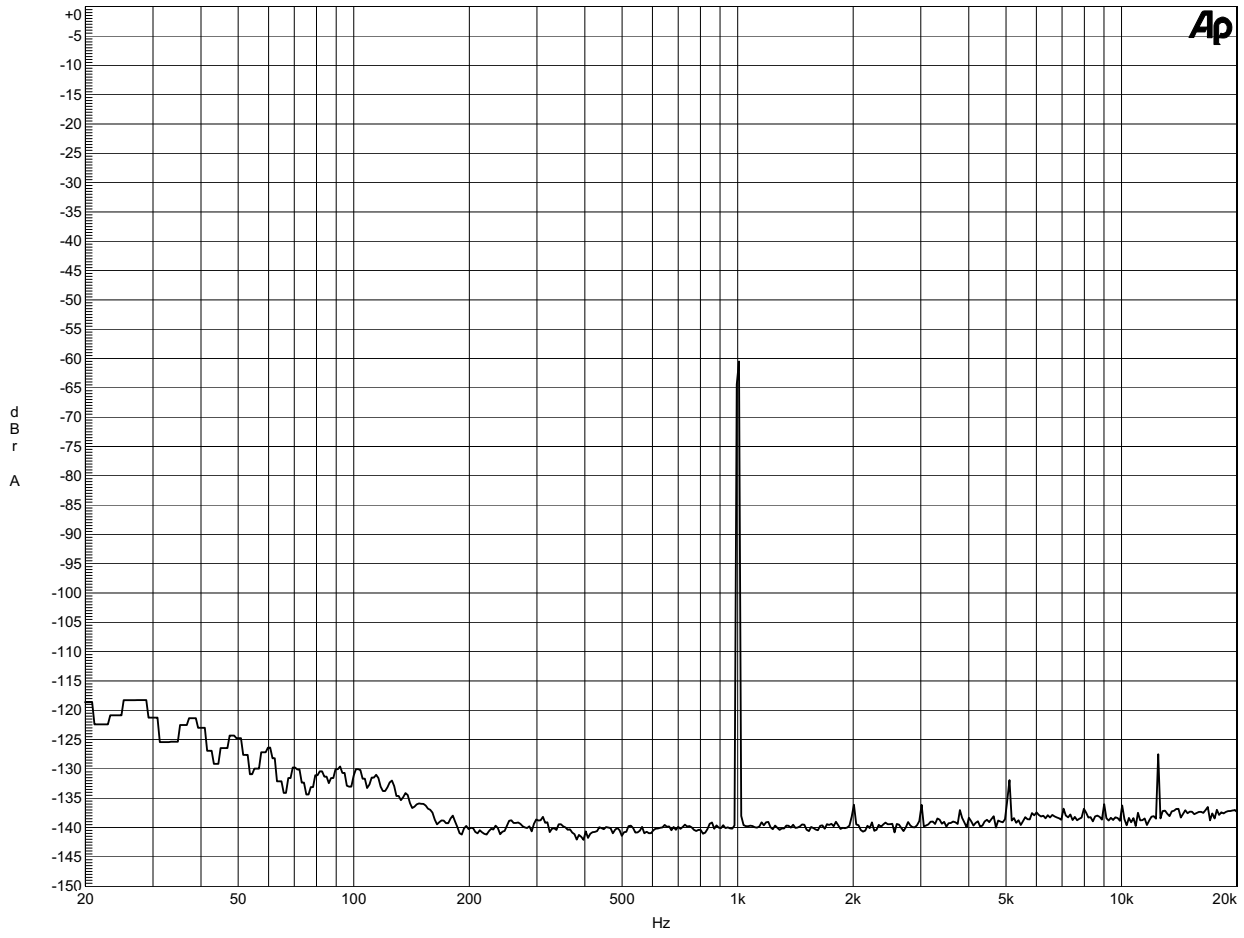

Figure 21. FFT at -60 dBFS and 1 kHz - J1, L/R Outputs (2.1 Disabled)

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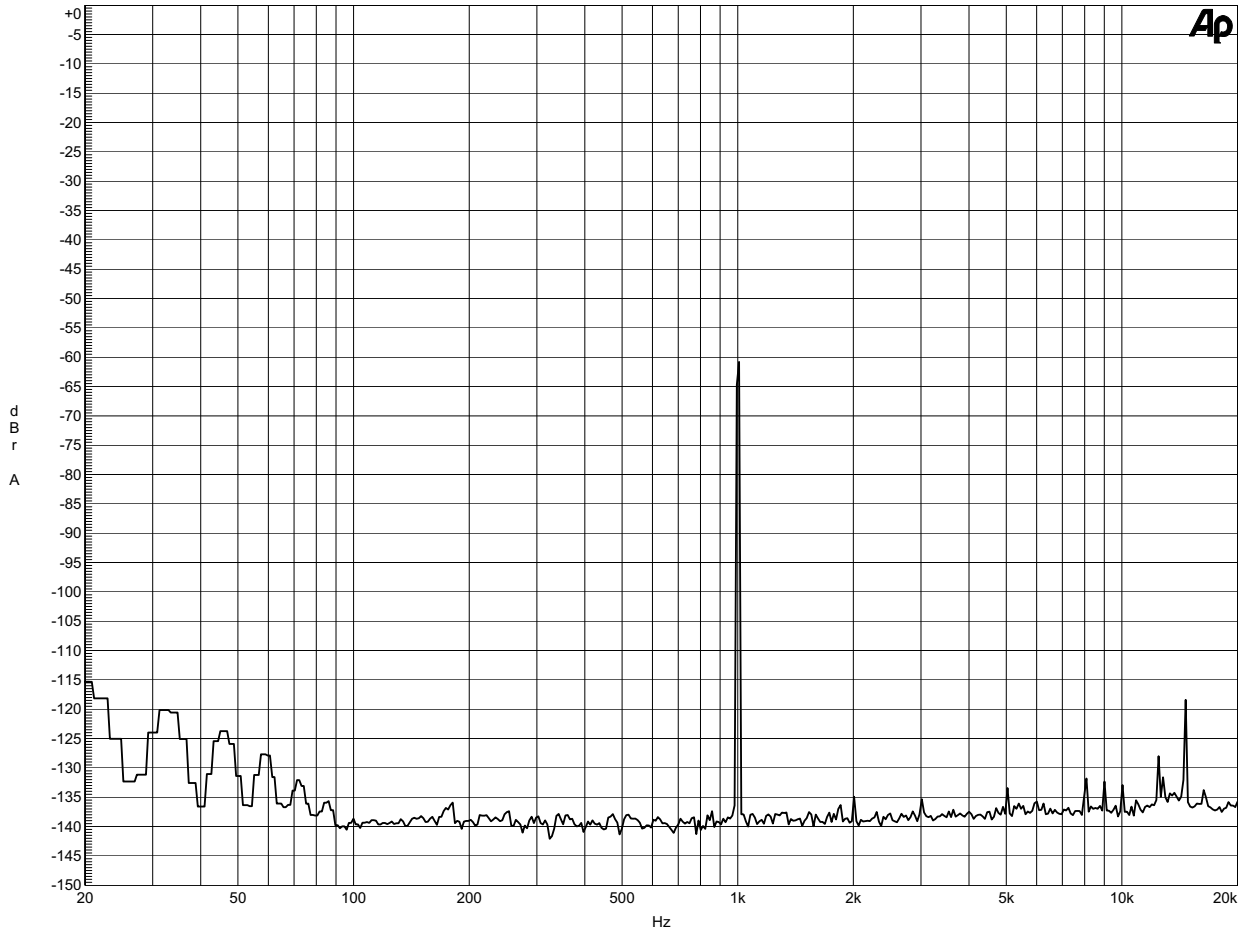

Figure 22. FFT at -60 dBFS and 1 kHz - J2, LFE Output (2.1 Disabled)

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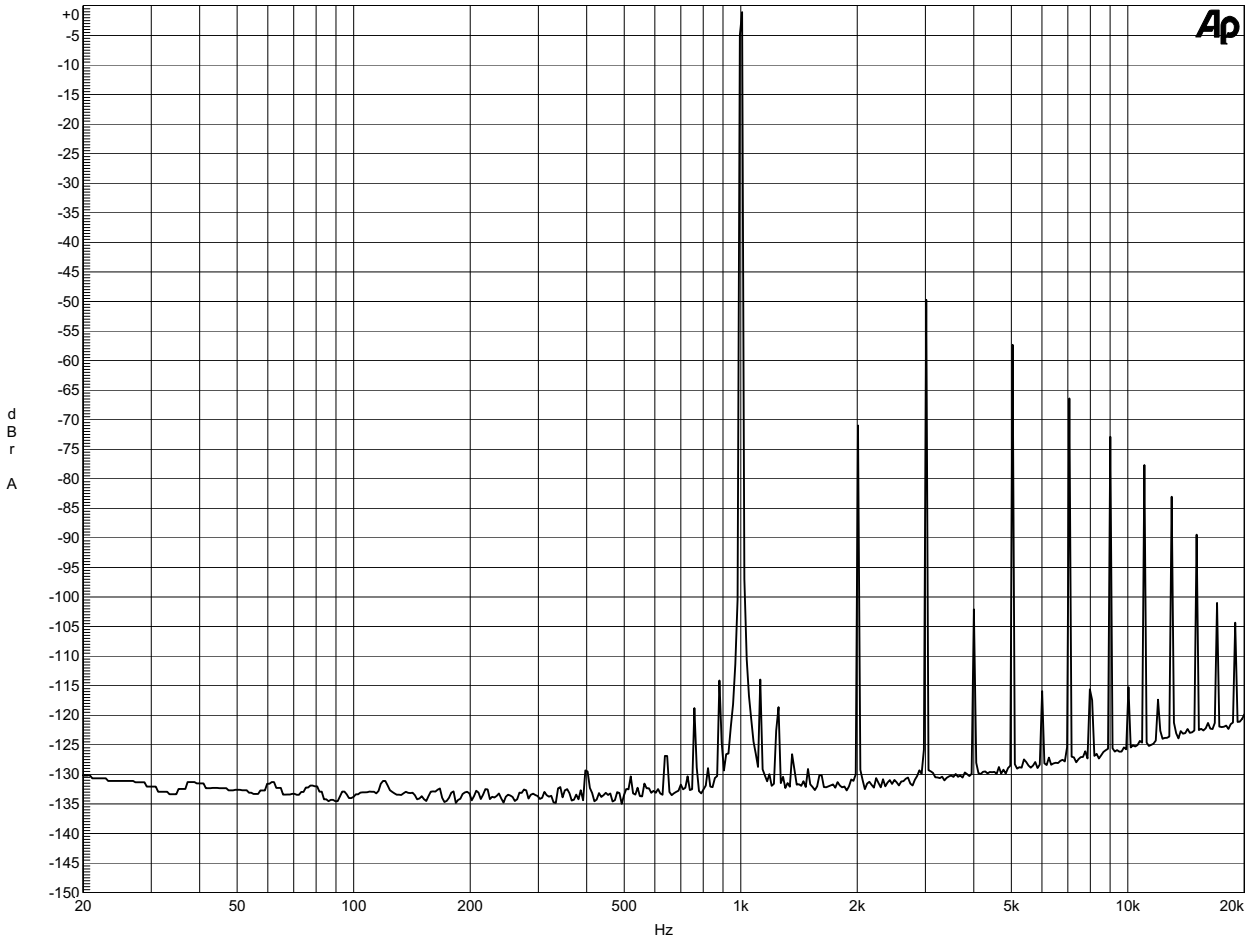

Figure 23. FFT at 0 dBFS and 1 kHz - J1, L/R Outputs (2.1 Disabled)

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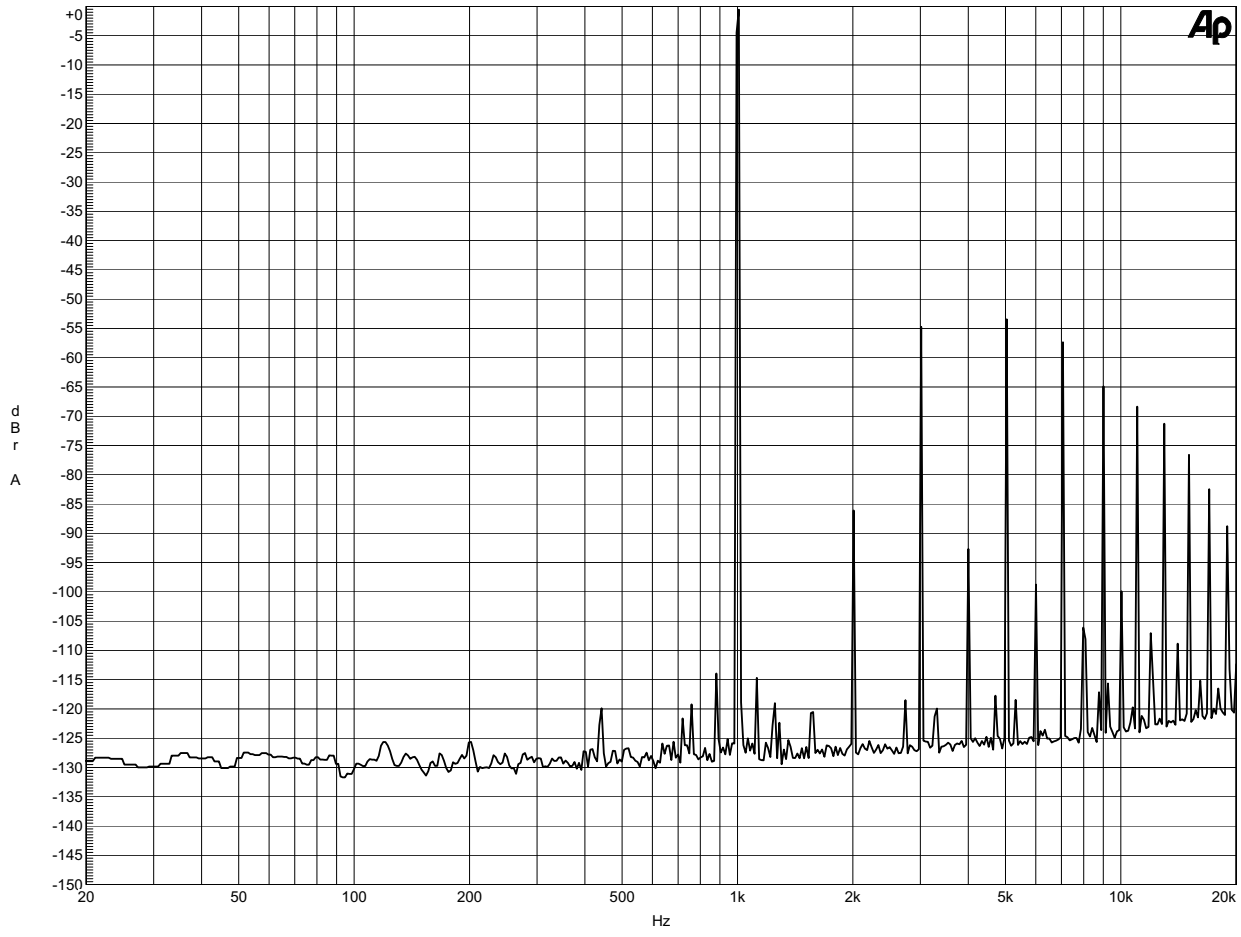

Figure 24. FFT at 0 dBFS and 1 kHz - J2, LFE Output (2.1 Disabled)

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10.ORDERING INFORMATION

Product	Description	Order#
CRD44130-FB	2x20 W + 1x40 W Reference Design for the CS44130	CRD44130-FB

11.REVISION HISTORY

Release	Changes
RD1	Initial Release
RD2	Added Software Mode Operation Section. Updated THD+N plots shown in Figures 17 through 20.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com.

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