



128Kx64 5V FLASH MODULE PRELIMINARY*

FEATURES

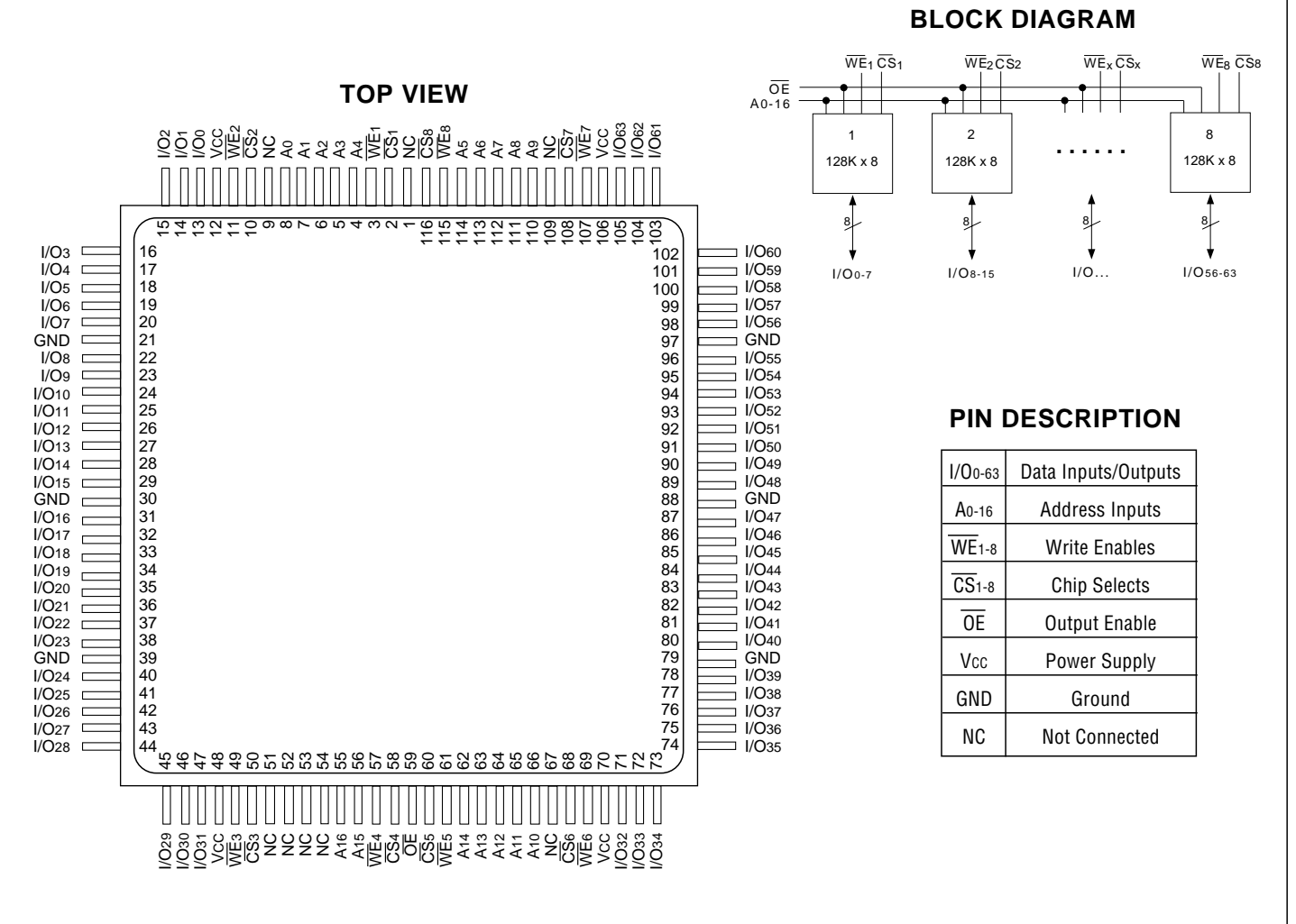
- Access Times of 60, 70, 90, 120, 150ns
- Packaging
 - 116 lead, 40mm square, Hermetic CQFP (Package 504)
- Sector Architecture
 - 8 equal size sectors of 16KBytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 100,000 Erase/Program Cycles Minimum (0°C to 70°C)
- Data Retention, 10 Year Minimum at 125°C
- Organized as 128Kx64, user configurable as 256Kx32, 512Kx16 or 1Mx8.

- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming; 5V (±10%) Supply
- Low Power CMOS, 8mA Standby Typical
- Hardware and Software Write Protection
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
WF128K64-XG4WX5 - 20 grams typical

** This data sheet describes a product under development and is subject to change without notice.*

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WF128K64-XG4WX5





ABSOLUTE MAXIMUM RATINGS (1)

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V _{CC})	-2.0 to +7.0	V
Signal voltage range (any pin except A ₉) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention Mil Temp	10 years	
Endurance (write/erase cycles) Mil Temp	10,000 cycles min.	
A ₉ Voltage for sector protect (V _{ID}) (3)	-2.0 to +14.0	V

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A₉ pin is -0.5V. During voltage transitions, A₉ may overshoot V_{SS} to -2V for periods of up to 20ns. Maximum DC input voltage on A₉ is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
A ₉ Voltage for Sector Protect	V _{ID}	11.5	12.5	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
\overline{OE} capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	100	pF
\overline{WE} capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
\overline{CS} capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	100	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LOx32}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH}		280	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH}		400	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = 5.5, \overline{CS} = V _{IH} , f = 5MHz		13	mA
V _{CC} Static Current	I _{CC4}	V _{CC} = 5.5, \overline{CS} = V _{IH}		1.2	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Output High Voltage	V _{OH2}	I _{OH} = -100 μA, V _{CC} = 4.5	V _{CC} - 0.4		V
Low V _{CC} Lock Out Voltage	V _{LKO}		3.2		V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with \overline{OE} at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{WE} CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	60		70		90		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	30		35		45		50		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	30		30		45		50		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		45		45		50		50		ns
Chip Select Hold Time	t _{WHEH}	t _{CH}	0		0		0		0		0		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation (min)	t _{WHWH1}		14		14		14		14		14		μs
Chip and Sector Erase Time	t _{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery Time Before Write	t _{GHWL}		0		0		0		0		0		ns
V _{CC} Setup Time		t _{VCS}	50		50		50		50		50		μs
Chip Programming Time				12.5		12.5		12.5		12.5		12.5	sec
Output Enable Setup Time		t _{OES}	0		0		0		0		0		ns
Output Enable Hold Time (1)		t _{OEH}	10		10		10		10		10		ns

1. For Toggle and Data Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	60		70		90		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		60		70		90		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		60		70		90		120		150	ns
\overline{OE} to Output Valid	t _{GLQV}	t _{OE}		30		35		40		50		55	ns
Chip Select to Output High Z (1)	t _{EHQZ}	t _{DF}		20		20		25		30		35	ns
\overline{OE} High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		20		25		30		35	ns
Output Hold from Address, \overline{CS} or \overline{OE} Change, whichever is first	t _{AXQX}	t _{OH}	0		0		0		0		0		ns

1. Guaranteed by design, not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{CS} CONTROLLED
 (VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	60		70		90		120		150		ns
\overline{WE} Setup Time	tWLLEL	tWS	0		0		0		0		0		ns
\overline{CS} Pulse Width	tELEH	tCP	30		35		45		50		50		ns
Address Setup Time	tAVEL	tAS	0		0		0		0		0		ns
Data Setup Time	tDVEH	tDS	30		30		45		50		50		ns
Data Hold Time	tEHDH	tDH	0		0		0		0		0		ns
Address Hold Time	tELAX	tAH	45		45		45		50		50		ns
\overline{WE} Hold from \overline{WE} High	tEHWL	tWH	0		0		0		0		0		ns
\overline{CS} Pulse Width High	tEHEL	tCPH	20		20		20		20		20		ns
Duration of Programming Operation	tWHWH1		14		14		14		14		14		μs
Duration of Erase Operation	tWHWH2		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery before Write	tGHEL		0		0		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5		12.5		12.5	sec



FIG. 2
AC WAVEFORMS FOR READ OPERATIONS

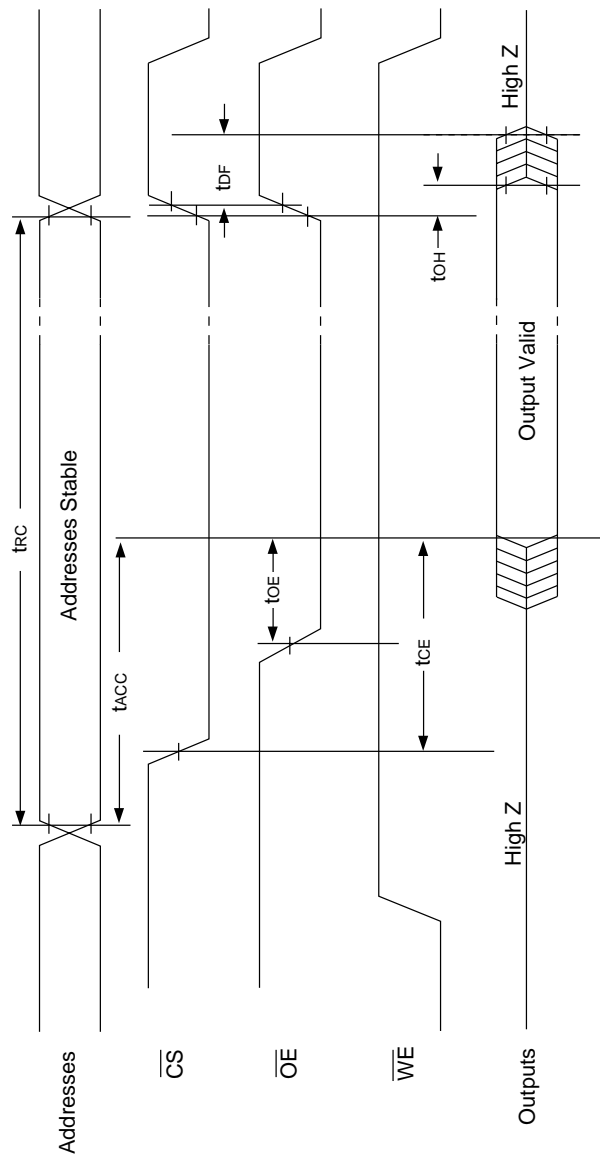
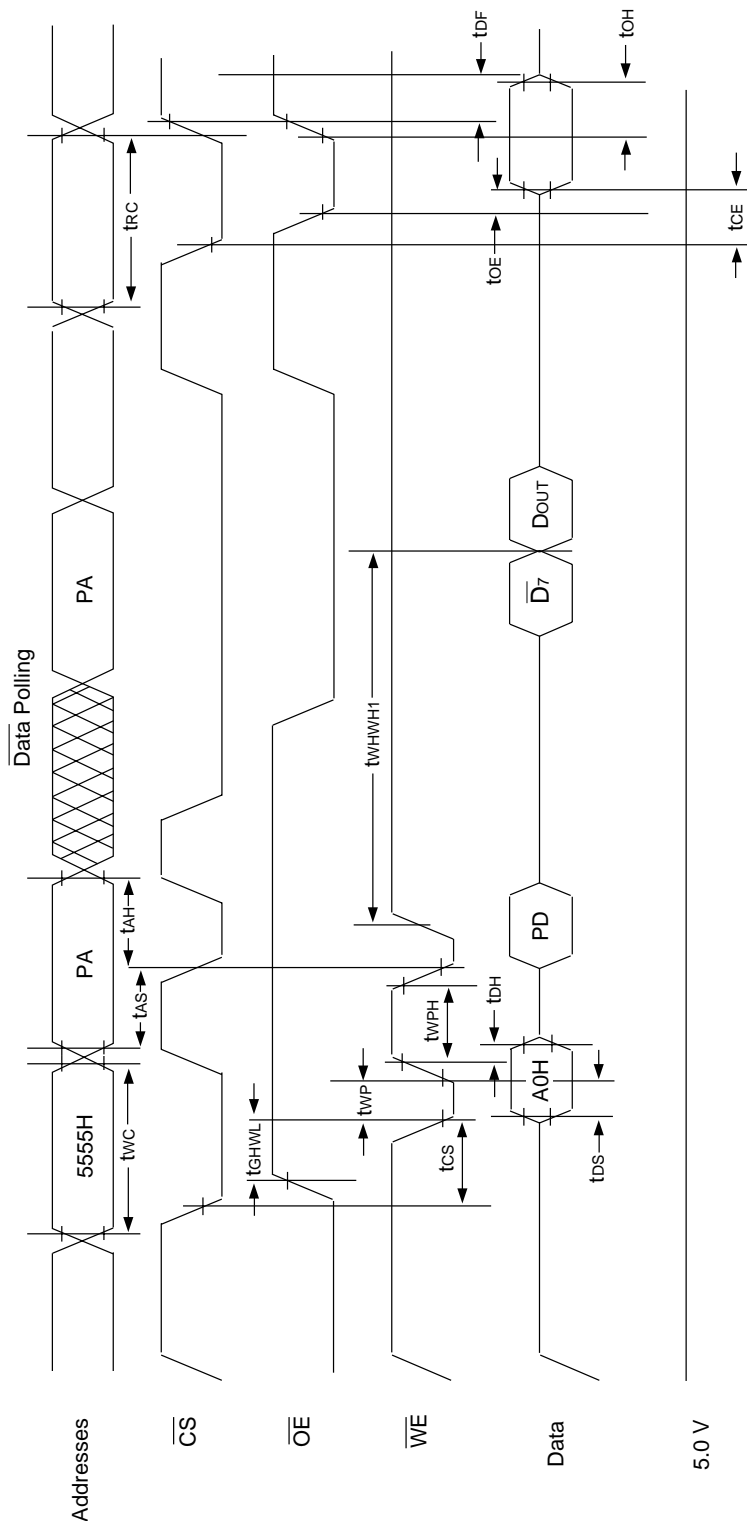




FIG. 3
WRITE/ERASE/PROGRAM OPERATION, \overline{WE} CONTROLLED

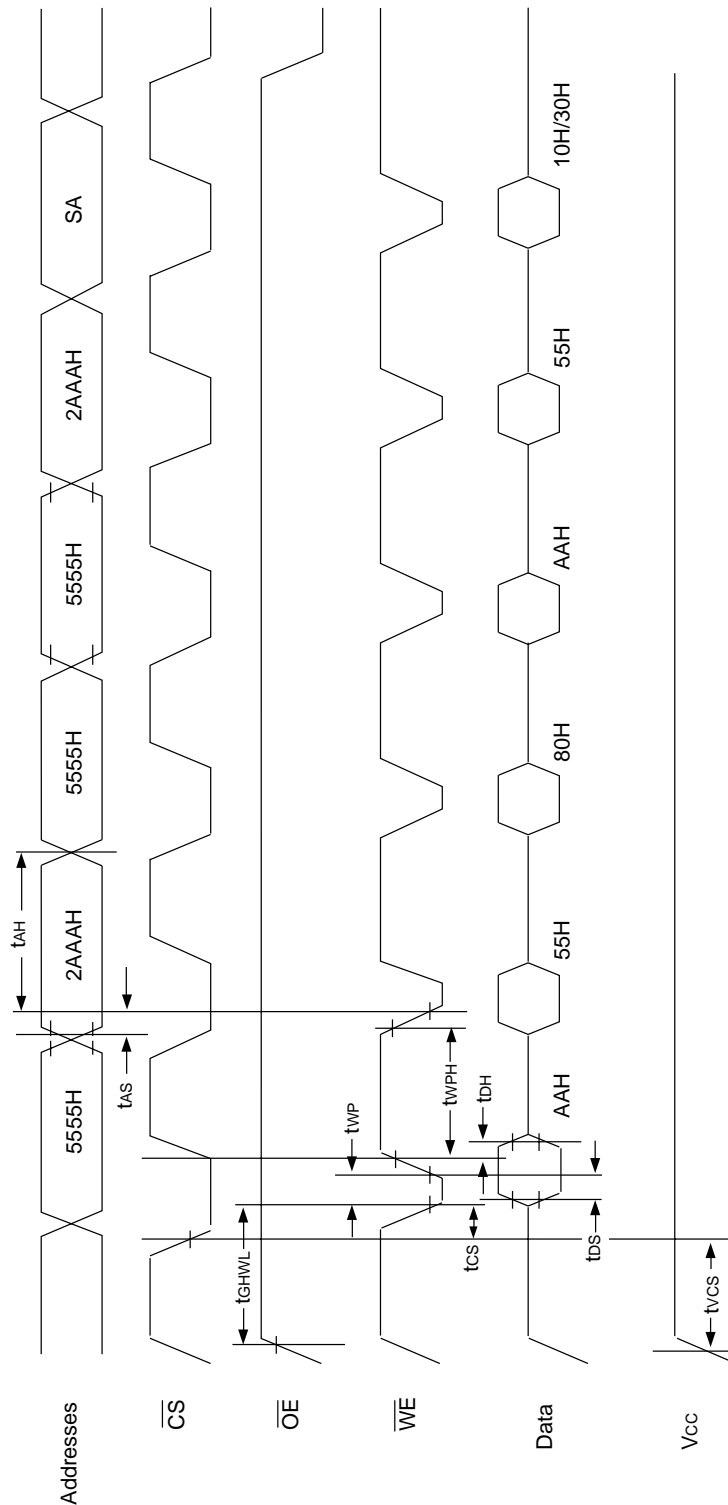


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 4
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



- NOTES:**
1. SA is the sector address for Sector Erase.



FIG. 5
AC WAVEFORMS FOR DATA POLLING DURING
EMBEDDED ALGORITHM OPERATIONS

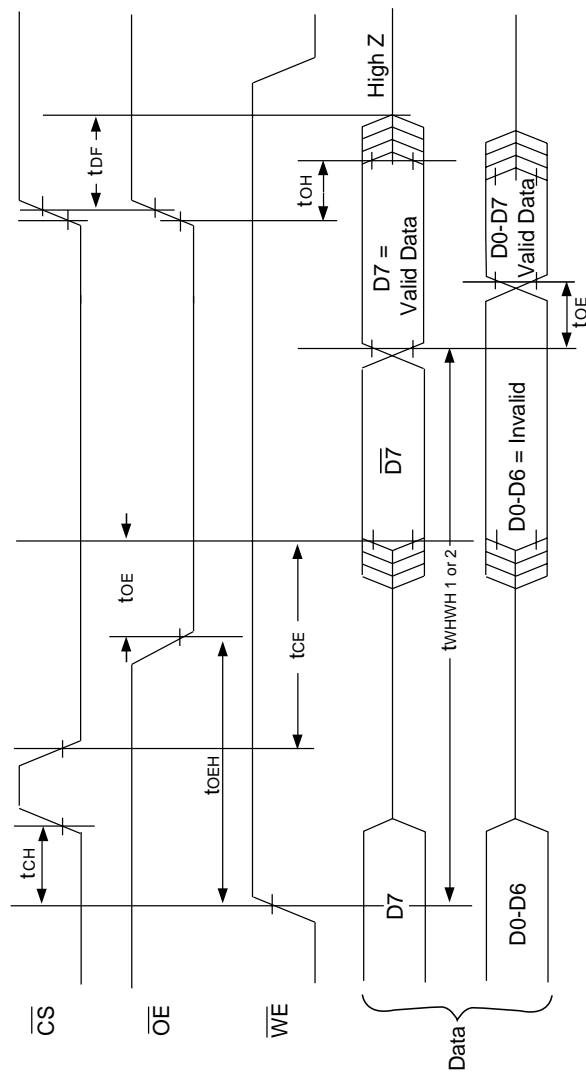
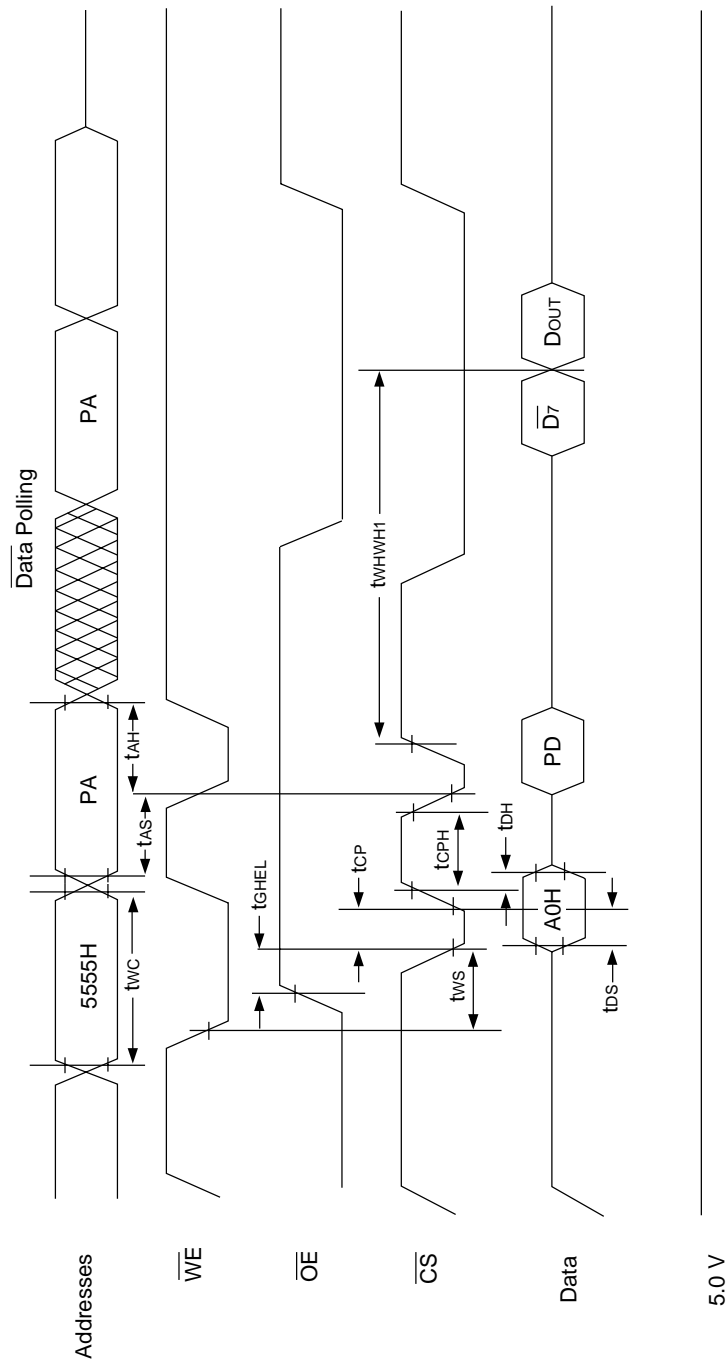




FIG. 6
WRITE/ERASE/PROGRAM OPERATION, \overline{CS} CONTROLLED

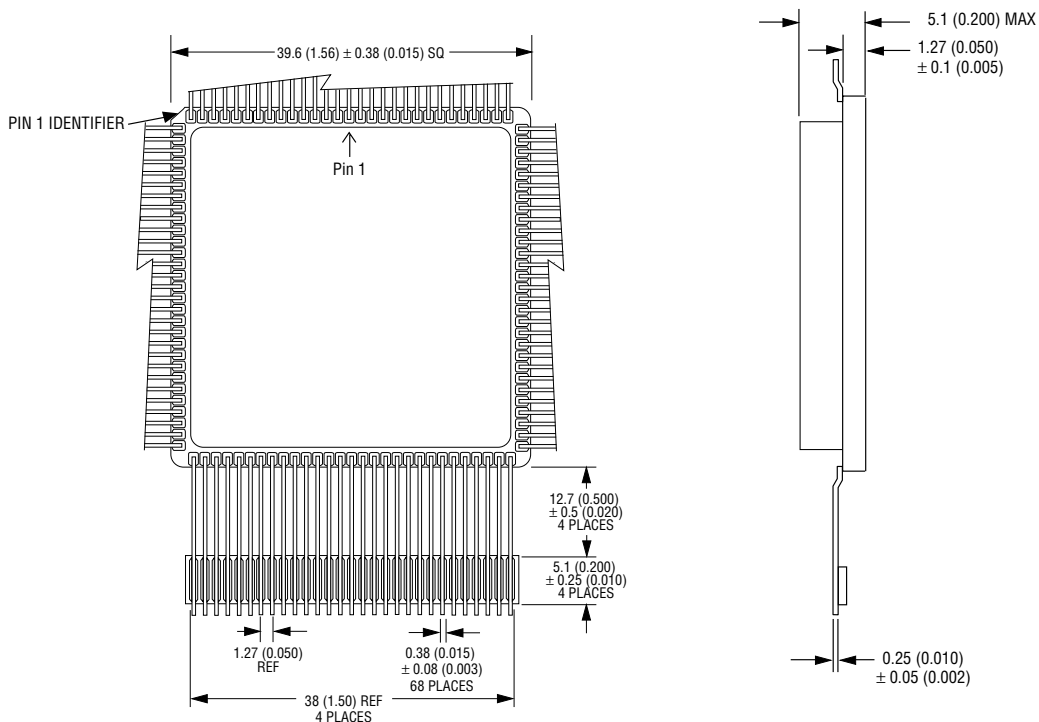


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to each chip.
4. D_{out} is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



PACKAGE 504: 116 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4W)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

