National Semiconductor

December 1990

ADC0882
8-Bit 20 MSPS Flash A/D Converter

General Description

The ADC0882 is a monolithic flash Analog to Digital converter capable of converting a video signal into a stream of 8-bit digital words at 20 MegaSamples Per Second (MSPS). The device is pin for pin compatible with TDC1048 but uses half the power. Since ADC0882 is a flash converter, a sample-and-hold circuit is not required.

The ADC0882 consists of 255 clocked latching comparators, precision resistive divider, encoding logic, and an output register. A single convert clock controls the conversion operation. The unit can be configured to give either true or inverted outputs, in binary or offset two's complement coding. All digital I/O is TTL compatible.

Applications

- Video Digitizing
- Medical Imaging
- High Energy Physics
- Digital Television
- Radar
- High Speed Data Links

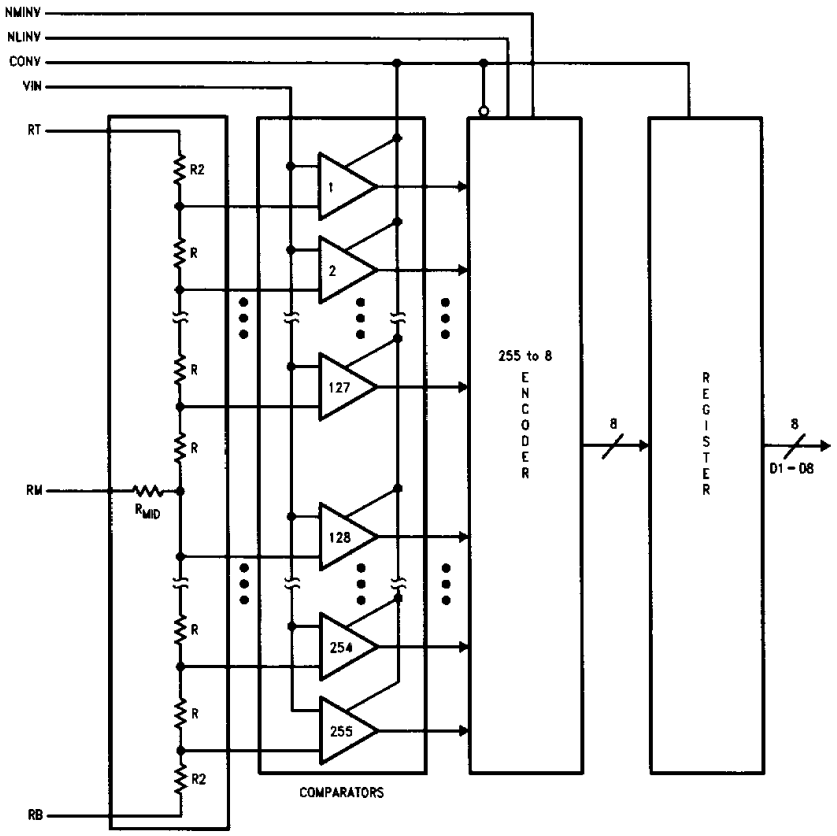
Key Specifications

■ Resolution	8 bits
■ Conversion rate	DC to 20 MSPS (min)
■ Full power bandwidth	7 MHz (min)
■ Small signal bandwidth (−3 dB)	30 MHz (min)
■ Linearity error	±½ LSB (max)
■ Analog input range	0V to −2V
■ Differential gain	0.7%
■ Differential phase	0.3°
■ Power dissipation	700 mW
■ Power supply	±5V or +5V/−5.2V

Features

- Drop-in replacement for TDC1038 and TDC1048
- Pin for pin compatible with ADC304, CXA1096P and CXA1296P
- No Sample-and-Hold circuit required
- Selectable data format
- Available in plastic DIP, CERDIP and PLCC

Block Diagram



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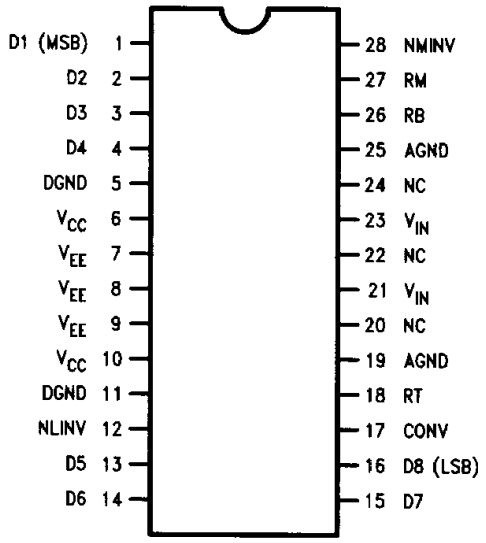
Connection Diagrams



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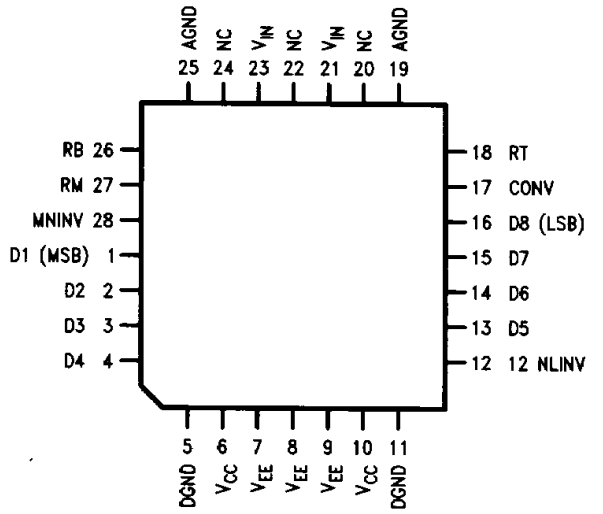
28-Lead CERDIP
J Package

28-Lead Plastic DIP
N Package



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28-Lead Plastic Chip Carrier
V Package

Ordering Information

Commercial ($0°C \leq T_A \leq 70°C$)	Package
ADC0882CCN/TDC1038N6C	N28B, 28-Pin Plastic
ADC0882CCJ/TDC1038B6C	J28A, 28-Pin CERDIP
ADC0882CCV/TDC1038R3C	V28A, 28-Lead Plastic Chip Carrier

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
Negative Supply Voltage (V_{EE})	+0.5V to −7.0V
Voltage at Logic Control Input and Outputs (Note 3)	−0.5V to (V_{CC} + 0.5V)
Voltage at Analog Inputs (V_{IN}, V_{RT}, V_{RB}) (Note 3)	V_{EE} to +0.5V
V_{RT}−V_{RB}	±2.2V
Input Current at Logic Control Inputs (Note 4)	±50 mA
Applied Current at Digital Outputs (Note 4)	±20 mA
Input Current at Analog Inputs (Note 4)	±100 mA
Power Dissipation at T_A = 25°C	See Note 5
Storage Temperature Range	−65°C to +150°C
ESD Rating	500V
Soldering Temperature All Packages (10 sec)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0882CCJ/TDC1038B6C	$0°C \le T_A \le +70°C$
ADC0882CCN/TDC1038N6C	$0°C \le T_A \le +70°C$
ADC0882CCV/TDC1038R3C	$0°C \le T_A \le +70°C$
V_{CC} Voltage	4.75V to 5.25V
V_{EE} Voltage	−4.75V to −5.5V
V_{RT} Most Positive Reference Voltage (Note 6)	−0.1V to 0.1V
V_{RB} Most Negative Reference Voltage (Note 6)	−1.9V to −2.1V
V_{RT} − V_{RB}	1.8V to 2.2V
Analog Input Voltage (V_{IN})	V_{RT} to V_{RB}

$t_{PWL} \ge 19$ ns, $t_{PWH} \ge 27$ ns

Converter Electrical Characteristics

The following specifications apply for V_{CC} = +5.25V, V_{EE} = −5.5V, V_{RB} = −2.0V, V_{AGND} = V_{DGND} = V_{RT} = GND, t_{PWL} = 19 ns and t_{PWH} = 27 ns unless otherwise specified. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**; all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit	Units (Limit)
STATIC CHARACTERISTICS					
	Resolution			**8**	Bits (Min)
	Integral Linearity Error			**0.2**	%FS(Max)
	Differential Linearity Error			**0.2**	%FS(Max)
	Code Size (Digital Output Step Size) (Note 8)		100	 **25** **175**	%LSB %LSB(Min) %LSB(Max)
	Offset Error, Top	V_{IN} = V_{RT}		**+15**	mV(Max)
	Offset Error, Bottom	V_{IN} = V_{RB}		**−15**	mV(Max)
	Offset Error Temperature Coefficient			**±20**	μV/°C(Max)
I_{REF}	Reference Current			**30**	mA(Max)
R_{REF}	Total Reference Resistance			**67**	Ω(Min)
V_{IN}	Analog Input Voltage Range			**V_{RB}** **V_{RT}**	V(Min) V(Max)
I_{IN}	Analog Input Constant Bias Current			**250**	μA(Max)
R_{IN}	Analog Input Equivalent Resistance	V_{IN} = V_{RB}		**80**	kΩ(Min)
C_{IN}	Analog Input Capacitance	V_{IN} = V_{RB}		**50**	pF (Max)

Converter Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5.25V, V_{EE} = −5.5V, V_{RB} = −2.0V, V_{AGND} = V_{DGND} = V_{RT} = GND, t_{PWL} = 19 ns and t_{PWH} = 27 ns unless otherwise specified. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**; all other limits T_A = 25°C.

Symbol	Parameter	Conditions		Typical (Note 7)	Limit	Units (Limit)
DYNAMIC CHARACTERISTICS						
S/(N+D)	Signal-to-Noise + Distortion Ratio Peak-Peak Signal/RMS Noise	V_{IN} = 2.0 V_{p-p}, 10 MHz BW	f_{IN} = 1.248 MHz		**54**	dB(Min)
			f_{IN} = 2.438 MHz		**53**	dB(Min)
S/(N+D)	Signal-to-Noise + Distortion Ratio RMS Signal/RMS Noise	V_{IN} = 2.0 V_{p-p}, 10 MHz BW	f_{IN} = 1.248 MHz		**45**	dB(Min)
			f_{IN} = 2.438 MHz		**44**	dB(Min)
	Full Power Bandwidth	V_{IN} = 2.0 V_{p-p}, No Spurious or Missing Codes			**7**	MHz(Min)
	−3 dB Small Signal Bandwidth	V_{IN} = −20 dB, FS = 0.2 V_{p-p}			**30**	MHz(Min)
	Full Scale Transient Response				**40**	ns(Min)
t_{STO}	Sampling Time Offset				**−2** **10**	ns(Min) ns(Max)
	Aperture Jitter				**60**	$ps_{rms(Max)}$
	Differential Phase Error	f_S = 4xNTSC		0.3	**1.0**	Degree(Max)
	Differential Gain Error	f_S = 4xNTSC		0.7	**2.0**	%(Max)

DC Electrical Characteristics

The following specifications apply for V_{CC} = +5.25V, V_{EE} = −5.5V, V_{RB} = −2.0V, V_{AGND} = V_{DGND} = V_{RT} = GND, t_{PWL} = 19 ns and t_{PWH} = 27 ns unless otherwise specified. **Boldface limits apply for T_A = T_{Min} to T_{Max}**; all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit	Units (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage			**2.0**	V(Min)
$V_{IN(0)}$	Logical "0" Input Voltage			**0.8**	V(Max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 2.4V		**50** **−200**	μA(Max) μA(Min)
		V_{IN} = V_{CC} = +5.25V		**1.0**	mA(Max)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0.4V		**−0.6**	mA(Max)
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_{OUT} = −400 μA		**2.4**	V(Min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_{OUT} = 4.0 mA		**0.5**	V(Max)
	Short-Circuit Output Current	Output High, One Pin to Ground, One Second Duration Max.		**−40**	mA(Max)
C_I	Digital Input Capacitance	f = 1 MHz		15	pF(Max)
I_{CC}	V_{CC} Supply Current	(Note 9)		**45**	mA(Max)
I_{EE}	V_{EE} Supply Current	(Note 9)		**−165**	mA(Max)

AC Electrical Characteristics

The following specifications apply for V_{CC} = +5.25V, V_{EE} = −5.5V, V_{RB} = −2.0V, V_{AGND} = V_{DGND} = V_{RT} = GND, t_{PWL} = 19 ns and t_{PWH} = 27 ns unless otherwise specified. **Boldface limits apply for T_A = T_{Min} to T_{Max};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit	Units (Limit)
f_S	Maximum Conversion Rate			**20**	MSPS(Min)
t_{PWL}	Convert (CONV) Pluse Width, Low			**19**	ns(Min)
t_{PWH}	Convert (CONV) Pulse Width, High			**27**	ns(Min)
t_D	Output Delay	V_{CC} +4.75V, Load 1, *Figure 4*		**30**	ns(Max)
t_{HO}	Output Hold Time	Load 1, *Figure 4*		**5**	ns(Min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

Note 3: Applied voltage must be current limited to the specified range.

Note 4: Forcing voltage must be limited to specified range.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), θ_{JC} (package junction to case thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 175°C, and the typical thermal resistances (θ_{JA} and θ_{JC}) of the ADC0882 follow:

Suffixes	Package Number	θ_{JA} °C/W	θ_{JC} °C/W
CCJ	J28A	50	12
CCN	N28A	45	17
CCV	V28A	65	14

Note 6: V_{RT} must be more positive than V_{RB}, and the voltage reference differential must be within the specified range.

Note 7: Typicals are at T_A = 25°C and represent most likely parametric norm.

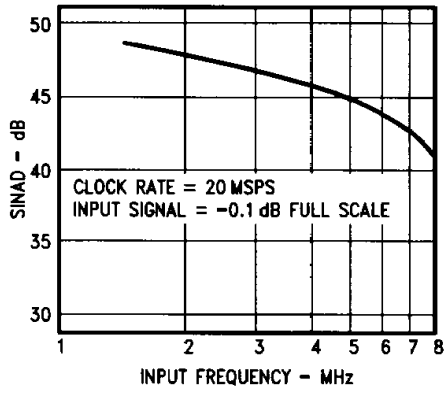
Note 8: Code size is the size of the individual codes, from code transition to code transition. It is often expressed as a percentage of the ideal code size. The ideal code size is given by: Input Voltage Range/2^N. Where N is the number of bits of resolution of the A/D converter.

Note 9: Worst case, all digital inputs and outputs LOW.

Typical Performance Characteristics

(T_A = 25°C, V_{CC} = +5V, V_{EE} = −5V)

Signal to Noise and Distortion Ratio vs Input Frequency



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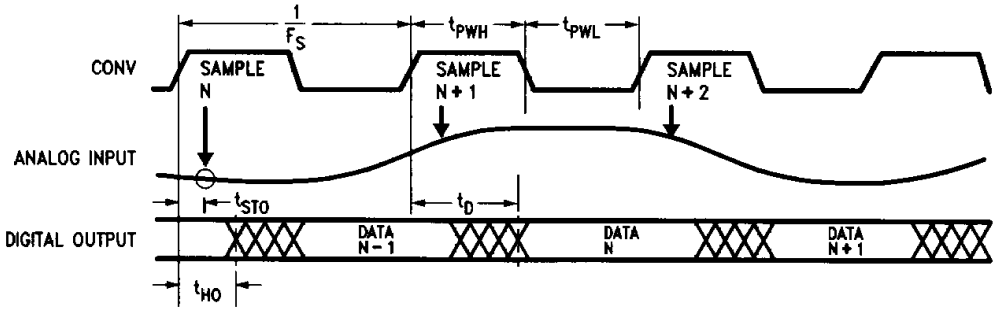

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FIGURE 1. Timing Diagram

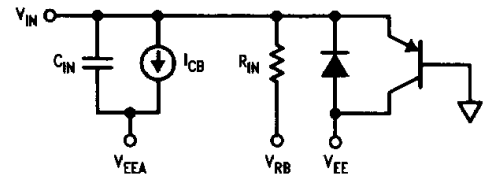
TABLE I. Output Coding Table

Input Voltage	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = High NLINV = High	NMINV = Low NLINV = Low	NMINV = Low NLINV = High	NMINV = High NLINV = Low
0.0000V	0000 0000	1111 1111	1000 0000	0111 1111
−0.0078V	0000 0001	1111 1110	1000 0001	0111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9922V	0111 1111	1000 0000	1111 1111	0000 0000
−1.0000V	1000 0000	0111 1111	0000 0000	1111 1111
−1.0078V	1000 0001	0111 1110	0000 0001	1111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−1.9844V	1111 1110	0000 0001	0111 1110	1000 0001
−1.9922V	1111 1111	0000 0000	0111 1111	1000 0000

Note 1: NMINV and NLINV are to be considered DC controls, they may be tied to V_{CC} for a logic "1" or to ground for a logic "0".

Note 2: Voltages are code midpoints.

Simplified Input and Output Circuits



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C_{IN} is nonlinear junction capacitance
V_{RB} is a voltage equal to the voltage on pin R_B

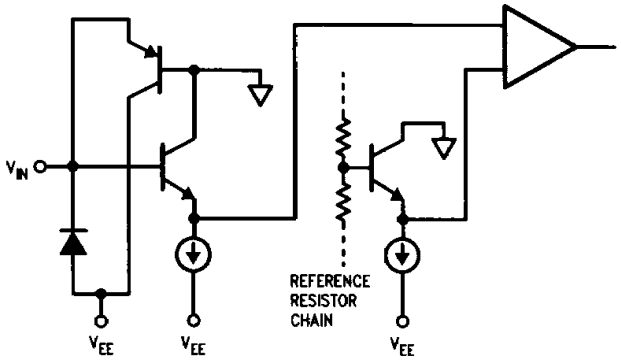

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FIGURE 2. Simplified Analog Input Circuits

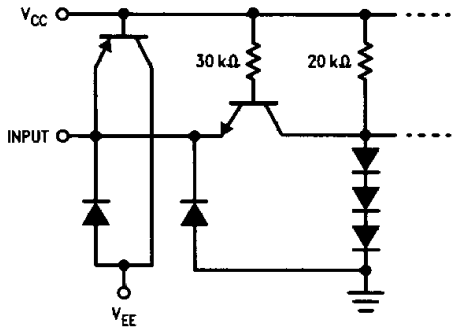

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FIGURE 3. Simplified Digital Convert Input Circuit

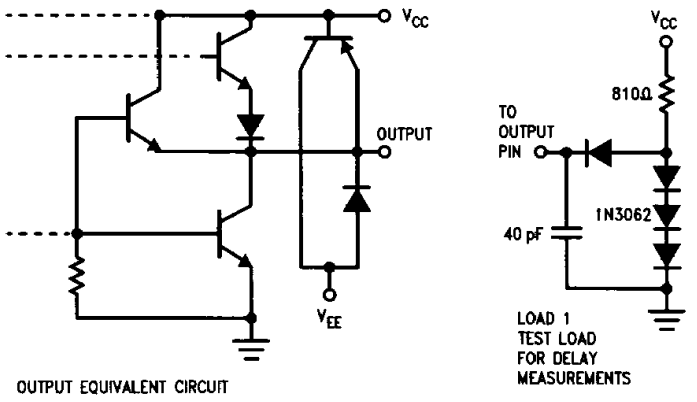

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FIGURE 4. Simplified Digital Output Circuit

Pin Descriptions

V_{CC}(6,10) These are the positive digital power supply pins. Normally, +5 V_{DC} should be applied and bypassed to digital ground with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

V_{EE}(7, 8, 9) These are the negative analog power supply pins. Normally, −5 V_{DC} should be applied and bypassed to analog ground with a 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor.

AGND(19, 25) These are the Analog ground pins.

DGND(5, 11) These are the Digital ground pins.

RT(18) This pin connects to the top of the reference resistor. Normally this pin is connected to AGND.

RM(27) This pin is connected to the middle of the reference resistor. A voltage may be applied to this pin to trim the converter's integral linearity (see Text).

RB(26) This pin is connected to the bottom of the reference resistor. Normally −2V is applied to this pin and should be bypassed to analog ground with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

V_{IN}(21,23) These are the analog signal input pins. The input signal range is from 0V to −2V.

CONV(17) A TTL convert signal is applied to this pin. A conversion is initiated at the rising edge of the signal.

NMINV(28) This is the Not Most Significant Bit Invert pin. A TTL signal at this pin controls the format of the output data (see Table I).

NLINV(12) This is the Not Least Significant Bit Invert pin. A TTL signal at this pin controls the format of the output data (see Table I).

D1–D8 (1, 2, 3, 4, 13, 14, 15, 16) These are the output data pins. D1 outputs the MSB data while D8 outputs the LSB Data.

NC(20, 22, 24) No connection.

Application Hints

OPERATION

The ADC0882 has three functional sections: a resistor/comparator array, encoding logic, and output registers. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (or thermometer code, since all the comparators whose reference is more negative than the input signal will be at logic "1" and all those whose reference is more positive will be at logic "0"). The encoding logic converts the N-of-255 code into the user's choice of coding. The output register holds the output constant between updates.

REFERENCE

The ADC0882 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. The specifications of the ADC0882 are guaranteed with V_{RT} (the voltage applied to the top of the reference resistor chain) at 0.0V ± 0.1V and V_{RB} (the voltage applied to the bottom of the reference resistor chain) at −2.0V ± 0.1V.

Linearity is guaranteed with no adjustment; however, a midpoint tap, R_M, allows trimming of converter integral linearity as well as the creation of a nonlinear transfer function. Note that ADC0882's integral nonlinearity is ±½ LSB maximum. If the maximum nonlinearity occurs at midscale then the circuit of *Figure 5* will allow the user to null out the linearity error at midscale. This adjustment may improve the overall integral linearity of the converter to less than ±½ LSB. The characteristic impedance seen at this node is approximately 220Ω and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and any noise introduced at this point will degrade the overall quantization Signal-to-Noise Ratio (SNR). Due to the slight variation in the reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor (0.01 μF to 0.1 μF) to ground is recommended. If the reference inputs are exercised dynamically (as in an automatic gain control circuit) a low impedance reference source is required. The reference voltages may be varied dynamically at up to 5 MHz; however, device performance is specified with fixed reference voltages as defined in the "Electrical Characteristics" tables.

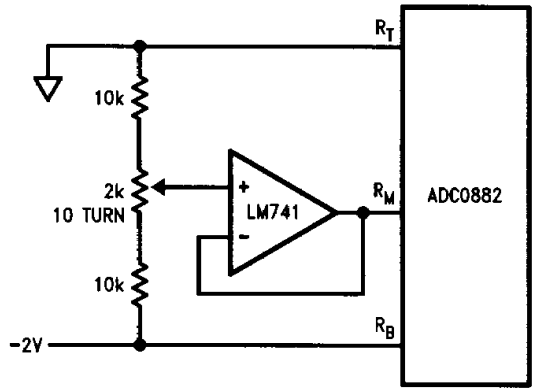

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FIGURE 5. Optional Midscale Linearity Adjust

ANALOG INPUT AND SOURCE IMPEDANCE CONSIDERATIONS

For precise quantization, the ADC0882 uses latching comparators. For optimum overall system performance the source impedance of the driving circuit must be less than 25Ω. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number from 0 to 255. When a signal outside the recommended input voltage range (0V to −2V) is applied, the output will remain at either full-scale value. The input signal will not damage the ADC0882 if it remains within the range specified in the "Absolute Maximum Ratings" table. Both analog input pins (V_{IN}) are connected together internally and therefore either one or both may be used.

CONVERT

The ADC0882 requires an external convert (CONV) signal. Because the ADC0882 is a flash converter it does not require a track-and-hold circuit. A sample is taken (the outputs of the comparators are latched) within t_{STO} (Sampling Time Offset) after a rising edge on the CONV pin. The result is encoded and then transferred to the output registers on the next rising edge. The digital output for sample N becomes valid t_D after the rising edge of clock N + 1 and remains valid until t_{HO} after the rising edge of clock N + 2.

OUTPUT FORMAT CONTROL

Two output format control pins, NMINV and NLINV, are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the "Output Coding Table". These active low pins may be tied to V_{CC} (through a 4.7k resistor) for a logic 1 or DGND for a logic 0.

OUTPUTS

The outputs of the ADC0882 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) loads or the equivalent. The outputs hold the previous data for a minimum of t_{HO} after the rising edge of the convert signal.

POWER SUPPLIES

The ADC0882 operates from two supply voltages: +5.0V and −5.0V. A −5.2V negative power supply may be used with a slight increase in power dissipation. The return path for I_{CC}, the current from the +5.0V supply, is DGND. The return path for I_{EE}, the current from the −5.0V supply, is AGND. All power and ground pins must be connected. Bypass V_{CC} with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor to the digital ground. Also bypass V_{EE} with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor to analog ground.

TYPICAL INTERFACE CIRCUIT

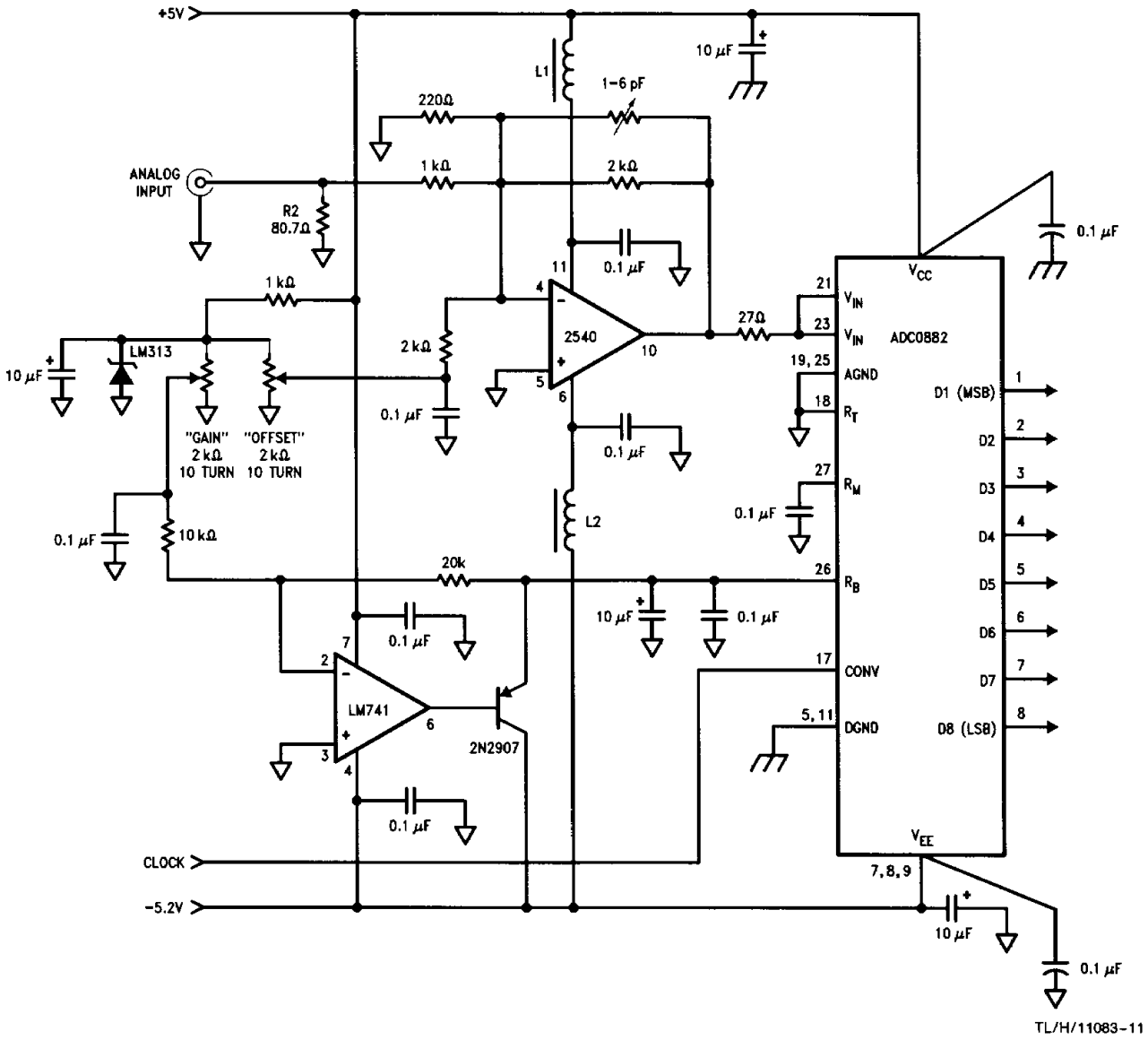
A typical interface circuit *(Figure 6)* shows a wideband operational amplifier driving the A/D converter directly. Bipolar inputs to the op amp can be accommodated by adjusting

Application Hints (Continued)

the offset control. A Zener diode provides a stable reference for the offset and gain controls. All V_{IN} pins are connected close to the device package and the input amplifier's feedback loop should be closed at that point. The buffer has an inverting gain of two, increasing a 1 V_{p-p} video input signal to the recommended 2 V_{p-p} input for the ADC0882. Proper decoupling is recommended for all systems.

A variable capacitor permits amplifier optimization for either step response or frequency response. This may be replaced with a fixed value capacitor as determined by evaluation of the final PC board layout.

The bottom reference voltage (V_{RB}) is supplied by an inverting amplifier, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain.



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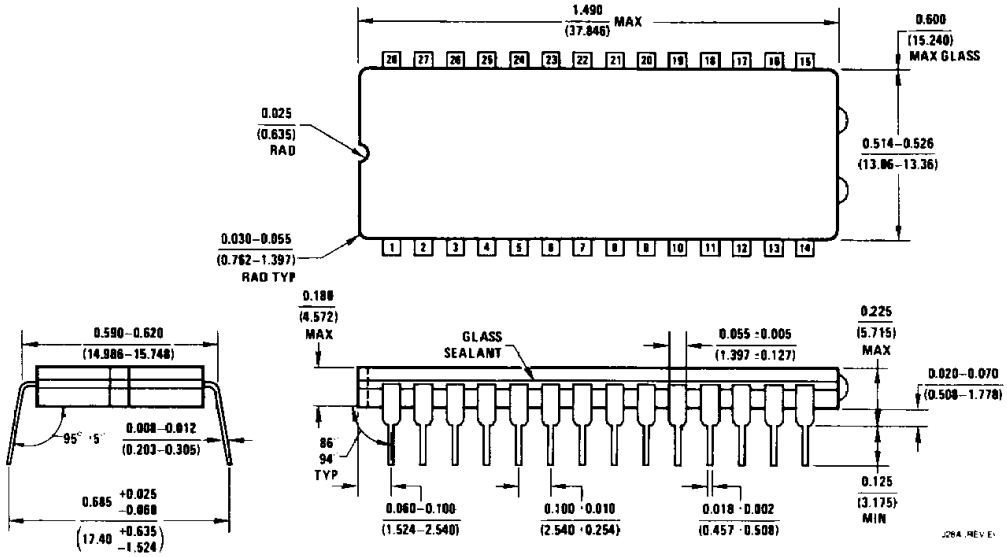
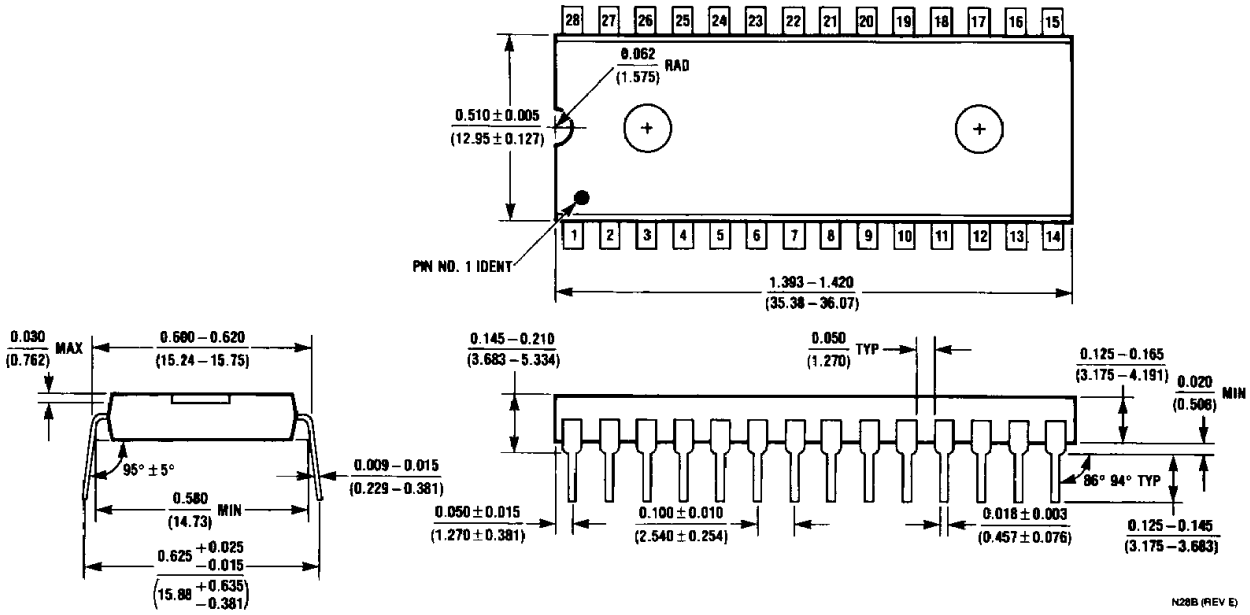
Note 1: L1, L2—Ferrite Bead, Fair—Rite #2743001112 or equivalent.

FIGURE 6. Typical Interface Circuit

Physical Dimensions inches (millimeters)

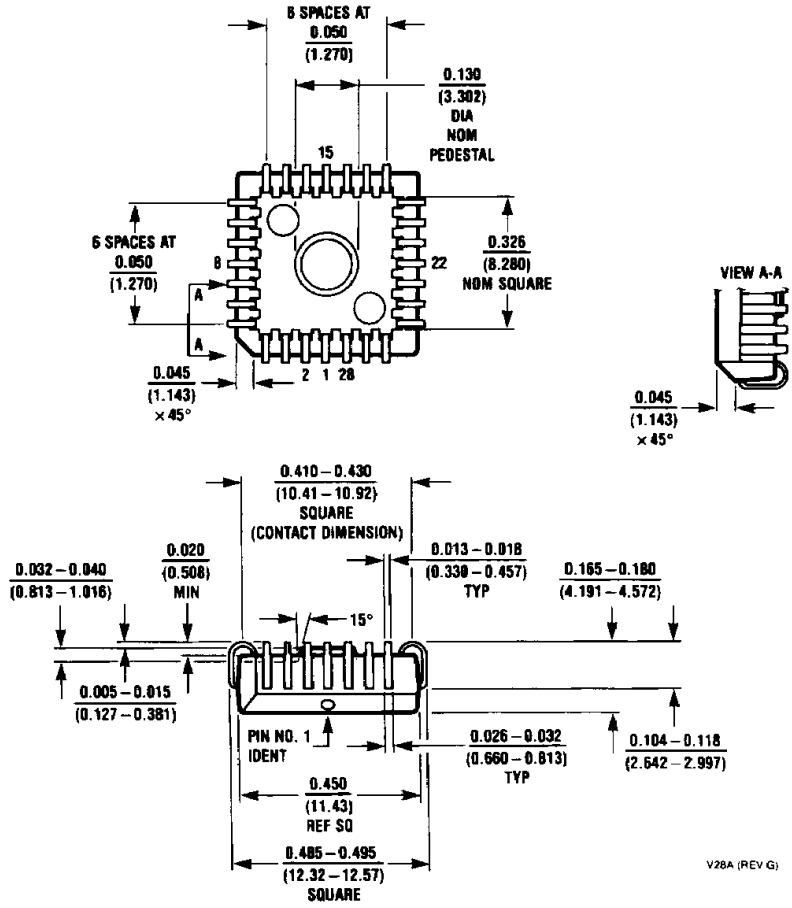


28-Pin CERDIP
ADC0882CCJ or TDC1038B6C
NS Package Number J28A



28-Pin Plastic
ADC0882CCN or TDC1038N6C
NS Package Number N28A

Physical Dimensions inches (millimeters)



28-Lead Plastic Chip Carrier
ADC0882CCV or TDC1038R3C
NS Package Number V28A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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