ADC-EK Series
Monolithic Integrating Analog-to-Digital Converters

FEATURES

- **Monolithic CMOS**
- **Binary or BCD models**
- **20 mW power consumption**
- **To 12-bit accuracy**
- **No missing codes**
- **Low cost**

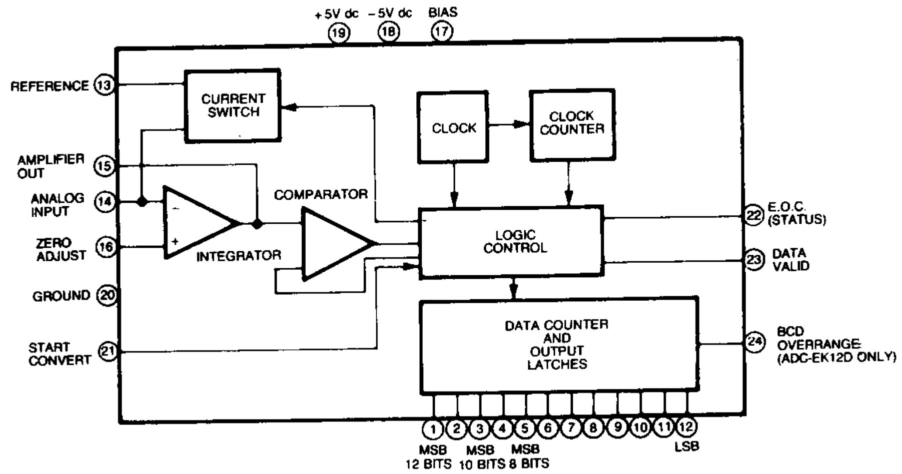
GENERAL DESCRIPTION

The ADC-EK series are low power, integrating A/D converters fabricated on a single monolithic chip using CMOS technology. The circuit employs a charge balancing integrator, current switch comparator, clock counter, data counter, and control logic circuitry to implement conversion. The charge balancing integration technique gives high linearity and noise immunity along with inherent monotonicity resulting in no missing codes. Output data appears in parallel form on latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The ADC-EK series consists of 5 different models with 8-, 10-, and 12-bit binary coding and 3½ digit BCD coding.

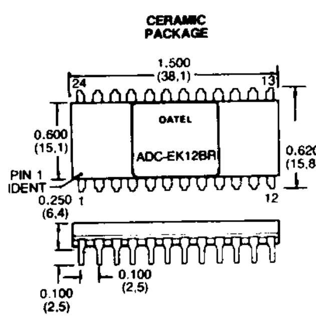
Conversion time is 1.8 to 24 milliseconds maximum depending on model. Nonlinearity is ±½ LSB maximum while differential nonlinearity is ±¼ LSB typical. Other specifications include gain tempco of ±25 ppm/°C typical and zero drift of ±50 μV/°C maximum. An external reference, integrating capacitor, and several other components are required for operation. The analog input voltage range is programmable by means of an external resistor which sets the current into the integrator at 10 μA full scale. Standard operating mode is unipolar but bipolar operation is accomplished using an external op amp to provide an offset current from the reference.

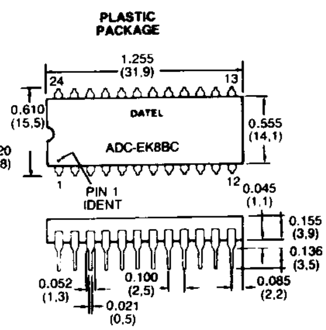
Power requirement is ±5V dc at 2 mA, giving a power consumption of only 20 mW. The units are packaged in 24 pin ceramic or plastic DIP's.

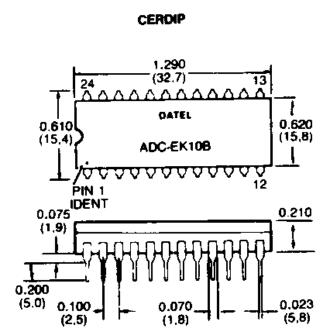
CAUTION: The ADC-EK Series are CMOS devices and should be handled carefully to prevent static charge pickup which might damage the devices. The devices should be kept in the shipping containers until ready for installation.



MECHANICAL DIMENSIONS
INCHES (MM)







INPUT/OUTPUT CONNECTORS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 OUT (MSB−12 BITS)	13	REFERENCE
2	BIT 2 OUT	14	ANALOG INPUT
3	BIT 3 OUT (MSB)−10 BITS	15	AMPLIFIER OUT
4	BIT 4 OUT	16	ZERO ADJUST
5	BIT 5 OUT (MSB−8 BITS)	17	BIAS
6	BIT 6 OUT	18	−5V POWER
7	BIT 7 OUT	19	+5V POWER
8	BIT 8 OUT	20	GROUND
9	BIT 9 OUT	21	START CONVERT
10	BIT 10 OUT	22	E.O.C. (STATUS)
11	BIT 11 OUT	23	DATA VALID
12	BIT 12 OUT (LSB-ALL)	24	BCD OVERRANGE*

*NO CONNECTION FOR OTHER MODELS

NOTE:
For 8- and 10-bit models, do not connect to unused data output terminals since they have internal connections.

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ABSOLUTE MAXIMUM RATINGS	ADC-EK8B/ 10B/12B	ADC-EK12DC/ DR/DM
I_{IN}	±10 mA	
I_{REF}	±10 mA	
Digital Input Voltage	−0.3V to V_{DD} + 0.3V	
$V_{DD} - V_{SS}$	18V	
Package Dissipation	500 mW	

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	See Ordering Information
Storage Temp. Range	−65°C to +150°C
Package	24 Pin DIP

FOOTNOTES:

1. For the ADC-EK 12DM only. Initial gain error is ±5%. Gain. Tempco is ±40 ppm/°C typical, ±80 ppm/°C maximum and Zero Drift Tempco is 80 μV/°C.
2. ADC-EK 12DM outputs can sink and source 500 μA.
3. Supply Sensitivity given for $V_{DD} = V_{SS} = 5V \pm 1V$.

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V Supplies, R_{BIAS} = 100K, unless otherwise noted.

ANALOG INPUTS		
Type Analog Input	Single Ended	
Full Scale Input Current	+10 μA	
Reference Current	−20 μA	
DIGITAL INPUTS		
Logical "1" V_{IN}	3.5V minimum	
Logical "0" V_{IN}	1.5V maximum	
Start Convert Pulse	>3.5V for 500 nanoseconds minimum	
OUTPUTS		
Parallel Output Data	8, 10, 12 Lines	12 Lines and Overrange
Logic "1" Output Voltage	+4.5V minimum at −10 μA. +2.4V minimum at −360 μA[2]	
Logic "0" Output Voltage	+0.4 maximum at −360 μA[2]	
E.O.C. (Status)	High During Conversion, Low When Completed	
Data Valid	High When Data Valid. Low When Data Changing	
PERFORMANCE		
Resolution	8, 10, 12 Bits	3½ Digits
Coding	Straight Binary	BCD
Nonlinearity	½ LSB, maximum	0.025% maximum
Differential Nonlinearity	¼ LSB, typical, ½ LSB maximum	0.025% maximum
Diff. Nonlinearity Tempco	±2.5 ppm/°C typical, ±5 ppm/°C maximum	
No Missing Codes	Over Operating Temperature Range	
Initial Gain Error, Adj. to Zero	+5, −3% maximum[1]	
Gain Temperature Coefficient	±25 ppm/°C typical, ±75 ppm/°C maximum[1]	
Initial Zero Error, Adj. to Zero	±50 mV maximum	
Zero Drift Tempco	±50 μV/°C maximum[1]	
Conversion Time, maximum	1.8 milliseconds (8 Bits) 6 milliseconds (10 Bits) 24 milliseconds (12 Bits)	12 milliseconds (3½ Digits)
Power Supply Sensitivity	±0.05% of Full-Scale Gain[3]	
POWER REQUIREMENTS		
Voltage, Rated Performance	±5V dc	
Voltage Range, Operating	±3.5V dc to ±7V dc	
Supply Quiescent Current		
ADC-EK8B, EK12DC	±5.0 mA	
ADC-EK10B, EK12B, EK12DR	±2.5 mA maximum	
ADC-EK12DM	±3.5 mA maximum	

TECHNICAL NOTES

1. The ADC-EK series are CMOS devices and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive form or shorting all pins together with aluminum foil. Do not connect in circuits under "power on" conditions. The input voltage should be applied after power is on. Do not open circuits the zero adjust, reference, or start convert pins while power is on. It should also be noted that the top and bottom of the ceramic package are connected to the positive supply.
2. Nominal values of input, reference, and offset resistors are given in the resistor table. Due to the possible ±5% tolerance of the external reference and +5% −3% tolerance on the converter scale factor, the actual resistor value can vary by almost ±10% R_G and R_T in the diagrams are for trimming gain and bipolar offset during calibration. It is recommended that R_G be 1% of R_{IN} (nominal) and R_T be 1% of R_{OFF} (nominal). They should both be 100 ppm/°C cermet trimming pots. The recommended procedure for selecting R_{IN} and R_{OFF} is to set the R_G and R_T to center of range and then choose 1% metal film resistor which gives the nearest fit at the full scale point 1111...111 for R_{IN} and one that gives the nearest fit to zero scale point 1000...000 for R_T.
3. To choose any intermediate scale values for R_{IN} and R_T or values of R_{REF} for other reference voltages, use the following formulas:

   $$R_{IN}\,(\text{nominal}) = \frac{FSR}{10\,\mu A}$$ FSR is the full scale range or total input voltage span for the converter.

   $$R_{OFF}\,(\text{nominal}) = \frac{V_{REF}}{5\,\mu A}$$

   $$R_{REF}\,(\text{nominal}) = \frac{V_{REF}}{20\,\mu A}$$

   It is recommended that large full-scale voltage ranges be chosen such as 0 to +10V, 0 to +5V etc., in order to keep the error due to input offset voltage drift to a minimum.
4. The temperature stability of the ADC-EK converters depends directly on the converter itself, R_{IN}, R_{REF}, R_{OFF}, and V_{REF}. Since the converter is typically ±20 ppm/°C it is recommended that a 10 ppm/°C reference be used along with 10 ppm/°C metal film resistors for R_{IN}, R_{REF}, and R_{OFF} for best performance over temperature. On a statistical basis this would give about 28 ppm/°C stability for the complete converter.

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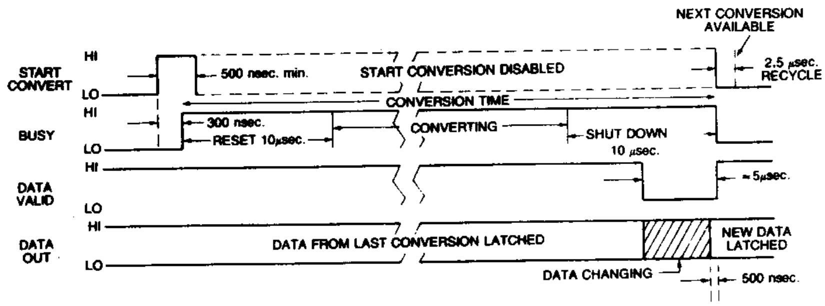
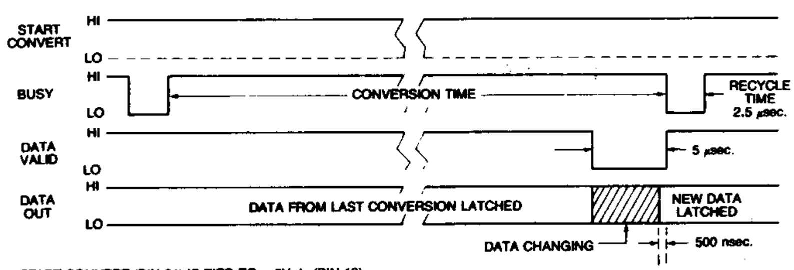
TECHNICAL NOTES (Cont'd)

5. Other passive components used with the converter may have tolerances as indicated here: R_C is a ±10% carbon composition resistor; C_C is a ±20% ceramic capacitor; C_{INT} is a ±10% glass or ceramic capacitor; R_{BIAS} is a ±10% carbon composition resistor; and the two zero adjust resistors are ±10% carbon composition type. It is recommended that two 0.1 μF bypass capacitors be used right at the power supply pins. C_{INT} should be connected as close as possible to pins 14 and 15 away from any noisy lines.
6. The start convert pulse initiates conversion on the low to high transition after which the conversion cycle cannot be interrupted and must run to completion.
7. Logic signals should not be routed under these devices or near the input reference, or zero adjust pins.
8. The unused data output pins on the 8- and 10-bit models should not be used for external connection points since they have internal connections to the converter.
9. All digital outputs will drive 2 low power TTL loads or 1 low power Schottky TTL load. They should not be overloaded as this will affect the performance of the converter.
10. Conversion accuracy is directly dependent on V_{REF}. In order to avoid degrading accuracy, V_{REF} voltage regulation must be ±0.04% for 8 bit models, ±0.01% for 10-bit models and ±0.0025% for 12-bit models.

CLOCKED OPERATION



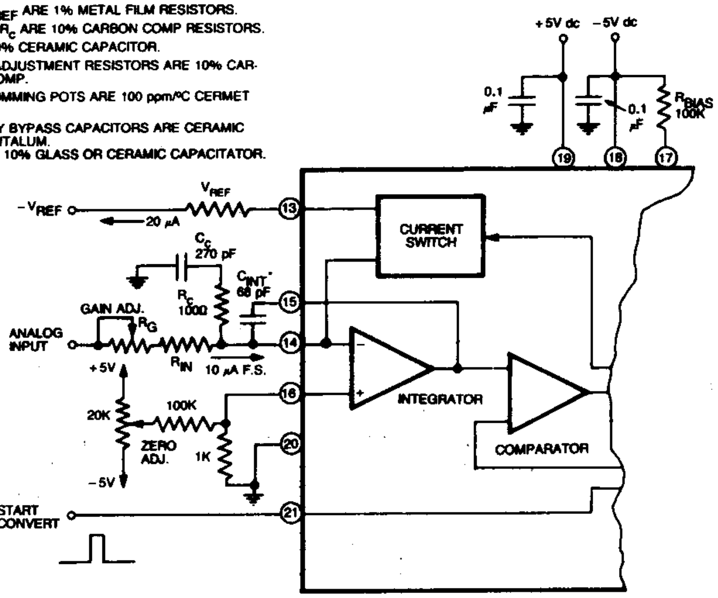
FREE RUNNING OPERATION



START CONVERT (PIN 21) IS TIED TO +5V dc (PIN 19).

CONNECTION FOR UNIPOLAR OPERATION

R_{IN}, R_{REF} ARE 1% METAL FILM RESISTORS.
R_{BIAS}, R_C ARE 10% CARBON COMP RESISTORS.
C_C is 20% CERAMIC CAPACITOR.
ZERO ADJUSTMENT RESISTORS ARE 10% CARBON COMP.
ALL TRIMMING POTS ARE 100 ppm/°C CERMET TYPE.
SUPPLY BYPASS CAPACITORS ARE CERAMIC OR TANTALUM.
C_{INT} IS 10% GLASS OR CERAMIC CAPACITATOR.



*33 pF FOR ADC-EK8B

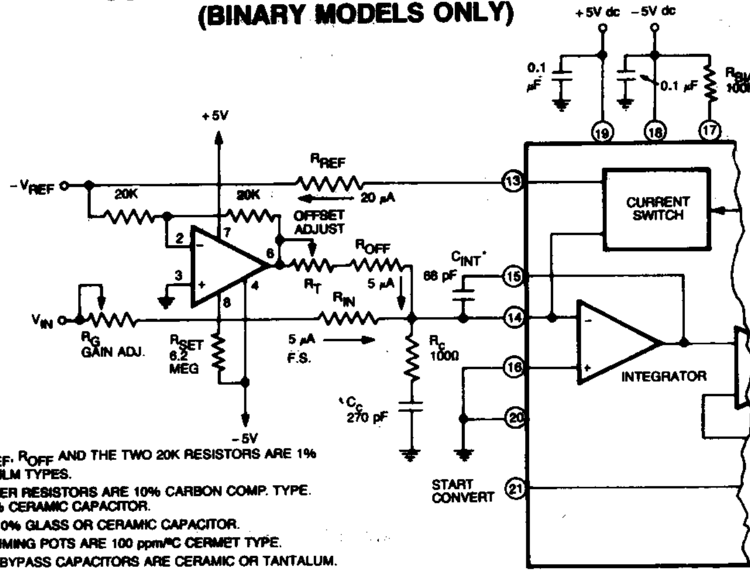
RESISTOR TABLES

UNIPOLAR RANGE	BIPOLAR RANGE	R_{IN} (NOMINAL)
0 TO +2V	±1V	200K
0 TO +5V	±2.5V	500K
0 TO +10V	±5V	1 MEG.
0 TO +20V	±10V	2 MEG.

V_{REF}	R_{REF} (NOMINAL)	R_{OFF} (NOMINAL)
−1.22V	61K	244K
−2.5V	125K	500K
−6.4V	320K	1.28 MEG.

CONNECTIONS

CONNECTION OF BIPOLAR OPERATION (BINARY MODELS ONLY)

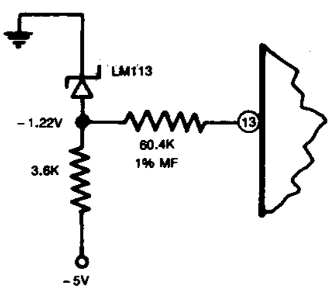


R_{IN}, R_{REF}, R_{OFF} AND THE TWO 20K RESISTORS ARE 1% METAL FILM TYPES.
ALL OTHER RESISTORS ARE 10% CARBON COMP. TYPE.
C_C is 20% CERAMIC CAPACITOR.
C_{INT} IS 10% GLASS OR CERAMIC CAPACITOR.
ALL TRIMMING POTS ARE 100 ppm/°C CERMET TYPE.
SUPPLY BYPASS CAPACITORS ARE CERAMIC OR TANTALUM.

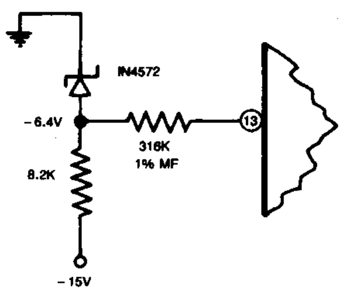
*33 pF FOR ADC-EK8B

REFERENCE CIRCUITS

1.22V BAND GAP REFERENCE USES EXISTING -5V SUPPLY



6.4V ZENER REFERENCE REQUIRES -15V SUPPLY



CODING TABLES

STRAIGHT BINARY

SCALE	8-BIT 0 TO +10V	8-BIT CODE	10-BIT 0 TO +10V	10-BIT CODE	12-BIT 0 TO +10V	12-BIT CODE
FS - 1 LSB	+9.96V	1111 1111	+9.990V	11 1111 1111	+9.9976V	1111 1111 1111
½ FS	+5.00	1000 0000	+5.000	10 0000 0000	+5.0000	1000 0000 0000
1 LSB	+0.04	0000 0001	+0.010	00 0000 0001	+0.0024	0000 0000 0001
0	0.00	0000 0000	0.000	00 0000 0000	0.0000	0000 0000 0000

OFFSET BINARY

SCALE	8-BIT ±5V	8-BIT CODE	10-BIT ±5V	10-BIT CODE	12-BIT ±5V	12-BIT CODE
+FS - 1 LSB	+4.96V	1111 1111	+4.990V	11 1111 1111	+4.9976V	1111 1111 1111
0	0.00	1000 0000	0.000	10 0000 0000	0.0000	1000 0000 0000
-FS + 1 LSB	-4.96	0000 0001	-4.990	00 0000 0001	-4.9976	0000 0000 0001
-FS	-5.00	0000 0000	-5.000	00 0000 0000	-5.0000	0000 0000 0000

BCD

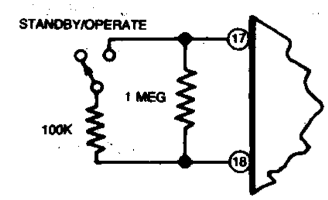
SCALE	FULL SCALE RANGE 0 TO +2V	0 TO +10V	0 TO +20V	CODE
FS - 1 LSB	+1.999V	+9.995V	+19.990V	1 1001 1001 1001
½ FS	+1.000	+5.000	+10.000	1 0000 0000 0000
1 LSB	+0.001	+0.005	+ 0.010	0 0000 0000 0001
0	0.000	0.000	0.000	0 0000 0000 0000

CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagrams for either unipolar or bipolar operation. Determine the input voltage range and select the required input resistors. Apply a logic high to the start convert input (pin 21) to give free-running operation.
2. **Zero and Offset Adjustments.** Apply a precision voltage reference source from the analog input resistor to ground. Adjust the reference source to zero + ½ LSB for unipolar operation or -FS + ½ LSB for bipolar operation. Adjust the zero or offset potentiometer so that the output code flickers between 000....000 and 000....001.
3. **Gain Adjustment.** Set the output of the reference source to +FS - 1½ LSB and adjust the gain trimming potentiometer so that the output code just flickers between 111....110 and 111....111.

   For BCD coding the output code should flicker between 1001 1001 1000 and 1001 1001 1001.

REDUCTION OF STAND-BY POWER



THIS REDUCES POWER CONSUMPTION TO ABOUT 200 μA DURING STANDBY.

ORDERING INFORMATION

MODEL NO.	OPER. TEMP. RANGE	PACKAGE
BINARY		
ADC-EK8B	0°C to +70°C	Plastic
ADC-EK10B	-25°C to +85°C	Cerdip
ADC-EK12B	-25°C to +85°C	Ceramic
BCD		
ADC-EK12DC	0°C to +70°C	Plastic
ADC-EK12DR	-25°C to +85°C	Ceramic
ADC-EK12DM	-55°C to +125°C	Ceramic

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT