Advance Information

MPC8260AEC/D
Rev. 0.7 5/2002

MPC826xA (HiP4) Family
Hardware Specifications

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This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for HiP4-enhanced derivatives of the PowerQUICC II™ MPC8260 communications processor (collectively referred to as the MPC826xA).

The following topics are addressed:

Table 1 shows the functionality that defines each derivative of the HiP4-enhanced PowerQUICC II family.

Table 1. HiP4 PowerQUICC II Family Derivatives

Functionality	Derivatives			
	MPC8260A	MPC8264A	MPC8265A	MPC8266A
HiP4 Process Enhancements	X	X	X	X
PCI Bridge			X	X
Transmission Convergence (TC) Layer		X		X
Inverse Multiplexing for ATM (IMA)		X		X

Until a revision of the current *MPC8260 PowerQUICC II User's Manual* (Rev 0) is available, several addendum documents supply information about the functionality of HiP4-enhanced PowerQUICC II devices. Table 2 lists each device and its related documentation.

Table 2. HiP4 PowerQUICC II Documentation

Document	Derivatives			
	MPC8260A	MPC8264A	MPC8265A	MPC8266A
MPC8260 PowerQUICC II User's Manual, Rev 0 (order number: MPC8260UM/D)	X	X	X	X
MPC8260A (HiP4) Supplement to the MPC8260 PowerQUICC II User's Manual (Preliminary) (order number: MPC8260AUMAD/D)	X	X	X	X
PCI Bridge Functional Specification (Preliminary) (order number: MPC8265AUMAD/D)			X	X
TC Layer Functional Specification (Preliminary) (order number: MPC8264AUMAD/D)		X		X
IMA Functional Specification (Preliminary) (order number: MPC8266AUMAD/D)		X		X

Figure 1 shows the block diagram for the HiP4 superset device, the MPC8266A.

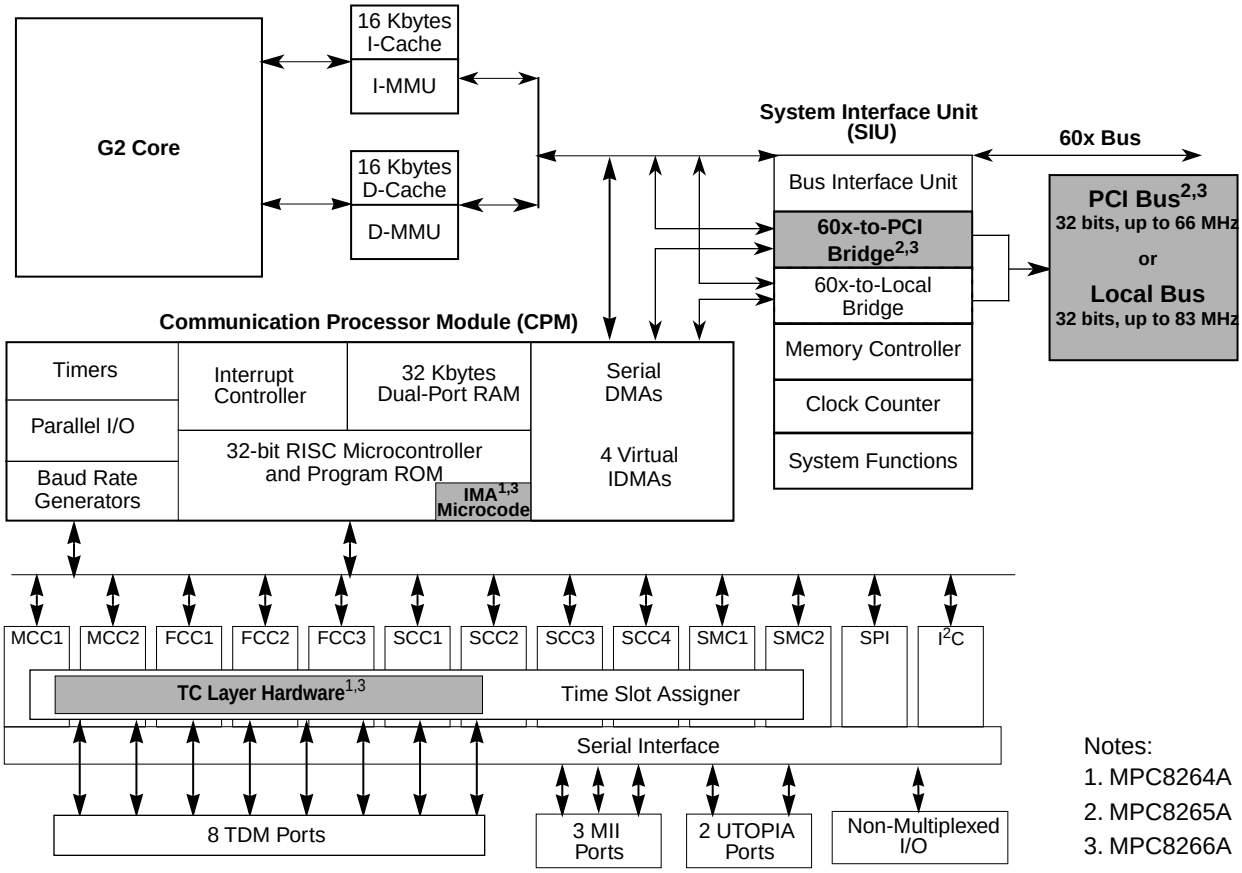


Figure 1. MPC8266A Block Diagram

1.1 Features

The major features of the MPC826xA family are as follows:

- Dual-issue integer core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 150–300 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - PowerPC architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 420 Dhrystones MIPS at 300 MHz)
  - Supports bus snooping for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O

Features

- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge (MPC8265A and MPC8266A only)
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols

- Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
- Serial DMA channels for receive and transmit on all serial channels
- Parallel I/O registers with open-drain and interrupt capability
- Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
- Three fast communications controllers supporting the following protocols:
  - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
  - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
  - Transparent
  - HDLC—Up to T3 rates (clear channel)
- Two multichannel controllers (MCCs)
  - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels.Each MCC can be split into four subgroups of 32 channels each.
  - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
- Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
  - Ethernet/IEEE 802.3 CDMA/CS
  - HDLC/SDLC and HDLC bus
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Binary synchronous (BISYNC) communications
  - Transparent
- Two serial management controllers (SMCs), identical to those of the MPC860
  - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces
  - Supports two groups of four TDM channels for a total of eight TDMs
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization

- Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Motorola interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces

— Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels

— Four independent 16-bit timers that can be interconnected as two 32-bit timers

Additional features of the MPC826xA family are as follows:

- CPM
  - — 32-Kbyte dual-port RAM
  - — Additional MCC host commands
  - — Eight transfer transmission convergence (TC) layers between the TDMs and FCC2 to support inverse multiplexing for ATM capabilities (IMA) (MPC8264A and MPC8266A only)
- CPM multiplexing
  - — FCC2 can also be connected to the TC layer.
- TC layer (MPC8264A and MPC8266A only)
  - — Each of the 8 TDM channels is routed in hardware to a TC layer block
    - Protocol-specific overhead bits may be discarded or routed to other controllers by the SI
    - Performing ATM TC layer functions (according to ITU-T I.432)
    - Transmit (Tx) updates
      - Cell HEC generation
      - Payload scrambling using self synchronizing scrambler (programmable by the user)
      - Coset generation (programmable by the user)
      - Cell rate by inserting idle/unassigned cells
    - Receive (Rx) updates
      - Cell delineation using bit by bit HEC checking and programmable ALPHA and DELTA parameters for the delineation state machine
      - Payload descrambling using self synchronizing scrambler (programmable by the user)
      - Coset removing (programmable by the user)
      - Filtering idle/unassigned cells (programmable by the user)
      - Performing HEC error detection and single bit error correction (programmable by user)
      - Generating loss of cell delineation status/interrupt (LOC/LCD)
  - — Operates with FCC2 (UTOPIA 8)
  - — Provides serial loop back mode
  - — Cell echo mode is provided
  - — Supports both FCC transmit modes
    - External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
    - Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.

— Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
— Cell counters for performance monitoring
  – 16-bit counters count
    – HEC error cells
    – HEC single bit error and corrected cells
    – Idle/unassigned cells filtered
    – Idle/unassigned cells transmitted
    – Transmitted ATM cells
    – Received ATM cells
  – Maskable interrupt is sent to the host when a counter expires
— Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
— May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported

- PCI bridge (MPC8265A and MPC8266A only)
  — PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  — On-chip arbitration
  — Support for PCI to 60x memory and 60x memory to PCI streaming
  — PCI Host Bridge or Peripheral capabilities
  — Includes 4 DMA channels for the following transfers:
    – PCI-to-60x to 60x-to-PCI
    – 60x-to-PCI to PCI-to-60x
    – PCI-to-60x to PCI-to-60x
    – 60x-to-PCI to 60x-to-PCI
  — Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265A) required by the PCI standard as well as message and doorbell registers
  — Supports the I_2O standard
  — Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  — Support for 66 MHz, 3.3 V specification
  — 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
  — Makes use of the local bus signals, so there is no need for additional pins

1.2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC826xA.

1.2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC826xA. Table 3 shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	-0.3 – 2.5	V
PLL supply voltage[2]	VCCSYN	-0.3 – 2.5	V
I/O supply voltage[3]	VDDH	-0.3 – 4.0	V
Input voltage[4]	VIN	GND(-0.3) – 3.6	V
Junction temperature	T_j	120	˚C
Storage temperature range	T_{STG}	(-55) – (+150)	˚C

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.
2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.
3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.
4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 4 lists recommended operational voltage conditions.

Table 4. Recommended Operating Conditions[1]

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.7 – 2.1[2]/ 1.9 –2.1[3]	V
PLL supply voltage	VCCSYN	1.7 – 2.1[2]/1.9–2.1[3]	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (-0.3) – 3.465	V
Junction temperature (maximum)	T_j	105[4]	˚C
Ambient temperature	T_A	0–70[4]	˚C

1 **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.
2 For devices operating at less than 233 MHz CPU, 166 MHz CPM, and 66 MHz bus frequencies.
3 For devices operating at greater than or equal to 233 MHz CPU, 166 MHz CPM, and 66 MHz bus frequencies.
4 Note that for extended temperature parts the range is $(-40)_{T_A}$– 105_{T_j}.

NOTE

VDDH and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (-5% and -0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 5 shows DC electrical characteristics.

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH[1]	I_{IN}	—	10	µA
Hi-Z (off state) leakage current, V_{IN} = VDDH[1]	I_{OZ}	—	10	µA
Signal low input current, V_{IL} = 0.8 V	I_L	—	1	µA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	µA
Output high voltage, I_{OH} = –2 mA except XFC, UTOPIA mode, and open drain pins In UTOPIA mode: I_{OH} = -8.0mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	—	V
In UTOPIA mode: I_{OL} = 8.0mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	—	0.5	V

Table 5. DC Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

Table 5. DC Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA $\overline{CS}$[0-9] $\overline{CS}$(10)/$\overline{BCTL1}$ $\overline{CS}$(11)/AP(0) BADDR[27–28] ALE $\overline{BCTL0}$ $\overline{PWE}$(0:7)/$\overline{PSDDQM}$(0:7)/$\overline{PBS}$(0:7) PSDA10/PGPL0 $\overline{PSDWE}$/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0:3]/LBS[0–3]/PCI_CFG[0–3[2] LSDA10/LGPL0/PCI_MODCKH0[2] LSDWE/LGPL1/PCI_MODCKH1[2] LOE/LSDRAS/LGPL2/PCI_MODCKH2[2] LSDCAS/LGPL3/PCI_MODCKH3[2] LGTA/LUPMWAIT/LGPL4/$\overline{LPBS}$ LSDAMUX/LGPL5/PCI_MODCK[2] $\overline{LWR}$ MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2)	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR[2] L_A15/$\overline{FRAME}$[2]/$\overline{SMI}$ L_A16/$\overline{TRDY}$[2] L_A17/$\overline{IRDY}$[2]/CKSTP_OUT L_A18/$\overline{STOP}$[2] L_A19/$\overline{DEVSEL}$[2] L_A20/IDSEL[2] L_A21/$\overline{PERR}$[2] L_A22/$\overline{SERR}$[2] L_A23/$\overline{REQ0}$[2] L_A24/$\overline{REQ1}$[2]/$\overline{HSEJSW}$[2] L_A25/$\overline{GNT0}$[2] L_A26/$\overline{GNT1}$[2]/$\overline{HSLED}$[2] L_A27/$\overline{GNT2}$[2]/$\overline{HSENUM}$[2] L_A28/$\overline{RST}$[2]/$\overline{CORE\_SRESET}$ L_A29/$\overline{INTA}$[2] L_A30/$\overline{REQ2}$[2] L_A31 LCL_D(0-31)/AD(0-31)[2] LCL_DP(0-3)/C/$\overline{BE}$(0-3)[2] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO				

[1] The leakage current is measured for nominal VDDH and VDD or both VDDH and VDD must vary in the same direction; that is, VDDH and VDD either both vary in the positive direction (+5% and +0.1 Vdc) or both vary in the negative direction (-5% and -0.1 Vdc).

[2] MPC8265A and MPC8266A only.

1.2.2 Thermal Characteristics

Table 6 describes thermal characteristics.

Table 6. Thermal Characteristics

Characteristics	Symbol	Value	Unit	Air Flow
Thermal resistance for TBGA	θ_{JA}	13.07[1]	°C/W	NC[2]
	θ_{JA}	9.55[1]	°C/W	1 m/s
	θ_{JA}	10.48[3]	°C/W	NC
	θ_{JA}	7.78[3]	°C/W	1 m/s

1 Assumes a single layer board with no thermal vias
2 Natural convection
3 Assumes a four layer board

1.2.3 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K/(T_J + 273° C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273° C) + \theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

1.2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC826xA have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 7 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3W (when the ambient temperature is 70˚ C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 7. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W)[2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

[1] Test temperature = room temperature (25˚ C)
[2] $P_{INT} = I_{DD} \times V_{DD}$ Watts

1.2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC826xA device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 8.

Table 8. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

[1] These are typical values at 65˚ C. The impedance may vary by ±25% with process and temperature.

Table 9 lists CPM output characteristics.

Table 9. AC Characteristics for CPM Outputs[1]

Spec_num Max/Min	Characteristic	Max Delay (ns)		Min Delay (ns)	
		66 MHz	83 MHz	66 MHz	83 MHz
sp36a/sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b/sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40/sp41	TDM outputs/SI	25	16	5	4
sp38a/sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b/sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42/sp43	PIO/TIMER/DMA outputs	14	11	1	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 10 lists CPM input characteristics.

Table 10. AC Characteristics for CPM Inputs[1]

Spec_num	Characteristic	Setup (ns)		Hold (ns)	
		66 MHz	83 MHz	66 MHz	83 MHz
sp16a/sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b/sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20/sp21	TDM inputs/SI	15	12	12	10
sp18a/sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b/sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22/sp23	PIO/TIMER/DMA inputs	10	8	3	3

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 2 shows the FCC external clock.

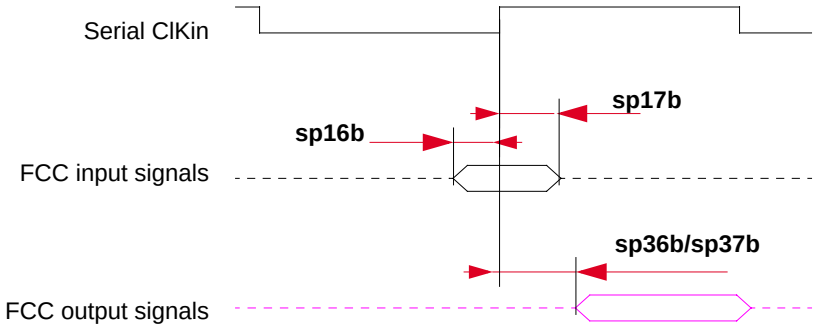


Figure 2. FCC External Clock Diagram

Figure 3 shows the FCC internal clock.

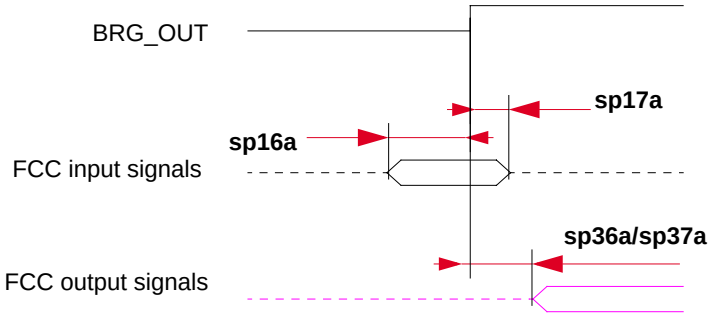


Figure 3. FCC Internal Clock Diagram

Figure 4 shows the SCC/SMC/SPI/I^{2}C external clock.

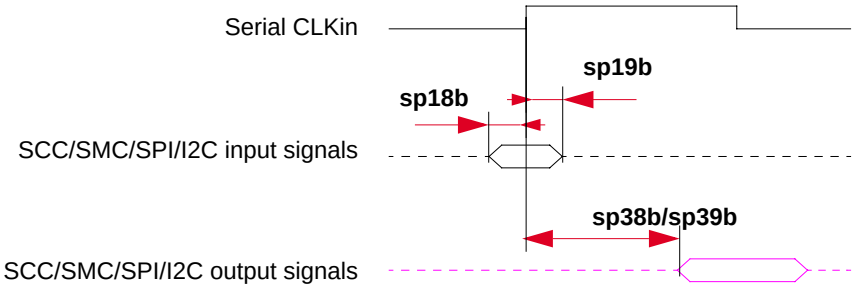


Figure 4. SCC/SMC/SPI/I^{2}C External Clock Diagram

Figure 5 shows the SCC/SMC/SPI/I^{2}C internal clock.

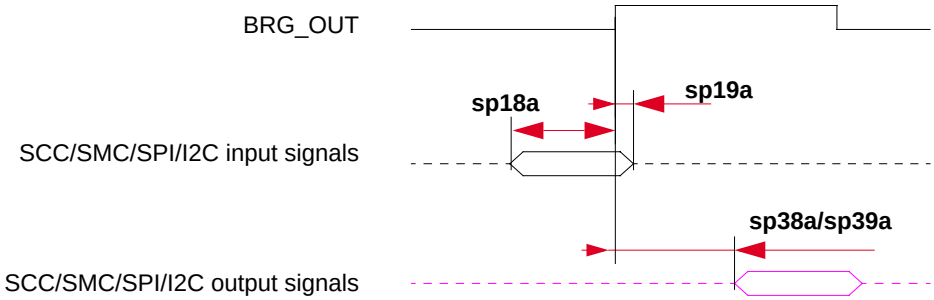


Figure 5. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

Figure 6 shows PIO, timer, and DMA signals.

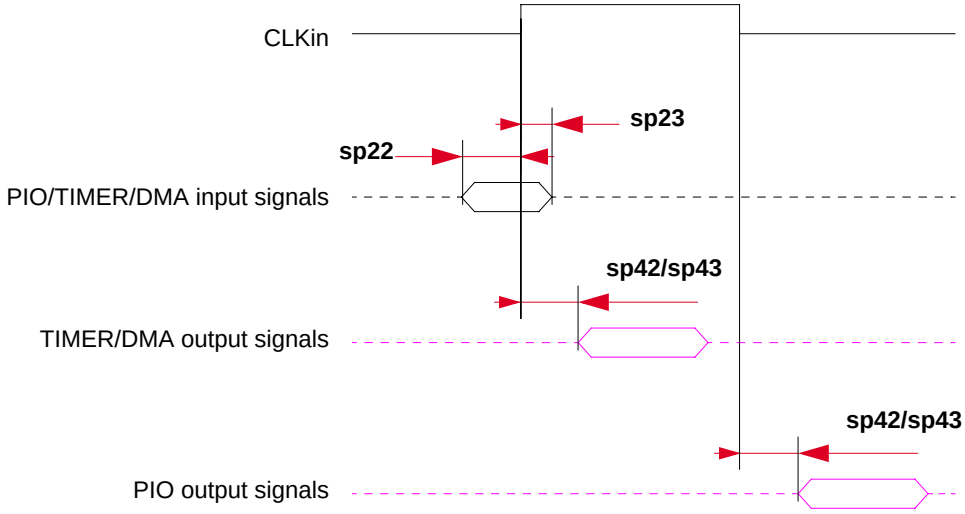


Figure 6. PIO, Timer, and DMA Signal Diagram

Table 12 lists SIU input characteristics.

Table 11. AC Characteristics for SIU Inputs[1]

Spec_num	Characteristic	Setup (ns)		Hold (ns)	
		66 MHz	83 MHz	66 MHz	83 MHz
sp11/sp10	$\overline{AACK}/\overline{ARTRY}/\overline{TA}/\overline{TS}/\overline{TEA}/\overline{DBG}/\overline{BG}/\overline{BR}$	6	5	1	1
sp12/sp10	Data bus in normal mode	5	4	1	1
sp13/sp10	Data bus in ECC and PARITY modes	8	6	1	1
sp14/sp10	DP pins	7	6	1	1
sp15/sp10	All other pins	5	4	1	1

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 12 lists SIU output characteristics.

Table 12. AC Characteristics for SIU Outputs[1]

Spec_num Max/Min	Characteristic	Max Delay (ns)		Min Delay (ns)	
		66 MHz	83 MHz	66 MHz	83 MHz
sp31/sp30	$\overline{PSDVAL}/\overline{TEA}/\overline{TA}$	7	6	0.5	0.5
sp32/sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a/sp30	Data bus	6.5	6.5	0.5	0.5
sp33b/sp30	DP	8	7	0.5	0.5
sp34/sp30	memc signals/ALE	6	5	0.5	0.5
sp35/sp30	all other signals	6	5.5	0.5	0.5

[1] Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 7 shows TDM input and output signals.

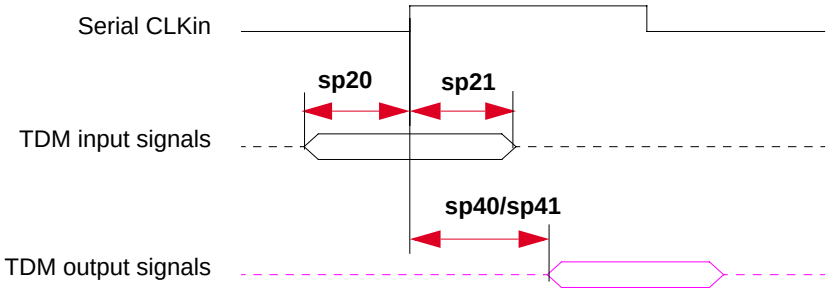


Figure 7. TDM Signal Diagram

Figure 8 shows the interaction of several bus signals.

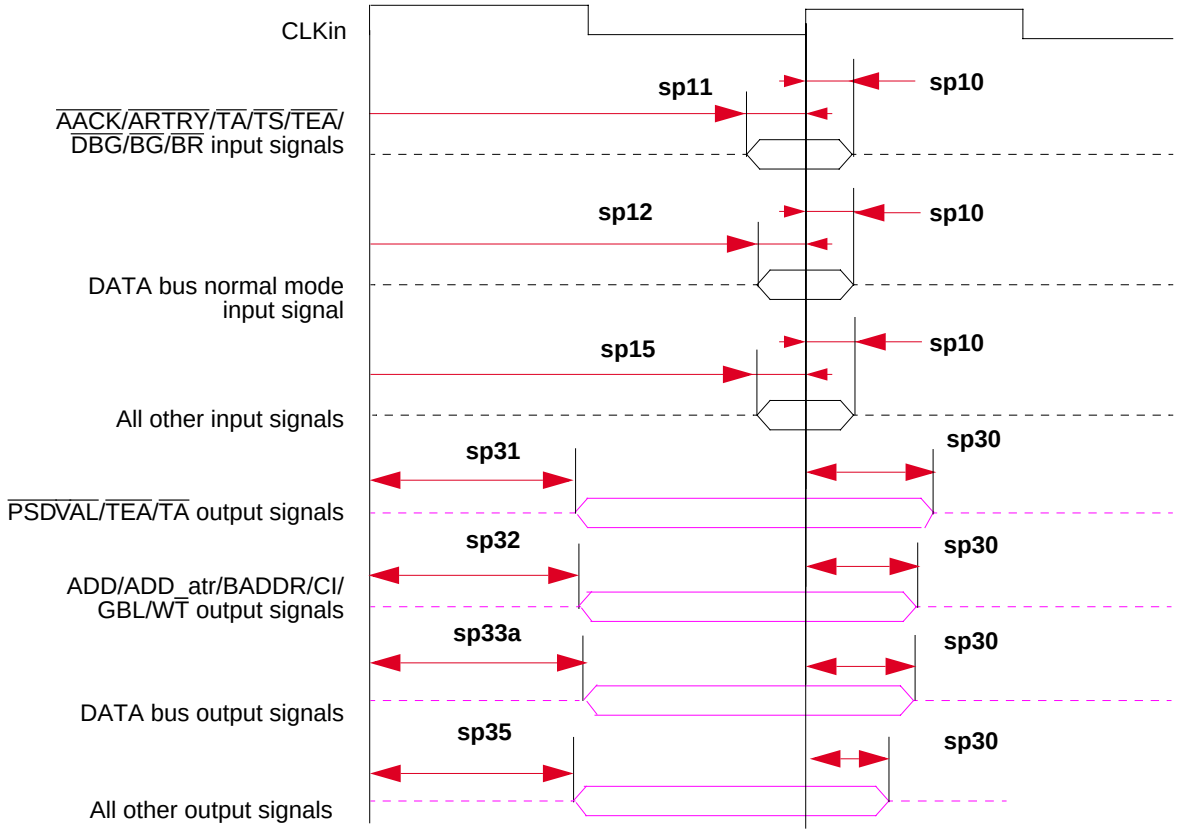


Figure 8. Bus Signals

Figure 9 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

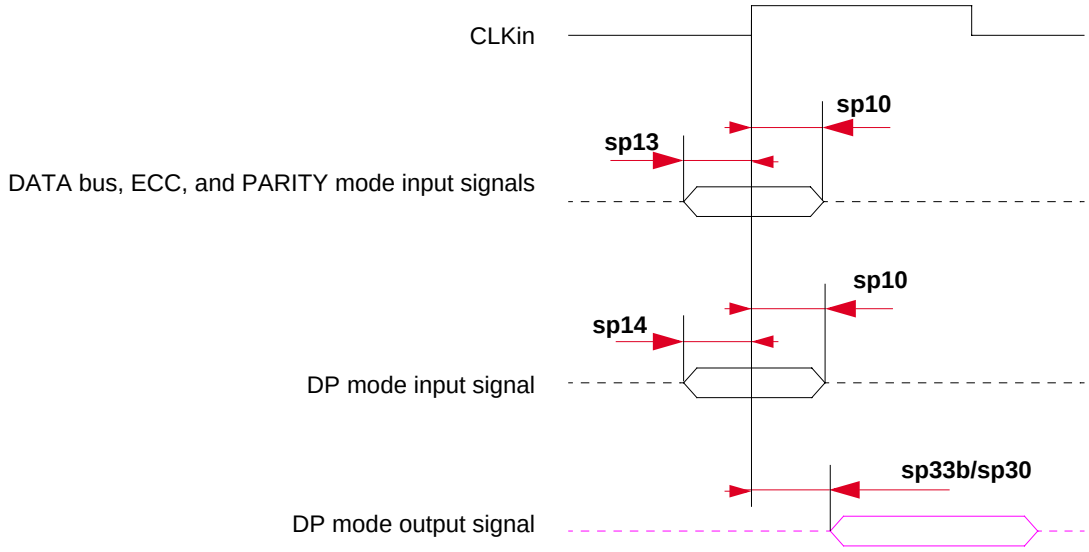


Figure 9. Parity Mode Diagram

Figure 10 shows signal behavior in MEMC mode.

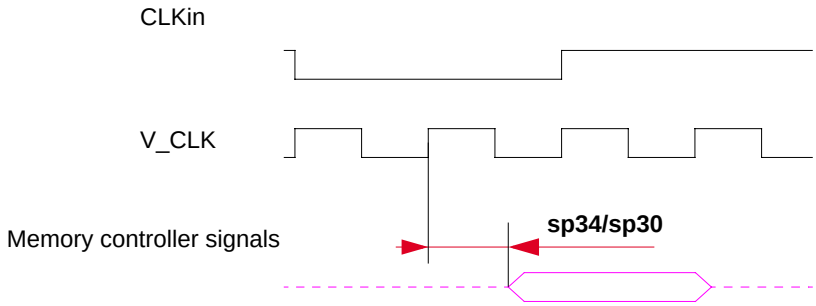


Figure 10. MEMC Mode Diagram

NOTE

Generally, all MPC826xA bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 13.

Table 13. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 11 is a graphical representation of Table 13.

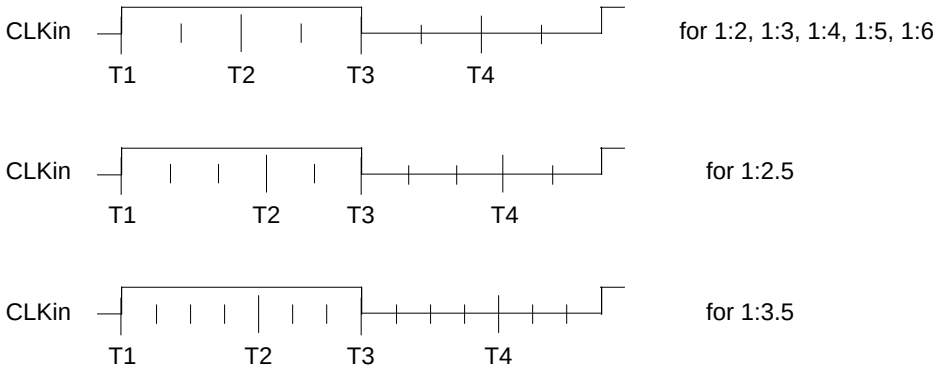


Figure 11. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

1.3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 14 shows the eight basic configuration modes. Another 49 modes are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

1.3.1 Local Bus Mode

Table 14 describes default clock modes for the MPC826xA.

Table 14. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 15 describes all possible clock configurations when using the hard reset configuration sequence. Note that clock configuration changes only after $\overline{\text{POR}}$ is asserted. Note also that basic modes are shown in boldface type.

Table 15. Clock Configuration Modes[1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz
0001_101	**33 MHz**	**3**	**100 MHz**	4	**133 MHz**
0001_110	**33 MHz**	**3**	**100 MHz**	5	**166 MHz**
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	**33 MHz**	**4**	**133 MHz**	**4**	**133 MHz**
0010_011	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz

Table 15. Clock Configuration Modes[1] (Continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**
0101_111	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**
0110_101	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz

Table 15. Clock Configuration Modes[1] (Continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz
1100_000[4]	66 MHz	2	133 MHz	Bypass	66 MHz
1100_001[4]	66 MHz	2.5	166 MHz	Bypass	66 MHz
1100_010[4]	66 MHz	3	200 MHz	Bypass	66 MHz

1 Because of speed dependencies, not all of the possible configurations in Table 15 are applicable.

2 The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than150 MHz and the CPM ranges between 66–233 MHz.

3 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 66 MHz input clock and MODCK_H–MODCK_L[0111–101] (with a core multiplication factor of 4 and a CPM multiplication factor of 3). The resulting configuration equals the part's maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, and 66 MHz bus.
2. 50 MHz input clock and MODCK_H–MODCK_L[0111–101] to achieve a configuration of 200 MHz CPU, 150 MHz CPM, and 50 MHz bus.
3. 40 MHz input clock and MODCK_H–MODCK_L[0010–011] to achieve a configuration of 200 MHz CPU, 160 MHz CPM, and 40 MHz bus.

Note that with each example, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part's rating.

4 At this mode the CPU PLL is bypassed (the CPU frequency equals the bus frequency).

1.3.2 PCI Mode

This section pertains to the MPC8265A and the MPC8266A only.

In PCI mode only, MODCK_HI[0:3] and PCI_MODCK come from the following external pins:

- **PCI_MODCK** = LGPL5
- **MODCK_HI[0:3]** = {LGPL0,LGPL1,LGPL2,LGPL3}

NOTE

The minimum Tval = 2 when PCI_MODCK = 1 and minimum Tval = 1 when PCI_MODCK = 0; therefore, board designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

Table 16. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

[1] Assumes MODCK_HI = 0000.
[2] The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.)

Table 17 describes all possible clock configurations when using the MPC8265A or the MPC8266A’s internal PCI bridge in host mode.

Table 17. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0001_000	**33 MHz**	**3**	**100 MHz**	5	**166 MHz**	**3/6**	**33/16 MHz**
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**	**4/8**	**33/16 MHz**
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000[3]	33 MHz	5	166 MHz	5	166 MHz	5	**33 MHz**
0011_001[3]	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz
0011_010[3]	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (Continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2/4**	**66/33 MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	**3/6**	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	**3/6**	**55/28 MHz**
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	**50/25 MHz**
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (Continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz
1100_000[4]	66MHz	2	133MHz	Bypass	66MHz	2/4	66/33 MHz
1100_001[4]	66MHz	2.5	166MHz	Bypass	66MHz	3/6	55/28 MHz
1100_010[4]	66MHz	3	200MHz	Bypass	66MHz	3/6	66/33 MHz

[1] Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 66 MHz input clock, MODCK_H–MODCK_L[0111–011] (with a core multiplication factor of 4 and a CPM multiplication factor of 3), and PCI_MODCK = 0 (see note 2 below). The resulting configuration equals the part's maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, 66 MHz 60x bus, and a PCI frequency of 66 MHz.
2. 50 MHz input clock, MODCK_H–MODCK_L[0111–011], and PCI_MODCK = 0 (see note 2below) to achieve a configuration of 200 MHz CPU, 150 MHz CPM, 50 MHz 60x bus, and a PCI frequency of 50 MHz.
3. 40 MHz input clock, MODCK_H–MODCK_L[0010–000], and PCI_MODCK = 0 (see note 2 below) to achieve a configuration of 200 MHz CPU, 160 MHz CPM, 40 MHz 60x bus, and a PCI frequency of 40 MHz.

Note that with each of the examples, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part's rating.

[2] The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.).

[3] In this mode, PCI_MODCK must be "0".

[4] In this mode the Core PLL is bypassed (core frequency equals to bus frequency; for debug purpose only).

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)[1]

MODCK[1–3][2]	Input Clock Frequency (PCI)[3]	CPM Multiplication Factor[3]	CPM Frequency	Core Multiplication Factor	Core Frequency[4]	Bus Division Factor	60x Bus Frequency[5]
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)[1] (Continued)

MODCK[1–3][2]	Input Clock Frequency (PCI)[3]	CPM Multiplication Factor[3]	CPM Frequency	Core Multiplication Factor	Core Frequency[4]	Bus Division Factor	60x Bus Frequency[5]
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

1 The user should verify that all buses and functions run frequencies that are within the supported ranges.
2 Assumes MODCK_HI = 0000.
3 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2.
4 Core frequency = (60x bus frequency)(core multiplication factor)
5 Bus frequency = CPM frequency / bus division factor

Table 19 describes all possible clock configurations when using the MPC8265A or the MPC8266A’s internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode [1]

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[2,3]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[4]	Bus Division Factor	60x Bus Frequency[5]
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	**150 MHz**	3	180 MHz	**2.5**	**60 MHz**
0010_010	50/25 MHz	3/6	**150 MHz**	3.5	210 MHz	**2.5**	**60 MHz**
0010_011	50/25 MHz	3/6	**150 MHz**	4	240 MHz	**2.5**	**60 MHz**
0010_100	50/25 MHz	3/6	**150 MHz**	4.5	270 MHz	**2.5**	**60 MHz**
0011_000	**66/33 MHz**	2/4	**133 MHz**	2.5	**110MHz**	**3**	**44 MHz**
0011_001	66/33 MHz	2/4	**133 MHz**	3	132 MHz	3	**44 MHz**
0011_010	66/33 MHz	2/4	**133 MHz**	3.5	154 MHz	3	**44 MHz**
0011_011	66/33 MHz	2/4	**133 MHz**	4	176MHz	3	**44 MHz**
0011_100	66/33 MHz	2/4	**133 MHz**	4.5	198 MHz	3	**44 MHz**
0100_000	**66/33 MHz**	**3/6**	**200 MHz**	2.5	**166 MHz**	**3**	**66 MHz**
0100_001	66/33 MHz	3/6	**200 MHz**	3	200 MHz	**3**	**66 MHz**
0100_010	66/33 MHz	3/6	**200 MHz**	3.5	233 MHz	**3**	**66 MHz**
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**

Table 19. Clock Configuration Modes in PCI Agent Mode (Continued)[1]

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[2,3]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[4]	Bus Division Factor	60x Bus Frequency[5]
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000[6]	33 MHz	5	166 MHz	2.5	**166 MHz**	2.5	**66 MHz**
0101_001[6]	33 MHz	5	166 MHz	3	200 MHz	2.5	**66 MHz**
0101_010[6]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[6]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[6]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (Continued)[1]

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[2,3]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[4]	Bus Division Factor	60x Bus Frequency[5]
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz
1100_000[7]	66/33MHz	2/4	133MHz	Bypass	66MHz	2	66 MHz
1100_001[7]	66/33MHz	3/6	200MHz	Bypass	80MHz	2.5	80 MHz
1100_010[7]	66/33MHz	3/6	200MHz	Bypass	66MHz	3	66 MHz

1 The user should verify that all buses and functions run frequencies that are within the supported ranges.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2.

3 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user’s part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 50 MHz input clock, MODCK_H–MODCK_L[0110–011] (with a core multiplication factor of 4, a CPM multiplication factor of 4, and a bus division factor of 3), and PCI_MODCK = 0 (see note 2 above). The PCI frequency is 50 MHz and the resulting configuration equals the part’s maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, and 66 MHz 60x bus.
2. 66 MHz input clock, MODCK_H–MODCK_L[0100–001], and PCI_MODCK = 1 (see note 2 above) to achieve a PCI frequency of 33 MHz and a configuration of 200MHz CPU, 200 MHz CPM, and 66 MHz 60x bus.
3. 40 MHz input clock, MODCK_H–MODCK_L[1001–011], and PCI_MODCK = 0 (see note 2 above) to achieve a PCI frequency of 40 MHz and a configuration of 160 MHz CPU, 160 MHz CPM, and 40 MHz 60x bus.

Note that with each of the examples, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part’s rating.

4 Core frequency = (60x bus frequency)(core multiplication factor)

5 Bus frequency = CPM frequency / bus division factor

6 In this mode, PCI_MODCK must be “1”.

7 In this mode the Core PLL is bypassed (core frequency equals bus frequency; for debug purpose only).

1.4 Pinout

This section provides the pin assignments and pinout list for the MPC826xA.

1.4.1 Pin Assignments

Figure 12 shows the pinout of the MPC826xA's 480 TBGA package as viewed from the top surface.

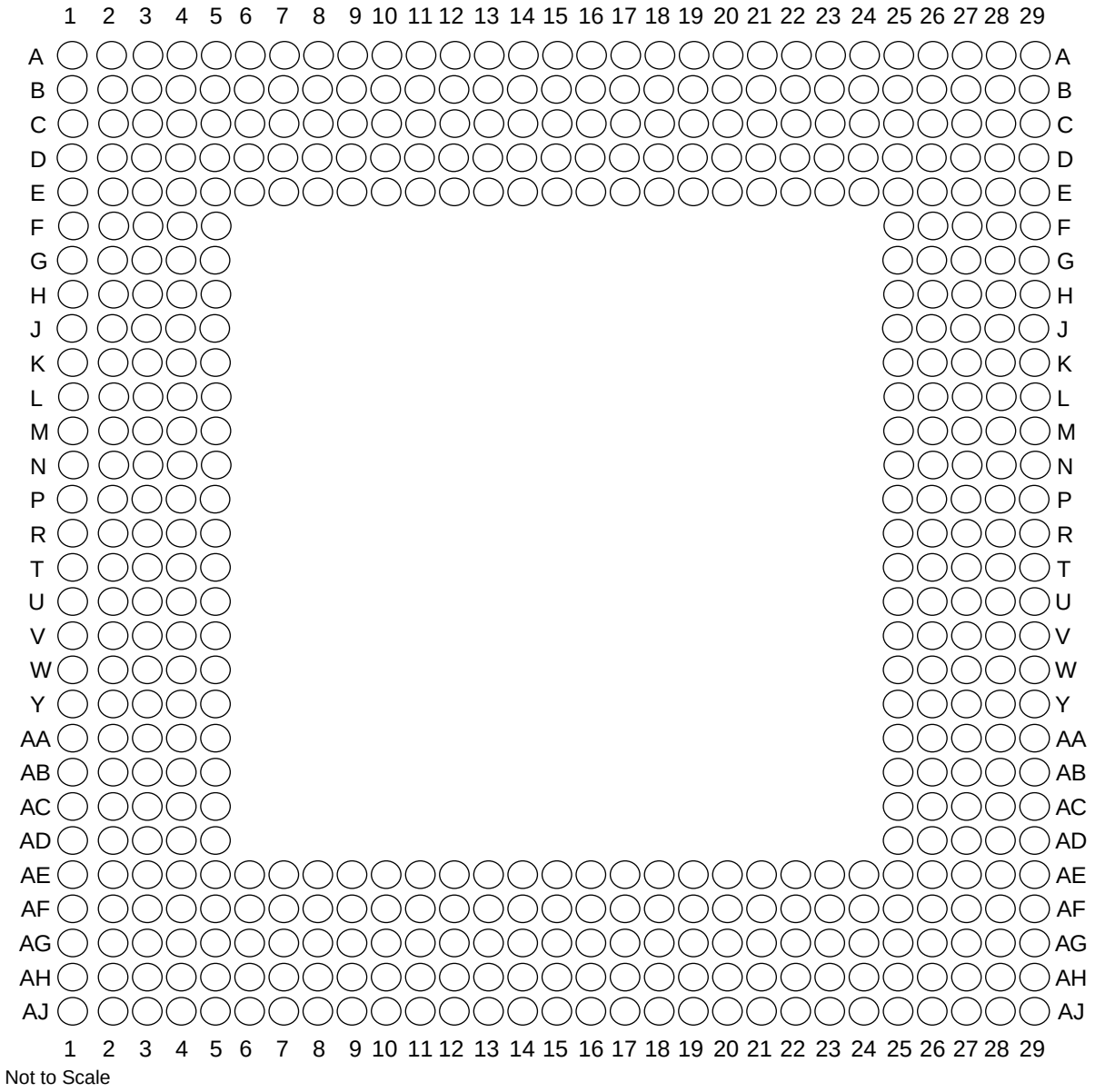


Figure 12. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Figure 13 shows the side profile of the TBGA package to indicate the direction of the top surface view.

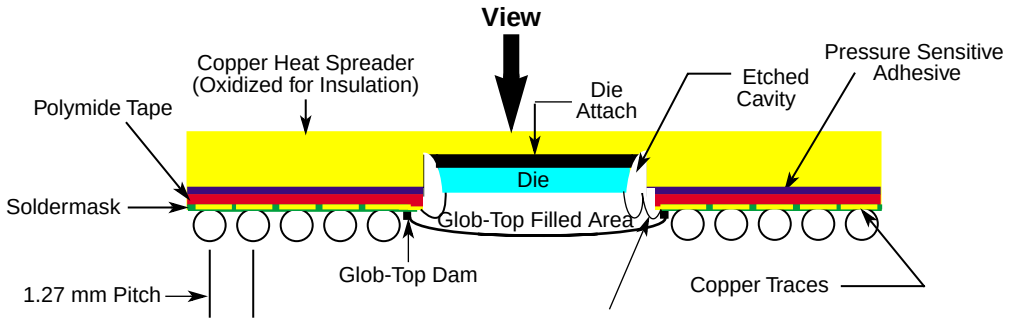


Figure 13. Side View of the TBGA Package

Table 20 shows the pinout list of the MPC826xA. Table 21 defines conventions and acronyms used in Table 20.

Table 20. Pinout List

Pin Name	Ball
$\overline{BR}$	W5
$\overline{BG}$	F4
$\overline{ABB}$/$\overline{IRQ2}$	E2
$\overline{TS}$	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1
A18	M5
A19	N5

Table 20. Pinout List (Continued)

Pin Name	Ball
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
$\overline{\text{TBST}}$	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
$\overline{\text{AACK}}$	F3
$\overline{\text{ARTRY}}$	E1
$\overline{\text{DBG}}$	V1
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20

Table 20. Pinout List (Continued)

Pin Name	Ball
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12

Table 20. Pinout List (Continued)

Pin Name	Ball
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/TLBISYNC/$\overline{\text{EXT\_DBG2}}$	E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	B21
$\overline{\text{IRQ6}}$/DP6/CSE0	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20
$\overline{\text{PSDVAL}}$	V3
$\overline{\text{TA}}$	C22
$\overline{\text{TEA}}$	V5
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$	W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	U2
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$	U3
$\overline{\text{L2\_HIT}}$/$\overline{\text{IRQ4}}$	Y4

Table 20. Pinout List (Continued)

Pin Name	Ball
CPU_BG/BADDR31/IRQ5	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
CS10/BCTL1	F29
CS11/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/LBS0/PCI_CFG0[1]	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1[1]	H27

Table 20. Pinout List (Continued)

Pin Name	Ball
$\overline{\text{LWE2}}$/$\overline{\text{LSDDQM2}}$/$\overline{\text{LBS2}}$/PCI_CFG2[1]	H26
$\overline{\text{LWE3}}$/$\overline{\text{LSDDQM3}}$/$\overline{\text{LBS3}}$/PCI_CFG3[1]	G29
LSDA10/LGPL0/PCI_MODCKH0[1]	D27
$\overline{\text{LSDWE}}$/LGPL1/PCI_MODCKH1[1]	C28
$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$/LGPL2/PCI_MODCKH2[1]	E26
$\overline{\text{LSDCAS}}$/LGPL3/PCI_MODCKH3[1]	D25
$\overline{\text{LGTA}}$/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$	C26
LGPL5/LSDAMUX/PCI_MODCK[1]	B27
$\overline{\text{LWR}}$	D28
L_A14/PAR[1]	N27
L_A15/$\overline{\text{FRAME}}$[1]/$\overline{\text{SMI}}$	T29
L_A16/$\overline{\text{TRDY}}$[1]	R27
L_A17/$\overline{\text{IRDY}}$[1]/$\overline{\text{CKSTP\_OUT}}$	R26
L_A18/$\overline{\text{STOP}}$[1]	R29
L_A19/$\overline{\text{DEVSEL}}$[1]	R28
L_A20/IDSEL[1]	W29
L_A21/$\overline{\text{PERR}}$[1]	P28
L_A22/$\overline{\text{SERR}}$[1]	N26
L_A23/$\overline{\text{REQ0}}$[1]	AA27
L_A24/$\overline{\text{REQ1}}$[1]/HSEJSW[1]	P29
L_A25/$\overline{\text{GNT0}}$[1]	AA26
L_A26/$\overline{\text{GNT1}}$[1]/HSLED[1]	N25
L_A27/$\overline{\text{GNT2}}$[1]/$\overline{\text{HSENUM}}$[1]	AA25
L_A28/$\overline{\text{RST}}$[1]/$\overline{\text{CORE\_SRESET}}$	AB29
L_A29/$\overline{\text{INTA}}$[1]	AB28
L_A30/$\overline{\text{REQ2}}$[1]	P25
L_A31/DLLOUT[1]	AB27
LCL_D0/AD0[1]	H29
LCL_D1/AD1[1]	J29
LCL_D2/AD2[1]	J28
LCL_D3/AD3[1]	J27
LCL_D4/AD4[1]	J26
LCL_D5/AD5[1]	J25
LCL_D6/AD6[1]	K25
LCL_D7/AD7[1]	L29

Table 20. Pinout List (Continued)

Pin Name	Ball
LCL_D8/AD8[1]	L27
LCL_D9/AD9[1]	L26
LCL_D10/AD10[1]	L25
LCL_D11/AD11[1]	M29
LCL_D12/AD12[1]	M28
LCL_D13/AD13[1]	M27
LCL_D14/AD14[1]	M26
LCL_D15/AD15[1]	N29
LCL_D16/AD16[1]	T25
LCL_D17/AD17[1]	U27
LCL_D18/AD18[1]	U26
LCL_D19/AD19[1]	U25
LCL_D20/AD20[1]	V29
LCL_D21/AD21[1]	V28
LCL_D22/AD22[1]	V27
LCL_D23/AD23[1]	V26
LCL_D24/AD24[1]	W27
LCL_D25/AD25[1]	W26
LCL_D26/AD26[1]	W25
LCL_D27/AD27[1]	Y29
LCL_D28/AD28[1]	Y28
LCL_D29/AD29[1]	Y25
LCL_D30/AD30[1]	AA29
LCL_D31/AD31[1]	AA28
LCL_DP0/C0[1]/$\overline{\text{BE0}}$[1]	L28
LCL_DP1/C1[1]/$\overline{\text{BE1}}$[1]	N28
LCL_DP2/C2[1]/$\overline{\text{BE2}}$[1]	T28
LCL_DP3/C3[1]/$\overline{\text{BE3}}$[1]	W28
$\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$	T1
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$/$\overline{\text{APE}}$	D1
$\overline{\text{TRST}}$	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5

Table 20. Pinout List (Continued)

Pin Name	Ball
$\overline{\text{TRIS}}$	AB4
$\overline{\text{PORESET}}$	AG6
$\overline{\text{HRESET}}$	AH5
$\overline{\text{SRESET}}$	AF6
$\overline{\text{QREQ}}$	AA3
$\overline{\text{RSTCONF}}$	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3/FCC2_UTM_TXADDR2	AC29
PA1/$\overline{\text{REJECT1}}$/FCC2_UTM_TXADDR1/$\overline{\text{DONE3}}$	AC25
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{\text{DACK3}}$	AE28
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{\text{DACK4}}$/L1RXD1A2	AG29
PA4/$\overline{\text{REJECT2}}$/FCC2_UTM_RXADDR1/$\overline{\text{DONE4}}$	AG28
PA5/$\overline{\text{RESTART2}}$/DREQ4/FCC2_UTM_RXADDR2	AG26
PA6/L1RSYNCA1	AE24
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23
PA9/SMTXD2/L1TXD0A1	AH23
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11

Table 20. Pinout List (Continued)

Pin Name	Ball
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7
PA28/FCC1_UTM_RXENB/FCC1_UTS_RXENB/FCC1_MII_TX_EN	AD5
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/FCC1_RTS	AD3
PA31/FCC1_UTM_TXENB/FCC1_UTS_TXENB/FCC1_MII_COL	AB5
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/FCC3_RTS	AD28
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22
PB13/FCC3_MII_COL/L1RQB1/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17
PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14
PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13
PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12
PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2/ L1TXD2A1	AH11
PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_TXD/L1RXD1A1/L1RXDD2	AH16
PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1TXDD2	AE15
PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2	AJ9
PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9
PB26/FCC2_MII_CRS/FCC2_UT8_TXD1/L1RXDC2	AJ7
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6
PB28/FCC2_MII_RX_ER/FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1	AE3
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/ FCC2_MII_TX_EN	AE2

Table 20. Pinout List (Continued)

Pin Name	Ball
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2	AC5
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29
PC2/$\overline{\text{FCC3\_CD}}$/FCC2_UT8_TXD3/$\overline{\text{DONE2}}$	AE29
PC3/$\overline{\text{FCC3\_CTS}}$/FCC2_UT8_TXD2/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE27
PC4/$\overline{\text{FCC2\_UTM\_RXENB}}$/$\overline{\text{FCC2\_UTS\_RXENB}}$/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AF27
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AF24
PC6/$\overline{\text{FCC1\_CD}}$/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AJ26
PC7/$\overline{\text{FCC1\_CTS}}$/$\overline{\text{L1RQC1}}$/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AJ25
PC8/$\overline{\text{CD4}}$/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22
PC9/$\overline{\text{CTS4}}$/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21
PC10/$\overline{\text{CD3}}$/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AF20
PC11/$\overline{\text{CTS3}}$/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19
PC12/$\overline{\text{CD2}}$/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18
PC13/$\overline{\text{CTS2}}$/CLSN2/$\overline{\text{L1RQD1}}$/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18
PC14/$\overline{\text{CD1}}$/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16
PC16/CLK16/TIN4	AF15
PC17/CLK15/TIN3/BRGO8	AJ15
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14
PC19/CLK13/BRGO7	AG13
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12
PC21/CLK11/BRGO6	AJ11
PC22/CLK10/$\overline{\text{DONE1}}$	AG10
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10
PC24/FCC2_UT8_TXD3/CLK8/$\overline{\text{TOUT4}}$	AF9
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2
PC30/FCC2_UT8_TXD3/CLK2/$\overline{\text{TOUT1}}$	AE1
PC31/CLK1/BRGO1	AD1

Table 20. Pinout List (Continued)

Pin Name	Ball
PD4/BRGO8/L1TSYNCD1/L1GNTD1/FCC3_RTS/SMRXD2	AC28
PD5/FCC1_UT16_TXD3/DONE1	AD27
PD6/FCC1_UT16_TXD4/DACK1	AF29
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/FCC1_TXCLAV2	AF28
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27
PD11/L1RQB2/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23
PD12/SI1_L1ST2/L1RXDB1	AG23
PD13/SI1_L1ST1/L1TXDB1	AJ22
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20
PD15/FCC1_UT16_RXD1/L1RQC2/I2CSDA	AJ20
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/FCC1_UTM_RXCLAV3/SPICLK	AF16
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/FCC1_UTM_TXCLAV3/SPISEL/BRGO1	AH15
PD20/RTS4/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12
PD23/RTS3/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9
PD26/RTS2/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4
PD29/RTS1/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2	AG1
PD30/FCC2_UTM_TXENB/FCC2_UTS_TXENB/TXD1	AD4
PD31/RXD1	AD2
VCCSYN	AB3
VCCSYN1	B9
GNDSYN	AB1
CLKIN2[1,2]	AE11
SPARE4[3]	U5
PCI_MODE[1,4]	AF25

Table 20. Pinout List (Continued)

Pin Name	Ball
SPARE6[3]	V4
THERMAL0[5]	AA1
THERMAL1[5]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 MPC8265A and MPC8266A only.
2 On PCI devices (MPC8265A and MPC8266A) this pin should be used as CLKIN2. On non-PCI devices (MPC8260A and MPC8264A) this is a spare pin that must be pulled down or left floating.
3 Must be pulled down or left floating.
4 On PCI devices (MPC8265A and MPC8266A) this pin should be asserted if the PCI function is desired or pulled up or left floating if PCI is not desired. On non-PCI devices (MPC8260A and MPC8264A) this is a spare pin that must be pulled up or left floating.
5 For information on how to use this pin, refer to MPC8260 PowerQUICC II Thermal Resistor Guide available at www.motorola.com/semiconductors.

Symbols used in Table 20 are described in Table 21.

Table 21. Symbol Legend

Symbol	Meaning
$\overline{\text{OVERBAR}}$	Signals with overbars, such as $\overline{\text{TA}}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

1.5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC826xA.

1.5.1 Package Parameters

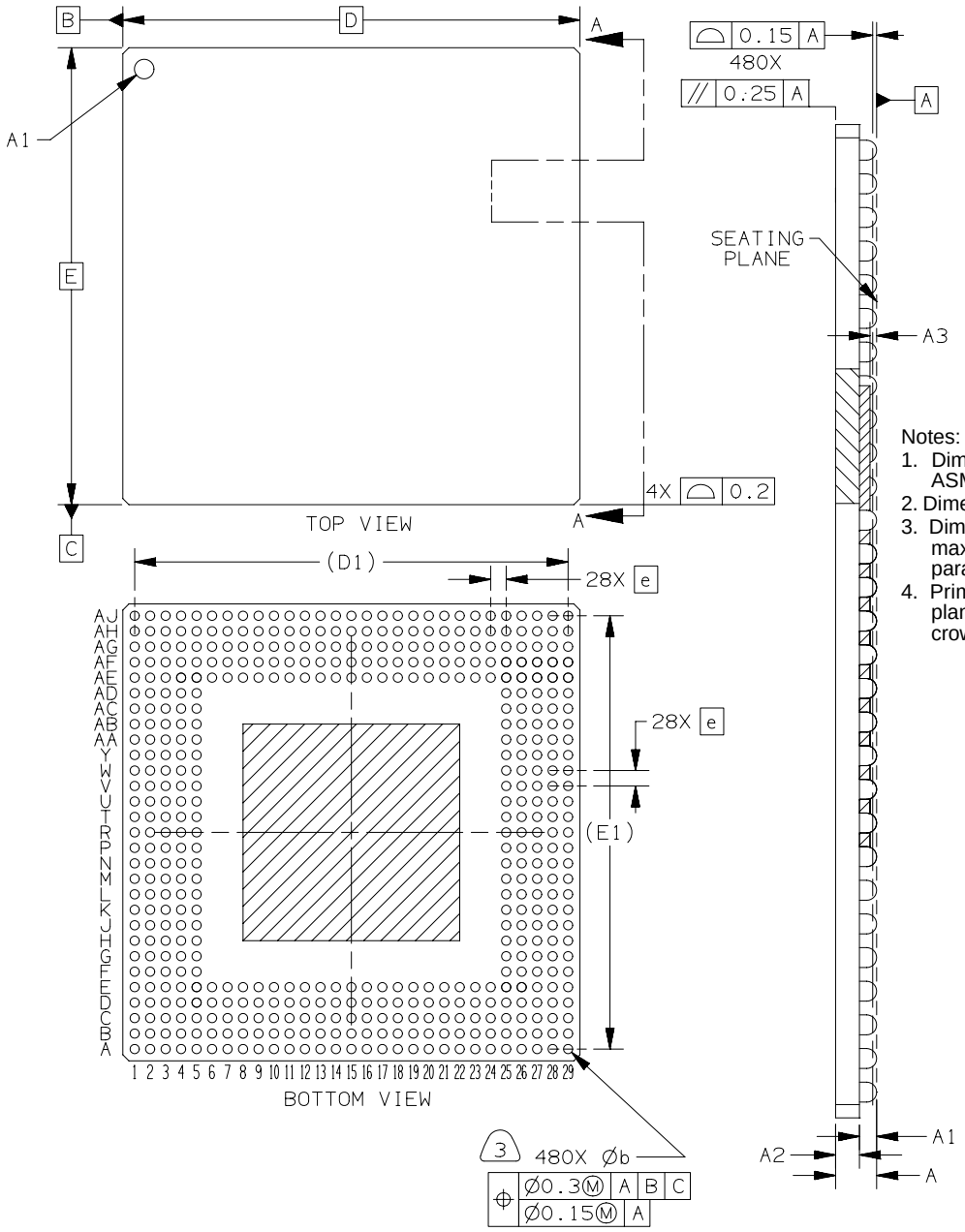
Package parameters are provided in Table 22. The package type is a 37.5 x 37.5 mm, 480-lead TBGA.

Table 22. Package Parameters

Parameter	Value
Package Outline	37.5 x 37.5 mm
Interconnects	480 (29 x 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

1.5.2 Mechanical Dimensions

Figure 14 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:
1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.
4. Primary data A and the seating plane are defined by the spherical crowns of the solder balls.

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature

1.6 Ordering Information

Figure 15 provides an example of the Motorola part numbering nomenclature for the MPC826xA. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Motorola sales office.

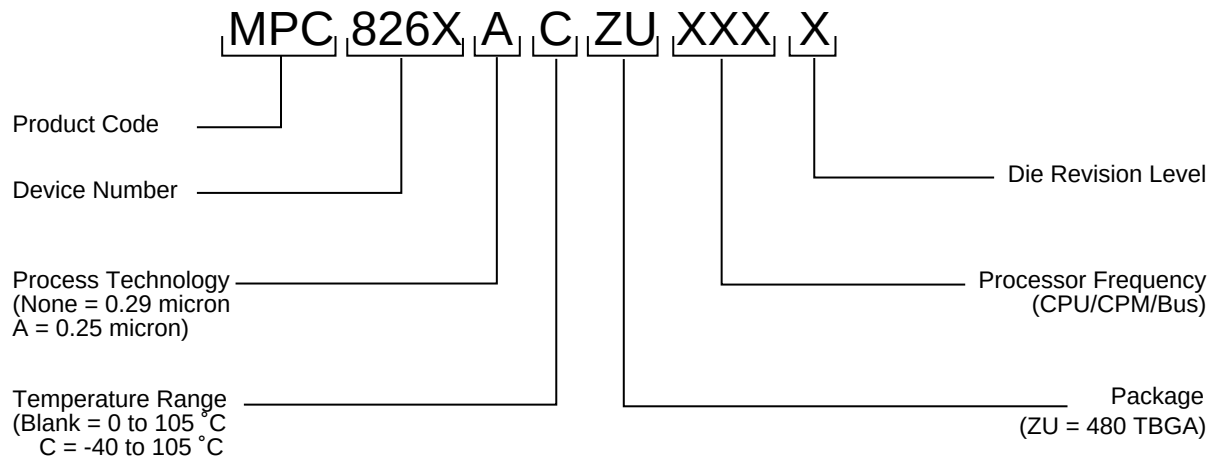


Figure 15. Motorola Part Number Key

1.7 Document Revision History

Table 23 lists significant changes in each revision of this document.

Table 23. Document Revision History

Document Revision	Substantive Changes
0	Initial version
0.1	Table 10, sp20/sp21: 66 MHz setup and hold times are 15 and 20 respectively. Delete ‘(10).’
0.2	• Revision of Table 7, “Power Dissipation” • Modifications to Figure 8, Table 4,Table 12, Table 13, and Table 18 • Modification to pinout diagram, Figure 12 • Additional revisions to text and figures throughout
0.3	• Note 3 for Table 3 • Section 1.2.1, “DC Electrical Characteristics”: Removal of “Warning” recommending use of bootstrap diodes. They are not needed. • sp12 in Table 11, sp32 in Table 12 • Note 2 for Table 16 and Table 17 • Addition of note at beginning of Section 1.3.2, “PCI Mode” • Note 1 for Table 18 and Table 19 • Additions to pinout, Table 20 for balls: B27, C28, D25, D27, E26, G29, H26–28, N25, P29, AF25, AA25, AB27

Table 23. Document Revision History (Continued)

Document Revision	Substantive Changes
0.4	• Note 2 for Table 4 (changes in italics): "...greater than or equal to 266 MHz, 200 MHz CPM..." • Table 19: core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 20: notes added to pins at AE11, AF25, U5, and V4.
0.5	• Table 20: modified notes to pins AE11 and AF25. • Table 20: added note to pins AA1 and AG4 (Therm0 and Therm1).
0.6	• Table 20: modified notes to pins AE11 and AF25.
0.7	• Section 1.1, "Features": minimum supported core frequency of 150 MHz • Section 1.1, "Features": updated performance values (under "Dual-issue integer core") • Table 4: Notes 2 and 3 • Addition of note on page 8:VDDH and VDD tracking • Table 15: Note 3 • Table 17: Note 1 • Table 19: Note 3

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