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MT933

3.3V 10/100 Fast Ethernet Transceiver to MII

DS5029 Issue no 3.0 June 2000

Features

- Integrated 10/100 Mbps Ethernet in a Single Chip Solution
- Single 3.3V Power Supply
- Half Duplex and Full Duplex in both 10BASE-T and 100BASE-TX
- Full MII for a Glueless MAC Connection
- Extended Register Set
- Integrated 10BASE-T Transceivers and Receive / Transmit Filters
- Integrated Adaptive Equaliser and Base Line Wander Correction (for FDDI Killer Packet)
- Full Auto-Negotiation Support for 10BASE-T and 100BASE-TX both Half and Full Duplex
- Link Status Change Interrupt
- Parallel Detection for Supporting Non Auto Negotiation in Legacy Link Partners
- Low Dynamic Current
- Deep Sleep Low Power Mode <1mA
- Internal Power on Reset
- 64 pin 1mm thick TQFP Package
- Single Magnetics for 10BASE-T and 100BASE-TX Operation for a Single RJ45 Connector
- Support for Flow Control 802.3 Specification
- Integrated 6 LED Driver

Ordering Information

MT933/CG/TP1N

- Low External Component Count
- Loop-back mode for diagnostics
- Intelligent power management (auto shutdown, auto wake)
- Low Transmit Jitter

Description

The MT933 is a single chip 3.3V CMOS physical layer solution from MII to the magnetics. It is designed for 10BASE-T and 100BASE-TX Ethernet, based on the IEEE 802.3 specifications.

The MT933 is compatible with the Auto Negotiation section of IEEE 802.3u and provides all the support needed for the 802.3 Full duplex specification.

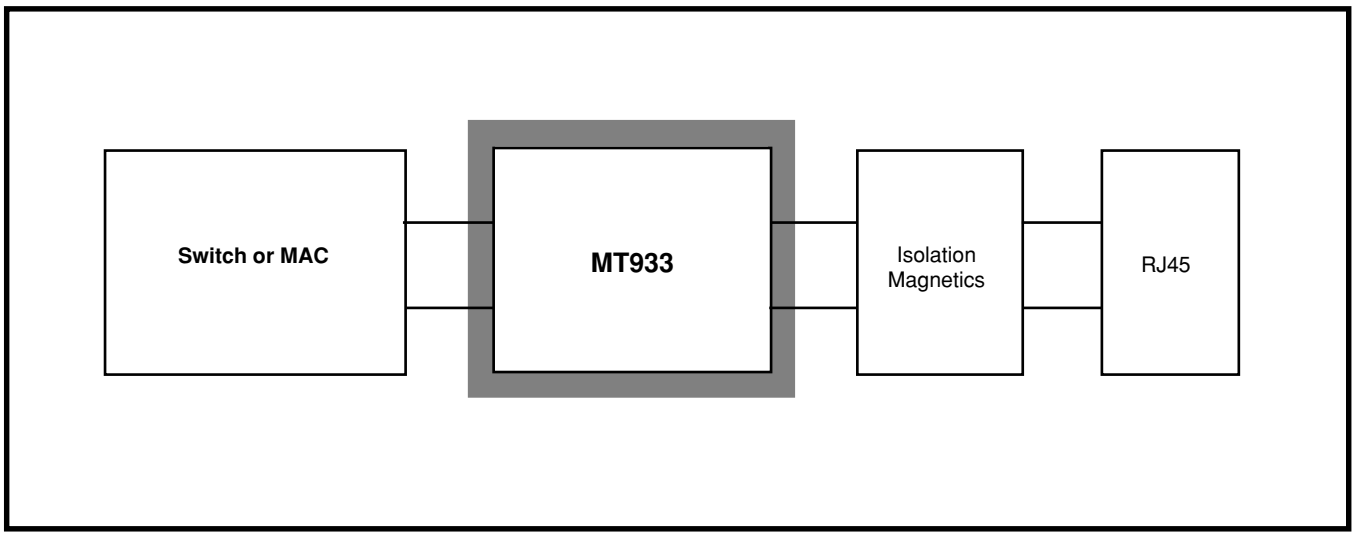


Figure 1 System block diagram

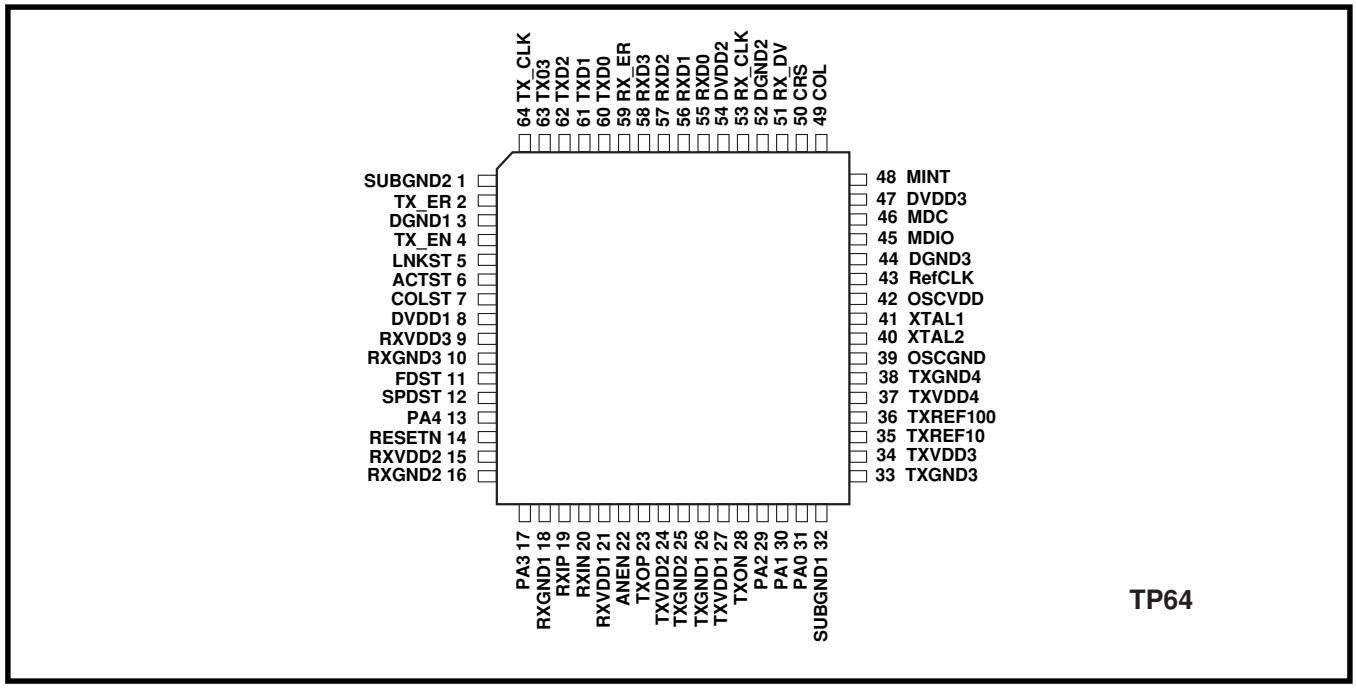


Figure 2Pin connections

Functional Description

The MT933 has three basic modes of operation: 10BASE-T, 100BASE-TX and LOW POWER modes. The Control block is designed to manage these modes by starting and stopping the 10M and 100M transceivers in a well-controlled manner such that no spurious signals are output on either the MII or twisted-pair interfaces. Furthermore, it continuously monitors the behaviour of the transceivers and takes corrective action if a fault is detected.

Other modes described herein are repeater mode and reset mode.

25MHz Reference Clock

The MT933 requires a 25MHz +/-100ppm timing reference for 802.3 compatible operation. This may be supplied either from the integrated oscillator or from an external source. When the integrated oscillator is used, a suitable crystal must be connected across the XTAL1 & XTAL2 pins (see “External Components”) and REFCLK must be tied low. When an external source is used, it must be input to the REFCLK pin and XTAL1 must be tied low. XTAL2 must be unconnected.

10Base-T Operation

10Mb/s Data Transfer on the MII

10Mb/s data is transferred across the MII with clock speeds of 2.5MHz. The MAC outputs data to the MT933 via the MII interface, on the TXD[3:0] bus. This data is synchronised to the rising edge of TX_CLK. To indicate that there is valid data for transmission on the MII, the MAC sets the TX_EN signal active. This forces the MT933 device to take in the data on the TXD[3:0] bus. This is serialised and directly encoded as Manchester data, before being output on the TXOP/TXON differential output for transmission through 1:Ö2 magnetics and onto the twisted-pair.

The transmit current is governed by the current through the TXREF10 pin, which must be grounded through a resistor as described in “External Components”.

RX10 Clock Recovery

The MT933 employs a digital delay line controlled by the 100MHz Synthesizer DLL to derive a sampling clock from the incoming signal. The recovered clock runs at twice the data rate (nominally 20MHz). When a signal is received from the Signal Detect block, it is used to strobe Link Pulses and Manchester encoded serial data.

The Manchester data stream will be decoded into a 4-bit parallel data bus, RXD[3:0]. The RXD bus is clocked out on RX_CLK rising. The MT933 must detect the first 4 bits of pre-amble before RX_DV is set high. When RX_DV is high, any Manchester coding violation will set RX_ER high. RX_DV is reset by a continuous sequence of zeroes, or by the end-of-packet IDLE terminator (11 11 00 00). Whilst RX_DV is low, the data is invalid.

100MHz Synthesizer

This synthesizer employs a delay-locked loop (DLL) to generate a 100MHz timing reference from the 25MHz reference clock. This 100MHz reference is used by the 10BASE-T transmit and receive functions and is divided by 5 to provide a 20MHz data strobe. The 20MHz clock is used to derive the 2.5 MHz TX_CLK in 10BASE-T mode. The synthesizer is disabled when not in 10BASE-T mode.

TX10 Pulse Shaper & Filter

The Pulse Shaper & Filter employs a digital Finite Impulse Response filter (FIR) to pre-compensate for line distortion and to remove high frequency components in accordance with the 802.3 Standard. The Pulse Shaper & Filter is disabled when not in 10BASE-T mode.

TX10 Latency

When connected to appropriate magnetics the latency through the TX10 path is less than 2BT (200ns) for data transmissions. This timing is measured from the rising edge of TX_CLK to the output of the transmit magnetics. The TX10 path will not transmit up to the first two Manchester encoded bits of a data transmission, as permitted by the 802.3 Standard.

RX10 Filter & RX10 Signal Detect

These blocks work in unison to remove noise and to block signals that do not achieve the voltage levels specified in 802.3. Signals that do not achieve the required level are not sampled in the Clock Recovery block and are not passed to the outputs.

RX10 Latency

When connected to appropriate magnetics the latency through the RX10 path is less than 6BT (600ns). This timing is measured from the input of the receive magnetics to the rising edge of RX_CLK. The RX10 path may ignore up to three Manchester encoded bits at the start of data reception (802.3 allows up to 5 bits).

100Base-TX Operation

100Mb/s Data Exchange on the MII Interface

100Mb/s data is transferred across the MII with clock speeds of 25MHz. The MAC outputs data to the MT933 via the MII interface, on the TXD[3:0] bus. This data is synchronised to the rising edge of TX_CLK. To indicate that there is valid data for transmission on the MII, the MAC sets the TX_EN signal active. This forces the MT933 device to take in the data on the TXD[3:0] bus and replace the first octet of the MAC preamble with Start-of-Stream Delimiter (SSD) symbols to indicate the start of the Physical Layer Stream.

When the data transfer across the MII is complete, the MAC deasserts the TX_EN signal and the MT933 adds End-of-Stream Delimiters (ESD) symbols onto the end of the data stream. The complete data stream (the Physical Layer Stream) is encoded from 4 bits into 5 bits, scrambled, converted to MLT3 and driven to the TXOP and TXON pin differentially.

The TX100 path is disabled when not in 100BASE-TX mode and, with the exception of the RX100 Signal Detect, the RX100 Receive Path is disabled when not in 100BASE-TX mode.

125MHz Synthesizer

This synthesizer employs a phase-locked loop (PLL) to generate a 125MHz timing reference from the 25MHz reference clock. This 125MHz reference is used by the 100BASE-TX transmit function and is divided by 5 to provide a 25MHz data strobe on TX_CLK. TX_CLK is frequency and phase locked to the 25MHz reference with a small phase offset. The synthesizer is disabled when not in 100BASE-TX mode.

TX100 PISO, Encoder and Scrambler

Data from the MII is loaded into the TX100 PISO, Encoder and Scrambler on the rising edge of TX_CLK. It is converted to serial MLT3 for outputting to the TX100 Driver. The TXD[3] bit is output first. The PISO & Encoder do not operate until the 125MHz Synthesizer is locked to the 25MHz reference. This avoids transmission of spurious signals onto the twisted-pair.

TX100 Driver

The TX100 Driver outputs the differential signal onto the TXOP and TXON pins. It operates with 1:root 2 magnetics to provide impedance matching and amplification of the signal in accordance with the 802.3 specifications. The transmit current is governed by the current through the TXREF100 pin, which must be grounded through a resistor as described in “External Components”. The TX100 driver is disabled in 10BASE-T mode and in loop back mode.If no data is being transmitted from the MAC, the MT933 outputs idle symbols of 11111 (suitably scrambled).

TX100 Latency

The transmit latency from the first TX_CLK rising when TX_EN is high to the first bit of the “J” symbol on the cable is 8BT.

RX100 Equalizer & Base-line Wander Correction

The RX100 Equalizer compensates for the signal attenuation and distortion resulting from transmission down the cable and through the isolation transformers. The Equalizer is self-adjusting and is designed to restore signals received from up to 10dB cable attenuation (at 16MHz). When the Equalizer is active it adjusts to the incoming signal within 1ms. Thereafter, the Equalizer will continuously adjust to small variations in signal level without corrupting the received data.

The 100BASE-TX MLT3 code contains significant low frequency components which are not passed through the isolation transformers and cannot be restored by an adaptive equalizer. This leads to a phenomenon known as Base-line Wander which will cause an unacceptable increase in error rate if not corrected. The MT933 employs a quantized feedback technique to restore the low frequency components and thus maintain a very low error rate even when receiving signals such as the “killer packet” described in the TP_PMD spec.

RX100 Clock Recovery

The RX100 Clock Recovery circuit uses a Phase-Locked Loop (PLL) to derive a sampling clock from the incoming signal. The recovered clock runs at the symbol bit rate rate (nominally 125MHz) and is used to clock the MLT3 decoder and the Serial to Parallel converter (SIPO).

The recovered clock is divided by 5 to generate the receive clock (RX_CLK) which is used to strobe received data across the MII interface. When no signal is detected in 100BASE-TX mode, the PLL is locked to the reference clock and runs at 125MHz. This ensures that RX_CLK runs continuously at 25MHz in 100BASE-TX mode. When a signal is present, the Clock Recovery PLL remains locked to the reference until the equalizer has adjusted, then it requires up to 1ms to phase lock to the incoming signal. No data is passed to the MII interface until lock is established.

RX100 SIPO, Decoder and Descrambler

The RX100 SIPO, Decoder and Descrambler convert the received signal from serial MLT3 to 4-bit wide parallel receive data on the MII. This appears on the RXD[3:0] bus which is clocked out on the falling edge of RX_CLK. When a frame starts the MT933 decodes the SSD symbols and then asserts the RX_DV signal, in order to inform the MAC that valid data is available. When the MT933 detects the ESD, it deasserts the RX_DV signal.

RX100 Latency

The latency from the first bit of the “J” symbol on the cable to CRS assertion is between 11 and 15BT. The latency from the first bit of the “T” symbol on the cable to CRS de-assertion is between 19 and 23BT.

100Mb/s Transmit Errors

If the MT933 detects that the TX_ER signal has gone active whilst the TX_EN signal is active, then it will propagate the detected error onto the cable by transmitting the symbol “00100” . Figure 3 shows the meaning of the different states of TX_EN and TX_ER. TX_ER is sampled inside the MT933 on the rising edge of TX_CLK.

TX_EN	TX_ER	TXD [3:0]	Indication
0	X	ignored	Normal inter frame data
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Figure 3. 100Mb/s Transmit Error States

100Mb/s Receive Errors

When there is no data on the cable, the receiver will see only the idle code of scrambled 1's. If a non idle symbol is detected, the receiver looks for the SSD so that it can align the incoming message for decoding. If any 2 non consecutive zeros are detected within 10 bits, but are not the SSD symbols a false carrier indication is signalled to the MII by asserting RX_ER and setting RXD[3:0] to 1110 whilst keeping RX_DV inactive. The remainder of the message is ignored until 10 bits of 1's are detected.

If any data is decoded after a SSD which is neither a valid data code nor an ESD, then an error is flagged by setting RX_ER active whilst the RX_DV signal is active. This also happens if 2 idle codes are detected before a valid ESD has been received or descramble synchronisation is lost during packet reception. The states of RX_DV and RX_ER are summarised in Figure 4. RX_ER is clocked on the falling edge of RX_CLK, and will remain active for at least 1 period of RX_CLK.

RX_DV	RX_ER	RXD [3:0]	Indication
0	0	0000 through 1111	Normal inter frame
0	1	1110	False carrier indication
1	0	0000 through 1111	Normal data reception
1	1	0101 or 0110	Data reception with errors

Figure 4. 100Mb/s receive error states

CONTROLS

Initialization, mode selection and other options are governed by the control inputs and register as described in the following paragraphs.

Initialization (RESET_N)

The MT933 incorporates a power-on-reset circuit for self-initialization on power-up. During initialization the open-drain RESET_N pin is driven low and all data outputs are disabled to prevent spurious outputs to the twisted-pair and to the MII interface. RESET_N will remain low until the power supply has been stable for at least 400ns. The MT933 will then release RESET_N allowing the external pull-up to pull the pin high. Device initialisation will not commence until RESET_N is high. This allows the user to extend the inactive period by externally holding RESET_N low. It will not normally be necessary for the user to reset the MT933 because it is designed to automatically recover from fault conditions. However, if required, the user may initialize the device by doing a hardware or software reset.

Reset Mode

There are two types of reset in the MT933 - hardware and software. The hardware reset is activated by setting the RESET_N pin to logic 0, and holding it low for at least 100ns. This mode causes an over-all reset in the MT933 - both analog and digital circuitry are reset. Whilst RESET_N is low, the SPDST and FDST pins are inputs, and are used to determine the speed and duplex capability which will be advertised during auto-neg. A low on SPDST advertises 100M capability. A high on FDST advertises full duplex capability.

The software reset is activated by setting bit 15 in register 0 high. This bit is a self clear bit and causes a partial reset of the device.

Figure 5 summarises the different blocks to be reset and which reset will affect them:

Block	HW Reset	SW reset
management register	yes	yes
PCS state machine (RCV, XMT, ANEG)	yes	yes
XMT scrambler	yes	yes
RCV scramble	yes	yes
control state machine	yes	No
analog	yes	No

Figure 5. Effects of Reset

Note: Holding RESET_N low will hold the device in a static, low power state.

Low-Power Mode

This function is set via the management interface. Using MDC and MDIO, Bit 11 of register 0 is written high to put the MT933 into Low-Power mode. The type of low power mode is dependant on bits 14 and 15 in register 24.

For 24[15:14] = 0:0 the 10BASE-T and 100BASE-TX transceivers are disabled. The oscillator continues to run. Both RX_CLK and TX_CLK are stopped, the RXD bus is held low and TXD, TXEN, and TXER are ignored. MDC and MDIO are still active for new commands. This mode is intended to conserve power when the network connection is not required and the TXOP/TXON output is undriven. Typical current consumption is less than 10mA.

For 24[15:14] = 0:1, everything is turned off, including the voltage references and the oscillator. This mode must be exited via the management interface. Typical current consumption is 0.5mA.

For 24[15:14] = 1:0, the only function available is the signal detect. The MT933 will detect a signal amplitude on the cable and activate the interrupt. MINT can be selected as either an active low or high interrupt. Typical current consumption is less than 10mA.

For 24[15:14] = 1:1, the MT933 will automatically power down into a sleep mode if no activity is seen on the cable for approx 2 seconds. Power up is also automatic if activity is seen. Typical current consumption is less than 10mA.

Loopback Mode

Diagnostic loopback may be selected at any time by asserting setting Bit 14 in register 0. In 10BASE-T mode transmission to the TXOP/ TXON output will be stopped and the RX10 Clock Recovery will receive input from the TX10 transmit path rather than from the RXIP/RXIN inputs. In 100BASE-TX mode transmission to the TXOP/TXON output will be stopped and the RX100 Clock Recovery will receive input from the TX100 transmit path.

Repeater Mode

The MT933 can be put into Repeater Mode by setting register 24 bit 0 high. In this mode, the CRS will be active on receive only. In 100Mbps repeater mode, the MT933 is able to perform a disconnect function from the MII. This function is enabled by bit 1 in register 24. (Note that if the device is not in repeater mode, this bit has no effect). The MT933 will disconnect from the MII if it receives two consecutive false CRS events with no good frame in between them or if a false CRS event is longer then 480 +/- 4BT. If the MT933 receives a good carrier event (480 +/- 4BT) or a good idle event (idle symbols for a period of 25000 to 30000 bit time) it will resume frame transfer to the MII.

A false CRS event happens if, at the beginning of a carrier event, the JK symbols are not received correctly.

When the MT933 is in 100M mode it will count all false CRS events in register 27 bits 7:0. This counter is self cleared upon read. If a disconnect event occurs between the consecutive reads of register 27, bit 15 in the register will set high.

Auto-Negotiation Enable (ANEN)
Auto-negotiation may be hardware disabled by setting the ANEN pin to logic zero. During operation, auto-negotiation can be disabled by setting the ANEN pin low or by setting bit 12 of register 0 to zero. If auto-neg is disabled, the MT933 will lose the link, and link will be re-established only after the MT933 control state machine has determined the speed using bits 13 and 8 of register 0 to determine speed and duplex respectively.

MII Management Interface, MDC and MDIO

The management interface is a 2 wire serial interface connecting a PHY to a management entity. The management unit controls the PHY and gathers information on the status of the PHY. It does this via the implemented registers using MDC to clock the data on the MDIO pin.

Link Status Change Interrupt, MINT

MINT is, by default, an active low interrupt which is activated whenever a change in the link status occurs. It can be changed to be active high by setting bit 13 in register 24. The interrupt will remain active until the controller acknowledges the interrupt by writing to register 21 (any data). Should one or more link status changes occur between the assertion of MINT and an ackowledge, then MINT will be deasserted and then reasserted (deassertion time between 100ns and 150ns). Only a single interrupt event may be queued at any one time. Multiple status changes between an ackowledge will generate only a single queued interrupt.

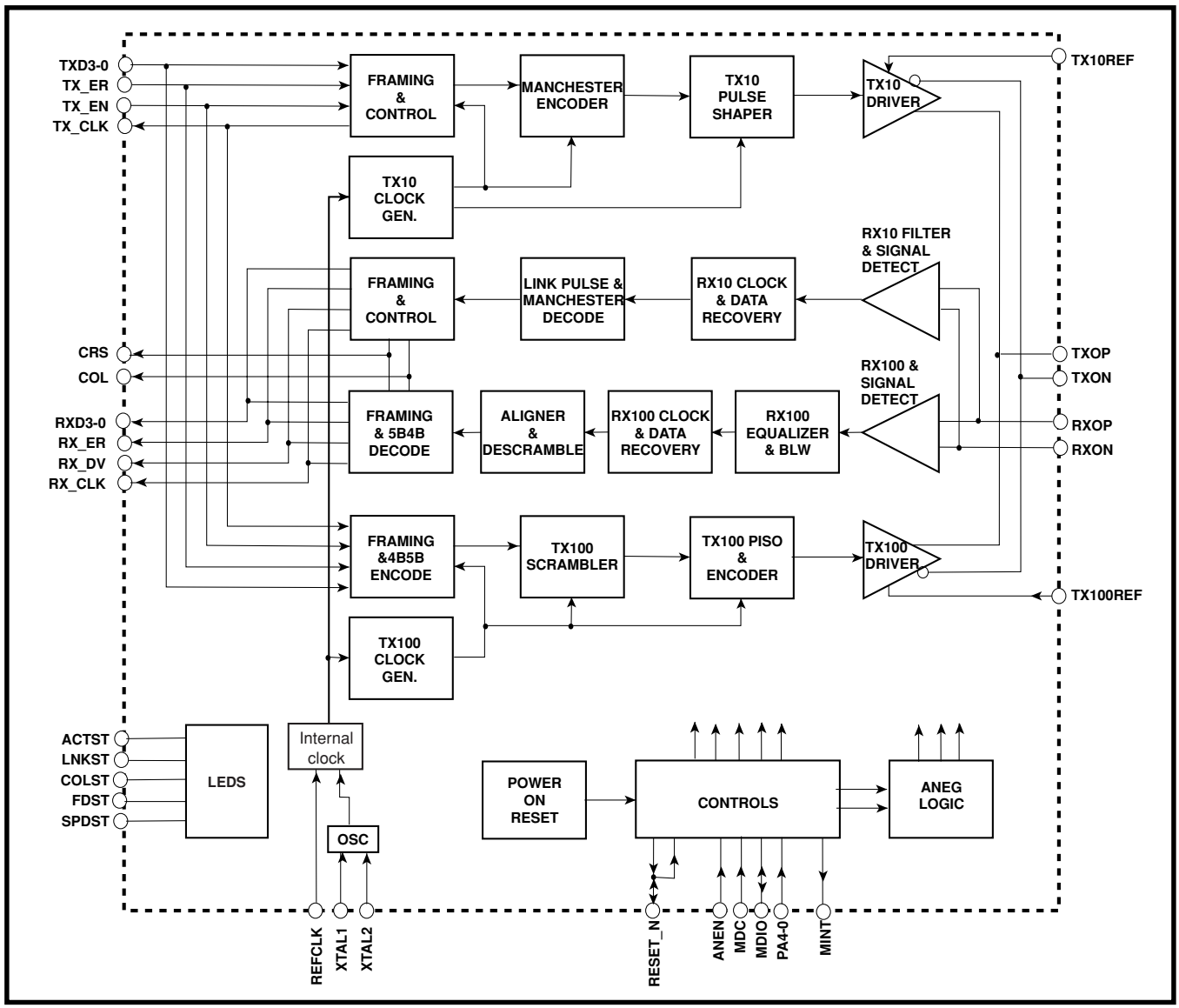


Figure 6 MT933 block diagram

Pin list

Pin #	Name	Type	Description
MD interface			
20	RXIN	Input	Differential receive pair from magnetics (-)
19	RXIP	Input	Differential receive pair from magnetics (+)
28	TXON	Output	100 Differential transmit pair to magnetics (-)
23	TXOP	Output	100 Differential transmit pair to magnetics (+)
35	TXREF10	Input	10BASE-T transmitter current setting pin
36	TXREF100	Input	100BASE-TX transmitter current setting pin
14	RESETN	IOput	Active low, power on reset output and external reset input
41	XTAL1	Input	25MHz crystal input
40	XTAL2	Input	25MHz crystal input
MII interface			
46	MDC	Input	Management interface clock (up to 2.5MHz)
45	MDIO	IOput	Management data
53	RX_CLK	Output	Receive clock (2.5MHz for 10, 25MHz for 100)
55, 56, 57, 58	RXD0, RXD1, RXD2, RXD3	Output	Receive data MII interace
51	RX_DV	Output	Receive data valid. Active high.
59	RX_ER	Output	Receive error. Active high. (RXD4 in symbol mode)
43	REFCLK	Input	Reference clock
64	TX_CLK	Output	Transmit clock (2.5MHz for 10, 25MHz for 100)
60, 61, 62, 63	TXD0, TXD1, TXD2, TXD3	Input	Transmit Data MII interface
4	TX_EN	Input	Transmit Enable. Active high.
2	TX_ER	Input	Transmit Error. Active high. (TXD4 in symbol mode)
50	CRS	Output	Carrier sense signal. Active high.
49	COL	Output	Collision signal. Active high.
22	ANEN	Input	Auto Negotiation enable. Active high.
48	MINT	Output	MII interrupt control.
6	ACTST	Output	Receive / transmit active indication (LED interface). Active low.
7	COLST	Output	Collision active indication (LED interface) Active low.
11	FDST	IOput	Full duplex indication when RESET_N high (LED interface). Active low. Input when RESET_N is low. High input means 933 advertises full duplex capability.
	5	LNKST	Output Link OK indication (LED interface). Active low.
12	SPDST	IOput	Speed indication when RESET_N high (LED interface). High for 100Mb/s mode. Input when RESET_N is low. Low input means 933 advertises 100Mb/s capability.
31, 30, 29, 17, 13	PA0, PA1, PA2, PA3, PA4	Input	Phy address

General

The following is the register set that is implemented in the MT933 device:

The interface to these registers is via the MDC and MDIO signals. The address of the MT933 is specified by the PA<4:0> static inputs The MD command is issued by the controller and can be read or write:

command	preamble	start data	op code	phy address	reg number	TA	Data
READ	32 bits of 1	01	10	5 bits	5 bits	Z0	16 bit from phy
WRITE	32 bits of 1	01	01	5 bits	5 bits	10	16 bit from MAC

SC = Self clear

RO = read only

RW = read or write

LL = latch low until register read

LH = latch high until register read

Register Set
reg 0 - control register

Bit	Bit name	Description	Default	R/W
0.15	Reset	1 = PHY reset 0 = Normal operation	0	RW SC
0.14	Loopback	1 = Loopback mode active 0 = Normal operation	0	RW
0.13	Speed selection	1 = 100 Mbps 0 = 10 Mbps	1	RW
0.12	ANEG enable	1 = Enable ANEG process 0 = Disable ANEG process	1	RW
0.11	Power down	1 = Power down active 0 = Normal operation	0	RW
0.10	Isolation	1 = isolation in process 0 = Normal operation	0	RW
0.9	Restart ANEG	1 = Restart the ANEG process 0 = Normal operation	0	RW SC
0.8	Duplex selection	1= Full Duplex mode 0 = Half duplex mode	1	RW
0.7	Collision test	1 = Collision test active 0 = Normal operation	0	RW
0.6:0	Reserved	Write as 0 ignore on read.		

reg 1- status register

Bit	Bit name	Description	Default	R/W
1.15	100BaseT4	1 = PHY able to perform 100BaseT4 0 = PHY not able to perform 100BaseT4	0	RO
1.14	100BASE-TX - FDX	1 = PHY able to perform 100BASE-TX 0 = PHY not able to perform 100BASE-TX	1	RO
1.13	100BASE-TX - HDX	1 = PHY able to perform 100BASE-TX 0 = PHY not able to perform 100BASE-TX	1	RO
1.12	10BASE-T - FDX	1 = PHY able to perform 10BASE-T 0 = PHY not able to perform 10BASE-T	1	RO
1.11	10BASE-T - HDX	1 = PHY able to perform 10BASE-T 0 = PHY not able to perform 10BASE-T	1	RO
1.10	100BaseT2 - FDX	1 = PHY able to perform 100BaseT2 0 = PHY not able to perform 100BaseT2	0	RO
1.9	100BaseT2 - HDX	1 = PHY able to perform 100BaseT2 0 = PHY not able to perform 100BaseT2	0	RO
1.8:7	Reserved	ignore when read	0	RO
1.6	MF preamble suppression	1= Phy accept management frames with short preamble 0 = normal preamble only	0	RO
1.5	ANEG complete	1 = ANEG process completed 0 = ANEG process not completed or not active	0	RO
1.4	Remote fault	1= Remote fault condition detected 0 = no Remote fault condition detected	0	RO LH
1.3	ANEG able	1 = Phy is able to perform ANEG 0 = Phy is not able to perform ANEG	1	RO
1.2	Link status	1= Link is up 0 = Link is down	0	RO LL
1.1	Jabber detect	1 = jabber condition detected 0 = normal operation	0	RO
1.0	Extended regs	1 = extended register capability 0 = no extended registers	1	RO

reg 2/3- MT933 Identifier register

Bit	Bit name	Description	Default	R/W
2.15:0	OUI	Mitel OUI bits	0282	RO
3.15:0	OUI/device ID	Mitel OUI bits and device code	1C7X	RO

reg 4- ANEG advertisement register

Bit	Bit name	Description	Default	R/W
4.15	NP	Next page able - the MT933 is not able to perform next page	0	RO
4.14	reserved		0	RO
4.13	remote fault	0 = no remote fault detected 1= a remote fault been detected	0	R/W
4.12:10	reserved		0	R/W
4.9:5	Technology	T4, 100Fdx, 100Hdx, 10Fdx, 10Hdx	0F	R/W
4.4:0	selector field		01	R/W

reg 5- ANEG link partner ability register

Bit	Bit name	Description	Default	R/W
5.15	NP	partner is next page capable	0	RO
5.14	ACK	partner sent an acknowledge bit	0	RO
5.13	remote fault	partner detected a remote fault	0	RO
5.12:5	ability	partner's technology ability	0	RO
5.4:0	selector field	partner selector field	0	RO

reg 6- ANEG expansion register

Bit	Bit name	Description	Default	R/W
6.15:5	reserved		0	RO
6.4	parallel detect fault	0 = aneg process finished. No fault detected 1 = a fault has been detected	0	RO LH
6. 3	link partner next page able	0 = Link partner is not next page able 1 = Link partner is next page able	0	RO
6.2	next page able	0 = MT933 is not able for next page	0	RO
6.1	Page received	0 = no new page been received 1= a new page has been received and is in reg 5	0	RO LH
6.0	link partner aneg able	0 = Link partner is not aneg able 1 = Link partner is aneg able	0	RO

reg 16, 17, 18, 19, 20 - Test registers

Bit	Bit name	Description	Default	R/W
15:0	reserved	test mode only	0000	res

reg 21 - MII interrupt control register

Bit	Bit name	Description	Default	R/W
21.15:0	Clear Interrupt	Write any data pattern to clear MINT	0	WO

reg 22, 23 - Test registers

Bit	Bit name	Description	Default	R/W
15:0	reserved	test mode only	0000	res

reg 24- MT933 specific register

Bit	Bit name	Description	Default	R/W
24.15:14	PWRCON[1:0]	Low power controls: 00 = full receive path active. No transmit. 01 = Deep sleep (all off including VREF & OSC) 10 = Sleep (generate MII interrupt on activity) 11 = auto shut down, auto wake on activity	00	RW
24.13	MINTPOL	1 = MINT output active high 0 = MINT output active low	0	RW
24.12	Pol Dis	1 = disable 10Base-T autopolarity correction	0	RW
24.11	SQE disable	1 = disable SQE in 10Base-T half duplex mode	0	RW
24.10	JAB disable	0 = in case of jabber the 10Base-T will cut the transmitted frame (normal operation) 1 = Jabber function disable	0	RW
24. 9	loop 10	1 = enable MII loopback in 10Base-T half duplex mode	0	RW
24.8	Force RX	Force receive regardless of link	0	RW
24.7	Force TX	Force transmit regardless of link	0	RW
24.6	CRS_CTL	CRS behavior in full duplex mode:- 0 = CRS is active for transmit only 1= CRS active for receive or transmit	0	RW
24.5	MF	1 = MDIO data accepted without preamble	0	RW
24.4	Byp ALIGN	0 = normal operation 1 = bypass the aligner function	0	RW
24.3	Byp ENC	0 = normal operation 1 = bypass the 4B5B encoder function	0	RW
24.2	Byp SCR	0 = normal operation 1 = bypass the scrambler function	0	RW
24.1	DISCEN	0 = disable disconnection events 1 = enable disconnect on false carrier detection	0	RW
24:0	RPTR	Set repeater mode (affects CRS generation)	0	RW

reg 25 - ANEG status

Bit	Bit name	Description	Default	R/W
25.15:14	reserved	test mode only - do not set high	0	RO
25.13	Pol	1 indicates polarity reversal on RX inputs (10Base-T)	0	RO
25.12:8	PA	copy of PHY address pins	PA<4:0>	RO
25.7	aneg complete	1 = aneg completed 0 = aneg did not complete (same as reg1.5)	0	RO
25.6	Duplex	ANEG result - duplex operation 0 = HDX, 1 = FDX	0	RO
25.5	speed	ANEG result - speed of operation 0 = 10M, 1 = 100M	0	RO
25.4	ability mtc	1 = abilities match between registers 4 & 5	0	RO
25.3:0	ANEG state	ANEG state machine current state	0	RO

reg 26 - Symbol error counter

Bit	Bit name	Description	Default	R/W
26.15:0	RX_ERR counter	number of RX_ERR events since last read - Clears either in change of speed or read of this reg.	0	RO SC

reg 27 - False carrier event counter

Bit	Bit name	Description	Default	R/W
27.15	disconnect	the disconnect mechanism status	0	RO LH
27.14:8	reserved		0	RO
27.7:0	false CRS counter	number of False CRS events since last read. Active only when DISCEN = 1”.	0	RO SC

reg 28, 29, 30, 31 - Test registers

Bit	Bit name	Description	Default	R/W
15:0	reserved	test mode only	0000	res

Operating Conditions

Supply voltage	+3.0V to 3.6V
Ambient temperature	0°C to +70°C

DC Electrical Characteristics

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
DC parameters - input					
High level input voltage	V_{IH}	2	V_{DD}	V	
Low level input voltage	V_{IL}	V_{SS}	0.8	V	
High level input current	I_{IH}	-	1	µA	
Low level input current	I_{IL}	-	–1	µA	no pull up
Pin capacitance to ground		-	8	pF	including package
DC parameters - output -6mA buffers					
High level output voltage	V_{OH}	2.4	V_{DD}	V	
Low level output voltage	V_{OL}	V_{SS}	0.4	V	
High level output current	I_{OH}	-	–6	mA	
Low level output current	I_{OL}	-	6	mA	
Rise time		-	4	nS	0.4V to 2.4V into 20pF load
Fall time		-	4	nS	0.4V to 2.4V into 20pF load
Pin capacitance to ground		-	8	pF	
Differential Output					
Peak Differential Voltage		2.2	2.8	V	10Mbs mode
High Level		0.95	1.05	V	100Mbs mode
Zero Level		-0.05	0.05	V	100Mbs mode
low Level		-1.05	-0.95	V	100Mbs mode

Note: Differential outputs are 802.3 compliant

AC Electrical Characteristics

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
Differential Output					
Baseline to +Vout		3	5	nS	100Mbs mode
Baseline to -Vout		3	5	nS	100Mbs mode
+Vout to Baseline		3	5	nS	100Mbs mode
-Vout to Baseline		3	5	nS	100Mbs mode

Note: Differential outputs are 802.3 compliant

AC Electrical Characteristics (continued)

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
REFCLK					
Frequency		25±100ppm		MHz	
Duty cycle		45	55	%	
RXCLK					
Frequency		25±100ppm		MHz	100Mbs mode
Duty cycle		40	60	%	100Mbs mode
Frequency		2.5±100ppm		MHz	10Mbs mode
Duty cycle		40	60	%	10Mbs mode
TXCLK					
Frequency		25±100ppm		MHz	100Mbs mode
Duty cycle		40	60	%	100Mbs mode
Frequency		2.5±100ppm		MHz	10Mbs mode
Duty cycle		40	60	%	10Mbs mode
MDC					
Frequency		-	2.5	MHz	
Minimum high/low		160	-	ns	
Supply Current		**Typ**	**Max**		
10Base-T Idle		80	85	mA	Measured at 3.3V
10Base-T Active		130	180	mA	Room Temperature
100Base-T Idle		125	130	mA	These Figures include
100Base-T Active		130	135	mA	the current flowing
Sleep Mode		5	6	mA	in the Transmit resistors
Deep sleep mode		0.25	1	mA	
Resetn = 0		1	2	mA	

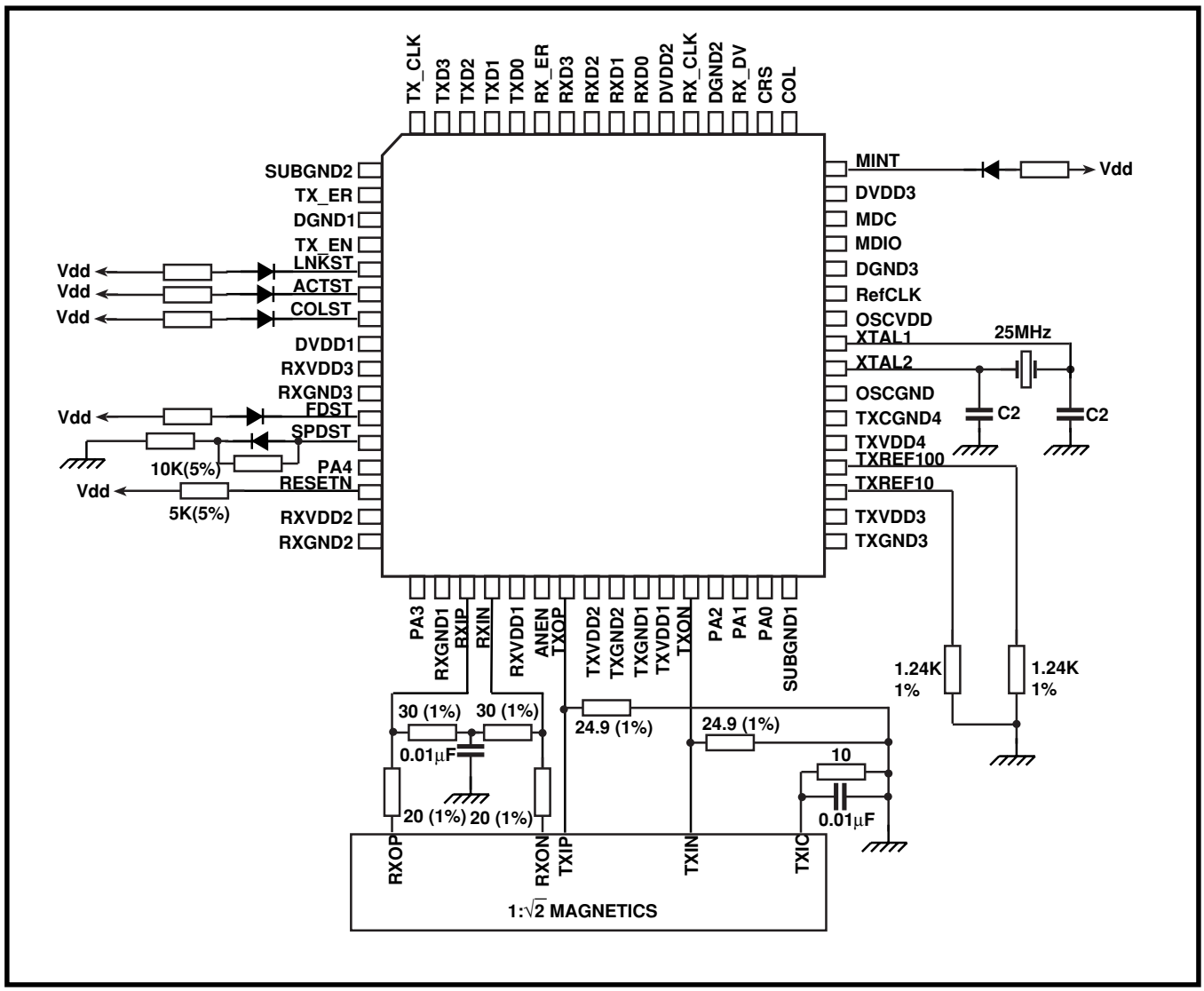


Figure 7 External Components

EXTERNAL COMPONENTS

Connecting an External 25MHz Reference

If an external clock is used then it should be driven into the REFCLK input, and XTAL1 must be connected to ground. XTAL2 must be left unconnected. If a crystal is used, REFCLK must be connected to ground.

RESETN Pull-up Resistor

This resistor is required regardless of whether or not RESETN is used externally.

RX Input Decoupling

The method of using a split input load resistor and de-coupling the centre tap reduces common mode noise.

Crystal Oscillator

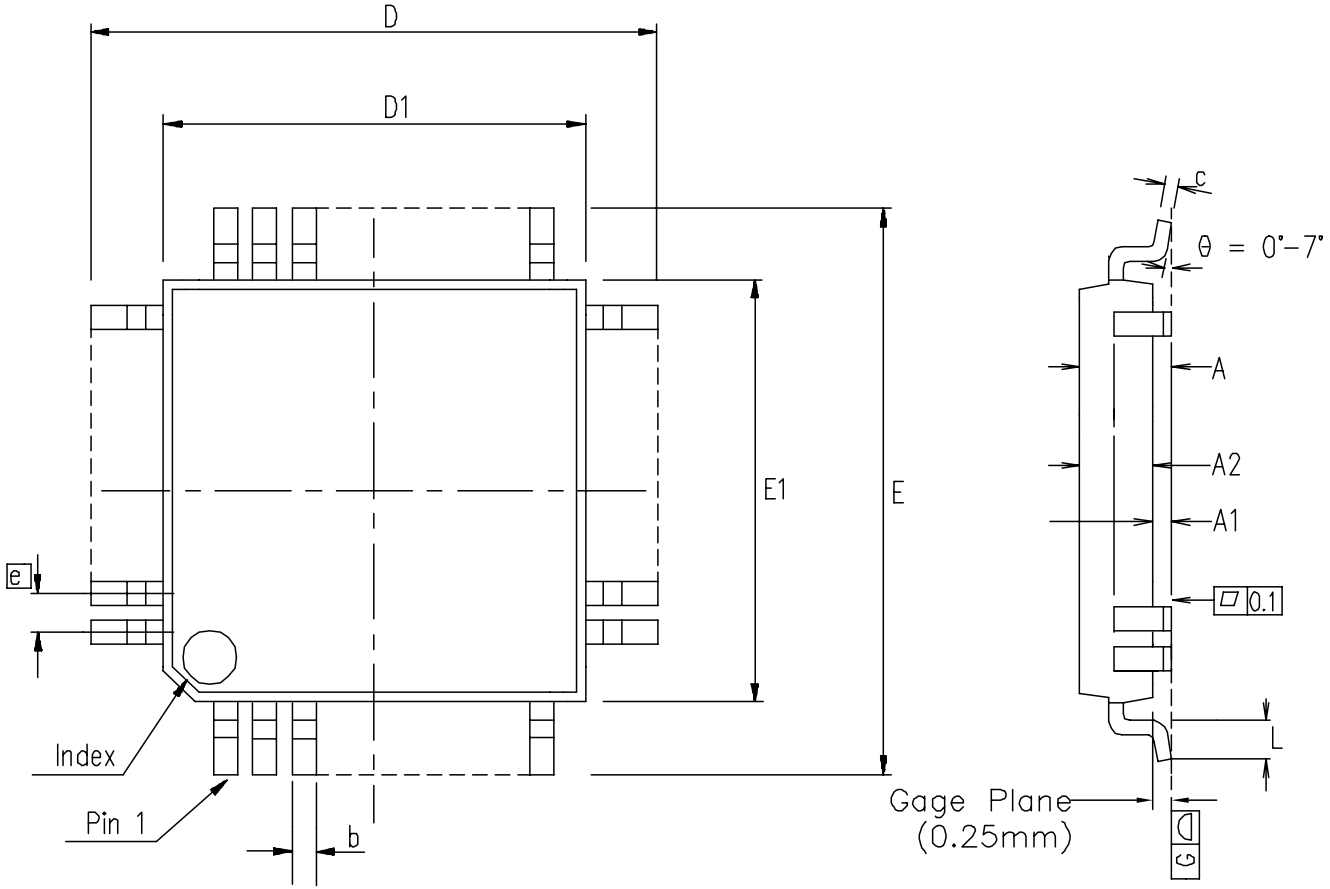
For IEEE802.3 compliance the oscillator must run at 25MHz ±100ppm. The MT933 on-chip circuitry contributes less than 40ppm variability to the oscillator frequency, therefore the crystal must be specified to 60ppm. This must include variations due to temperature and ageing. The crystal must be capable of dissipating 0.5mW of power.

External capacitors are required on the XTAL1 & XTAL2 pins. Manufacturer's recommendations should be followed.

Tracking to the crystal and the capacitors must be as short as possible. Other signal paths must not cross the area.

The MT933 is supported by the following magnetics:

VENDOR	MAGNETICS
Pulse	H1119



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.20		---	0.047
A1	0.05	0.15		0.002	0.006
A2	0.95	1.05		0.037	0.041
D	12.00 BSC			0.472 BSC	
D1	10.00 BSC			0.394 BSC	
E	12.00 BSC			0.472 BSC	
E1	10.00 BSC			0.394 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	64				
ND	16				
NE	16				
NOTE	SQUARE				

Conforms to JEDEC MS–026 ACD Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

ISSUE	1	2				MITEL SEMICONDUCTOR
ACN	203170	207075				
DATE	14OCT97	5JUL99				
APPROVED						

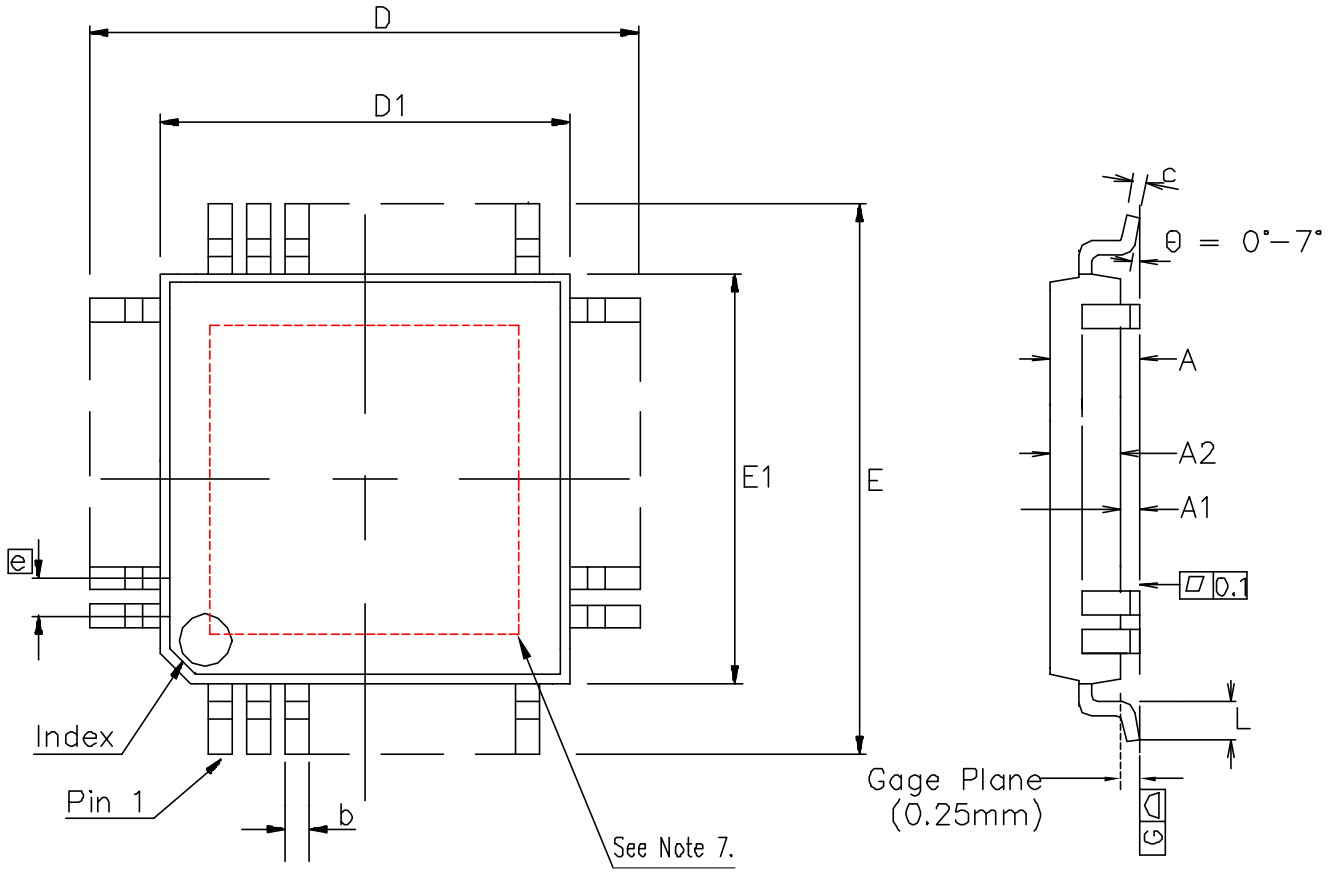
Title:
Package Outline Drawing for 64 Lds TQFP (TP)
(10 x 10 x 1.0)mm, Body + 2mm

Drawing Number
GPD00450

© Mitel

Format No.

ORIGINATING SITE: SWINDON



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	Pin features				
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ND	16				
NE	16				
NOTE	SQUARE				

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Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protrusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.
7. Dashed area represents exposed paddle for e-PAD Packages only.
   - See leadframe drawing for e-Pad dimension.
   - Metal area of exposed die pad shall be within 0.30mm of nominal pad size.

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ISSUE	1	2	3	
ACN	203170	207075	213856	
DATE	14Oct97	5Jul99	17Dec02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

TP/TH

Package Code QD/QG

Package Outline for 64 Lead TQFP / e-Pad TQFP 10x10x1.0mm, +2.0mm (footprint)

GPD00450

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