CMOS MT9125
Dual ADPCM Transcoder
Preliminary Information

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Features

- Dual channel full duplex transcoder
- 32 kbit/s and 24 kbit/s ADPCM coding,
- compatible to G.721 & and G.723 (1988) and ANSI T1.303-1989
- Low power operation, total 25mW typical
- Asynchronous 4.096 MHz master clock operation
- Transparent ADPCM bypass capability
- Serial interface for both PCM and ADPCM data streams
- ST-BUS interface supported
- Pin selected μ-law or A-law operation
- Pin selected CCITT or sign-magnitude PCM coding
- Single 5 volt power supply
- Optional reset value (CCITT Table 3/G.721) capability

Applications

- Pair gain
- Voice mail systems
- Wireless set base stations

Ordering Information

MT9125AE	24 Pin Plastic DIP (600 mil)
MT9125AP	28 Pin PLCC

-40 to +85°C

Description

The Dual-channel ADPCM transcoder is a low power, CMOS device capable of two encoder functions and two decoder functions. Two 64 kbit/s PCM channels are compressed into two 32 kbit/s ADPCM channels, and two 32 kbit/s ADPCM channels are expanded into two 64 kbit/s PCM channels. The 32 kbit/s ADPCM transcoding algorithm utilized conforms to CCITT Recommendation G.721 and ANSI T1.303-1989. The device also supports a 24 kbit/s (three bit word) algorithm (CCITT/G.723).

Switching, on-the-fly, between 32 kbit/s and 24 kbit/s, is possible by toggling the appropriate Mode Select (MS1-MS4) control pins.

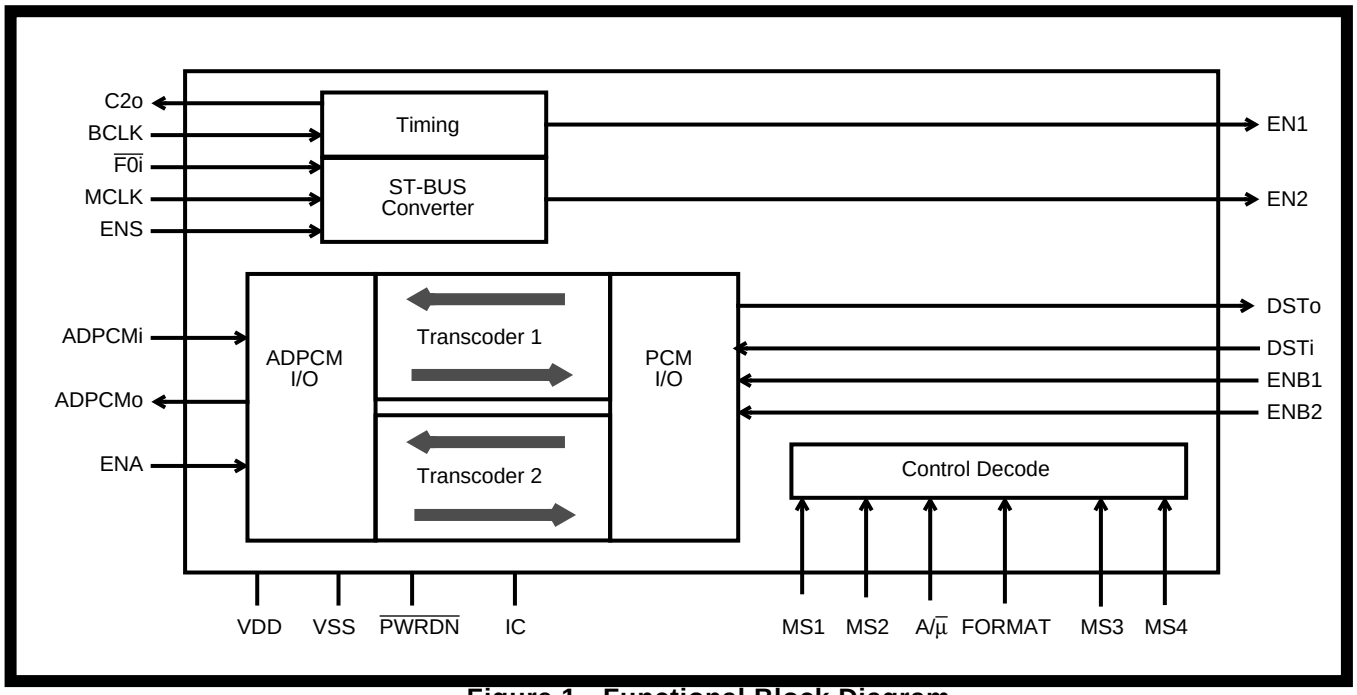


Figure 1 - Functional Block Diagram

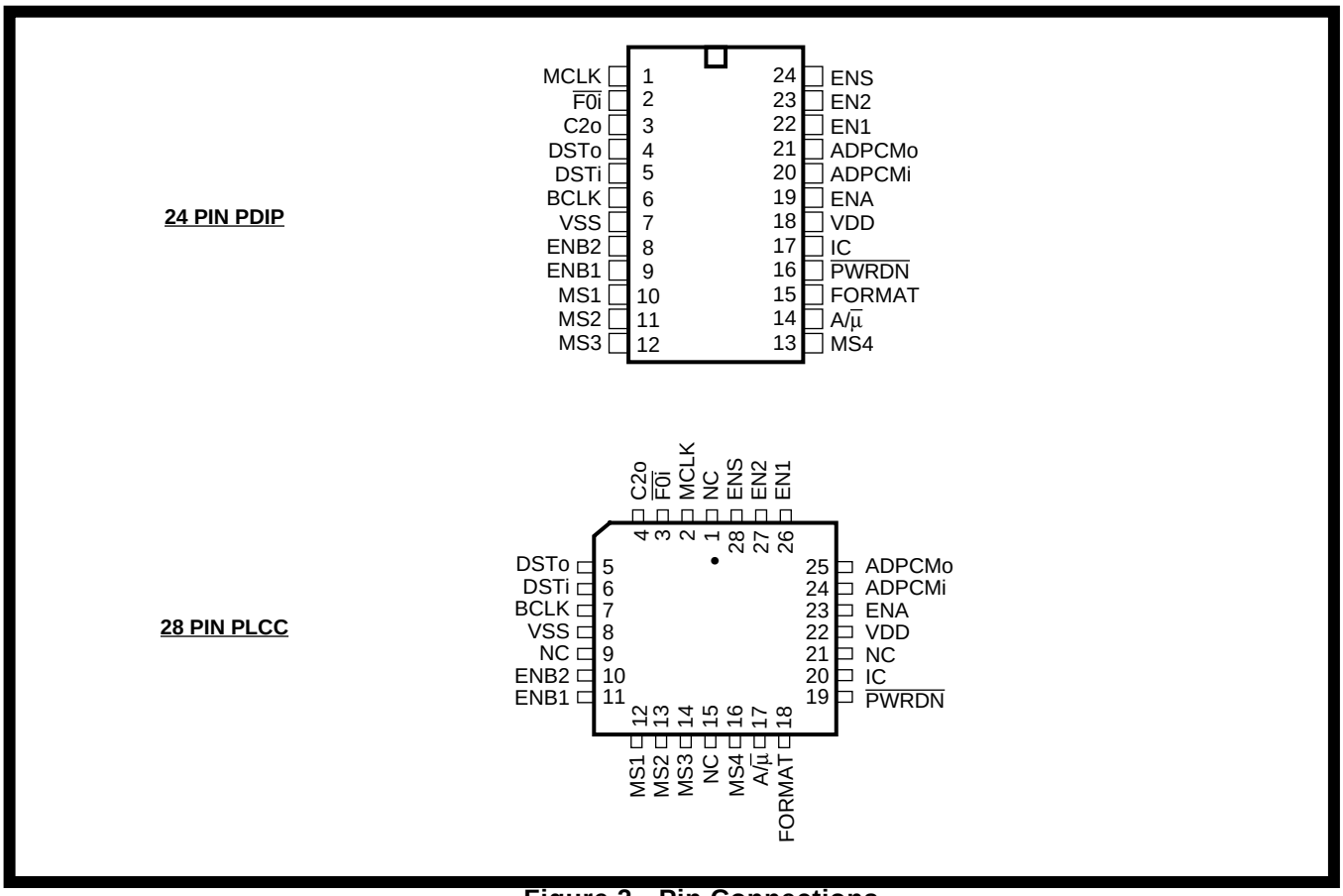


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
DIP	PLCC		
1	2	MCLK	Master Clock input. This 4.096 MHz clock is used as an internal master clock and must be provided during both ST-BUS and SSI modes of operation. This is a TTL level input. In ST-BUS mode the MCLK input (also known as $\overline{C4i}$ in ST-BUS terms) is derived from the synchronous 4.096 MHz clock available from the layer 1 transceiver device. The $\overline{C4i}$ clock, input to MCLK, is used in this mode as both the internal master clock and for deriving the C2o output clock and EN1/EN2 output enable strobes. In SSI mode a 4.096 MHz master clock must be derived from an external source. This master clock may be asynchronous relative to the 8 kHz frame reference.
2	3	$\overline{F0i}$	Frame alignment input pulse for ST-BUS interface operation. This input should be tied low if ST-BUS operation is not required. This is a TTL level input.
3	4	C2o	2.048MHz Clock output for ST-BUS applications. This clock is MCLK divided by 2 and inverted. The C2o output activity state is governed by the $\overline{F0i}$ input pin condition. **F0i input** — **C2o output** V_{SS} — disabled (SSI mode automatically activated) V_{DD} — enabled Active $\overline{F0i}$ strobe — enabled and aligned to $\overline{F0i}$ due to $\overline{C4i}$ input at MCLK
4	5	DSTo	Serial PCM octet output stream. Refer to the serial timing diagram of Figure 12.
5	6	DSTi	Serial PCM octet input data stream. Refer to the serial timing diagram of Figure 12. This is a TTL level input.

Pin Description (continued)

Pin # DIP	Pin # PLCC	Name	Description
6	7	BCLK	Bit Clock input for both PCM and ADPCM ports; used in SSI mode only. The falling edge of this clock is used to clock data in on DSTi and ADPCMi. The rising edge is used to clock data out on DSTo and ADPCMo. Can be any rate between 128 kHz and 2.048 MHz. Refer to the serial timing diagrams of Figures 12 and 13. When not used, this pin should be tied to V_{SS}. This is a TTL level input.
7	8	V_{SS}	Power supply ground (0 volts).
8	10	ENB2	Enable Strobe input for B2 channel PCM timing in SSI mode only. A valid 8-bit strobe must be present at this input if there are no ST-BUS signals at $\overline{F0i}$ and MCLK. When the device detects a valid frame pulse at $\overline{F0i}$, PCM timing for the B2 ST-BUS channel is decoded internally and the ENB2 input is ignored. When not used this pin should be tied to V_{SS}. This is a TTL level input.
9	11	ENB1	Enable Strobe input for B1 channel PCM timing in SSI mode only. A valid 8-bit strobe must be present at this input if there are no ST-BUS signals at $\overline{F0i}$ and MCLK. When the device detects a valid frame pulse at $\overline{F0i}$, PCM timing for the B1 ST-BUS channel is decoded internally and the ENB1 input is ignored. When not used this pin should be tied to V_{SS}. This is a TTL level input.
10, 11	12, 13	MS1, MS2	Mode select control input pins 1 and 2 for the B1 channel according to the following: **MS2** **MS1** **B1 Channel** 0 0 algorithm reset 0 1 ADPCM bypass mode (24 or 32 kbit/s) 1 0 24 kbit/s ADPCM mode 1 1 32 kbit/s ADPCM mode These are TTL level inputs.
12, 13	14, 16	MS3, MS4	Mode select control input pins 3 and 4 for the B2 channel according to the following: **MS4** **MS3** **B2 Channel** 0 0 algorithm reset 0 1 ADPCM bypass mode (24 or 32 kbit/s) 1 0 24 kbit/s ADPCM mode 1 1 32 kbit/s ADPCM mode These are TTL level inputs.
14	17	A/μ	Law select input. Selects $\overline{\mu}$-Law when low, A-Law when high. This is a TTL level input.
15	18	FORMAT	Format select input. Selects CCITT PCM coding if high, or SIGN MAGNITUDE PCM if low. This is a TTL level input.
16	19	$\overline{PWRDN}$	Power Down input. Logic low on this pin forces the device to assume an internal power down mode where all operation is halted. This mode minimizes power consumption. Outputs are tri-stated. This is a schmidt trigger input.
17	20	IC	Internal Connection. Tie to V_{SS} for normal operation.
18	22	V_{DD}	Positive power supply input, 5 volts $\pm$ 10%.
19	23	ENA	Enable Strobe input for both input and output ADPCM channels; used for SSI operation only. Refer to Figure 3. When not used, tie to VSS. This is a TTL level input.
20	24	ADPCMi	Serial ADPCM word input data stream. Refer to the serial timing diagram of Fig. 13. This is a TTL level input.
21	25	ADPCMo	Serial ADPCM word output stream. Refer to the serial timing diagram of Fig.13.

Pin Description (continued)

Pin #		Name	Description
DIP	PLCC		
22	26	EN1	Channel 1 Output Enable strobe. This output is decoded from the ST-BUS $\overline{C4i}$ and $\overline{F0i}$ signals and its position, within the ST-BUS stream, may be controlled via the ENS pin. Refer to the ST-BUS relative timing diagram shown in Figure 4.
23	27	EN2	Channel 2 Output Enable strobe. This output is decoded from the ST-BUS $\overline{C4i}$ and $\overline{F0i}$ signals and its position, within the ST-BUS stream, may be controlled via the ENS pin. Refer to the ST-BUS timing diagram shown in Figure 4.
24	28	ENS	Enable Select input for ST-BUS operation only. This control pin changes the ST-BUS channel position of EN1 and EN2 as well as the ADPCM channel position. Refer to the ST-BUS timing diagram shown in Figure 4. When not used this pin should be tied to V_{DD}. This is a TTL level input.
	1, 9, 15, 21	NC	No Connection. Leave open circuit.

Functional Description

The Dual-channel ADPCM Transcoder is a low power, CMOS device capable of two encoder functions and two decoder functions. Two 64 kbit/s PCM channels (PCM octets) are compressed into two 32 kbit/s ADPCM channels (ADPCM words), and two 32 kbit/s ADPCM channels (ADPCM words) are expanded into two 64 kbit/s PCM channels (PCM octets). The ADPCM transcoding algorithm utilized conforms to CCITT recommendation G.721 and ANSI T1.303-1989. The device also supports a 24 kbit/s (three bit word) algorithm (CCITT/G.723). Switching, on-the-fly, between 32 kbit/s and 24 kbit/s is possible by toggling the appropriate Mode Select (MS1-MS4) control pins.

The internal circuitry requires very little power to operate; 25mW typically for dual channel operation. A master clock frequency of 4.096 MHz is required for the circuit to complete two encode channels and two decode channels. Operation with an asynchronous master clock, relative to the 8 kHz reference, is allowed.

All optional functions of the device are pin selected, no microprocessor is required. This allows a simple interface with industry standard Codecs, Dual Codecs, Digital Phone devices, and Layer 1 transceivers.

The PCM and ADPCM serial busses are a Synchronous Serial Interface (SSI), allowing serial clock rates from 128 kHz to 2.048 MHz. Additional pins on the device allow an easy interface to an ST-BUS component. On chip channel counters provide channel enable outputs, as well as a 2.048 MHz clock output, useful for driving the timing input pins of standard CODEC devices.

Serial I/O Ports (ADPCMi, ADPCMo, ENA, ENB1, ENB2, DSTi, DSTo, C2o, EN1, EN2, ENS, $\overline{F0i}$)

Serial I/O data transfer to the Dual ADPCM Transcoder is provided through the PCM and the ADPCM ports. Serial I/O port operation is similar for both ST-BUS and SSI modes. The Dual ADPCM Transcoder determines the mode of operation by monitoring the signal applied to the $\overline{F0i}$ pin. When a valid ST-BUS Frame Pulse (244ns low going pulse) is connected to the $\overline{F0i}$ pin the transcoder will assume ST-BUS operation. If $\overline{F0i}$ is tied continuously to V_{SS} the transcoder will assume SSI operation. Pin functionality in each of these modes is described in the following sub-sections.

ADPCM Port Operation (ADPCMi, ADPCMo, ENA)

The ADPCM port consists of ADPCMi, ADPCMo and ENA. ADPCM port functionality is similar for both ST-BUS and SSI operation, the difference being in where the BCLK signal is derived and in where the ADPCM words are placed within the 8 kHz frame.

For SSI operation (i.e., when $\overline{F0i}$ is tied continuously to V_{SS}) both channels of ADPCM code words are transferred over ADPCMi/ADPCMo at the bit clock rate (BCLK) during the channel time defined by the input strobe at ENA. Refer to Figure 3 and to Figure 13. Data is latched into the ADPCMi pin with the falling edge of BCLK while output data is made available at ADPCMo on the rising edge of BCLK.

For ST-BUS operation (i.e., when a valid ST-BUS frame pulse is applied to the $\overline{F0i}$ input) the bit rate, at 2.048 MHz, is generated internally from the master clock input at the MCLK pin. The BCLK and ENA inputs are ignored. Data is latched into the ADPCMi pin at the three-quarter bit position which occurs at the second rising edge of MCLK ($\overline{C4i}$) within the bit cell boundary. Output data, on ADPCMo, is made available at the first falling edge of MCLK ($\overline{C4i}$) within the bit cell boundary. Refer to Figure 13.

ADPCM word placement, within the ST-BUS frame, is governed by the logic state applied at the ENS input pin. Referring to Figure 4, when ENS = 0, the ADPCM words are placed in channel 2 while when ENS = 1 the ADPCM words are placed in channel 3. Unlike the PCM octets the ADPCM words never reside within the ST-BUS channel 0 or 1 timeslots.

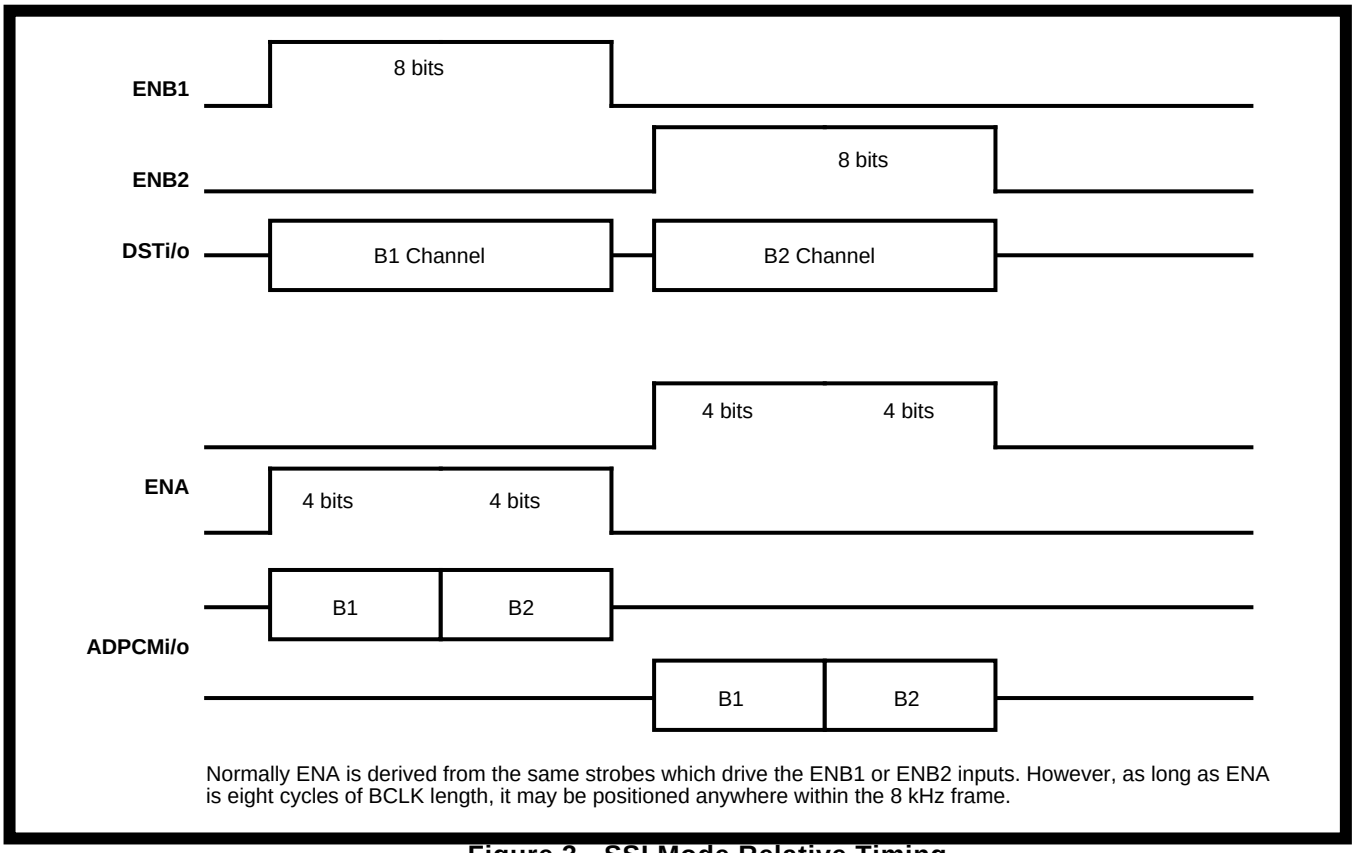
PCM Port Operation (DSTi, DSTo, ENB1, ENB2)

The PCM port consists of DSTi, DSTo, ENB1 and ENB2. PCM port functionality is almost identical for both ST-BUS and SSI operation, the difference being from where the BCLK signal is derived and whether the enable strobes are generated internally or sourced externally.

Both channels of PCM octets are transferred over DSTi/DSTo at the bit clock rate during the channel time defined by the input strobes at ENB1 and ENB2 or by internally generated timeslots.

For ST-BUS operation, (i.e., when a valid ST-BUS frame pulse is applied to the $\overline{F0i}$ input) the bit rate, at 2.048 MHz, is generated internally from the master clock input at the MCLK pin. The BCLK and ENA inputs are ignored. ST-BUS timeslot assignment is also generated internally and can be programmed into channels 0 and 1 or into channels 2 and 3 with the ENS input pin. Refer to Figure 4. In this mode the ENB1 and ENB2 inputs are ignored by the device. The decoded channel timeslots (0 and 1 or 2 and 3) are made available, along with the 2.048 MHz bit clock, at EN1, EN2 and C2o for controlling CODEC devices as shown in the Applications section (refer to Figures 7 and 11). Data is latched into the DSTi pin at the three-quarter bit position which occurs at the second rising edge of MCLK ($\overline{C4i}$) within the bit cell boundary. Output data, on DSTo, is made available at the first falling edge of MCLK ($\overline{C4i}$) within the bit cell boundary. Refer to Figure 12.

For SSI operation, (i.e., when $\overline{F0i}$ is tied continuously to V_{SS}) the bit rate is set by the input clock presented at the BCLK pin. Data is transferred at the bit clock rate (BCLK) during the B1 and B2 channels as defined by input strobes ENB1 and ENB2, respectively. Note that ENB1 and ENB2 are also used as the framing inputs for internal operation of



Normally ENA is derived from the same strobes which drive the ENB1 or ENB2 inputs. However, as long as ENA is eight cycles of BCLK length, it may be positioned anywhere within the 8 kHz frame.

Figure 3 - SSI Mode Relative Timing

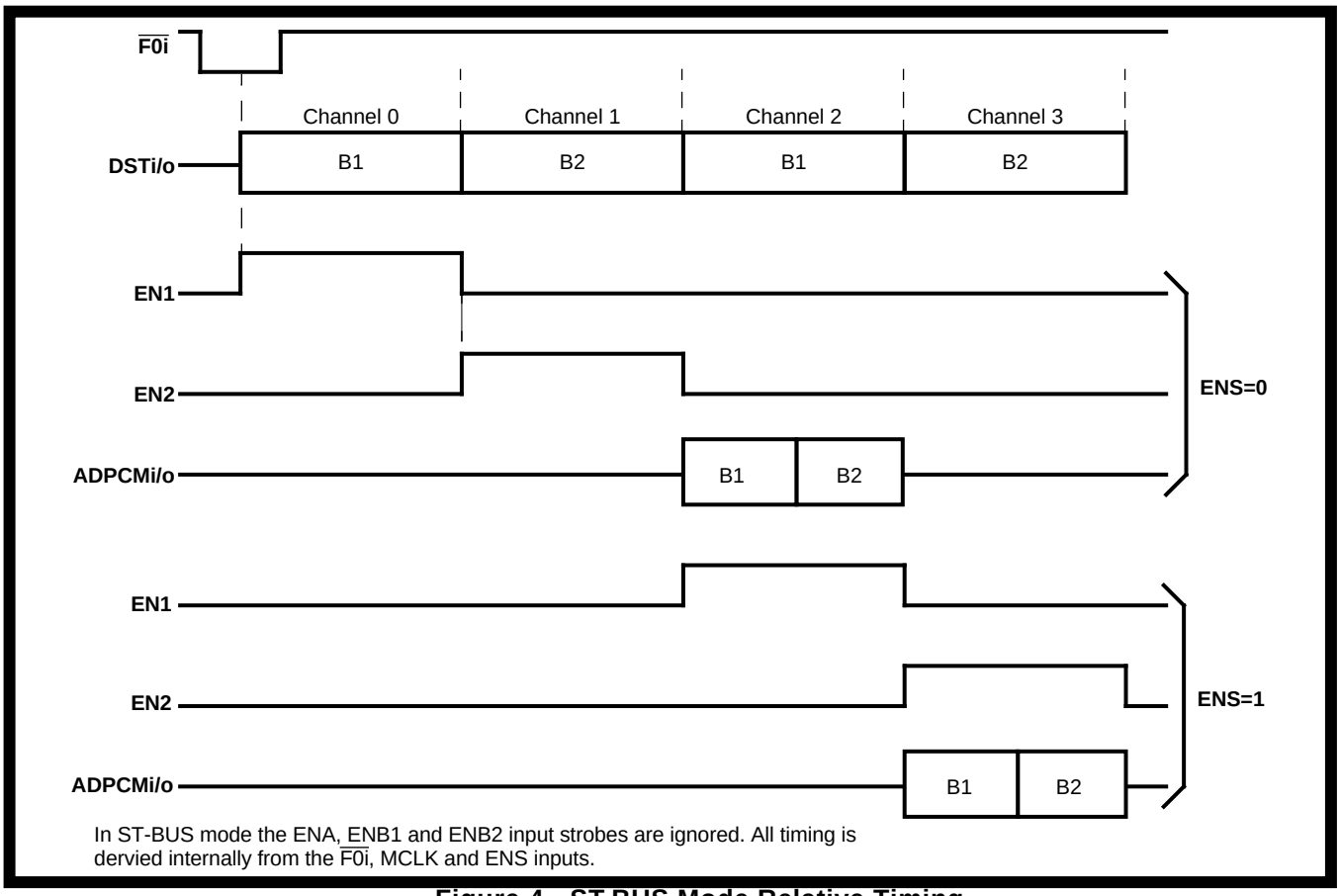


Figure 4 - ST-BUS Mode Relative Timing

the device and must, therefore, be present whenever a transcoding operation is required. These inputs may be tied together and connected to the same strobe for single channel operation. Only the B1 nibble is valid in this mode. Data is latched into the DSTi pin with the falling edge of the bit clock while output data is made available at DSTo on the rising edge of the bit clock.

ST-BUS Conversion (F0i, C2o, EN1, EN2, ENS)

A simple converter circuit is incorporated which allows ST-BUS signals to be converted to SSI signals. In this manner it is very simple for an ST-BUS application to be mixed with CODECs utilizing a strobed data I/O.

This converter circuit consists of the F0i input and C2o, EN1 and EN2 output pins (as well as the MCLK input master clock). The output C4b clock and frame pulse strobe (F0b), from the ST-BUS layer 1 transceiver, are connected directly to the master clock (MCLK) and frame pulse (F0i) inputs of the transcoder. A 2.048 MHz (C2o) bit clock output is made available when a valid Frame Pulse is connected to the F0i pin or the F0i pin is tied high. If the F0i pin is tied low the C2o output is forced continuously to a logic low level (not tri-stated). Forcing the C2o output to logic low enhances power conservation as well as removing a non-required clock signal from the circuit. This 2.048 MHz bit clock may be used to control external CODEC functions.

The 4.096 MHz and frame pulse signals are also decoded into two output strobes corresponding to the B1 and B2 channel timeslots of the ST-BUS. These strobes (EN1 and EN2) are then used to control the timing inputs of an external CODEC. A typical example of this connection scheme is shown in the application diagram of Figure 7.

The Enable Strobe pin (ENS) is used to position the output strobes EN1 and EN2 within the ST-BUS frame. Referring to Figure 4, when ENS=0 the output strobes are positioned in channels 0 and 1 of the ST-BUS frame. When ENS=1 the output strobes are positioned in channels 2 and 3 of the ST-BUS frame. This flexibility allows the transcoder to be used in ST-BUS basic rate applications where channels 0 and 1 are defined as the D and C channels, respectively, and also in line-card applications where the full 2.048 MHz bandwidth is used for conveying data and/or digitally encoded voice information.

Mode Selection (MS1, MS2, MS3, MS4)

Separate mode select pins are available for per-channel B1 and B2 operation. MS1 and MS2 are used to configure the B1 channel while MS3 and MS4 configure the B2 channel. Normally the mode select pins are operated as static control lines. The exception to this is for on-the-fly programming to/ from 32 kbit/s from/to 24 kbit/s modes.

B1 Channel			B2 Channel	
MS2	MS1	Operational Mode	MS4	MS3
0	0	algorithm reset	0	0
0	1	ADPCM bypass mode (24 or 32 kbit/s)	0	1
1	0	24 kbit/s ADPCM mode	1	0
1	1	32 kbit/s ADPCM mode	1	1

Algorithm Reset Mode

An algorithm reset is accomplished by forcing all mode select pins simultaneously to logic zero. While asserted, this will cause the device to incrementally converge the internal variables of both channels to the 'Optional reset values' per G.721. Invoking the reset conditon on only one channel will cause that channel to be reset properly and the other channel's operation to be undefined. This optional reset requires that the master clock (MCLK) and frame pulse (ENB1/2 or $\overline{F0i}$) remain active and that the reset condition be valid for at least four frames. Note that this is not a power down mode.

ADPCM By-Pass Mode

In ADPCM bypass mode the B1 and B2 channel words are transparently relayed (with a two-frame delay) to/from the ADPCM port and placed into the most significant nibbles of the B1 and B2 channel PCM octets. Refer to Figure 5. The ability to transfer ADPCM words transparently through the transcoder enables set-to-set connections for wireless telephony applications.

24 kbit/s Mode

In 24 kbit/s mode (CCITT G.723) PCM octets are transcoded into three bit words rather than the four bit words of the standard 32 kbit/s ADPCM. This is useful in situations where lower bandwidth transmission is required. Dynamic operation of the mode select control pins will allow switching from 32 kbit/s mode to 24 kbit/s mode on a frame by frame basis. Figure 6 shows the internal pipelining of the conversion sequence and how the mode select pins are to be used. Fig. 15 details the timing

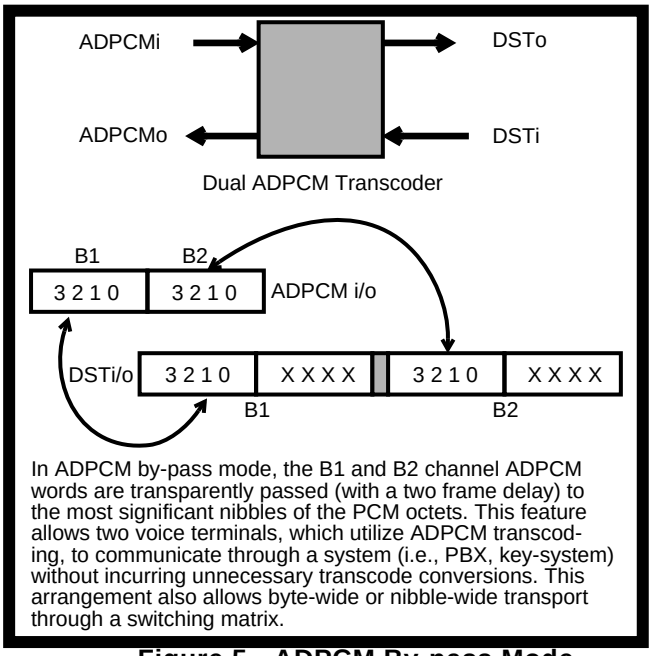


Figure 5 - ADPCM By-pass Mode

requirements necessary for on-the-fly control of the Mode Select pins. The 3-bit ADPCM words occupy the most significant bit positions of the standard 4-bit ADPCM word.

32 kbit/s ADPCM Mode

In 32 kbit/s mode PCM octets are transcoded into four bit words as described in CCITT G.721. This is the standard mode of operation and, if the other modes are not required, can be implemented by simply tying the per-channel mode select pins to V_{DD}.

Master Clock (MCLK)

A 4.096 MHz master clock is required for execution of the dual transcoding algorithm. The algorithm requires 512 cycles of MCLK during one frame for proper operation. This input, at the MCLK pin, may be asynchronous with the 8 kHz frame provided that the lowest frequency, and/or deviation due to clock jitter, still meets the minimum strobe period requirement of 512 t_{C4P} -50nSec. (See AC Electrical Characteristics - Serial PCM/ADPCM Interfaces.)

For example, a system producing large jitter values can be accommodated by running an over-speed MCLK to ensure that a minimum 512 MCLK cycles per frame is obtained. The minimum MCLK period is 190 nSeconds, which translates to a maximum frequency of 5.26 MHz. Extra MCLK cycles (>512/ frame) are acceptable because the transcoder is re-aligned by the appropriate strobe signals each frame.

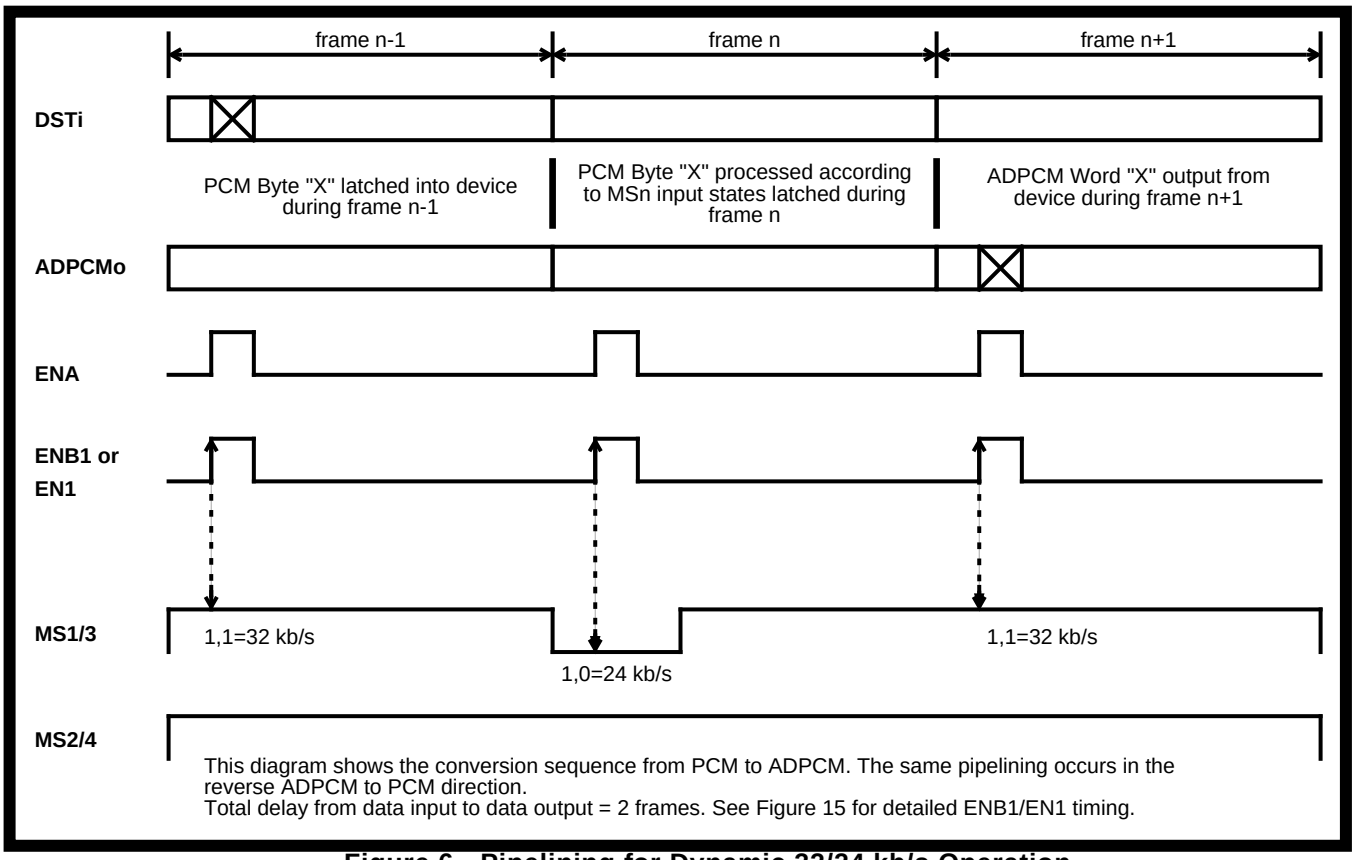


Figure 6 - Pipelining for Dynamic 32/24 kb/s Operation

Bit Clock (BCLK)

For SSI operation the bit rate, for both ADPCM and PCM ports, is determined by the clock input at BCLK. BCLK must be eight periods in duration and synchronous with the 8 kHz frame input at ENB1. Data is sampled at DSTi and at ADPCMi concurrent with the falling edge of BCLK. Data is available at DSTo and ADPCMo concurrent with the rising edge of BCLK. BCLK may be any rate between 128 kHz and 2.048 MHz. Refer to Figures 12 and 13.

For ST-BUS operation BCLK is ignored and the bit rate is internally set to 2.048 MHz.

PCM Law Control (A/μ, FORMAT)

The PCM companding/coding law invoked by the transcoder is controlled via the A/$\overline{\mu}$ and FORMAT pins. CCITT G.711 companding curves, μ-Law and A-Law, are determined by the A/$\overline{\mu}$ pin (0=$\overline{\mu}$-Law; 1=A-Law). Per sample, digital code assignment can conform to CCITT G.711 (when FORMAT=1) or to Sign-Magnitude coding (when FORMAT=0). Table 1 illustrates these choices.

	FORMAT		
	0	1	
PCM Code	Sign-Magnitude **A/$\overline{\mu}$ = 0 or 1**	CCITT (G.711)	
		(A/$\overline{\mu}$ = 0)	**(A/μ = 1)**
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
- Zero	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 1

Processing Delay through the Device

One 8 kHz frame is required for serial loading of the input buffers, and one frame is required for processing, for a total of two frame delays through the device. All internal input/output PCM and ADPCM shift registers are parallel loaded through secondary buffers on an internal frame pulse. The device derives its internal frame reference from the $\overline{F0i}$, ENB1 and ENB2 pins in the following manner. If a valid ST-BUS frame pulse is present at the $\overline{F0i}$ pin the transcoder will assume ST-BUS operation and will use this input as the frame reference. In this

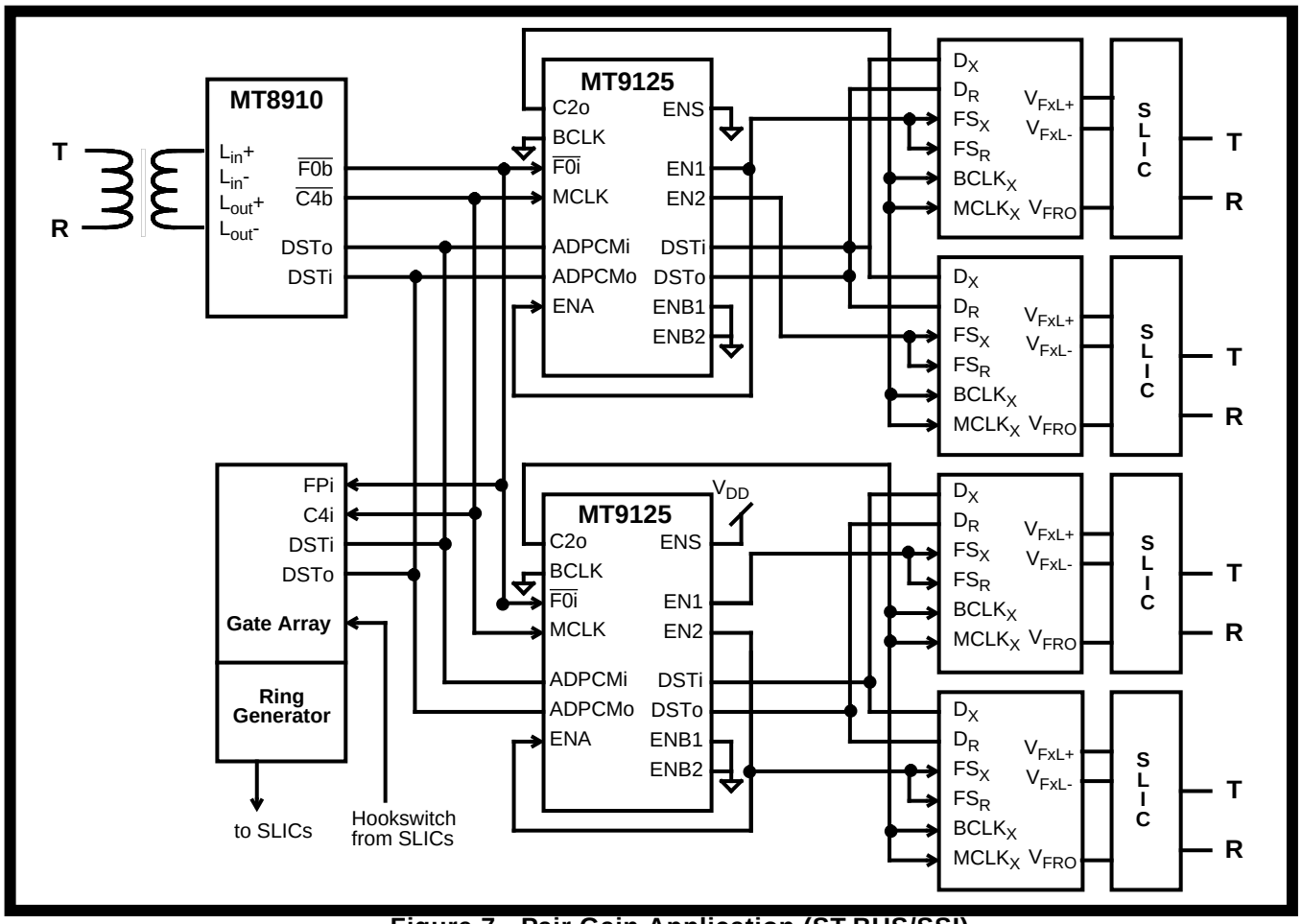


Figure 7 - Pair Gain Application (ST-BUS/SSI)

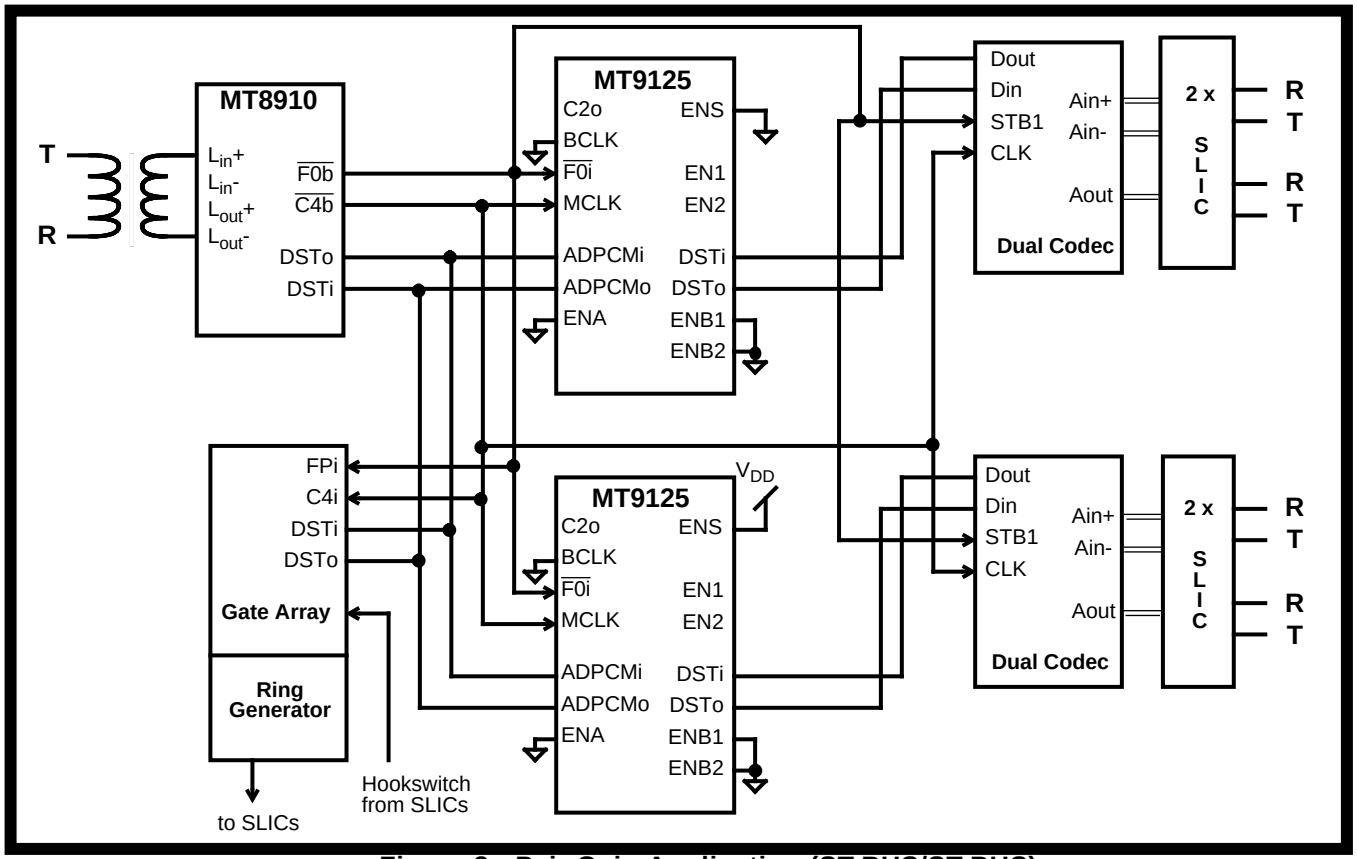


Figure 8 - Pair Gain Application (ST-BUS/ST-BUS)

configuration the ENB1 and ENB2 inputs are ignored. If $\overline{F0i}$ is tied continuously to V_{SS}, then SSI operation will be assumed and the transcoder will use the strobes connected to ENB1 and ENB2 as its internal reference.

Power-Down Operation ($\overline{PWRDN}$)

To minimize power consumption a pin selected, power-down option is provided. Device power down is accomplished by forcing the $\overline{PWRDN}$ pin to V_{SS}. This asynchronous control forces all internal clocking to halt and the C2o, EN1, EN2, DSTo and ADPCMo outputs to become tri-stated. Upon returning $\overline{PWRDN}$ to V_{DD} coincident with the next alignment signal, all outputs will return to their active state and the internal clocks are re-started. In this mode the ADPCM algorithm is not reset to the 'optional reset values', however, the self-convergent nature of the algorithm will ensure that convergence of the (AD)PCM streams will occur within 3496 frames as specified by CCITT G.721.

Removal of the BCLK and MCLK inputs is not necessary during power-down mode. If the device is released from power-down without a valid MCLK the ADPCMo and PCMo outputs will become active, driving either continuous logic high or logic low, until a MCLK signal is applied to resume internal operation.

$\overline{PWRDN}$ is a schmidt trigger input.

Applications

Various configurations of Pair Gain drops are depicted in Figures 7, 8 and 9. These show applications using mixed ST-BUS/SSI, all ST-BUS and all SSI implementations. Figure10 shows an ST-BUS line card application for Pair Gain while Figure 11 shows a 2-channel, wireless-set, base station application based upon ST-BUS.

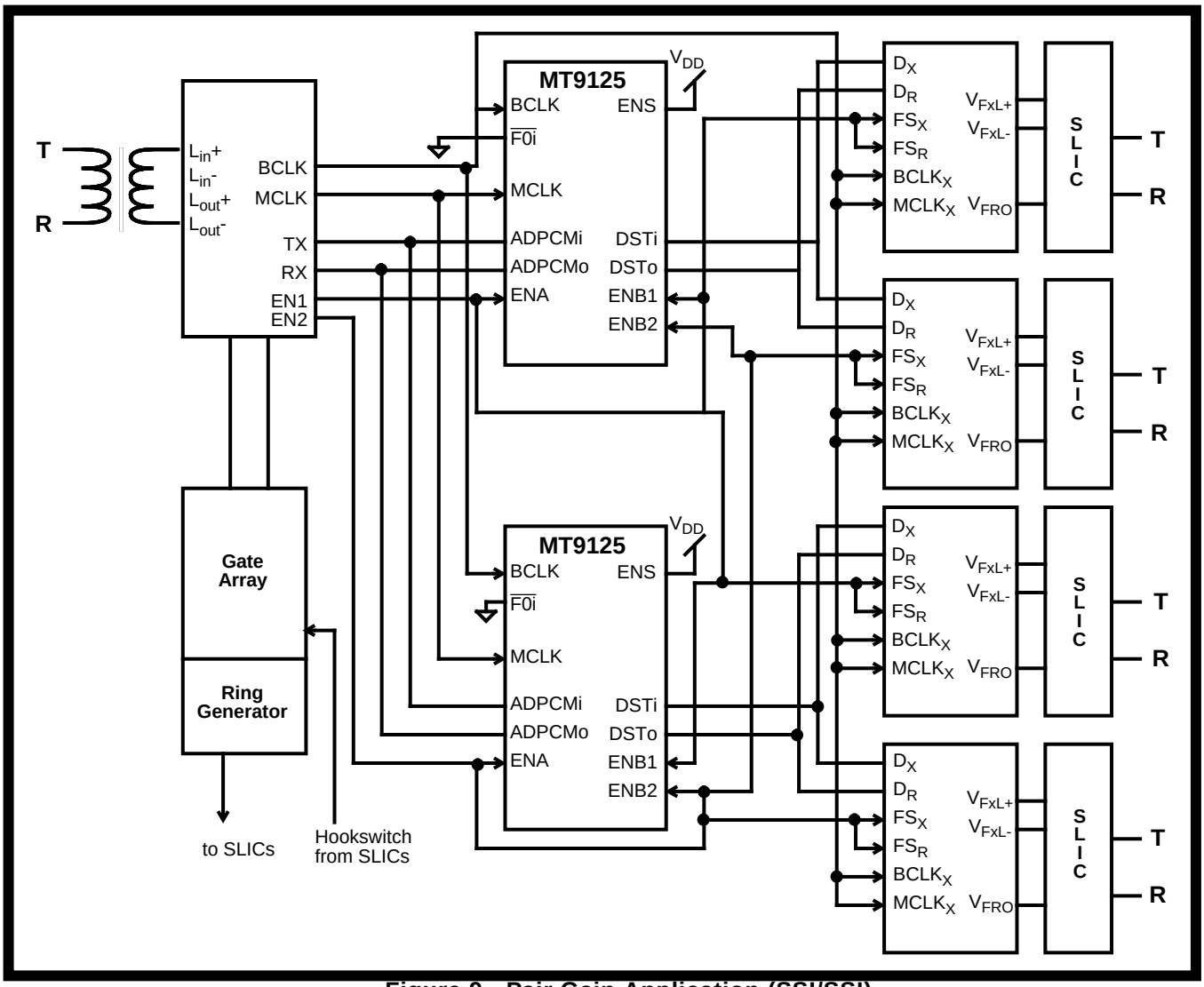


Figure 9 - Pair Gain Application (SSI/SSI)

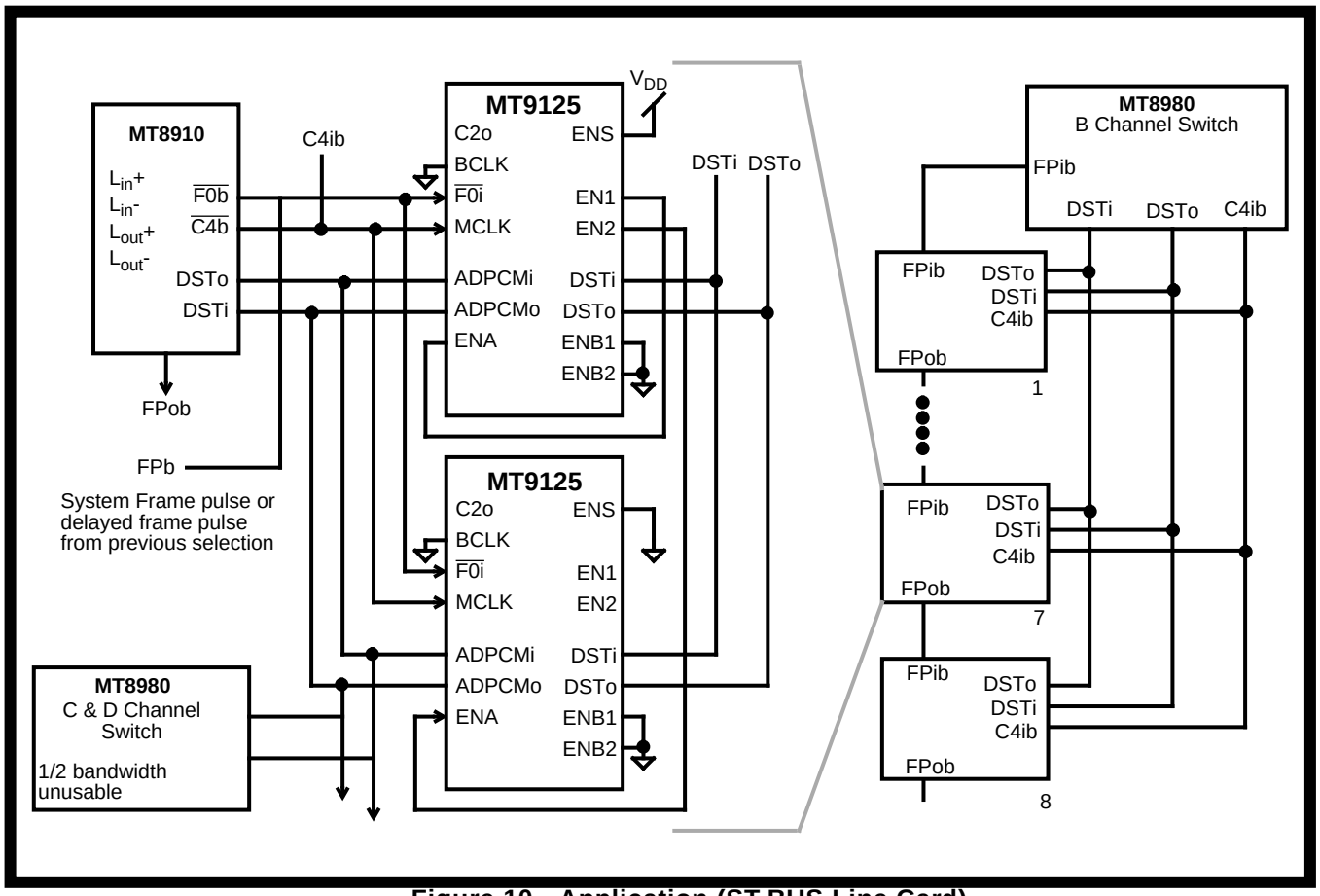


Figure 10 - Application (ST-BUS Line Card)

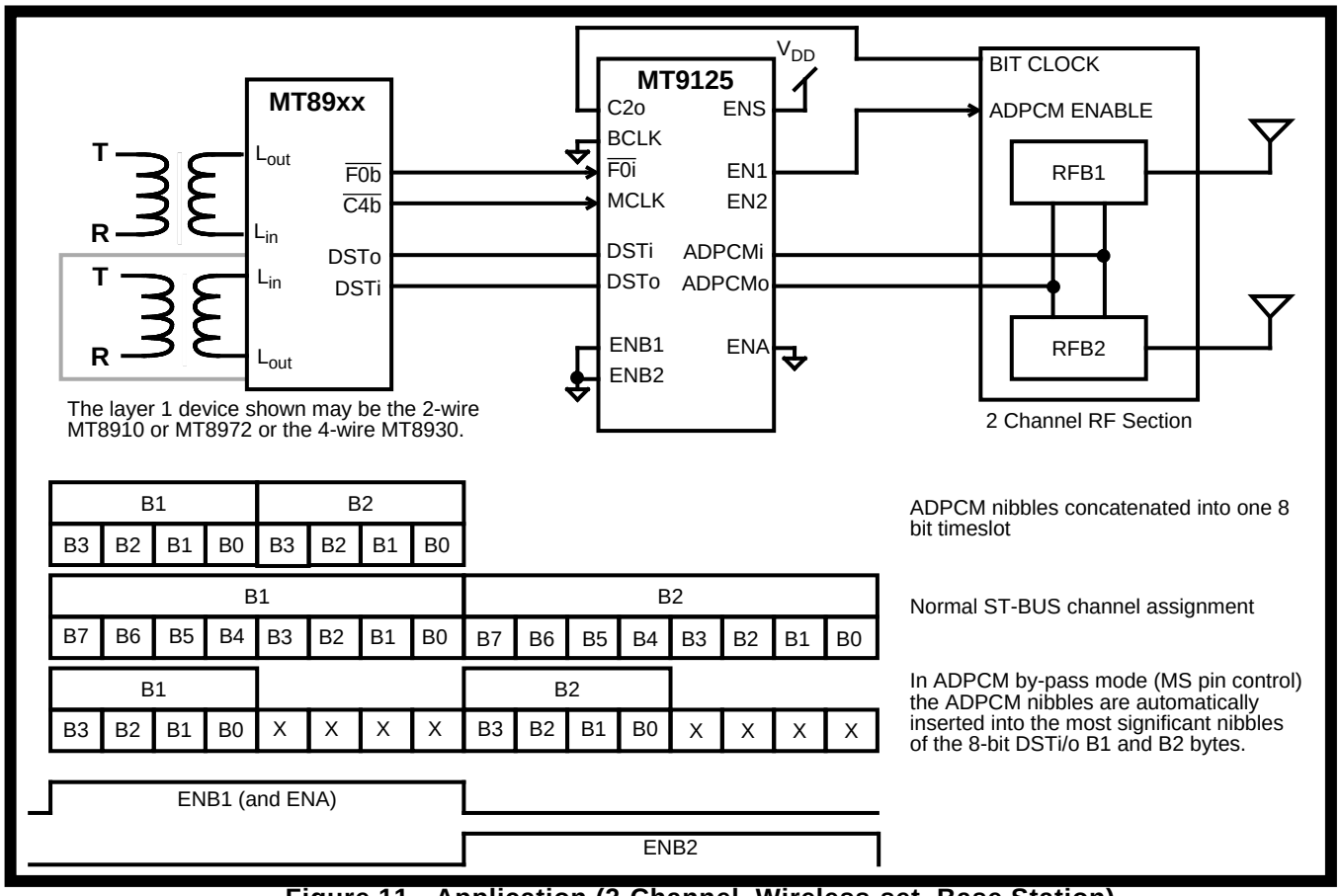


Figure 11 - Application (2-Channel, Wireless-set, Base Station)

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	7.0	V
2	Voltage on any I/O pin	V_i | V_o	-0.3	V_{DD}+ 0.3	V
3	Continuous Current on any I/O pin	I_i | I_o		±20	mA
4	Storage Temperature	T_{ST}	-65	150	°C
5	Power Dissipation	P_D		500	mW
6	Latch-up Immunity	I_{LU}	±100		mA

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
2	Input High Voltage	V_{IH}	2.4		V_{DD}	V	400mV noise margin
3	Input Low Voltage	V_{IL}	0		0.4	V	400mV noise margin
4	Operating Temperature	T_A	-40		85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current static operating	 I_{CC} I_{DD1}		 100 5		 µA mA	 $\overline{PWRDN}$ = 0 $\overline{PWRDN}$ = 1, clocks active
2	High level input voltage	V_{IH}	2.0			V	All inputs except $\overline{PWRDN}$
3	Low level input voltage	V_{IL}			0.8	V	All inputs except $\overline{PWRDN}$
4	Input leakage current	I_{IH}/I_{IL}		0.1	10	µA	V_{DD}=5.5V, V_{IN}=V_{SS} to V_{DD}
5	High level output voltage	V_{OH}	2.4			V	
6	Low level output voltage	V_{OL}			0.4	V	
7	Output low (sink) current	I_{OL}	4.0	15		mA	V_{OL}=0.4V, V_{DD}=4.5V
8	Output high (source) current	I_{OH}	4.0	10		mA	V_{OH}=2.4V, V_{DD}=4.5V
9	High impedance leakage	I_{OZ}		1	10	µA	V_{DD}=5.5V, V_{IN}=V_{SS} to V_{DD}
10	Output capacitance	C_o		10		pF	
11	Input capacitance	C_i		15		pF	
12	Positive Going Threshold Voltage ($\overline{PWRDN}$ only) Hysteresis Negative Going Threshold Voltage ($\overline{PWRDN}$ only)	V+ V_+ -V_- V_-	3.7	 1.0	 1.3	V V V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Serial PCM/ADPCM Interfaces (see Figures 12 & 13)

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Data Clock High	t_{CLH}	160			ns	C_L=150pF
2	Data Clock Low	t_{CLL}	160			ns	C_L=150pF
3	BCLK Period	t_{BCL}	400		7900	ns	C_L=150pF
4	Data Output Delay (excluding first bit)	t_{DD}		60		ns	C_L=150pF
5	Output Active to High Z	t_{AHZ}		60		ns	C_L=150pF
6	Strobe Signal Setup	t_{SSS}	80		t_{BCL}-80	ns	C_L=150pF
7	Strobe Signal Hold	t_{SSH}	80		t_{BCL}-80	ns	C_L=150pF
8	Strobe period relative to MCLK (ENB1, ENB2, ENA)		$512t_{C4P}$-50			ns	C_L=150pF
9	Data Input Setup	t_{DIS}	50			ns	C_L=150pF
10	Data Input Hold	t_{DIH}	50			ns	C_L=150pF
11	Strobe to Data Delay (first bit)	t_{SD}		60		ns	C_L=150pF
12	$\overline{F0i}$ Setup	t_{F0iS}	50	122	150	ns	C_L=150pF
13	$\overline{F0i}$ Hold	t_{F0iH}	50	122	150	ns	C_L=150pF
14	MCLK ($\overline{C4i}$) duty cycle	t_H/t_L x100	40	50	60	%	C_L=150pF
15	MCLK ($\overline{C4i}$) period	t_{C4P}	190		244.2	ns	C_L=150pF
16	Data Output delay	t_{DSToD}			125	ns	C_L=150pF
17	Data in Hold time	t_{DSTiH}	50			ns	C_L=150pF
18	Data in Setup time	t_{DSTiS}	50			ns	C_L=150pF

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

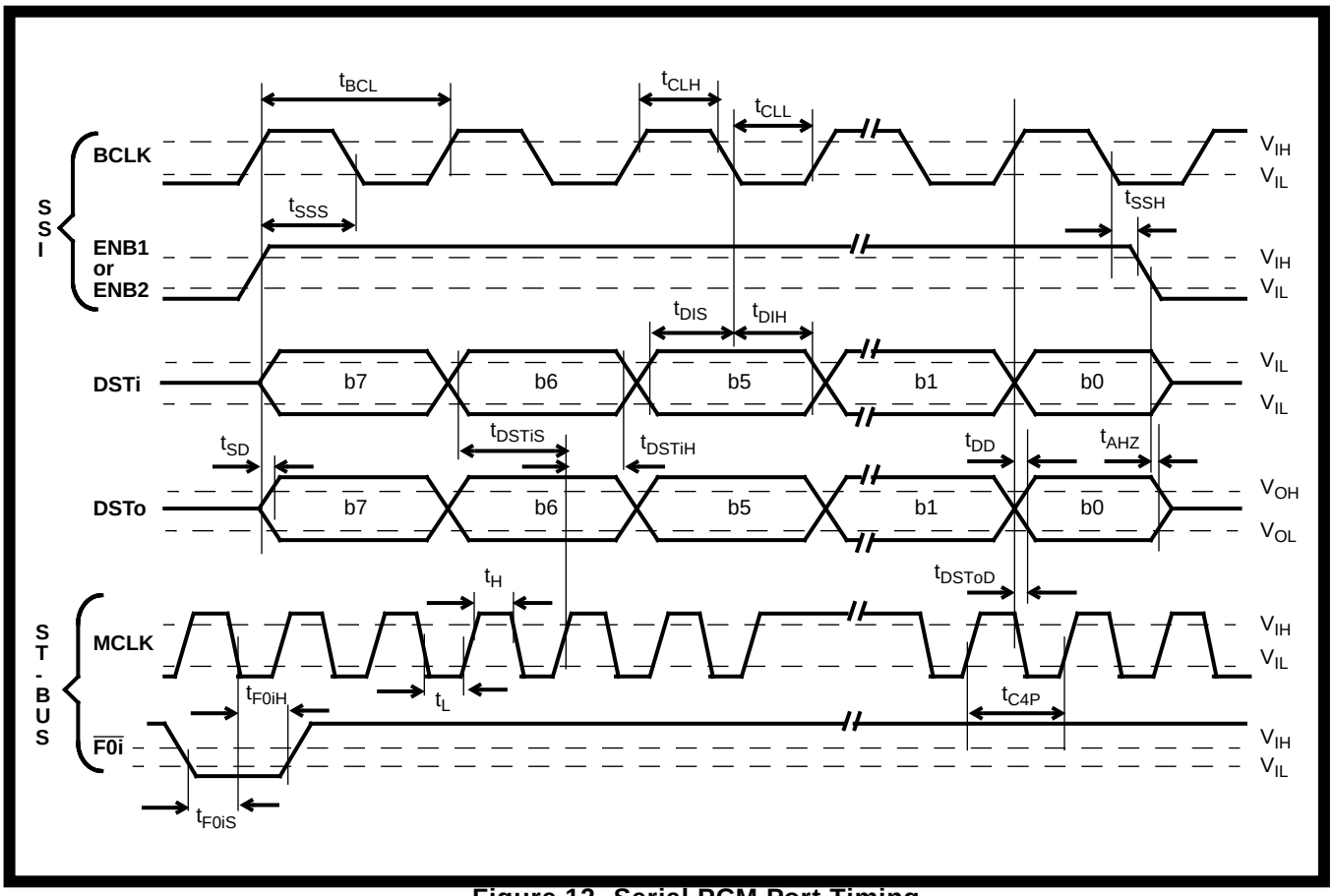


Figure 12- Serial PCM Port Timing

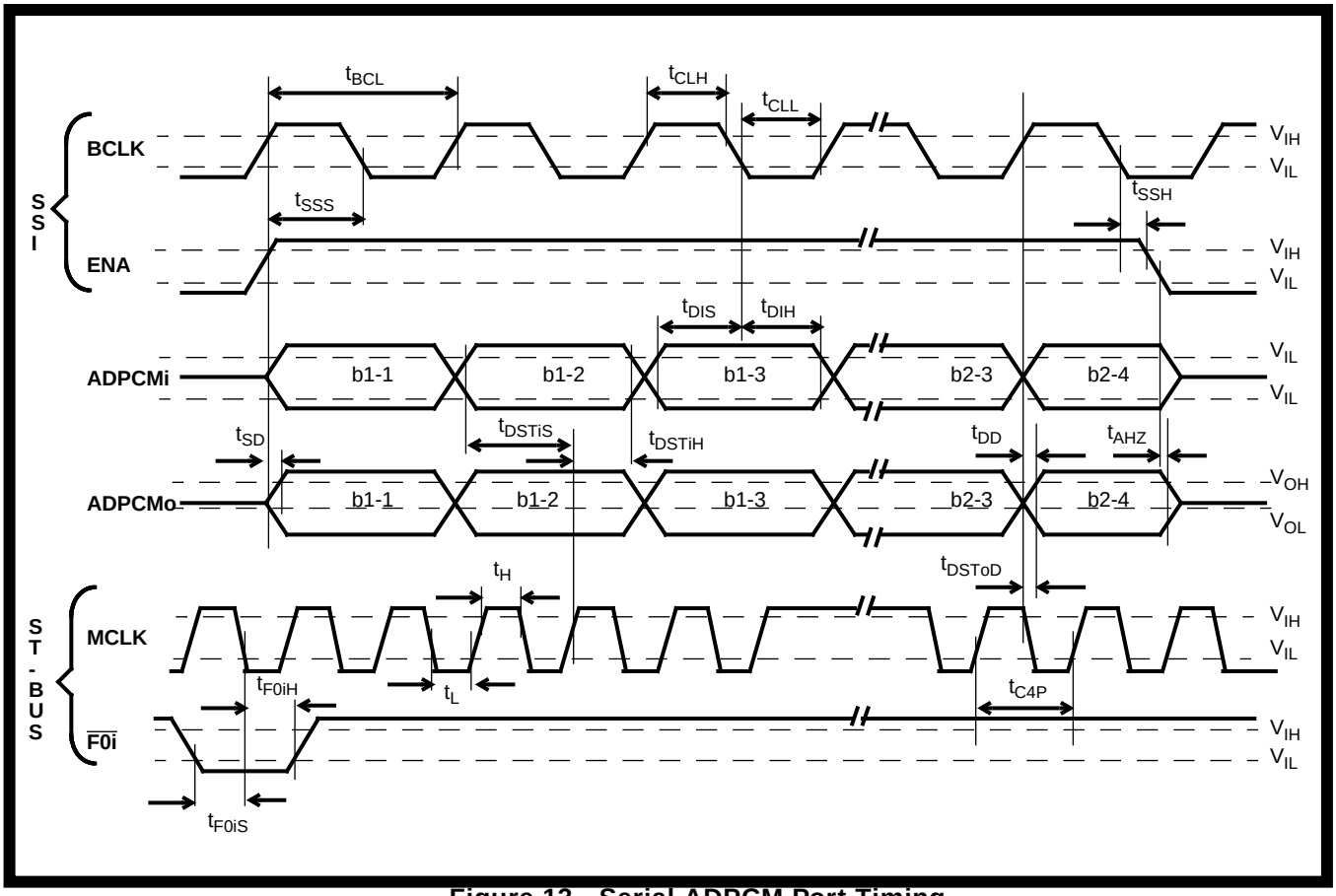


Figure 13 - Serial ADPCM Port Timing

AC Electrical Characteristics† - ST-BUS Conversion (see Figure 14)

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Delay MCLK falling to C2o rising	t_{D1}		100		ns	150pF Load
2	Delay MCLK falling to Enable	t_{D2}		100		ns	150pF Load

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

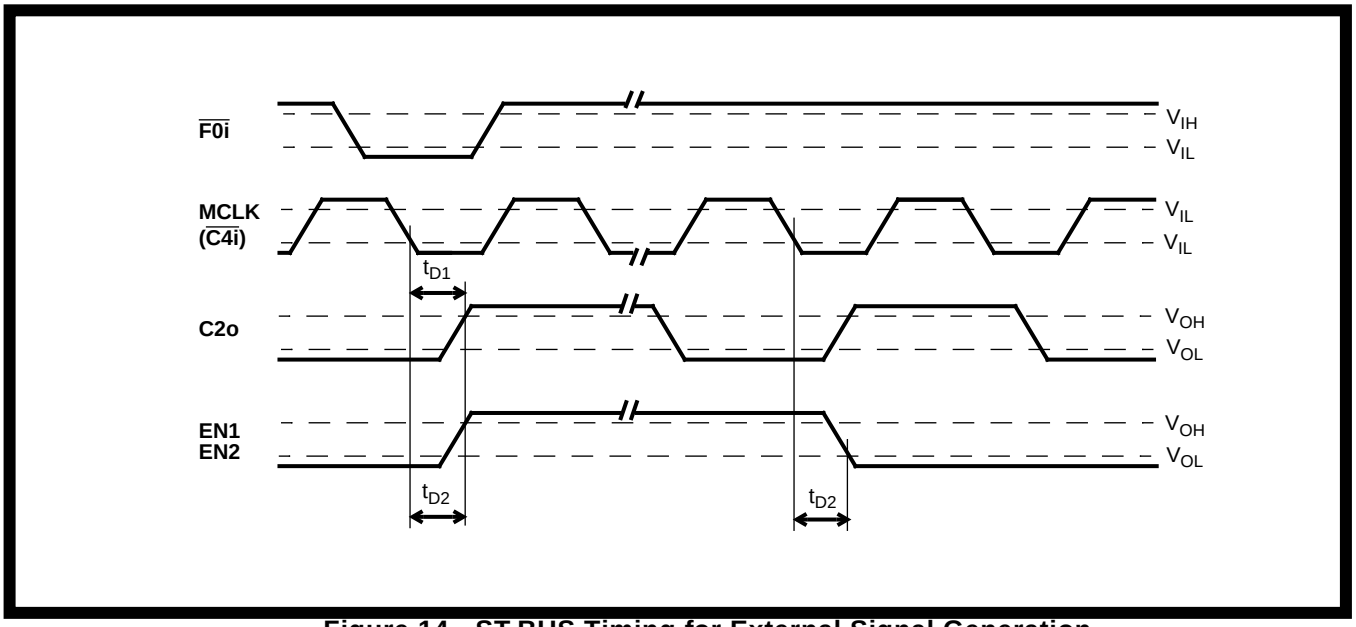


Figure 14 - ST-BUS Timing for External Signal Generation

AC Electrical Characteristics† - Mode Select Timing (see Figure 15)

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1		Mode Select Setup	t_{SU}	500			ns	
2		Mode Select Hold	t_{HOLD}			500	ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

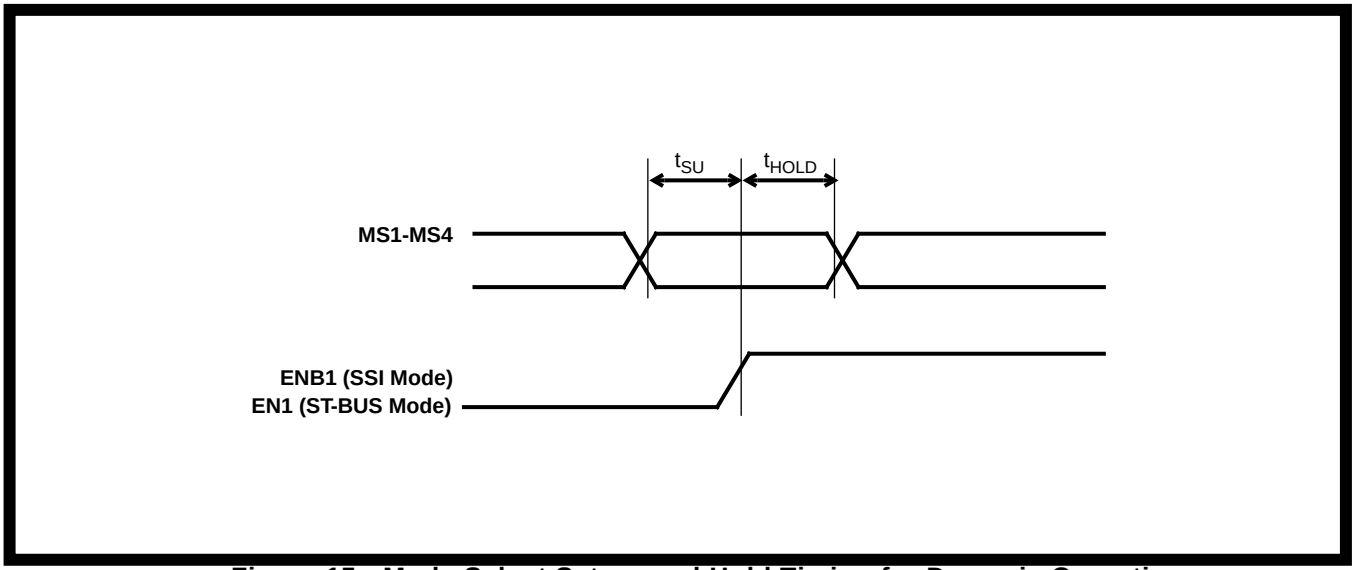


Figure 15 - Mode Select Set-up and Hold Timing for Dynamic Operation

Notes:

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