

**Features**

- Meets jitter requirements for AT&T TR62411 Stratum 3, 4 and Stratum 4 Enhanced for DS1 interfaces and for ETSI ETS 300 011 for E1 interfaces
- Provides C1.5, C3, C2, C4, C8 and C16 output clock signals
- Provides 8kHz ST-BUS framing signals
- Selectable 1.544MHz, 2.048MHz or 8kHz input reference signals
- Accepts reference inputs from two independent sources
- Provides bit error free reference switching - meets phase slope and MTIE requirements
- Operates in either Normal, Holdover and Freerun modes

**Applications**

- Synchronization and timing control for multitrunk T1 and E1 systems
- ST-BUS clock and frame pulse sources
- Primary Trunk Rate Converters

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**Ordering Information**

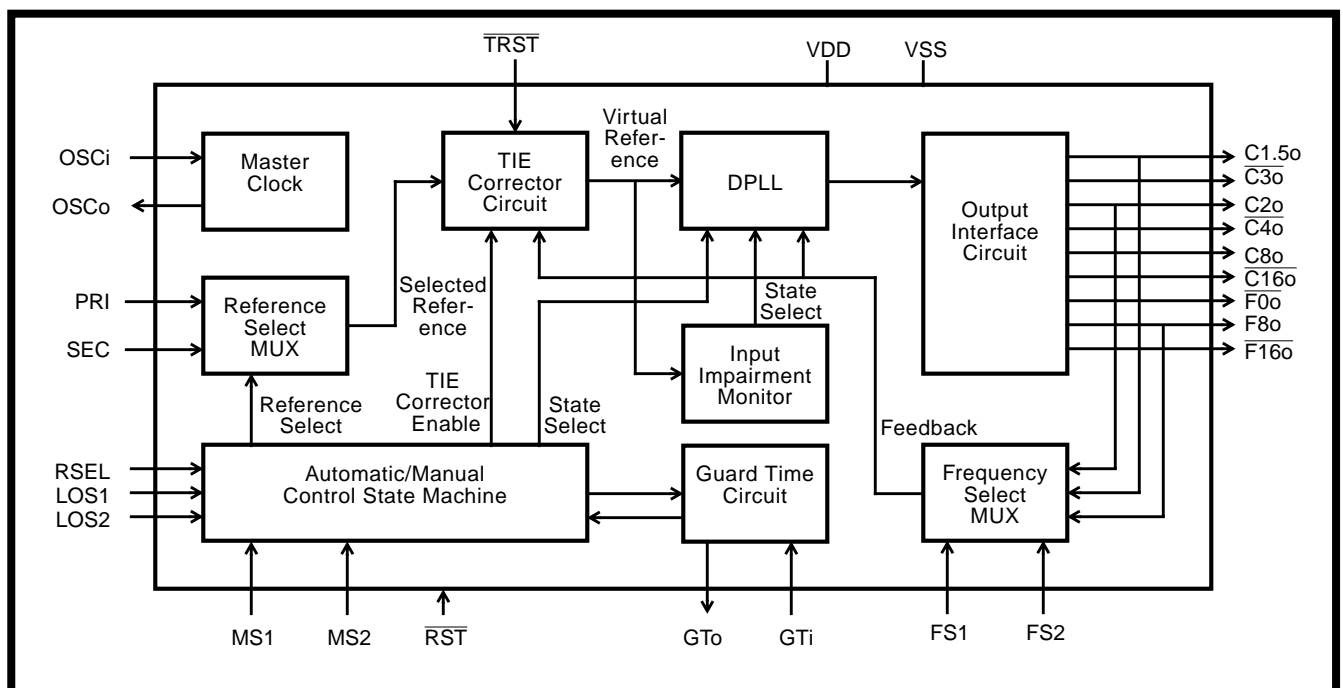
 MT9042BP 28 Pin PLCC  
 -40°C to +85°C

**Description**

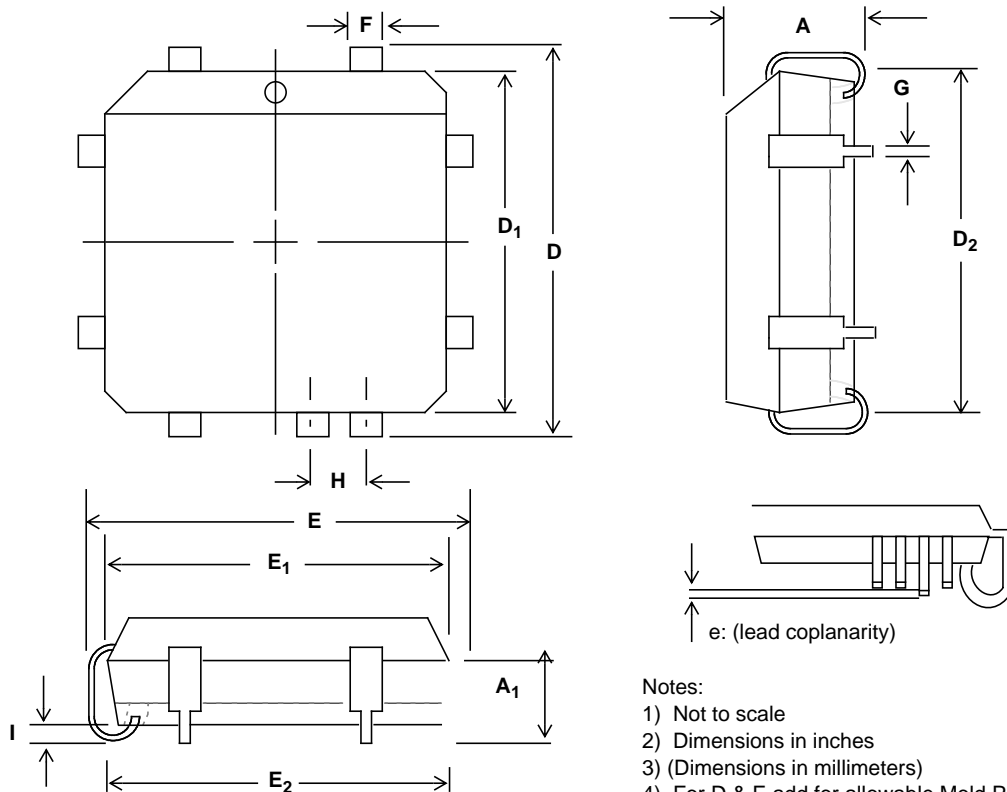
The MT9042B Multitrunk System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization signals for multitrunk T1 and E1 primary rate transmission links.

The MT9042B generates ST-BUS clock and framing signals that are phase locked to either a 2.048MHz, 1.544MHz, or 8kHz input reference.

The MT9042B is compliant with AT&T TR62411 Stratum 3, 4 and 4 Enhanced, and ETSI ETS 300 011. It will meet the jitter tolerance, jitter transfer, intrinsic jitter, frequency accuracy, holdover accuracy, capture range, phase slope and MTIE requirements for these specifications.


**Figure 1 - Functional Block Diagram**

# Package Outlines



- Notes:
- 1) Not to scale
  - 2) Dimensions in inches
  - 3) (Dimensions in millimeters)
  - 4) For D & E add for allowable Mold Protrusion 0.010"

Dim	20-Pin		28-Pin		44-Pin		68-Pin		84-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
<b>A</b>	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
<b>A<sub>1</sub></b>	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
<b>D/E</b>	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	1.185 (30.10)	1.195 (30.35)
<b>D<sub>1</sub>/E<sub>1</sub></b>	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
<b>D<sub>2</sub>/E<sub>2</sub></b>	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
<b>e</b>	0	0.004	0	0.004	0	0.004	0	0.004	0	0.004
<b>F</b>	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
<b>G</b>	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
<b>H</b>	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
<b>I</b>	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	

Plastic J-Lead Chip Carrier - P-Suffix



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