MT90225/226

16/8 Port TC PHY Device

Data Sheet

April 2003

Features

General

- Supports unframed serial streams up to 10 Mb/s per T1/E1 or DSL link
- Single chip ATM TC (Transmission Convergence) processor
- Versatile TDM Interface compatible with most popular T1, E1 or DSL framers
- Supports primary rate ISDN lines and Fractional T1/E1
- MT90225 supports up to 16 serial links & MT90226 supports up to 8 serial links
- MT90225/226 and MT90222/223/224 share the same product package and pinout configuration.

Standards Compliant

- ATM Forum - ATM over Fractional T1/E1 (AF-PHY-0130.00)
- ITU G.804 cell mapping into T1 and E1 transmission systems & ITU I.432 cell delineation

Ordering Information

MT90225AG 384 Pin PBGA
MT90226AG 384 Pin PBGA

-40 to 85°C

TC and UNI

- ATM framing using cell delineation
- HEC (header error control) verification & generation, error detection, and idle/unassigned cell filtering
- TC layer statistics and error counts i.e. HEC errors with MIB support
- Provides 8 & 16-bit UTOPIA Level 1 and 2 MPHY Interface (MT90225/226 device slaved to ATM device)
- 16 bit Microprocessor Interface, compatible with Intel and Motorola busses
- Loopback modes for diagnosis & testing
- JTAG Test Support,
- 2.5V core, 3.3V I/O with 5V tolerant inputs
- 384 pin PGBA with 1.0 mm pitch balls

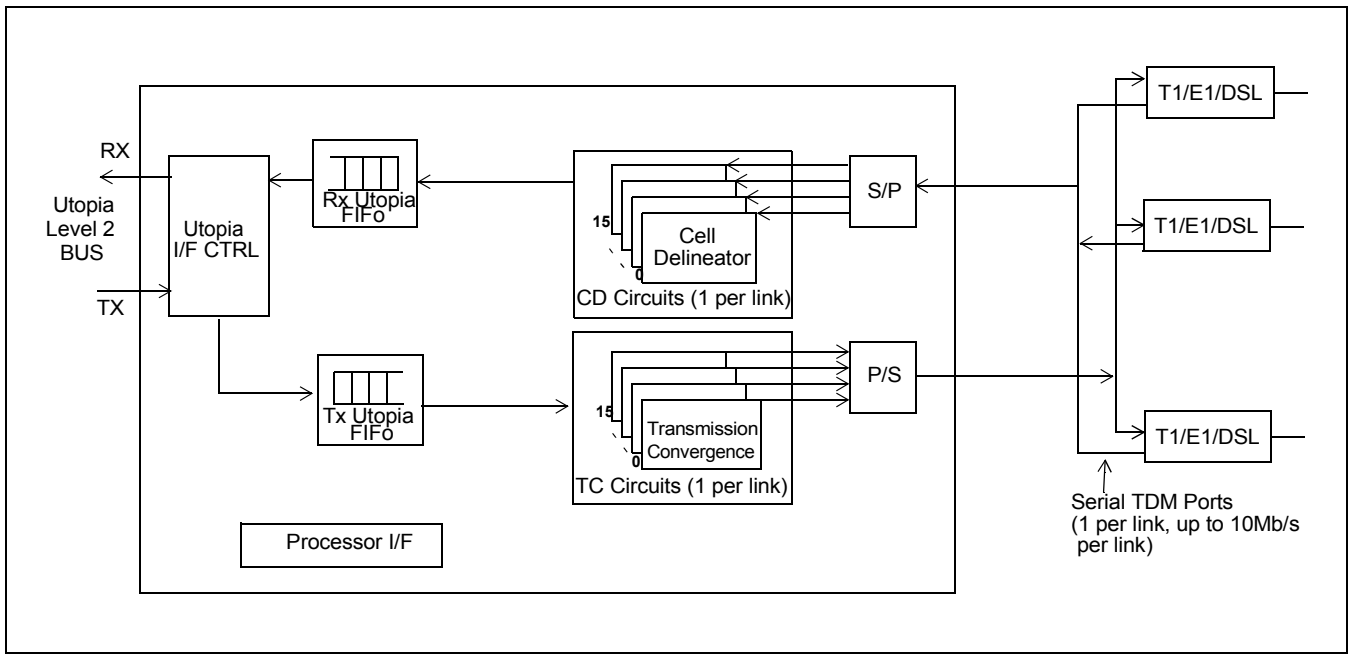

Figure 1 - MT90225/226 Functional Block Diagram

Applications

Provides cost effective solutions to implement TC (Transmission Convergence) functions over T1, E1, J1 or DSL transport facilities in broadband access networks. Typical applications are for trunking or subscriber access in:

- Integrated multi-service access platforms
- Access multiplexers
- Next-generation DLCs
- Wireless local loop
- 3G wireless base-stations

Overview

The MT90226 and MT90225 form a family of similar devices, differing only in the maximum number of serial links, and are collectively referred to as MT90225/226. It should be noted throughout this document whenever reference is made to the number of serial links that the MT90225 offers a maximum of 16 serial links (links 15:0), while the MT90226 offers a maximum of 8 serial links (links 14,12,10,8,6,4,2 and 0). Pin and register compatibility has been maintained to offer interchangeability.

Description

The MT90225/226 device is targeted to systems implementing TC or UNI (User Network Interface) specifications for T1/E1 rates or DSL rates. In the MT90225/226 architecture, up to 16/8 physical and independent serial links can be terminated through the utilization of off-the-shelf, traditional T1/E1/J1 framers/LIUs and DSL chip sets.

The MT90225/226 device provides ATM system designers with a flexible architecture when implementing ATM access over existing trunk interfaces, allowing a migration towards ATM service technology. The MT90225/226 is compliant with ATM TC/UNI specifications for T1/E1 rates. The MT90225/226 can be configured to operate in different TDM modes to facilitate the implementation of ATM over T1/E1/DSL at both CPE and Central Office sites.

The device allows for bandwidth scaleability through the use of the UTOPIA MPHY, Level 1 and Level 2 specification at rates up to 52Mhz.

Main functions that are implemented in the MT90225/226 device are:

- Utopia Level 1 or 2 PHY Interface
- Incoming HEC verification and correction (optional),
- Generation of a new HEC byte
- Format outgoing bytes into multi-vendor TDM formats
- Retrieve ATM Cells from the incoming multi-vendor TDM format
- Perform cell delineation
- Provide various counters to assist in performance monitoring
- Generation and insertion of Idle Cells; The Idle cells are pre-defined.
- Provide structured Interrupt scheme to report various events
- 16-bit microprocessor interface (adaptable to Intel or Motorola interfaces)
- loopbacks

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	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A		DSTi[4]	NC	VDD5	DSTi[2]	NC	RXSYNCi[0]	NC	NC	NC	NC	NC	NC	VDD5	NC	NC	NC	NC	VDD5	PD	NC	TMS	$\overline{\text{Reset}}$	NC	NC		A
B	NC	VSS	RXSYNCi[4]	NC	RXCKi[2]	NC	DSTi[0]	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	PD	PD	PD	TDI	$\overline{\text{TRST}}$	Test4	NC	VSS	NC	B
C	NC	NC	VSS	RXCKi[4]	NC	RXSYNCi[2]	RXCKi[0]	Latch-Clk	NC	NC	VDD5	NC	NC	NC	NC	NC	NC	PD	PD	Test3	TDO	VDD5	NC	VSS	URx-Data[0]	URx-Data[2]	C
D	RXSYNCi[6]	NC	NC	VSS	V3.3	NC	VDD5	Test2	NC	V2.5	NC	NC	V3.3	V2.5	NC	NC	V3.3	PD	PD	TCK	V3.3	VSS	VSS	URx-Data[1]	URx-Data[3]	URx-Data[4]	D
E	DSTi[6]	NC	NC	V3.3																			VSS	URx-Data[5]	VDD5	URx-Data[6]	E
F	VDD5	NC	RXCKi[6]	NC																			V3.3	URx-Data[7]	URx-Data[8]	URx-Data[9]	F
G	RXCKi[8]	DSTi[8]	NC	RXSYNCi[8]																			URx-Data[10]	URx-Data[11]	URx-Data[12]	URx-Data[13]	G
H	VDD5	NC	NC	NC																			URx-Data[14]	URx-Data[15]	URxPar	VDD5	H
J	NC	RXCKi[10]	RXSYNCi[10]	DSTi[10]																			URx-SOC	URx-Clav	NC	VDD5	J
K	RXSYNCi[12]	NC	NC	V3.3																			V2.5	URxClk	$\overline{\text{URxEnb}}$	URxA-ddr[0]	K
L	NC	RXCKi[12]	DSTi[12]	NC							VSS	VSS	VSS	VSS	VSS	VSS							URxA-ddr[2]	URxA-ddr[1]	URxA-ddr[3]	URxA-ddr[4]	L
M	DSTi[14]	RXSYNCi[14]	NC	NC							VSS	VSS	VSS	VSS	VSS	VSS							UTx-Data[0]	VDD5	UTx-Data[1]	NC	M
N	NC	VDD5	RXCKi[14]	V2.5							VSS	VSS	VSS	VSS	VSS	VSS							V3.3	UTx-Data[2]	UTx-Data[3]	UTx-Data[4]	N
P	NC	NC	NC	V3.3							VSS	VSS	VSS	VSS	VSS	VSS							V2.5	UTx-Data[6]	VDD5	UTx-Data[5]	P
R	PD	PD	NC	DSTo[14]							VSS	VSS	VSS	VSS	VSS	VSS							UTx-Data[9]	UTx-Data[10]	UTx-Data[8]	UTx-Data[7]	R
T	TXCKio[14]	TXSync-io[14]	PD	NC							VSS	VSS	VSS	VSS	VSS	VSS							UTx-Data[13]	VDD5	UTx-Data[12]	UTx-Data[11]	T
U	PD	DSTo[12]	TXCKio[12]	V2.5																			V3.3	UTxPar	UTx-Data[15]	UTx-Data[14]	U
V	VDD5	TXSync-io[12]	NC	PD																			UTxClk	$\overline{\text{UTxEnb}}$	UTx-Clav	UTx-SOC	V
W	PD	DSTo[10]	TXCKio[10]	TXSync-io[10]																			UTxA-ddr[2]	UTxA-ddr[3]	UTxA-ddr[1]	UTxA-ddr[0]	W
Y	NC	PD	PD	DSTo[8]																			UTxA-ddr[4]	REFCK[0]	VDD5	NC	Y
AA	TXCKio[8]	VDD5	TXSync-io[8]	V3.3																			REFCK[2]	REFCK[3]	NC	REFCK[1]	AA
AB	NC	PD	PD	VSS																			V3.3	VDD5	PLL-REF[1]	PLL-REF[0]	AB
AC	DSTo[6]	TXCKio[6]	NC	VSS	V3.3	PD	NC	VDD5	NC	V3.3	VSS	VSS	V2.5	V3.3	up_a[10]	up_a[7]	V2.5	$\overline{\text{up\_irq}}$	NC	up_d[10]	V3.3	VSS	VSS	NC	NC	Clk	AC
AD	TXSync-io[6]	VDD5	VSS	NC	NC	NC	TXSync-io[4]	PD	TXSync-io[2]	DSTo[0]	TXSync-io[0]	VDD5	VSS	up_oe or up_rd	VDD5	up_a[6]	up_a[3]	up_a[0]	up_d[14]	up_d[11]	up_d[8]	up_d[5]	up_d[2]	VSS	NC	Test1	AD
AE	NC	VSS	NC	NC	PD	DSTo[4]	NC	DSTo[2]	PD	NC	VSS	VSS	VSS	$\overline{\text{up\_cs}}$	up_a[11]	up_a[8]	up_a[4]	up_a[1]	up_d[15]	up_d[12]	VDD5	up_d[6]	up_d[4]	up_d[1]	VSS	NC	AE
AF		NC	NC	NC	NC	TXCKio[4]	PD	TXCKio[2]	PD	TXCKio[0]	VSS	VSS	VSS	VSS	up_r/$\overline{\text{w}}$ or $\overline{\text{up\_wr}}$	up_a[9]	up_a[5]	up_a[2]	VDD5	up_d[13]	up_d[9]	up_d[7]	NC	up_d[3]	up_d[0]		AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 2 - MT90226 Pinout (Bottom View)

Pin Diagram - MT90225

The MT90225 uses a 384 pin PBGA with a 1.0mm ball pitch.

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A		DSTi[4]	RXCKi [3]	VDD5	DSTi[2]	RXSYN Ci[1]	RXSYN Ci[0]	NC	NC	NC	NC	NC	NC	VDD5	NC	NC	NC	NC	VDD5	PD	NC	TMS	Reset	NC	NC		A
B	NC	VSS	RXSYN Ci[4]	DSTi[3]	RXCKi [2]	DSTi[1]	DSTi[0]	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	PD	PD	PD	TDI	TRST	Test4	NC	VSS	NC	B
C	DSTi[5]	NC	VSS	RXCKi [4]	RXSYN Ci[3]	RXSYN Ci[2]	RXCKi [0]	Latch Clk	NC	NC	VDD5	NC	NC	NC	NC	NC	NC	PD	PD	Test3	TDO	VDD5	NC	VSS	URx Data[0]	URx Data[2]	C
D	RXSYN Ci[6]	RXSYN Ci[5]	NC	VSS	V3.3	RXCKi [1]	VDD5	Test2	NC	V2.5	NC	NC	V3.3	V2.5	NC	NC	V3.3	PD	PD	TCK	V3.3	VSS	VSS	URx Data[1]	URx Data[3]	URx Data[4]	D
E	DSTi[6]	NC	RXCKi [5]	V3.3																			VSS	URx Data[5]	VDD5	URx Data[6]	E
F	VDD5	DSTi[7]	RXCKi [6]	RXSYN Ci[7]																			V3.3	URx Data[7]	URx Data[8]	URx Data[9]	F
G	RXCKi [8]	DSTi[8]	RXCKi [7]	RXSYN Ci[8]																			URxD ata[10]	URxD ata[11]	URxD ata[12]	URxD ata[13]	G
H	VDD5	RXCKi [9]	RXSYN Ci[9]	DSTi[9]																			URxD ata[14]	URxD ata[15]	URx Par	VDD5	H
J	RXSYN Ci[11]	RXCKi [10]	RXSYN Ci[10]	DSTi [10]																			URx SOC	URx Clav	NC	VDD5	J
K	RXSYN Ci[12]	RXCKi [11]	DSTi [11]	V3.3																			V2.5	URx-CLK	URx Enb	URxA ddr[0]	K
L	RXSYN Ci[13]	RXCKi [12]	DSTi [12]	NC							VSS	VSS	VSS	VSS	VSS	VSS							URxA ddr[2]	URxA ddr[1]	URxA ddr[3]	URxA ddr[4]	L
M	DSTi [14]	RXSYN Ci[14]	DSTi [13]	RXCKi [13]							VSS	VSS	VSS	VSS	VSS	VSS							UTx Data[0]	VDD5	UTx Data[1]	NC	M
N	RXSYN Ci[15]	VDD5	RXCKi [14]	V2.5							VSS	VSS	VSS	VSS	VSS	VSS							V3.3	UTx Data[2]	UTx Data[3]	UTx Data[4]	N
P	DSTi [15]	RXCKi [15]	DSTo [15]	V3.3							VSS	VSS	VSS	VSS	VSS	VSS							V2.5	UTx Data[6]	VDD5	UTx Data[5]	P
R	TXCKio [15]	TXSyn cio[15]	NC	DSTo [14]							VSS	VSS	VSS	VSS	VSS	VSS							UTx Data[9]	UTxD ata[10]	UTxD ata[8]	UTxD ata[7]	R
T	TXCKio [14]	TXSyn cio[14]	TXCKio [13]	DSTo [13]							VSS	VSS	VSS	VSS	VSS	VSS							UTxD ata[13]	VDD5	UTxD ata[12]	UTxD ata[11]	T
U	TXSyn cio[13]	DSTo [12]	TXCKio [12]	V2.5																			V3.3	UTxPar	UTxD ata[15]	UTxD ata[14]	U
V	VDD5	TXSyn cio[12]	DSTo [11]	TXCKio [11]																			UTxClk	UTx Enb	UTx Clav	UTx SOC	V
W	TXSyn cio[11]	DSTo [10]	TXCKio [10]	TXSyn cio[10]																			UTx Addr[2]	UTx Addr[3]	UTx Addr[1]	UTx Addr[0]	W
Y	DSTo [9]	TXCKio [9]	TXSyn cio[9]	DSTo [8]																			UTx Addr[4]	REFCK [0]	VDD5	NC	Y
AA	TXCKio [8]	VDD5	TXSyn cio[8]	V3.3																			REFCK [2]	REFCK [3]	NC	REFCK [1]	AA
AB	DSTo [7]	TXCKio [7]	TXSyn cio[7]	VSS																			V3.3	VDD5	PLL REF[1]	PLL REF[0]	AB
AC	DSTo [6]	TXCKio [6]	DSTo [5]	VSS	V3.3	TXSyn cio[5]	NC	VDD5	DSTo [1]	V3.3	VSS	VSS	V2.5	V3.3	up_a [10]	up_a[7]	V2.5	up_irq	NC	up_d [10]	V3.3	VSS	VSS	NC	NC	Clk	AC
AD	TXSyn cio[6]	VDD5	VSS	NC	NC	NC	TXSyn cio[4]	TXSyn cio[3]	TXSyn cio[2]	DSTo [0]	TXSyn cio[0]	VDD5	VSS	up_oe or up_rd	VDD5	up_a[6]	up_a[3]	up_a[0]	up_d [14]	up_d [11]	up_d[8]	up_d[5]	up_d[2]	VSS	NC	Test1	AD
AE	NC	VSS	NC	NC	TXCKio [5]	DSTo [4]	DSTo [3]	DSTo [2]	TXCKio [1]	NC	VSS	VSS	VSS	up_cs	up_a [11]	up_a[8]	up_a[4]	up_a[1]	up_d [15]	up_d [12]	VDD5	up_d[6]	up_d[4]	up_d[1]	VSS	NC	AE
AF		NC	NC	NC	NC	TXCKio [4]	TXCKio [3]	TXCKio [2]	TXSyn cio[1]	TXCKio [0]	VSS	VSS	VSS	VSS	up_r/w or up_wr	up_a[9]	up_a[5]	up_a[2]	VDD5	up_d [13]	up_d[9]	up_d[7]	NC	up_d[3]	up_d[0]		AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 3 - MT90225 Pinout (Bottom View)

MT90226 Pin Description

Pin #	Name	I/O	Description
ATM Input Port Signals (UTOPIA Transmit Interface)			
U2,U1,T4,T2, T1,R3,R4,R2, R1,P3,P1,N1, N2,N3,M2,M4	UTxData [15:0]	I	**UTOPIA Transmit Data Bus.** 16 (or 8) bit wide data driven from ATM LAYER device to MT90226. Bit 15 (or 7) is the MSB. All arriving data between the last word (byte) of the previous cell and the first word (byte) of the following cell (indicated by the SOC signal) is ignored. UTxData[15:8] have internal weak pull-downs.
U3	UTxPar	I	**UTOPIA Transmit Parity.** Odd (or Even) Parity bit generated by the ATM LAYER. The parity bit is sampled on the rising edge of UTxClk. UTxPar has an internal weak pull-down.
V1	UTxSOC	I	**UTOPIA Transmit Start of Cell Signal.** Active HIGH signal asserted by the ATM LAYER device when TxData[15:0] ([7:0]) contains the first valid word (byte) of the cell. After this signal is high, the following 26 word (52 bytes) should contain valid data. The MT90226 waits for another TxSOC and $\overline{\text{TxEnb}}$ signal after reading a complete cell.
V4	UTxClk	I	**UTOPIA Transmit Clock.** Transfer clock from the ATM Layer device to the MT90226 which synchronizes data transfers on TxData[15:0] ([7:0]). This signal is the clock of the incoming data. Data is sampled on the rising edge of this signal.
V3	$\overline{\text{UTxEnb}}$	I	**UTOPIA Transmit Data Enable.** Active LOW signal asserted by the ATM LAYER device during cycles when TxData contains valid cell data.
V2	UTxClav	O	**UTOPIA Transmit Cell Available Signal.** For cell-level flow control in a MPHY environment, TxClav is an active high tri-stateable signal from the MT90226 to the ATM LAYER device.
Y4,W3,W4, W2,W1	UTxAddr [4:0]	I	**Transmit Address**.Five bit wide address bus driven by the ATM layer device to poll and select the appropriate PHY address. TxAddr[4] is the MSB.
ATM Output Port Signals (UTOPIA Receive Interface)			
H3,H4,G1,G2, G3,G4,F1,F2, F3,E1,E3,D1, D2,C1,D3,C2	URxData [15:0]	O	**UTOPIA Receive Data Bus.** 16 (or 8) bit wide data driven from MT90226 to ATM layer device. RxData[15] ([7]) is the MSB. To support multiple PHY configurations, RxData is driven only when RxEnb and port is selected. It is tri-stated otherwise.
H2	URxPar	O	**UTOPIA Receive Parity.** Odd (or Even) Parity bit generated by the MT90226 to the ATM Layer.
J4	URxSOC	O	**UTOPIA Receive Start of Cell Signal.** Active high asserted by the MT90226 when RxData contains the first valid word (byte) of a cell.
K3	URxClk	I	**UTOPIA Receive Clock**. This signal is the clock driven from the ATM layer to the PHY layer. Data changes after the rising edge of this signal.
K2	$\overline{\text{URxEnb}}$	I	**UTOPIA Receive Data Enable.** Active LOW signal asserted by the ATM layer device to indicate that URxData[15:0] ([7:0]) and URxSOC will be sampled at the end of the next cycle. In multiple PHY configurations, $\overline{\text{URxEnb}}$ is used to tri-state URxData and URxSOC MT90226 outputs. In this case, URxData and URxSOC would be enabled only in cycles following those with $\overline{\text{URxEnb}}$ asserted. In UTOPIA L1, $\overline{\text{URxEnb}}$ must not be tied low and must transition from high (disabled) to low (enabled) to indicate the beginning of data transfer.

MT90226 Pin Description (continued)

Pin #	Name	I/O	Description
J3	URxClav	O	**UTOPIA Receive Cell Available Signal.** For cell-level flow control in a MPHY environment, URxClav is an active high tri-stateable signal from the MT90226 to ATM LAYER device.
L1, L2, L4, L3, K1	URxAddr [4:0]	I	**Receive Address**. Five bit wide address bus driven from the ATM to PHY device to select the appropriate PHY address. URxAddr[4] is the MSB.
Processor Interface Signals			
AE8,AD8,AF7, AE7,AD7,AC7, AF6,AD6,AF5, AE5,AD5,AE4, AF3,AD4,AE3, AF2	up_d [15:0]	I/O	**Processor Data Bus**. Data Bus to exchange data between the MT90226 and a local processor.
AE12,AC12, AF11,AE11, AC11,AD11, AF10,AE10, AD10,AF9, AE9,AD9	up_a [11:0]	I	**Processor Address Bus**. Used to select the internal registers and memory locations of the MT90226.
AF12	up_r/$\overline{w}$ or $\overline{up\_wr}$	I	**Processor Read/Not Write (Motorola Mode).** This is an input signal. If low, data is written from the processor to the MT90226. If high, data is read from the MT90226 to the processor. **Processor Not Write (Intel Mode).** This is an input signal, active low. If low, data is written from the processor to the MT90226.
AD13	up_oe or $\overline{up\_rd}$	I	**Output enable (Motorola Mode).** This is an input signal. This signal should be tied to GND for Motorola timing mode. **Processor Read (Intel Mode).** This is an input signal, active low. If low, data is read from the MT90226.
AE13	$\overline{up\_cs}$	I	**Chip Select**. This is an active low input signal. If this signal is high, the MT90226 ignores all other signals on its processor bus. If this signal is low, the MT90226 accepts the signals on its processor bus.
AC9	$\overline{up\_irq}$	O	**Processor Interrupt Request**. Open drain signal. If this signal is low, the MT90226 signals to the processor that an interrupt condition is pending inside the MT90226.
TDM Interface Signals			
R23 U25 W25 Y23 AC26 AE21 AE19 AD17	DSTo [14] [12] [10] [8] [6] [4] [2] [0]	O	**Serial TDM Data Output**. Serial stream which contains transmit data. The output is set to high impedance for unused time slots and if the link is not used. It is aligned with TXCKio and TxSYNCio.

MT90226 Pin Description (continued)

Pin #	Name	I/O	Description
M26 L24 J23 G25 E26 A25 A22 B20	DSTi [14] [12] [10] [8] [6] [4] [2] [0]	I	**Serial TDM Data Input**. Serial stream which contains receive data. It is aligned with RXCKi and RxSYNCi. These pins have internal weak pull-downs.
T26 U24 W24 AA26 AC25 AF21 AF19 AF17	TXCKio [14] [12] [10] [8] [6] [4] [2] [0]	I/O	**TDM Interface Transmit Clock.** This pin is an input or an output as selected by the **TDM TX Link Control** registers. The TXCK source is software selectable and can be either one of the eight RXCK or one of the four REFCK signals when defined as output. When defined as input, the proper clock signal is provided to the input pin. The clock polarity is determined by the **TDM TX Link Control** registers. These pins have internal weak pull-downs.
T25, V25, W23, AA24, AD26, AD20, AD18, AD16	TXSYNCio [14] [12] [10] [8] [6] [4] [2] [0]	I/O	**Transmit Line Frame Pulse**. This pin is an input or an output as selected by the **TDM TX Link Control** registers. It is the frame reference (typically 8 kHz) used as transmit synchronization for the TDM system interface. When an output, the TXSYNC is generated from the TXCK signal and is independent from other TXSYNC signals. Two major modes are available: generic and ST-Bus: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTo lines. 2. For generic TDM Interfaces, it can be programmed to generate or receive either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
M25 K26 J24 G23 D26 B24 C21 A20	RXSYNCi [14] [12] [10] [8] [6] [4] [2] [0]	I	**Receive line Frame Pulse**. It is the frame reference (typically 8 kHz) used as receive synchronization for the TDM system interface. Two major modes are available: generic and ST-Bus: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTi lines. 2. For generic TDM Interfaces, it can be programmed to accept either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
N24 L25 J25 G26 F24 C23 B22 C20	RXCKi [14] [12] [10] [8] [6] [4] [2] [0]	I	**TDM Interface Receive Clock.** This input line represents the clock for the receive serial TDM data. The expected frequency value to be received at this input clock is defined by the user through the **RX Link TDM Control** register. These pins have internal weak pull-downs.
AB2, AB1	PLLREF [1:0]	O	**Output reference to an external PLL**.

MT90226 Pin Description (continued)

Pin #	Name	I/O	Description
AA3,AA4, AA1,Y3	REFCK [3:0]	I	**Input Reference Clock** inputs 3 to 0. Receive the de-jittered transmit clock reference to be internally routed to the TXCKio transmit clocks. These pins have internal weak pull-downs.
			System Signals
AC1	Clk	I	**System Clock (50 MHz nominal)**. In the MT90226, this clock is used for all internal operations of the device.
C19	LatchClk	I	**Counter Latch Clock.** The clock present at this input can be divided internally to produce the latch signal for the internal counters. Refer to the **Counter Transfer Command** register for more details. This pin has an internal pull-down.
A4	$\overline{\text{Reset}}$	I	**System Reset.** This is an active low input signal. It causes the device to enter the initial state. The Clk signal must be active to reset the internal registers.
D7	TCK	I	**JTAG Test Clock.** TCK should be pulled down if not used.
A5	TMS	I	**JTAG Test Mode Select**. TMS is sampled on the rising edge of TCK.
B6	TDI	I	**JTAG Test Data Input**. This pin has an internal weak pull-down.
C6	TDO	O	**JTAG Test Data Output**. **Note:** TDO is tristated by $\overline{\text{TRST}}$ pin.
B5	$\overline{\text{TRST}}$	I	**JTAG Test Reset** (active low). Should be asserted LOW on power-up and during reset. Must be HIGH for JTAG boundary-scan operation. This pin has an internal weak pull-down.
AD1	Test1	I	**Test1.** Must be tied Low
D19	Test2	O	**Test2**. Must be left not connected (NC).
C7	Test3	I	**Test3**. Must be pulled up to V3.3 for normal operation. **NOT 5V TOLERANT.**
B4	Test4	O	**Test4**. Must be left not connected (NC)
			Power Signals
E2,H1,J1,M3, P2,T3,Y2,AB3, AE6,AF8, AD12,AD15, AC19,AD25, AA25,V26, N25,H26,F26, A23,D20,C16, A13,A8,C5	VDD5	S	**5 Volt supply pin**. Connect to a 5 volt supply when interfacing to 5 volt signals, otherwise, connect to a 3.3 Volt supply.
AA23,AB04, AC06,AC13, AC17,AC22, D6,D10,D14, D22,E23,F4, K23,N4,P23, U4	V3.3	S	**3.3 Volt supply pin for I/O pins.** Connect to a 3.3 Volt supply.
D13,D17,N23, U23,AC10, AC14,K4,P4	V2.5	S	**2.5 Volt supply for core.** Connect to a 2.5 Volt power supply.

MT90226 Pin Description (continued)

Pin #	Name	I/O	Description
AB23,AC4, AC5,AC23, AD3,AD24, AE2,AE25,B2, B25,C3,C24, D4,D5,D23,E4, L11,L12,L13, L14,L15,L16, M11,M12,M13, M14,M15,M16, N11,N12,N13, N14,N15,N16, P11,P12,P13,P 14,P15,P16, R11,R12,R13, R14,R15,R16, T11,T12,T13, T14,T15,T16	VSS	S	**Ground.**
AC16,AE16, AF16,AC15, AE15,AF15, AD14,AE14 AF13, AF14	IC	I	**Internal Connection.** Must be grounded externally.

MT90226 Pin Description (continued)

Pin #	Name	I/O	Description
B1,J2,M1,Y1, AA2,AC2,AD2, AE1,AC3,AF4, AC8,AE17, AC20,AD21, AF22,AF23, AD22,AE23, AF24,AE24, AF25,AD23, AE26,R24, L23,E25,C25, B26,D24,C15, A6,A3,C4, B3,A2 P24, T23, V24,Y26, AB26, AC24, AE20,AC18 P26, M24, K24, H23, F25, C26, B23, B21 N26, L26, J26, H24, F23, D25, C22, A21, P25, M23, K25, H25, G24, E24, A24, D21 A9,C10,B10, A10,C11,D11,B 11,A11,C12,D1 2,B12,A12,C13 ,B13,A14,B14, C14,A15,B15 D15,A16,B16 B17,C17,A18, B18,D18,C18, A19,B19 D16, A17	NC	I	**Not Connected.**
R26, T24, V23, Y25, AB25, AE22, AF20, AE18, R25, U26, W26, Y24, AB24, AC21, AD19, AF18 B7,A7,D8,C8, B8,D9,C9,B9	PD	I	**Pull-down.** Connect to VSS via a high value resistor e.g. 10kohm. Don't tie to VSS directly.

MT90225 Pin Description

Pin #	Name	I/O	Description
ATM Input Port Signals (UTOPIA Transmit Interface)			
U2,U1,T4,T2, T1,R3,R4,R2, R1,P3,P1,N1, N2,N3,M2,M4	UTxData [15:0]	I	**UTOPIA Transmit Data Bus.** 16 (or 8) bit wide data driven from ATM LAYER device to MT90225. Bit 15 (or 7) is the MSB. All arriving data between the last word (byte) of the previous cell and the first word (byte) of the following cell (indicated by the SOC signal) is ignored. UTxData[15:8] have internal weak pull-downs.
U3	UTxPar	I	**UTOPIA Transmit Parity.** Odd (or Even) Parity bit generated by the ATM LAYER. The parity bit is sampled on the rising edge of UTxClk. UTxPar has an internal weak pull-down.
V1	UTxSOC	I	**UTOPIA Transmit Start of Cell Signal.** Active HIGH signal asserted by the ATM LAYER device when TxData[15:0] ([7:0]) contains the first valid word (byte) of the cell. After this signal is high, the following 26 word (52 bytes) should contain valid data. The MT90225 waits for another TxSOC and $\overline{\text{TxEnb}}$ signal after reading a complete cell.
V4	UTxClk	I	**UTOPIA Transmit Clock.** Transfer clock from the ATM Layer device to the MT90225 which synchronizes data transfers on TxData[15:0] ([7:0]). This signal is the clock of the incoming data. Data is sampled on the rising edge of this signal.
V3	$\overline{\text{UTxEnb}}$	I	**UTOPIA Transmit Data Enable.** Active LOW signal asserted by the ATM LAYER device during cycles when TxData contains valid cell data.
V2	UTxClav	O	**UTOPIA Transmit Cell Available Signal.** For cell-level flow control in a MPHY environment, TxClav is an active high tri-stateable signal from the MT90225 to the ATM LAYER device.
Y4,W3,W4, W2,W1	UTxAddr [4:0]	I	**Transmit Address**.Five bit wide address bus driven by the ATM layer device to poll and select the appropriate PHY address. TxAddr[4] is the MSB.
ATM Output Port Signals (UTOPIA Receive Interface)			
H3,H4,G1,G2, G3,G4,F1,F2, F3,E1,E3,D1, D2,C1,D3,C2	URxData [15:0]	O	**UTOPIA Receive Data Bus.** 16 (or 8) bit wide data driven from MT90225 to ATM layer device. RxData[15] ([7]) is the MSB. To support multiple PHY configurations, RxData is driven only when RxEnb and port is selected. It is tri-stated otherwise.
H2	URxPar	O	**UTOPIA Receive Parity.** Odd (or Even) Parity bit generated by the MT90225 to the ATM Layer.
J4	URxSOC	O	**UTOPIA Receive Start of Cell Signal.** Active high asserted by the MT90225 when RxData contains the first valid word (byte) of a cell.
K3	URxClk	I	**UTOPIA Receive Clock**. This signal is the clock driven from the ATM layer to the PHY layer. Data changes after the rising edge of this signal.
K2	$\overline{\text{URxEnb}}$	I	**UTOPIA Receive Data Enable.** Active LOW signal asserted by the ATM layer device to indicate that URxData[15:0] ([7:0]) and URxSOC will be sampled at the end of the next cycle. In multiple PHY configurations, $\overline{\text{URxEnb}}$ is used to tri-state URxData and URxSOC MT90225 outputs. In this case, URxData and URxSOC would be enabled only in cycles following those with $\overline{\text{URxEnb}}$ asserted. In UTOPIA L1, $\overline{\text{URxEnb}}$ must not be tied low and must transition from high (disabled) to low (enabled) to indicate the beginning of data transfer.

MT90225 Pin Description (continued)

Pin #	Name	I/O	Description
J3	URxClav	O	**UTOPIA Receive Cell Available Signal.** For cell-level flow control in a MPHY environment, URxClav is an active high tri-stateable signal from the MT90225 to ATM LAYER device.
L1, L2, L4, L3, K1	URxAddr [4:0]	I	**Receive Address**. Five bit wide address bus driven from the ATM to PHY device to select the appropriate PHY address. URxAddr[4] is the MSB.
Processor Interface Signals			
AE8,AD8,AF7, AE7,AD7,AC7, AF6,AD6, AF5,AE5,AD5, AE4,AF3,AD4, AE3,AF2	up_d [15:0]	I/O	**Processor Data Bus**. Data Bus to exchange data between the MT90225 and a local processor.
AE12,AC12, AF11,AE11, AC11,AD11, AF10,AE10, AD10,AF9, AE9,AD9	up_a [11:0]	I	**Processor Address Bus**. Used to select the internal registers and memory locations of the MT90225.
AF12	up_r/$\overline{w}$ or $\overline{up\_wr}$	I	**Processor Read/Not Write. Motorola Mode.** This is an input signal. If low, data is written from the processor to the MT90225. If high, data is read from the MT90225 to the processor. **Processor Not Write (Intel Mode).** This is an input signal, active low. If low, data is written from the processor to the MT90225.
AD13	up_oe or $\overline{up\_rd}$	I	**Output enable (Motorola Mode).** This is an input signal. This signal should be tied to GND for Motorola timing mode. **Processor Read (Intel Mode).** This is an input signal, active low. If low, data is read from the MT90225.
AE13	$\overline{up\_cs}$	I	**Chip Select**. This is an active low input signal. If this signal is high, the MT90225 ignores all other signals on its processor bus. If this signal is low, the MT90225 accepts the signals on its processor bus.
AC9	$\overline{up\_irq}$	O	**Processor Interrupt Request**. Open drain signal. If this signal is low, the MT90225 signals to the processor that an interrupt condition is pending inside the MT90225.
TDM Interface Signals			
P24,R23,T23, U25,V24,W25, Y26,Y23, AB26,AC26, AC24,AE21, AE20,AE19, AC18,AD17	DSTo [15:0]	O	**Serial TDM Data Output 15-0**. Serial stream which contains transmit data. The output is set to high impedance for unused time slots and if the link is not used. It is aligned with TXCKio and TXSYNCio.

MT90225 Pin Description (continued)

Pin #	Name	I/O	Description
P26,M26,M24, L24,K24,J23, H23,G25,F25, E26,C26,A25, B23,A22,B21, B20	DSTi [15:0]	I	**Serial TDM Data Input 15-0**. Serial stream which contains receive data. It is aligned with RXCKi and RXSYNCi. These pins have internal weak pull-downs.
R26,T26,T24, U24,V23,W24, Y25,AA26, AB25,AC25, AE22,AF21, AF20,AF19, AE18,AF17	TXCKio [15:0]	I/O	**TDM Interface Transmit Clock 15-0.** This pin is an input or an output as selected by the **TDM TX Link Control** registers. The TXCK source is software selectable and can be either one of the sixteen RXCK or one of the four REFCK signals when defined as output. When defined as input, the proper clock signal is provided to the input pin. The clock polarity is determined by the **TDM TX Link Control** registers. These pins have internal weak pull-downs.
R25,T25,U26, V25,W26,W23, Y24,AA24, AB24,AD26, AC21,AD20, AD19,AD18, AF18,AD16	TXSYNCio [15:0]	I/O	**Transmit Line Frame Pulse 15-0**. This pin is an input or an output as selected by the **TDM TX Link Control** registers. It is the frame reference (typically 8 kHz) used as transmit synchronization for the TDM system interface. When an output, the TXSYNC is generated from the TXCK signal and is independent from other TXSYNC signals. Two major modes are available: generic and ST-BUS: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTo lines. 2. For generic TDM Interfaces, it can be programmed to generate or receive either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
N26,M25,L26, K26,J26,J24, H24,G23,F23, D26,D25,B24, C22,C21,A21, A20	RXSYNCi [15:0]	I	**Receive line Frame Pulse 15-0**. It is the frame reference (typically 8 kHz) used as receive synchronization for the TDM system interface. Two major modes are available: generic and ST-BUS: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32/64/128 channel frame of the ST-BUS interface at DSTi lines. 2. For generic TDM Interfaces, it can be programmed to accept either a positive or negative pulse polarity that marks the first bit of the TDM system interface. These pins have internal weak pull-downs.
P25,N24,M23, L25,K25,J25, H25,G26,G24, F24,E24,C23, A24,B22,D21, C20	RXCKi [15:0]	I	**TDM Interface Receive Clock 15-0.** This input line represents the clock for the receive serial TDM data. The expected frequency value to be received at this input clock is defined by the user through the **RX Link TDM Control** register. These pins have internal weak pull-downs.
AB2,AB1	PLLREF [1:0]	O	**Output reference to an external PLL**.
AA3,AA4, AA1,Y3	REFCK [3:0]	I	**Input Reference Clock** inputs 3 to 0. Receive the de-jittered transmit clock reference to be internally routed to the TXCKio transmit clocks. These pins have internal weak pull-downs.
System Signals			
AC1	Clk	I	**System Clock (50 MHz nominal)**. In the MT90225, this clock is used for all internal operations of the device.

MT90225 Pin Description (continued)

Pin #	Name	I/O	Description
C19	LatchClk	I	**Counter Latch Clock.** The clock present at this input can be divided internally to produce the latch signal for the internal counters. Refer to the **Counter Transfer Command** register for more details. This pin has an internal pull-down.
A4	$\overline{\text{Reset}}$	I	**System Reset.** This is an active low input signal. It causes the device to enter the initial state. The Clk signal must be active to reset the internal registers.
D7	TCK	I	**JTAG Test Clock.** TCK should be pulled down if not used.
A5	TMS	I	**JTAG Test Mode Select**. TMS is sampled on the rising edge of TCK.
B6	TDI	I	**JTAG Test Data Input**. This pin has an internal weak pull-down.
C6	TDO	O	**JTAG Test Data Output**. **Note:** TDO is tristated by $\overline{\text{TRST}}$ pin.
B5	$\overline{\text{TRST}}$	I	**JTAG Test Reset** (active low). Should be asserted LOW on power-up and during reset. Must be HIGH for JTAG boundary-scan operation. This pin has an internal weak pull-down.
AD1	Test1	I	**Test1.** Must be tied Low
D19	Test2	O	**Test2**. Must be left not connected (NC).
C7	Test3	I	**Test3**. Must be pulled up to V3.3 for normal operation. **NOT 5V TOLERANT.**
B4	Test4	O	**Test4**. Must be left not connected (NC)
Power Signals			
E2,H1,J1,M3, P2,T3,Y2,AB3, AE6,AF8, AD12,AD15, AC19,AD25, AA25,V26, N25,H26,F26, A23,D20,C16, A13,A8,C5	VDD5	S	**5 Volt supply pin**. Connect to a 5 volt supply when interfacing to 5 volt signals, otherwise, connect to a 3.3 Volt supply.
AA23,AB04, AC06,AC13, AC17,AC22, D6,D10,D14, D22,E23,F4, K23,N4,P23, U4	V3.3	S	**3.3 Volt supply pin for I/O pins.** Connect to a 3.3 Volt supply.
D13,D17,N23, U23,AC10, AC14,K4,P4	V2.5	S	**2.5 Volt supply for core.** Connect to a 2.5 Volt power supply.

MT90225 Pin Description (continued)

Pin #	Name	I/O	Description
AB23,AC4, AC5,AC23, AD3,AD24, AE2,AE25,B2, B25,C3,C24, D4,D5,D23,E4, L11,L12,L13, L14,L15,L16, M11,M12,M13, M14,M15,M16, N11,N12,N13, N14,N15,N16, P11,P12,P13, P14,P15,P16, R11,R12,R13, R14,R15,R16, T11,T12,T13, T14,T15,T16	VSS	S	**Ground.**
AC16,AE16, AF16,AC15, AE15,AF15, AD14,AE14 AF13, AF14	IC	I	**Internal Connection.** Must be grounded externally.
B1,J2,M1,Y1, AA2,AC2,AD2, AE1,AC3,AF4, AC8,AE17, AC20,AD21, AF22,AF23, AD22,AE23, AF24,AE24, AF25,AD23, AE26,R24, L23,E25,C25, B26,D24,C15, A6,A3,C4, B3,A2 A9,C10,B10, A10,C11,D11, B11,A11,C12, D12,B12,A12, C13,B13,A14, B14,C14,A15, B15 D15, A16, B16 B17,C17,A18, B18,D18,C18, A19,B19 D16, A17	NC	I	**Not Connected.**
B7,A7,D8,C8, B8,D9,C9,B9	PD		**Pull-down.** Connect to VSS via a high value resistor e.g. 10kohm. Don't tie to VSS directly.

1.0 Device Architecture

The MT90225/226 implements Transmission Convergence layer functions.

The primary function of MT90225/6 is to transfer the cells from the UTOPIA Interface to a serial (TDM) port and from TDM ports to UTOPIA interface without any overhead. Up to 16 UTOPIA PHY addresses can be supported - one per serial port. A different UTOPIA PHY address is assigned to each one of the links.

1.1 MT90225/6 Main Functions

The MT90225/226 circuitry implements the following functions:

- Utopia Level 1 or 2 PHY Interface
- Incoming HEC verification and correction (optional),
- Generation of a new HEC byte
- Format outgoing bytes into multi-vendor TDM formats
- Retrieve ATM Cells from the incoming multi-vendor TDM format
- Perform cell delineation
- Provide various counters to assist in performance monitoring
- Generation and insertion of Idle Cells; The Idle cells are pre-defined.
- Provide structured Interrupt scheme to report various events
- 16-bit microprocessor interface (adaptable to Intel or Motorola interfaces)
- loopbacks

The MT90225/226 can be separated into four major independent blocks and three support blocks.The four major independent blocks are:

- the ATM Transmit Path
- the ATM Receive Path
- the TDM Interface
- the UTOPIA Interface

The three support blocks are:

- the Counter Block
- the Interrupt Block
- the Microprocessor Interface Block

2.0 The ATM Transmit Path

The transmit path corresponds to a cell flow from the ATM Layer towards the PHY Layer. The ATM cell path on the transmit side starts at the UTOPIA L2 or L1 Interface. Once ATM cells are received at the UTOPIA port, the device transfers these cells to the transmit block.

The MT90225/226 provides ATM cell mapping and transmission convergence blocks to transport ATM cells over a maximum of sixteen flexible serial interface ports. These serial interface ports communicate with most off-the-shelf T1/E1/J1 framers, SHDSL modems or other low speed link devices.

Each of these serial links can be assigned to a TC link. The MT90225 supports up to 16 serial links, while the MT90226 supports up to 8 serial links.

The functional block diagram at Figure 4 illustrates the transmit function of the MT90225.

2.1 Cell In Control

In general terms, the MT90225/226 transmit input port has the following properties:

- cell level handshaking complies with the ATM Forum UTOPIA L1 and L2 Specification
- behaves like a UTOPIA MPHY Device or Single PHY Device
- each port can be enabled or disabled independently
- parity (odd or even) can be checked
- optionally verifies and then generates the HEC for incoming cells
- includes the ATM Forum polynomial when generating the HEC (default option that can be disabled)
- either passes or removes incoming Idle cells
- either passes or removes incoming Unassigned cells
- provides a counter per UTOPIA port for the total number of Idle/Unassigned/Filler cells with a valid HEC or optionally the total number of User cells (24 bits/16 bit latched)
- provides a counter per UTOPIA port for the total number of cells with wrong incoming HEC (24 bits/16 bit latched)
- provides a counter per UTOPIA port for the total number of cells handled (24 bits/16 bit latched)
- provides counters for Parity errors

The input port can be enabled to remove (filter) Unassigned or Idle cells. If Unassigned or Idle Cell Filtering is enabled, the device checks for and discards Unassigned or Idle cells. This function is programmed in the **UTOPIA Input Control (0x0052)** register.

Section 5.0 describes the UTOPIA Interface in more detail.

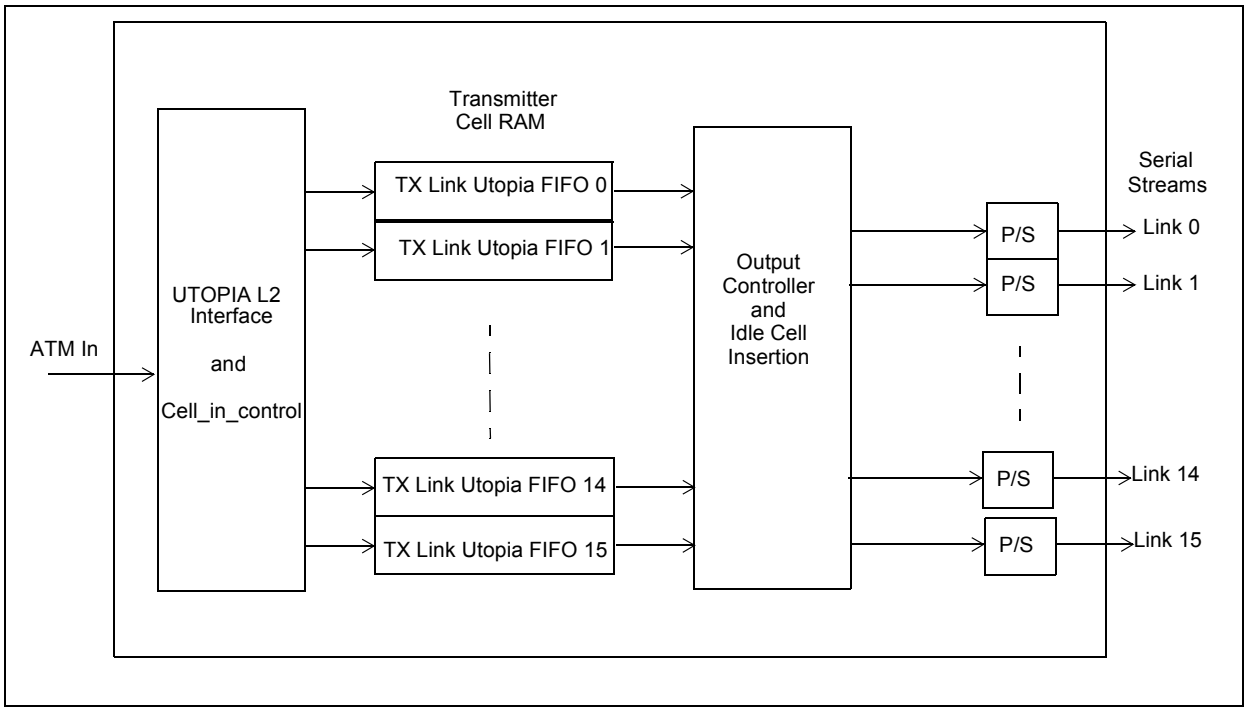


Figure 4 - MT90225/226 Functional Block Diagram -Transmitter

2.2 The ATM Transmission Convergence

The Transmit Convergence (TC) function integrates the circuitry to support ATM cell payload scrambling, HEC generation and the generation of Idle cells for use with the T1/E1/J1 or DSL trunks. Each of the available ATM TC circuits can use the polynomial $X^{43} + 1$ to scramble the ATM cell payload field. The MT90225/226 ATM cell payload scrambling function can be disabled.

The ITU I.432 polynomial $X^8 + X^2 + X + 1$ is used to generate the HEC field of the ATM cell. By default, the ATM Forum polynomial $X^6 + X^4 + X^2 + 1$ is added to the calculated HEC octet. The addition of the ATM Forum polynomial can be disabled. The resulting calculation is then written on the HEC field and the ATM cell is ready for transmission over the flexible TDM Interface.

In cases where the TC block requests a cell to be transferred to any of the serial interfaces and the TX Link UTOPIA FIFO has no cell ready for transmission, then the TC block will automatically send an IDLE cell to the line. The default values for the Idle cells comply with the ATM Forum Specification and are pre-loaded in the MT90225/226 following a reset. The **TX Cell RAM Control (0x0080)** register can be used to re-initialize the TX Cell RAM. The content of the Idle cell is pre-initialized with the header bytes set at 0x00, 0x00, 0x00 and 0x01. The payload bytes are set to 0x6A.

Idle Cells are transmitted on the TC serial Interface until the bit corresponding to the link in the **UTOPIA Input Link PHY Enable (0x0050)** register is set. Then, the ATM User cells are transferred from the Input UTOPIA port to the TX serial port.

2.2.1 TX Cell RAM and TX Link FIFO Length

The internal TX Cell RAM can hold up to 119 cells. A one cell space for predefined Idle Cell is reserved for MT90225/226 operation.

The remaining 118 cells can be assigned to any of the 16/8 TX Link UTOPIA FIFOs. The MT90225/226 implements one TX Link UTOPIA FIFO for each link. Each TX Link UTOPIA FIFO is associated with one TX UTOPIA PHY Address. Please refer to section 5.0 "UTOPIA Interface Operation" for more details.

ATM cells received from the ATM port are placed in a TX LINK UTOPIA FIFO, waiting to be transmitted. If the Idle/Unassigned cell removal option is selected, these cells are dropped. If the TX LINK UTOPIA FIFO is empty, an Idle cell is sent to the output link.

TX Link FIFO Length Definition Register (0x008B - 0x0092) are used to set the size of the TX Link UTOPIA FIFO. A maximum of 15 cells can be assigned to any single FIFO. The size of unused TX Link UTOPIA FIFOs should be set to zero.

2.3 Parallel to Serial TDM Interface

ATM cell octet byte alignment conforms to ITU G.804 recommendations for T1 or E1 framer parallel to serial format conversion.

The **TDM TX Link Control Register (0x0600-0x060F)** and **TDM RX Link Control Register (0x0700-0x070F)** registers are used to select the serial mode of operation. Additionally, the serial links can operate at rates up to 2.5Mb/s individually, or up to 5.0Mb/s when paired or 10Mb/s when grouped in fours. Refer to Description of the TDM interface in Section 4.0 for more details.

3.0 The ATM Receive Path

The receive path corresponds to the cell flow from the PHY (serial TDM) interfaces to the ATM UTOPIA Interface. The MT90225/226 provides cell delineation and optional cell filtering to discard Unassigned or Idle cells on each link.

Up to sixteen/eight incoming serial (typically TDM) lines can be connected to the MT90225/226 receiver and forwarded to the UTOPIA L2 interface served by an external ATM-Layer device. Figure 5 illustrates four of the sixteen possible UTOPIA ports that can be addressed through the UTOPIA Interface.

The size of the RX UTOPIA FIFO is fixed at 4 cells. The Idle cells are automatically removed at the RX TDM block and all other valid received cells are transferred to the RX UTOPIA FIFO.

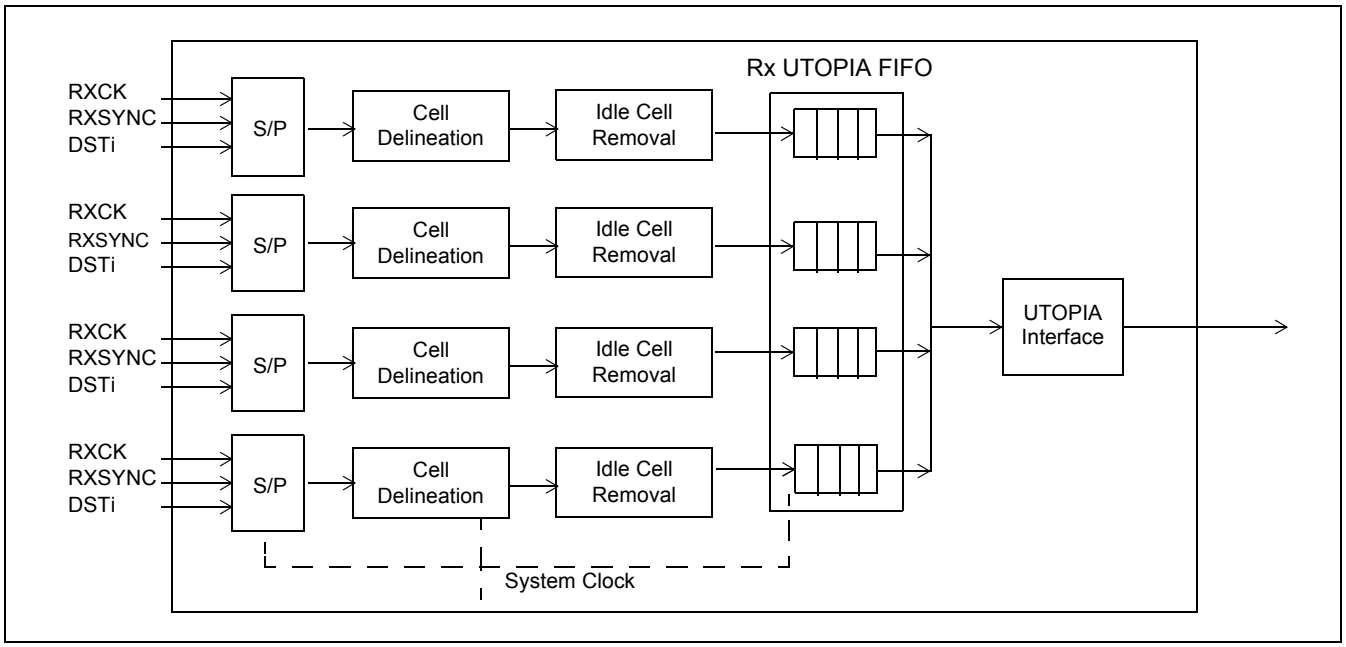


Figure 5 - Example of TC Mode Operation (Using Four of Sixteen Possible UTOPIA-Output Ports)

3.1 Cell Delineation Function

This block provides the circuitry necessary to perform functions such as Cell Delineation (CD), cell payload de-scrambling, HEC verification and filtering of Idle cells. The CD circuit delineates ATM cells received from the payload of the T1, E1, J1 or DSL frame through the flexible TDM Interface.

When performing delineation, valid HEC calculations are interpreted to indicate cell boundaries. The CD circuit performs a sequential hunt for a correct HEC sequence. While performing this hunt, the cell delineation state machine is in the HUNT state. Figure 6 depicts a state diagram of the cell delineation operation.

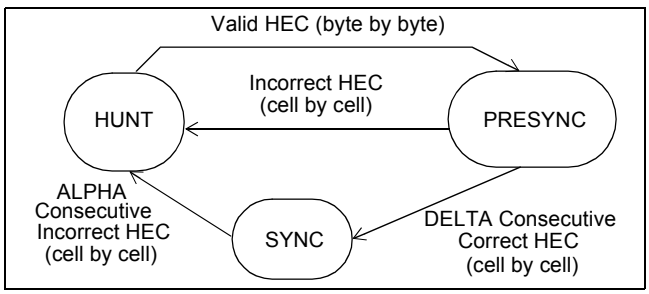


Figure 6 - Cell Delineation State Diagram

When a valid HEC is found, the CD circuit locks on the cell boundary and enters the PRESYNC state. The PRESYNC state keeps checking the HEC to ensure that the previous indication was not false. False indications are interpreted to mean the circuit is not tracking valid ATM cells. After entering the PRESYNC state, the first false indication triggers a transition back to HUNT state.

If the PRESYNC state HEC is correct, then a transition to the SYNC state occurs after *"δ"* cells (DELTA in ITU I.432) are correctly received. In the SYNC state, the CD circuit treats the incoming ATM cell stream as stable and the MT90225/226 functions normally.

While in the SYNC state, if an incorrect HEC is obtained *"α"* consecutive times (ALPHA in ITU I.432), cell delineation is considered lost and a transition is made back to the HUNT state (see Figure 5).

As defined by the ITU I.432 recommendations, the value of ALPHA and DELTA determine the robustness of the delineation method. The value of ALPHA and DELTA for the Cell Delineation state machine are defined in the **Cell Delineation (0x00C9)** register. Only one set of values is defined for the sixteen Cell Delineation state machines. The status of the CD state machine for each link is available in bits 0 through 15 of the **Cell Delineation Status (0x00E6)** register.

The ITU I.432 suggested values are: ALPHA = 7; and DELTA = 6.

Loss of Cell Delineation (LCD) is detected by counting the number of incorrect cells while in HUNT state. The MT90225/226 provides an internal **Loss of Delineation (0x00C8)** register to set the threshold for this count. A value of 360 in the LCD register would correspond to 79 msec for E1 and 100 msec for T1 applications. The LCD state for each link is available in bit 1 of the **IRQ Link Status (0x0435 - 0x4444)** registers.

The LCD and End of LCD status bit reports the current condition of the Cell Delineation State Machine at the time it is read, and can optionally generate an interrupt (IRQ). Table 1 provides the time, in microseconds, for the CD circuit to receive a full ATM cell from the T1 and E1 frame payloads.

Format	Average Cell Time (μs)
T1	276
E1	221

Table 1 - Cell Acquisition Time

While the cell delineation state machine is in the SYNC state, the verification circuit implements the state machine shown in Figure 7.

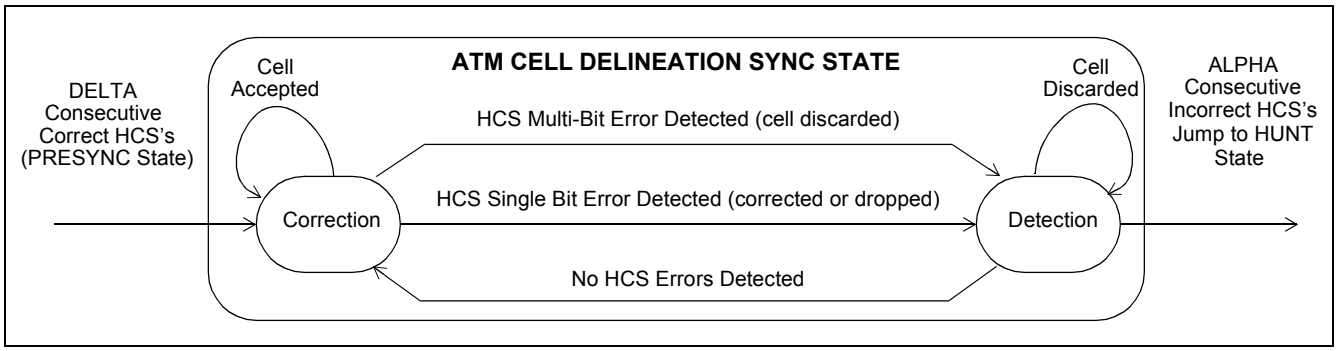


Figure 7 - SYNC State Block Diagram

In normal operation, the HEC verification state machine remains in the'correction' state. Incoming cells containing no HEC errors are passed through. Incoming single-bit errors can be corrected if required by the application (i.e., single bit error correction can be enabled or disabled).

After correction (when enabled), the resulting ATM cell is passed to the Rx Link UTOPIA FIFO.

If a single or multi bit error occurs, the state machine transitions to the 'detection' state. When a cell with a good HEC is detected, the state machine returns to the 'correction' state. The HEC calculation normally includes the ATM FORUM polynomial ($X^6 + X^4 + X^2 + 1$). The use of the polynomial can be disabled by writing to bit 1 or 9 of the **RX Link Control (0x00C0-0x00C7)** register.

3.1.1 Cell Delineation with Sync signal

When a serial TDM stream is used with a sync signal such as a TDM Frame Pulse, byte alignment is guaranteed. As a result, the hunt algorithm searches for the cell boundary based on a predefined number of bytes. If it fails, the hunt algorithm shifts one byte and tries again.

3.1.2 Cell Delineation without Sync signal

When a serial TDM stream is used without a sync signal (e.g. in non-framed mode), byte alignment is not guaranteed. The hunt algorithm searches for the cell boundary based on a predefined number of bytes. If it fails, the hunt algorithm shifts one bit and tries again. When the hunt algorithm succeeds, it will have determined both the cell boundary and the byte alignment. This mode of operation is selected by setting bit 10 of **TDM RX Link Control (0x0700-0x070F)** register.

3.2 De-Scrambling and ATM Cell Filtering

The CD circuit can de-scramble the cell payload field. The de-scrambling algorithm can be enabled or disabled using bit 5 or 13 of the **RX Link Control (0x00C0-0x00C7)** registers.

The MT90225/226 can be programmed, using the **RX Link Control (0x00C0-0x00C7)** registers, to discard received ATM cells with HEC errors using bits 2 and 10.

HEC error correction is optional and can be enabled by the CPU. When the option to correct an incoming HEC value with 1 bit error is selected, the HEC is corrected and the cell is not counted as a cell with a bad HEC. If the option to remove the cells that are received with a bad HEC is selected, then the incoming cells are discarded. The counter is not incremented if the HEC value is corrected, when the option is enabled.

Incoming Idle and Unassigned cells can be detected and dropped automatically.

4.0 Description of the TDM Interface

The Transmit TDM blocks are independent of the Receive TDM blocks. The TX port of a framer can be connected to any of the MT90225/226 TX UTOPIA Input ports and the RX port of a framer can be connected to any of the MT90225/226 RX UTOPIA Output ports.

The TDM interface provides a variety of modes to work with different T1/E1/DSL framers for various applications. In general, there are four major modes: Single mode, Wire-OR mode, Multiplex mode and Non-framed mode. Each mode can be further divided into several minor modes.

4.1 Single mode

In this mode, all links are active and can be used. Its minor modes of operation include Generic 1.544MHz mode (F-bit and 24 time slots), Generic 2.048MHz mode (32 time slots), and ST-BUS mode (32 time slots).

Mapping registers are used to determine when a time slot is used to carry the ATM traffic. There are two 16-bit mapping registers for each TDM TX and for each TDM RX links. Each bit of the 2 registers (total of 32 bits) controls one time slot. A bit value of 1 corresponds to an active time slot. A value of 0 corresponds to an inactive time slot and the output is in High Impedance mode for that time slot. The TDM TX link is independent of the TDM RX link and can have different mapping (using different time slots and optionally a different number of time slots).

Fractional T1/E1 and nx64 channel modes are implemented by programming bits in the mapping registers to enable the use of the required time slots.

4.1.1 Single mode - Generic 1.544MHz

This is also known as T1 generic mode. In this mode, data rate is 1.544 Mb/s, clock is 1.544 MHz and frame pulse is 8 KHz. A frame is 193 bits long and a frame pulse is present (either generated or accepted as input). The first bit, indicated by the frame pulse, is not used to carry any useful information; it is in high impedance on Tx link and is ignored on Rx link. The 24 time slots (192 bits) are controlled by the lowest 24 bits of the mapping register associated with a link. Fractional T1 is supported by activating (selecting) any of the first 24 time slots defined in the mapping register.

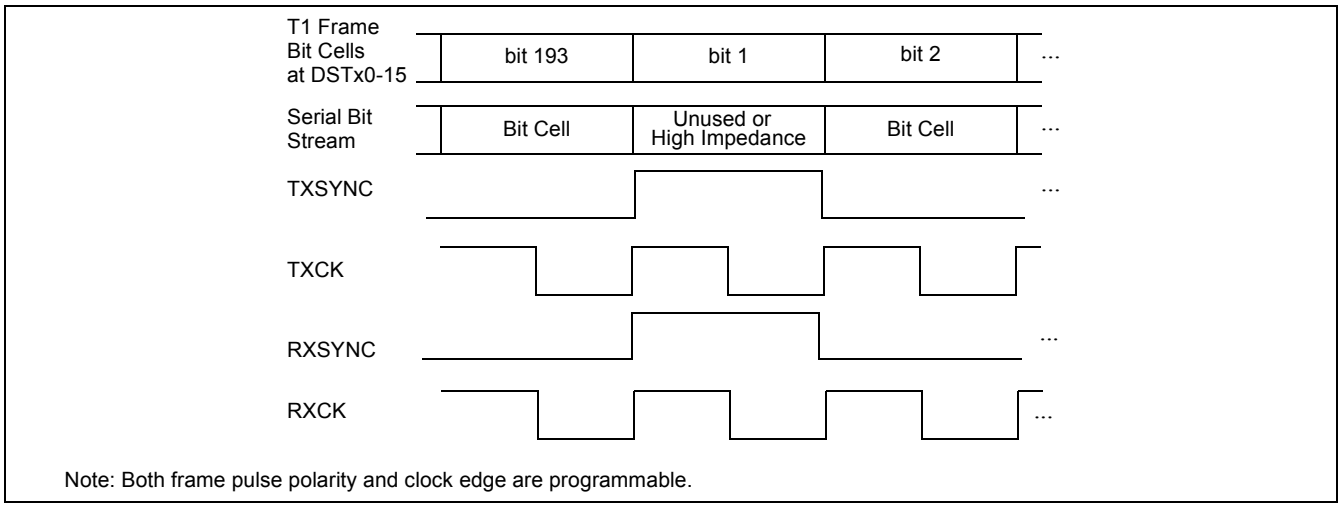


Figure 8 - Single mode - Generic 1.544 MHz

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings.

Data rate (bits 6:5) = 00
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.1.2 Single mode - Generic 2.048MHz

This is used for generic nx64 connections, where n can be any number from 1 to 32. In this mode, data rate is 2.048 Mb/s. A clock of 2.048 MHz is used and the Frame pulse is indicating the first bit of the first time slot of a frame of 32 time slots. The mapping registers are used to determine the number of time slots used and their position in the frame. This enables a direct interface to existing T1 or E1 framers and opens up the option to interface to generic nx64 devices. Fractional T1/E1 is supported as well by selecting the time slots that are used to carry ATM traffic.

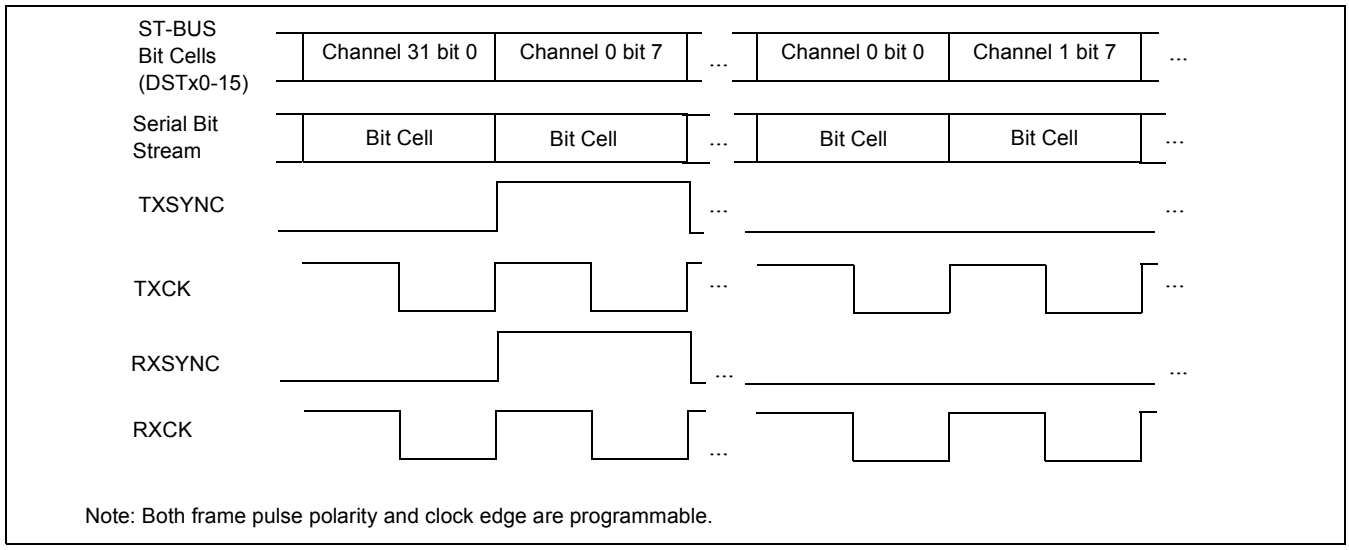


Figure 9 - Single mode - Generic 2.048 MHz

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings.

Data rate (bits 6:5) = 01
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.1.3 Single mode -ST-BUS

This is used for T1/E1 connection with ST-BUS, where data rate is 2.048 Mb/s, clock is 4.096 MHz and frame pulse is 8KHz. A standard ST-BUS mode is supported with 32 time slots in each frame. The Frame format and clock speed meet the ST-BUS or MVIP standard. The mapping registers are used to determine which of the 32 time slots are used to carry TDM traffic.

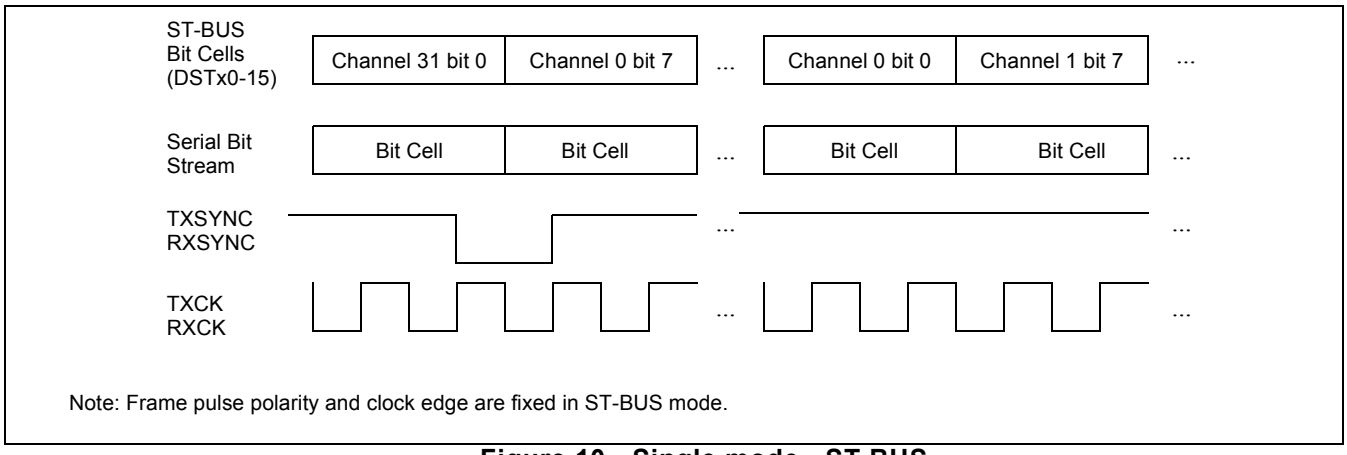


Figure 10 - Single mode - ST-BUS

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings.

Data rate (bits 6:5) = 01
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.2 Wire-OR mode

In this mode, two or four links are logically OR'ed together to share a single stream. This is particularly useful for fractional T1/E1 applications where links using different time slots can be multiplexed together onto a single stream in order to facilitate the interface to a single T1 or E1 framer.

Links that are OR'ed together can have any one of the Single mode discussed in Section 4.1. To avoid any contention, mapping registers of those links must not have the same bit set.

All links in Wire-OR mode must be configured in the same as they were in Single mode, except for **TDM Link Control** registers. Two minor modes are available, 2-link grouping and 4-link grouping.

4.2.1 Wire-OR mode - 2 link grouping

Two links in a pair are OR'ed together by using this mode. The links that are paired are pre-determined: link 0 is paired with link 1, link 2 is paired with link 3 and so on. When link 0 and link 1 are paired, the pins associated with link 1 cannot be used and are tri-stated, however, bit 7 of its **TDM TX(RX) Link Control** registers must be set. The two links operate using the Clock and SYNC signals of link 0. The same logic applies for the other pairs.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings. Note that both links in a pair must have the same settings.

Data rate (bits 6:5) = 00 or 01
Multiplex mode (bits 4:3) = 01
Clock and Sync format (bit 2) = 0 or 1
Enable (bit 7) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.2.2 Wire-OR mode - 4 link grouping

Four links in a group are OR'ed together by using this mode. The links that are grouped are pre-determined: links 0, 1, 2 and 3 are grouped and the OR'ed input/output is available on link 0 only. Pins associated with links 1, 2 and 3 cannot be used and are tri-stated, however, bit 7 of **TDM TX(RX) Link Control** registers for those three links must be set. The four links operate using the Clock and SYNC signal of link 0. The same logic applies for the other groups.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings. Note that all four links in a group must have the same settings.

Data rate (bits 6:5) = 00 or 01
Multiplex mode (bits 4:3) = 10
Clock and Sync format (bit 2) = 0 or 1
Enable (bit 7) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0

4.3 Multiplex mode

A multiplex mode is offered by many multi-channel T1/E1 framers to multiplex several T1/E1 links on to one high speed data link. The same mode is available on MT90225/226, where two or four 2.048 Mb/s links are multiplexed using a common clock of 8.192 or 16.384 MHz. In this major mode, two or four links running at 2.048 bps (either 2.048MHz Single mode or 4.096MHz Single mode) are interleaved on a time slot basis (byte by byte) to provide a multiplexed link at a data rate of 4.096 Mb/s or 8.192 Mb/s.

In Multiplex mode, links are treated or processed the same way as they are in Single mode. The only difference is the way that data is carried on TDM bus. In Single mode, each link uses its own TDM port to carry data, whereas in Multiplex mode two or four links shares a single high speed port. As in Wire-OR mode, links in Multiplex mode must be configured in the same as they were in Single mode, except for **TDM Link Control** registers.

When multiplexed mode is used, the time slots on the multiplexed links have to use a common synchronized clock source and Frame Pulse for the multiplexed links. Multiplexing of fractional T1/E1 is also possible through the control of merged mapping registers.

Only ST-BUS mode is supported in Multiplex mode.

There are two minor modes in Multiplex mode, 2-link multiplexing and 4-link multiplexing.

4.3.1 Multiplex mode - 2 link multiplexing

In this mode, two links of 2.048 Mb/s are multiplexed onto a single link of 4.096 Mb/s. The links that are paired are pre-determined: link 0 is multiplexed with link 1, link 2 is multiplexed with link 3 and so on. When link 0 and link 1 are multiplexed, the pins associated with link 1 cannot be used and are tri-stated, however, bit 7 of its **TDM TX(RX) Link Control** registers must be set. The two links operate using the Clock and SYNC signals of link 0. The same logic applies for the other groups.

As an example of this grouped multiplexing, the MT90225/226 support eight high speed links on links 0, 2, 4, 6, 8 10, 12 and 14.

Unlike Single mode, the only clock format supported is ST-BUS mode. The data rate is 4.096 Mb/s. A clock of 8.192 MHz is used and the Frame pulse indicates the first bit of the first time slot of a frame of 64 time slots. The mapping registers of the 2 physical links are merged by bit-to-bit interleaving to form a larger mapping register supporting up to 64 time slots.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings. Note that both links in a pair must have the same settings.

Data rate (bits 6:5) = 10
Multiplex mode (bits 4:3) = 01
Clock and Sync format (bit 2) = 1
Enable (bit 7) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0
TX clock direction (bit 9 of **TDM TX Link Control** only) = 1

4.3.2 Multiplex mode - 4 link multiplexing

In this mode, four links of 2.048 Mb/s are multiplexed onto a single link of 8.192 Mb/s. The links that are combined are pre-determined: links 0, 1, 2 and 3 are grouped and the multiplexed input/output is available on link 0. When link 0 is used, the pins associated with links 1, 2 and 3 cannot be used and are tri-stated, however, bit 7 of **TDM TX(RX) Link Control** registers for those three links must be set. The four links operate using the Clock and SYNC signal of link 0. The same logic applies for the other groups.

As an example of this grouped multiplexing, the MT90225/226 supports four high speed links on links 0, 4, 8 and 12.

Unlike Single mode, the only clock format supported is ST-BUS mode. The data rate is 8.192 Mb/s. A clock of 16.384 MHz is used and the Frame pulse indicates the first bit of the first time slot of a frame of 128 time slots. The mapping registers of the 4 physical links are merged by bit-to-bit interleaving to form a larger mapping register supporting up to 128 time slots.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings. Note that all four links in a group must have the same settings.

Data rate (bits 6:5) = 11
Multiplex mode (bits 4:3) = 10
Clock and Sync format (bit 2) = 1
Enable (bit 7) = 1
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 0
TX clock direction (bit 9 of **TDM TX Link Control** only) = 1

4.4 Non-framed mode

Single mode, Wire-OR mode and Multiplexed mode are all dealing with framed data, that is, a frame pulse must be present to give both byte and frame alignment. However, MT90225/226 also support a non-framed mode where only a serial bit stream and clock are available for each link. Moreover, a wide range of data rate is supported by this mode, which makes it particularly useful in DSL applications where the line rate may vary.

When used in Non-framed mode, RXSYNC must be de-asserted. For example, if RXSYNC is defined as active low frame pulse (bit 0 cleared in **TDM RX Link Control** register), RXSYNC input pin must be tied to high. The same applies to TXSYNC when it is an input pin.

Mapping registers must all be set to 0xFFFF in Non-framed mode. Serial clock rate and data rate must be the same. Moreover, bit mode cell delineation (bit 10 in **TDM RX Link Control** registers) must be selected, and register **0x0741** must be written by 0x36.

Three minor modes are available in Non-framed mode, resulting to different data rate and link number.

4.4.1 Non-framed mode - 2.5Mbps

In Non-framed mode, all links are able to run from 0 up to 2.5 Mb/s. On the transmit side, if the TXCK and TCSYNC are programmed as inputs, TXSYNC must be disabled state, and the transmitter will be "free running" and will output serial data continuously. If the TXSYNC is defined as output, a frame pulse is generated for every 256 TXCK cycles, but can be ignored.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by the following settings.

Data rate (bits 6:5) = 01
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 1

4.4.2 Non-framed mode - 5.0Mbps

If a serial link of more than 2.5Mbps but less than 5.0Mbps data rate is required, this mode can be applied. For every two links in a pair, one is disabled and the other is able to run from 0 up to 5.0 Mb/s. The links that are paired are pre-determined: link 0 with link 1, link 2 with link 3 and so on. The link that will remain enabled in each pair is also pre-determined. They are link 0, 2, 4, 6, 8, 10, 12 and 14.

For the pair of link 0 and link 1, the pins associated with link 1 cannot be used and are tri-stated. On the transmit side of link 0, if the TXCK and TCSYNC are programmed as inputs, TXSYNC must be de-asserted, and the transmitter will be "free running" and will output serial data continuously. If the TXSYNC is defined as output, a frame pulse is generated for every 512 TXCK cycles, but can be ignored. The same logic applies for the other pairs.

For any disabled link, its associated registers are all disabled, except for mapping registers that must be set to all one. No other configuration is necessary for disabled links.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by writing the following settings into those enabled links only.

Data rate (bits 6:5) = 10
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 1

4.4.3 Non-framed mode - 10.0Mbps

If a serial link of more than 5Mbps but less than 10.0Mbps data rate is required, this mode can be applied. For every four links in a group, three are disabled and the other is able to run from 0 up to 10.0Mbps. The four links that can be grouped are pre-determined: link 0,1, 2, 3 are one group; link 4, 5, 6, 7 are one group and so on. The link that will remain enabled in each group is also pre-determined. They are link 0, 4, 8 and 12.

For the group of link 0, 1, 2 and 3, the pins associated with link 1, 2 and 3 cannot be used and are tri-stated. On the transmit side of link 0, if the TXCK and TCSYNC are programmed as inputs, TXSYNC must be de-asserted, and the transmitter will be "free running" and will output serial data continuously. If the TXSYNC is defined as output, a frame pulse is generated for every 1024 TXCK cycles, but can be ignored. The same logic applies for the other groups.

For any disabled link, its associated registers are all disabled, except for mapping registers that must be set to all one. No other configuration is necessary for disabled links.

This mode is selected in **TDM TX Link Control (0x0600-0x060F)** and **TDM RX Link Control (0x0700-0x070F)** by writing the following settings into those enabled links only.

Data rate (bits 6:5) = 11
Multiplex mode (bits 4:3) = 00
Clock and Sync format (bit 2) = 0
Cell delineation mode (bit 10 of **TDM RX Link Control** only) = 1

4.5 Clock formats

In any framed modes, the Frame signal format can be one of two options. It can be of a generic format (active high or low during the first bit of the frame) or ST-BUS format (active low at the boundary of the frame). In the generic modes, the clock polarity can be selected to have a rising or falling edge at the bit boundary.

The TXCK and TXSYNC signals can be either outputs or inputs.

4.6 TDM Loopback Mode

Two loopback modes are provided where the TDM RX inputs are internally routed back to the TDM TX outputs (remote loopback) with the RX block fully operational, and where the TDM TX outputs are routed back to the TDM RX inputs for test purposes (metallic loopback). The TX and RX links have to be programmed in the same mode for the loopback to operate properly. Bit 8 of the **TDM TX Link Control Register (0x0600-0x060F)** controls the remote loopback and bit 8 of the **TDM RX Link Control (0x0700-0x070F)** register controls the metallic loopback.

To use remote loopback, TXCK and TXSYNC must be configured as output sourcing from the RXCK and RXSYNC of the same port. The loopback is on a per link basis with the limitation that physical links are paired: i.e. TX link 0 is connected to RX link 0 and so on.

Besides TDM loopacks, there is also a UTOPIA loopback described in the section 5.7.

4.7 Serial to Parallel (S/P) and Parallel to Serial (P/S) Converters

Each serial TDM link has assigned S/P and P/S units. The P/S unit takes a byte from the cell RAM and converts it to a serial bit stream. The S/P unit takes a byte from the DSTi input and converts it to parallel format for use by the Cell Delineation block.

P/S and S/P units can be set-up differently on a per port and per direction basis (i.e. the transmit and receive function of the same port can use different configurations). The following features are supported:

- programming links as T1 or E1
- using ST-BUS and Generic TDM modes
- enabling/disabling the P/S and S/P units (if they are disabled the associated outputs are Tri-stated)
- selecting TDM timeslots as per mapping registers.
- independently programming the polarity of RXCK, TXCK, RXSYNC and TXSYNC signals (Generic TDM mode only)
- generating/accepting TXSYNC and TXCLK signals to support most T1 and E1 framers (depending on the programmed mode)
- monitoring RXSYNC signal period and reporting the unexpected occurrence of a synchronization signal
- monitoring TXSYNC signal period (when defined as input) and reporting the unexpected occurrence of a synchronization signal
- generating a TXSYNC pulse on every TDM frame when defined as output

When the TXCK and TXSYNC signals are outputs, the source for the TXCLK is software selectable from any of the RXCK inputs or any of the four external REFCKs. The TXSYNC signal is generated from the TXCK and is independent from (not aligned with) the RXSYNC or other TXSYNC signals.

4.8 Clocking Options

TXCK and TXSYNC can be either input or output signals. When TXCK and TXSYNC are inputs, they are generated by external circuitry. When TXCK and TXSYNC are outputs, TXCK source is software selectable and can be any of the RXCK signals or four external REFCK inputs (see Figure 11). The TXSYNC is generated from the TXCK signal.

The RXCK pins are always defined as inputs and the proper signal must be provided to each input.

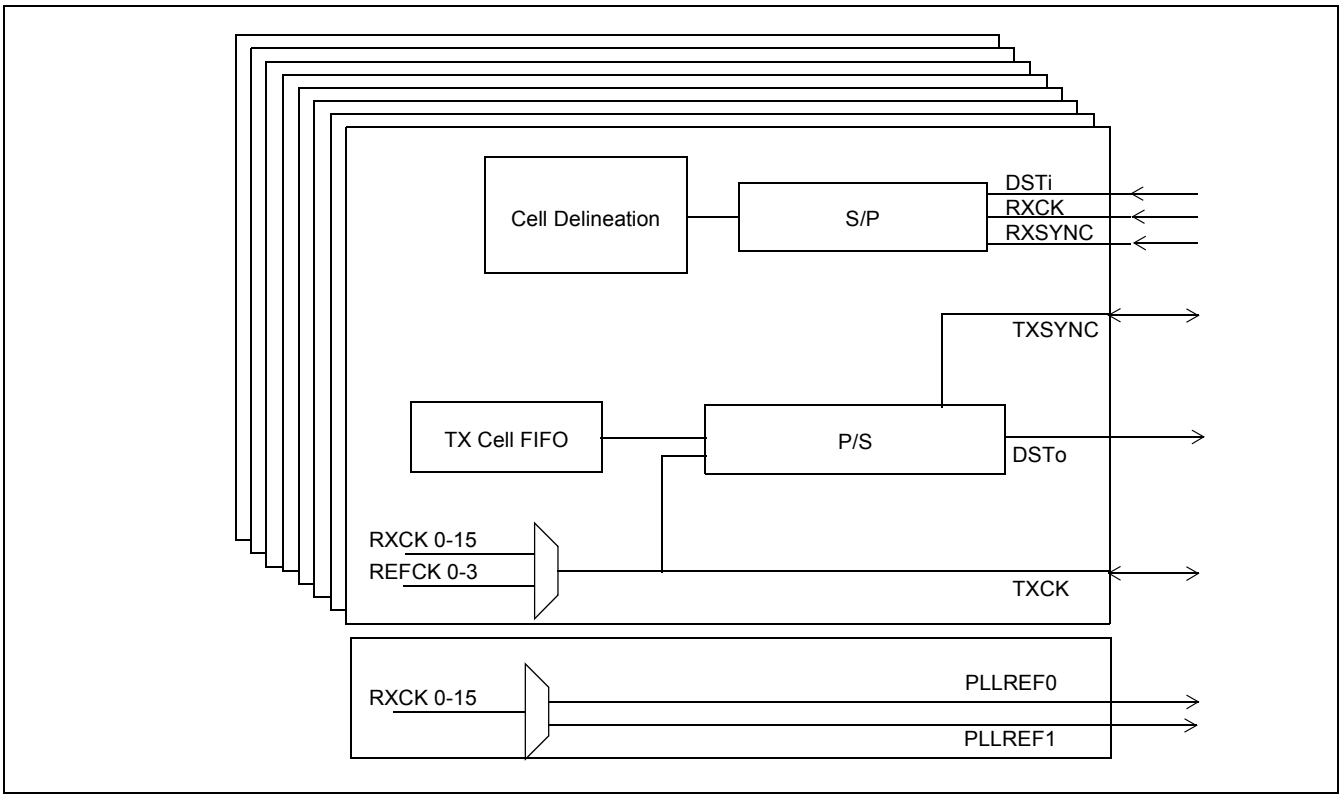


Figure 11 - TXCK and TXSYNC Output Pin Source Options

4.8.1 Verification of the RXSYNC Period

The RXSYNC signal is used to align the incoming DSTi data to retrieve all the T1 or E1 channels. The RXSYNC pulse can be present for each TDM frame (8Khz) or once per Superframe (an integer number of frames, typically 12 or 16). The period and position of the RXSYNC is verified for each receive block independently. A status bit (1 per link) in the **RXSYNC Status (0x0730)** register is set if the synchronization pulse occurs at an unexpected time in the frame. The RX block will be re-aligned with this new synchronization pulse.

4.8.2 Verification of the TXSYNC Period

The TXSYNC signal is used to align the outgoing DSTo data to retrieve all the T1 or E1 channels. When defined as input, the TXSYNC pulse can be present for each TDM frame (8Khz) or once per Superframe (every 12 or 24 TDM frames). The period and position of the TXSYNC is verified for each transmit block independently. A status bit (1 per link) in the **TXSYNC Status (0x0633)** register is set if the synchronization pulse occurs at an unexpected time in the frame. The TX block will be re-aligned with this new synchronization pulse.

4.8.3 Primary and Secondary Reference Signals

Two output pins are provided to simplify the external circuitry required when using an external PLL. These two pins, PLLREF0 and PLLREF1, re-route any of the RXCK signals and drive the primary and secondary reference signals of a PLL under software control. Refer to Section 8, Application Notes, for examples.

4.8.4 Verification of Clock Activity

The MT90225/226 implements circuitry to determine whether or not a selected clock signal is active. This feature is used to ensure a clock is operational before using it as a source for one or more transmit links. A read of the **TXCK Status (0x0630), RXCK Status (0x0631)** or **REFCK Status (0x0632)** register indicates a faulty clock if a bit is '1'. A value of '0' for these bits means that activity was observed on this clock. This circuitry does not measure the frequency of a clock signal, it only detects activity on the TXCK, RXCK and REFCK signals.

4.8.5 Clock Selection

The clock selection circuitry selects the desired clock signal and ensures a smooth, glitch free, transition between the current clock source and the new clock source. Clock source activity can be verified using the **TXCK Status (0x0630), RXCK Status (0x0631)** or **REFCK Status (0x0632)** registers.

5.0 UTOPIA Interface Operation

The MT90225/226 supports the UTOPIA L1 and L2 Mode, 8 or 16 bit wide bus at up to 52MHz, with odd/even parity, for cell level handshake only. Each port can be assigned an address ranging from 0 to 30. The address value of 31 is reserved and should not be used.

The TX and RX paths of each link has its own PHY address. These PHY addresses are defined in the **UTOPIA Input Link Address** (**0x0040-0x0047)** and **UTOPIA Output Link Address (0x000-0x0007)** registers. The **UTOPIA Input LINK PHY Enable (0x0050)** and the **UTOPIA Output Link PHY Enable (0x0010)** registers are used to enable the PHY address of the links.

The MT90225/226 UTOPIA port uses handshaking signals to process data streams. The start of a cell (SOC) is marked by the UTOPIA SOC sync signal. This signal is active during the transfer of the first byte of a cell. The 52 bytes that follow the arrival of the first byte of a cell are interpreted as belonging to the same cell and are stored accordingly (note that SOC sync signals received during the loading of these 52 bytes are ignored).

The Cell Available status line (Clav) is used to communicate to the ATM controller whether the MT90225/226 has space for a cell in the PHY address that was polled in the previous cycle. Whenever there is space for a cell in the TX direction or a cell ready in the RX direction, the TXClav and/or RXClav signal will be driven High or Low. When the address does not correspond to any enabled PHY address inside the MT90225/226, the TXClav and RXClav signal are set to high impedance mode. The use of an external pull-down may be required for the proper operation of the Utopia bus in MPHY mode.

Note that the transmit or receive Utopia clock frequencies do not have to be synchronized with the system clock by their frequencies cannot exceed the system clock frequency.

5.1 ATM Input Port

The UTOPIA interface input clock TxClk is independent of the system clock. The UTOPIA TxClk can be up to 52 MHz. The incoming cell is stored directly in the internal TX Cell RAM where the TX UTOPIA FIFOs are implemented.

The Tx byte clock (TxClk) is checked against the system clock. If the incoming byte clock frequency is lower than 1/128 of the system clock, bit 2 of the **General Status (0x040E)** register will be set. This bit is cleared by overwriting it with 0. This aids in debugging as the presence of a UTOPIA clock is required not only for data transfer but also for proper operation of the UTOPIA registers.

The total space for the UTOPIA input cells for all links is 118. These 118 cells are shared between 16 TX UTOPIA FIFOs. The size (length) of each TX UTOPIA FIFO is defined by writing to the **TX LINK FIFO Length Definition (0x008B-0x0092)** registers.

The device will not accept a cell from the UTOPIA Interface if the internal Cell Ram is full. Status bit 0 in the General Status (0x040E) register is set to 1 to indicate the ’no free cell in TX Cell RAM’ condition. The status bit can be cleared by overwriting it with 0.

The UTOPIA Input block has the option to verify the HEC of the cell coming from the ATM layer. Four different options are available and are selected by bits 1 and 0 of the **UTOPIA Input Control (0x0052)** register.

- The ’00’ option is used to always accept a cell from the ATM layer. The HEC is verified and if wrong, the UTOPIA Input counter associated with the UTOPIA port for cells with bad HEC is incremented. The MT90225/226 will re-generate a valid HEC based on the content of the 4-byte header that was received.

- The ’01’ option is used to verify the HEC of an incoming cell. If the HEC value is wrong and if it can be corrected (1 bit error), then the cell is corrected and accepted as a good cell. The bad HEC counter is not incremented if the HEC is corrected. The bad HEC counter is incremented if the HEC value cannot be corrected. In this mode, the cell is always accepted. The MT90225/226 will re-generate a valid HEC based on the content of the 4-byte header that was received.
- The ’10’ option is used to verify the HEC on the incoming cell and discard the cell if the HEC value is wrong. The bad HEC counter is incremented if a cell is discarded.
- The ’11’ option is similar to mode ’01’ except that if the HEC value cannot be corrected, then the cell is discarded. If the HEC value is corrected, the bad HEC counter is not incremented.

5.2 ATM Output Port

The MT90225/226 supports a 53 byte cell stream via the ATM output port. Cells received at the ATM output port are stored in the RX UTOPIA FIFO before being processed by the UTOPIA Interface. The output of the UTOPIA Interface can be stopped by the ATM Layer device by de-asserting the RxENB* signal.

The start of a cell is marked with the SOC signal, which is active during the transmission of the first byte of a cell. The following 52 bytes are expected to belong to the same cell.

The RX byte clock (RxClk) can be up to 52 MHz and is checked against the system clock. If the incoming byte clock frequency is lower than 1/128 of the system clock, bit 3 of the **General Status (0x040E)** register will be set. This bit is cleared by overwriting it with 0. This aids in debugging as the presence of a UTOPIA clock is required not only for data transfer but also for proper operation of the UTOPIA registers.

Overflow conditions in the RX UTOPIA FIFO associated with any of the 16 PHY RX Addresses cause a status bit to be set in either the **IRQ Link TC Overflow Status (0x0410-0x041F)**. These status bits are cleared by overwriting them with 0. Additionally, for each status bit there is an Interrupt Enable bit in the associated **IRQ Link TC Overflow Enable (0x0434)** register. When enabled, the status bit is reported in an Interrupt register. See section 6.2 Interrupt Block for more details.

The size of the RX UTOPIA FIFO is fixed at four cells for each of the PHY Addresses.

Note that in the receive direction, the parity bit that is generated is not valid if the receive Utopia clock is faster than 50 MHz.

5.3 UTOPIA Operation

Each Utopia port inside an MT90225/226 corresponds to a physical serial TDM (T1, E1, J1, DSL) line. Up to sixteen PHY ports can be supported by one MT90225. Up to eight MT90225/226s can be connected to a UTOPIA bus. The ports in the same device represent only one electrical load on the UTOPIA bus. The MT90225/226 supports the full UTOPIA L2 Interface limit of 31 PHY addresses.

The MPHY address at the input port of MT90225/226 (TxAddr[4:0]) is used to store the cell in one specific TX UTOPIA FIFO.

The MPHY address at the output port (RxAddr[4:0]) is used to retrieve the cells from the proper RX UTOPIA FIFO.

5.4 UTOPIA Operation With a Single PHY

A single ATM layer device with a UTOPIA L2 MPHY port can be connected to the ATM input port of one MT90225/226. Another ATM-Layer device using the UTOPIA L2 MPHY input interface is used to receive ATM cells from the MT90225/226.

The address pins should be set to the value programmed by the management interface.

5.5 UTOPIA Operation with Multiple PHY

When more than one MT90225/226 is connected to a single ATM Layer device the single TxClav and RxClav scheme is used. Direct Status Indication and Multiplexed Status Polling schemes are not supported. The necessary polling is performed by the ATM-Layer device.

The UTOPIA Interface transmit and receive addresses, provided by the ATM-Layer device, are used to de-multiplex the ATM-cell stream to as many as eight MT90225/226s (as limited by the UTOPIA L2 specification's maximum of eight device loads and 31 addresses). The maximum total available bandwidth for the serial lines served by each MT90225/226 device is 40 Mbits/s (totalling 5MBytes/s per MT90225/226 device).

5.6 UTOPIA Loopback

With UTOPIA loopback enabled, the Tx UTOPIA port will accept cells and loop these back to the Rx UTOPIA interface. The Rx UTOPIA interface will then output these cells.The UTOPIA loopback is enabled by setting the bit 9 in **UTOPIA Input Control Register (0x0052).**

5.7 Examples of UTOPIA Operation Modes

Figure 12 shows the connection of one ATM layer device to MT90225/226.

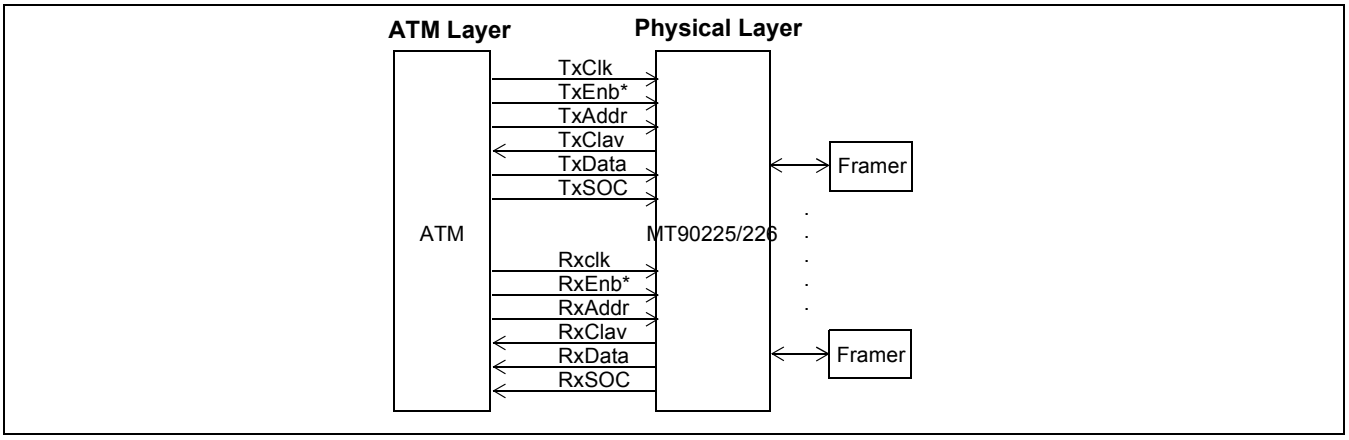


Figure 12 - ATM Interface to MT90225/226

Figure 13 shows the connection of one ATM Device with more than one MT90225/226.

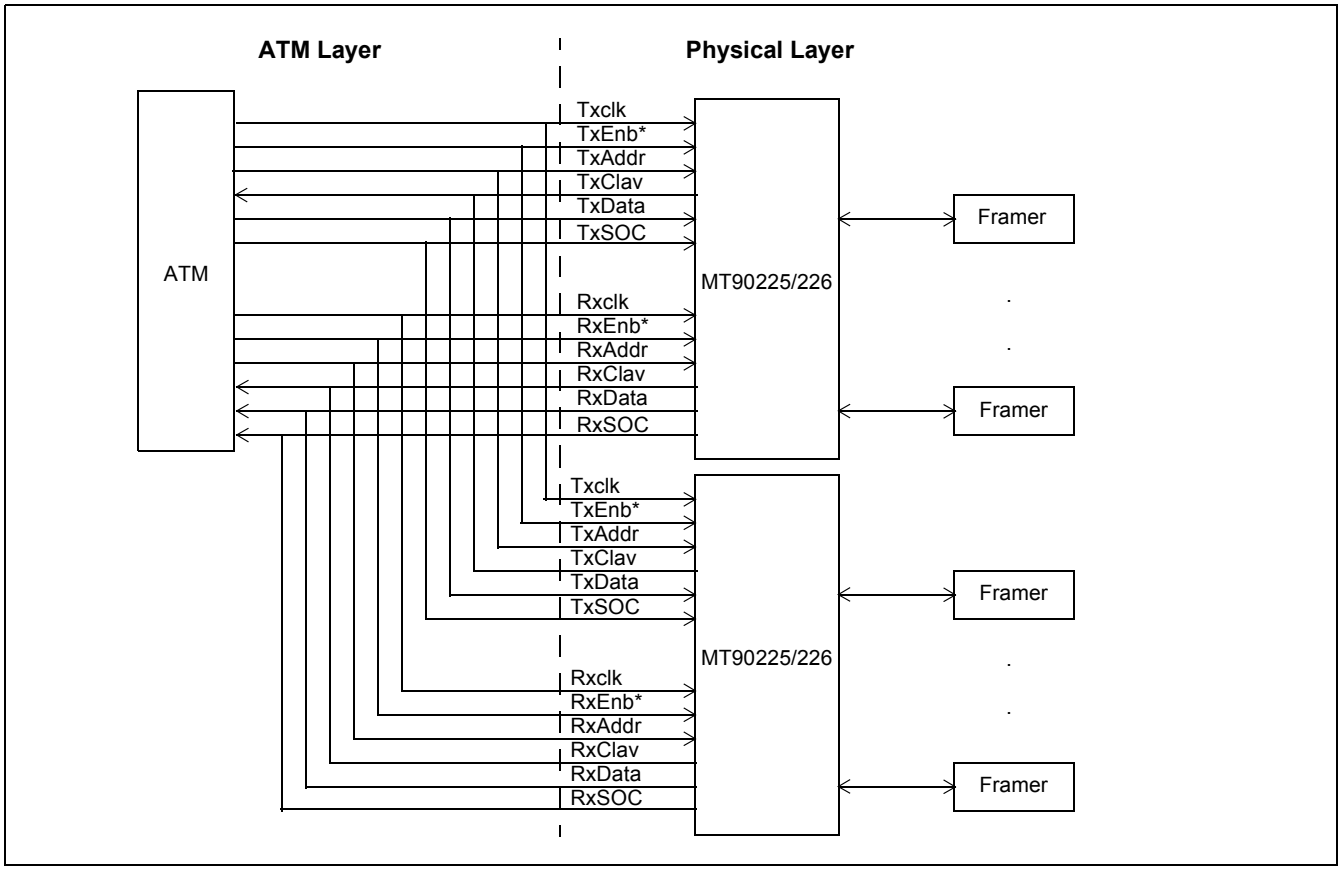


Figure 13 - ATM Interface to Multiple MT90225/226

6.0 Support Blocks

6.1 Counter Block

The MT90225/226 includes 144 24-bit counters to provide statistical information on the device's operation. All the counters are cleared by a hardware reset. A maskable interrupt can be generated when the counter overflows. Counters can also be latched to capture the state of all registers at once.

A predetermined value can also be loaded into a counter. This feature can be used to generate an interrupt after a specified number of cells is processed. Counter values are incremented by 1 for every event occurrence and, when the count reaches all 1's, will overflow (to all 0's).

6.1.1 UTOPIA Input I/F counters

There are four counters associated with the each of the 16 UTOPIA Inputs (from ATM layer to the MT90225/226) for a total of 64 counters. These counters record the following information:

- the total number of cells or the total number of user cells received at the UTOPIA Input I/F
- the total number of Idle Cells received at the UTOPIA Input I/F, removed or not
- the total number of Unassigned Cells received at the UTOPIA Input I/F, removed or not
- the number of cells having a single or multiple bit error in the HEC, removed or not but not including the cells where the HEC is corrected

6.1.2 Transmit TDM I/F Counters

There are two counters associated with the each of the sixteen transmit TDM links for a total of 32 Transmit counters. These counters record the following information:

- the total number of cells sent through the TDM link
- the total number of Idle cells or the total number of user cells sent through the TDM link

6.1.3 Receive TDM I/F Counters

There are three counters associated with each of the sixteen receive TDM links for a total of 48 receive counters. These counters record the following information and are active as soon as the RX TDM port is enabled:

- the total number of cells received through the TDM link.
- the total number of Idle cells or the total number of user cells received through the TDM link
- the total number of cells with wrong HEC, discarded or not, received through the TDM link but not including the cells where the HEC is corrected

6.1.4 Access to the Counters

Accessing (READ) counters is a three step operation. First, the desired counter must be selected by writing to the **Select Counter Register (0x0432)**. Second, the READ command ('0x00x101') is written to the **Counter Transfer Command (0x040F)** register. This command causes the current three byte count value to be copied from the specified counter to the two 16 bit-wide **Counter Byte 3 Register (0x0430)** and **Counter Bytes 2 and 1 Register (0x0431)** registers (note that this value is unchanged until another counter read command is issued). And third, the **Counter Byte 3 Register (0x0430)** and **Counter Bytes 2 and 1 Register (0x0431)** registers are read to obtain the three byte count value of the selected counter.

Pre-loading (WRITE) a counter is also a three step function. First, the three byte pre-load value is written to the two 16 bit-wide **Counter Byte 3 Register (0x0430)** and **Counter Bytes 2 and 1 Register (0x0431)** registers. Second, the identification of the counter to be pre-loaded is written to the **Select Counter Register (0x0432)**. And third, the WRITE command ('0x00x001') is written to the **Counter Transfer Command (0x040F)** register.

The IRQ enable bit of a counter is set, or reset, by selecting the counter and writing to the appropriate bit of the **Counter Transfer Command (0x040F)** register. The value'0x001010' enables the counter IRQ and 'xxx00010' disables (masks) it.

6.1.5 Latching counter mode

An additional mode of operation is available in the counter block where the values of all the counters are transferred, all at the same time, to a series of internal registers. The transfer can be initiated automatically based on an input signal or following a transfer command under software control.

When the source for the latch command is from the dedicated input pin, the user has the option to use directly this signal as a latch command or to divide the incoming signal by 8000 before generating the latch command (for example, using the 8 kHz F0 frame pulse signal to create 1 second intervals). Bits in the **Counter Transfer Command (0x040F)** register are defined to support these features.

The counters are 24 bits wide when operated without the latching option and are 16 bits wide when the latching feature is enabled. After each latch signal, the counters are reset to 0 in order to report the number of events between two latch commands.

Before the latching mode is enabled, the counters may be loaded (or reset), but the software should not write to the counters after the latching mode is enabled.

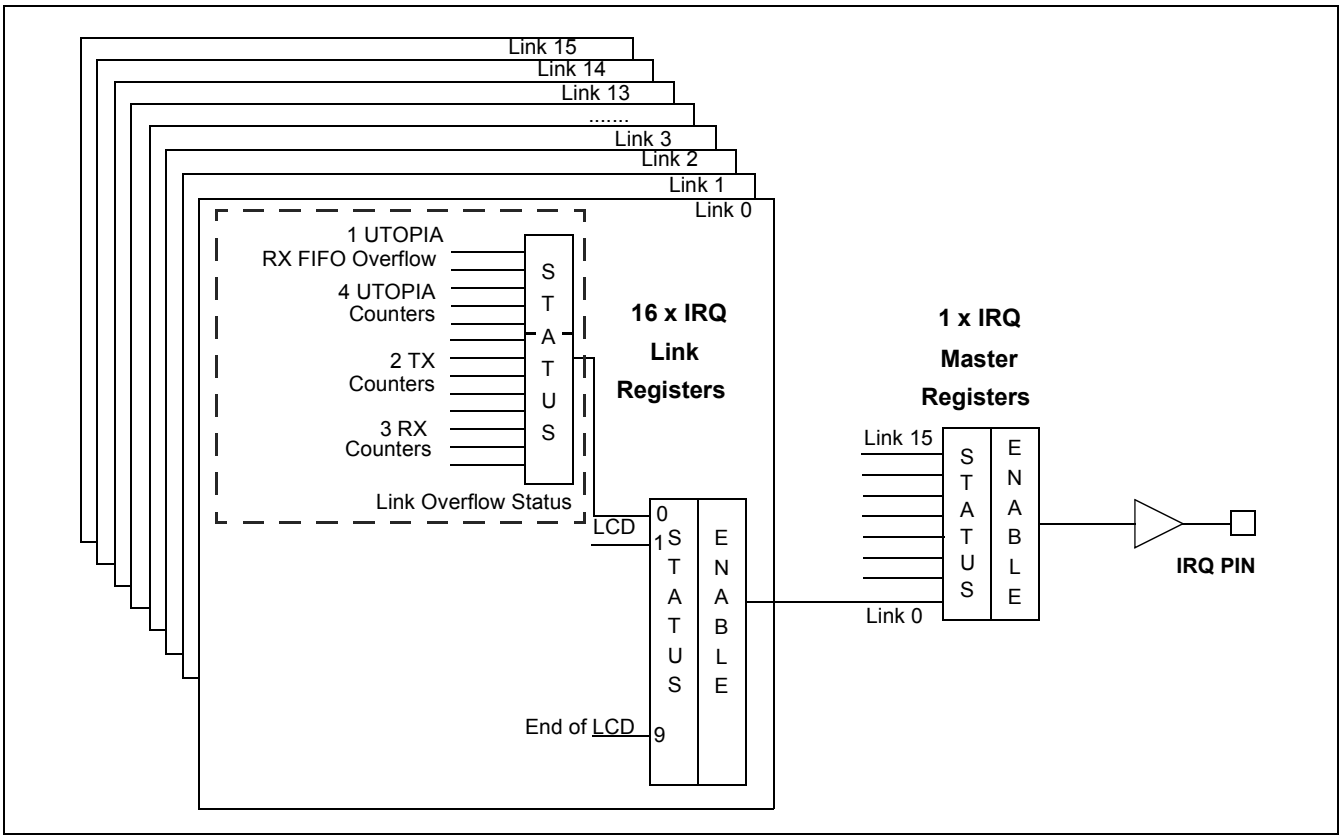


Figure 14 - IRQ Register Hierarchy

6.2 Interrupt Block

The MT90225/226 can generate interrupts from many sources. All interrupt sources can be enabled or disabled. Write action is required to clear the source of interrupt. Interrupts are grouped on a per link basis, with six sub-categories for each link. These special interrupts are only present in the Link 0 IRQ Status register. Refer to Figure 14 for a representation of the interrupt register hierarchy.

6.2.1 IRQ Master Status and IRQ Master Enable Registers

There is a **IRQ Master Status (0x0455)** register that reports interrupts generated by any event on any of the links. Each bit of this register corresponds to a link. A '1' in a bit position indicates that the associated link is reporting an interrupt condition. For each bit in the **IRQ Master Status (0x0455)** register, there is a corresponding bit in the **IRQ Master Enable (0x0433)** register. When any IRQ source is active and the corresponding Enable bit is '1', then the $\overline{\text{IRQ}}$ pin will go LOW (active).

The **IRQ Master Status (0x0455)** register always reports the current state of the source(s) of interrupt. It does not latch the interrupt request(s); it only reports that one or more bit(s) in one or more **IRQ Link Status** register(s) is (are) set.

The bits that are read as active ('1' value) are cleared when the source of the interrupt is cleared or when the corresponding bit(s) in the **IRQ Link Enable (0x0445-0x0454)** register(s) is (are) set to 0. Writing to or reading from the **IRQ Master Status (0x0455)** register has no effect on the level of the interrupt pin.

6.2.2 IRQ Link Status and IRQ Link Enable Registers

There are sixteen **IRQ Link Status (0x0435-0x0444)** and sixteen **IRQ Link Enable (0x0445-0x0454)** registers; one of each per link. The following types of interrupts are reported (in the least significant bits of the **IRQ Link Status** registers) for each link:

- Bit 9 latched: reports the end of an LCD (Loss of Cell Delineation) condition on a RX TDM link.
- Bit 1 latched: reports an LCD (Loss of Cell Delineation) condition on a RX TDM link.

Bit 0 (LSB) is a status bit. It reports an interrupt for an overflow condition in one or more of the **24** counters associated with the link. It is also used to report an overflow condition in the UTOPIA RX FIFO associated with a TDM link in TC mode. If enabled, a counter generates an interrupt request when it overflows (i.e starts over from 0 after reaching the maximum counter value). See Section 6.1 Counter Block for more details on the operation of the counters. These 13 sources of overflow can be identified through the **IRQ Link FIFO Overflow** and **IRQ UTOPIA FIFO Overflow** status registers.

Reading the **IRQ Link Status (0x0435-0x0444)** register does not clear the source of interrupt. The bit 0 status is reset by any one of the following procedures:

- disabling (masking) the IRQ for this specific counter
- clearing the overflow status bit in the **IRQ Link TC Overflow Status (0x0410-0x041F)** registers
- disabling the interrupt in the **IRQ Link TC Overflow Enable (0x0434)** or in the corresponding Link Counter registers.

Bits 1 to 6 and 9 to 11 of the **IRQ Link Status (0x0435-0x0444)** registers are latches that report the source of an interrupt. Writing a ’0’ these bits will reset the status bit (will reset the latch). Writing ’0’ to bit 0 has no effect on the status bit.

Writing a ’1’ has no effect on the bits 0 to 6 and 9 to 11 of the **IRQ Link Status (0x0435-0x0444)** register.

Each one of these 10 interrupt sources can be enabled by writing a ’1’ in the **IRQ Link Enable (0x0445-0x0454)** registers to the bit corresponding to the interrupt source.

In some situations, an interrupt source can be masked as part of an interrupt service routine. This makes it possible to detect further interrupts of higher priority. For example, if an interrupt for a counter is received, the source of the interrupt can be masked by writing 0 to the corresponding bit and then starting a separate process outside of the Interrupt Service Routine. The independent process would read, reload and re-enable the counter to produce another interrupt service request, if necessary. At the end of this process, the enable bit in the **IRQ Link Enable (0x0445-0x0454)** register would be set to ’1’ to detect any future interrupt requests.

6.2.3 IRQ Link TC Overflow Status Registers

The **IRQ Link TC Overflow Status Registers (0x0410 - 0x041F)** report the overflow condition from any of the counters associated with the TX TDM link, the RX TDM link or the TX UTOPIA I/F. They also report the overflow condition from the level of the UTOPIA RX FIFO. The 10 interrupt sources are organized as follows:

- 1 bit (12) for the RX UTOPIA FIFO overflow
- 4 bits (11:8) for the UTOPIA Input counters
- 2 bits (7,5) for the TX TDM Link counters
- 3 bits (3:1) for the RX TDM Link counters

6.3 Microprocessor Interface Block

6.3.1 Access to the Various Registers

Since the MT90225/226 and microprocessor operate from two different clock sources, access to a MT90225/226 register is asynchronous. Data is synchronized between the MT90225/226 and the microprocessor using either direct or indirect (synchronized) methods of access.

The direct method is used during a read access whenever data does not change or data changes do not represent any problem. There is no register that clears status bits upon a read access. A write action is always required to clear a status bit.

The indirect method is identified with 'S' (indirect and need to synchronize with a ready bit) whereas the direct access is identified with a 'D' in the register tables.

6.3.2 Direct Access

Direct access registers can be written or read directly by the microprocessor, without having to use other registers. Upon a write access to the MT90225/226 internal registers, the data is stored in an internal latch and transferred to the destination register within 2.5 system clock cycles (50 nsec at 50 MHz). No specific action is required if the microprocessor provides at least 50 nsec (with Chip Select signal inactive) between 2 consecutive write accesses or between a write and a read back of the same register. If the microprocessor is faster, then consecutive accesses must be inhibited or wait state(s) introduced (this option is available on most MCUs).

6.3.3 Indirect Access

Indirect access registers cannot be accessed directly by the microprocessor. The value is transferred back and forth using registers which hold a copy of the information (data) and internal address of the register. This is required to stabilize the read value. Accessing any of the 24 bit counters is an example of this type of access. A ready bit is implemented in the **Counter Transfer Command Register (0x040F)** when the transfer is completed.

6.3.4 Clearing of Status Bits

The status bits will remain set until cleared by a specific write action from the microprocessor. Status bits are cleared by overwriting a zero to the corresponding position in the source register. Each input status register has a related interrupt enable register. When enabled, setting a bit in the interrupt enable register causes an interrupt to occur in the corresponding status register bit.

6.3.4.1 Toggle Bit

Some registers include a toggle bit. Toggle bits are used to indicate a write action to any internal register has taken place. Typically, this bit is toggled 2.5 system clock cycles after performing the write action. To use the toggle bit, its state (either 0 or 1) must be read (polled) and its state is changed (toggled) when a write command is completed. This bit is particularly useful when the processor clock is much faster than the MT90225/226 system clock.

7.0 Register Descriptions

Throughout the following register descriptions, it should be noted that only the registers and register bits corresponding to available links are meaningful. Registers and register bits corresponding to unavailable links should be masked or otherwise ignored. The MT90225 has links 0:15. The MT90226 has links 0, 2, 4, 6, 8, 10, 12 and 14.

7.1 Register Summary

Address (Hex)	Access Type	Reset Value (Hex)	Description
0x0000-0x0007	D	0000	UTOPIA Output Link Address Registers
0x0010	D	0000	UTOPIA Output Link PHY Enable Registers
0x0011	D	0000	UTOPIA Output Control Register
0x0012	D	0000	UTOPIA Output User Defined Byte
0x0040-0x0047	D	0000	UTOPIA Input Link Address Registers
0x0050	D	0000	UTOPIA Input Link PHY Enable Register
0x0052	D	000X000000 000000	UTOPIA Input Control Register
0x0053	D	0000	UTOPIA Input Parity Error Register
0x0080	D	000000001X 000000	TX Cell RAM Control Register
0x008B-0x0092	D	0101	TX UTOPIA Link FIFO Length Definition Register
0x0C0 - 0x0C7	D	0C0C	RX Link Control Registers
0x00C8	D	000C	Loss of Delineation Register
0x00C9	D	0067	Cell Delineation Register
0x00DC	D	0000	RX Link Select Register
0x00E4	D	0000	RX State Register
0x00E6	D	0000	Cell Delineation Status Register
0x0299	D	0000	Reset Register
0x0318 - 0x031F	D	0808	TX Link Control Registers
0x0402	D	0000	UTOPIA Input Cell Counter Register
0x040E	D	0000	General Status Register
0x040F	Sync	0080	Counter Transfer Command Register
0x0410 - 0x041F	D	0000	IRQ Link TC Overflow Status Registers
0x0430	D	Sync	Counter Byte 3 Register
0x0431	D	Sync	Counter Bytes 2 and 1 Register
0x0432	D	Sync	Select Counter Register
0x0433	D	0000	IRQ Master Enable Register
0x0434	D	0000	IRQ Link TC Overflow Enable Register
0x0435 - 0x0444	D	0000	IRQ Link Status Registers
0x0445 - 0x0454	D	0000	IRQ Link Enable Registers
0x0455	D	0000	IRQ Master Status Register

Table 2 - Register Summary

Address (Hex)	Access Type	Reset Value (Hex)	Description
0x0600 - 0x060F	D	0000	TDM TX Link Control Register
0x0610 - 0x061F	D	0000	TDM TX Mapping (timeslots 15:0) Register
0x0620 - 0x062F	D	0000	TDM TX Mapping (timeslots 31:16) Register
0x0630	D	0000	TXCK Status Register
0x0631	D	0000	RXCK Status Register
0x0632	D	0000	REFCK Status Register
0x0633	D	0000	TXSYNC Status Register
0x0634- 0x0635	D	0000	PLL Reference Control Register
0x0700 - 0x070F	D	0000	TDM RX Link Control Register
0x0710 - 0x071F	D	0000	TDM RX Mapping (timeslots 15:0) Register
0x0720 - 0x072F	D	0000	TDM RX Mapping (timeslots 31:16) Register
0x0730	D	0000	RXSYNC Status Register
0x0741	D	0000	RX Automatic ATM Synchronization Register

Table 2 - Register Summary (continued)

7.2 Detailed Register Description:

Address (Hex): **0x000-0x007 (8 regs)**
Direct access **1 register per 2 links. Link 0 is paired with link 8, link 1 with link 9 and so on.**
Reset Value (Hex): **0000**

Bit #	Type	Description
15:13	R	Unused. Read all 0's.
12:8	R/W	UTOPIA PHY Address of link N+8.
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of link N.

Table 3 - UTOPIA Output Link Address Registers

Address (Hex): **0x0010 (1 reg)**
Direct access **1 register to for all links.**
Reset Value (Hex): **0000**

Bit #	Type	Description
15	R/W	Enable UTOPIA PHY address of link 15. A 1 enables the PHY port address.
14	R/W	Enable UTOPIA PHY address of link 14. A 1 enables the PHY port Address.
...	...	...
1	R/W	Enable UTOPIA PHY address of link 1. A 1 enables the PHY port Address.
0	R/W	Enable UTOPIA PHY address of link 0. A 1 enables the PHY port Address.

Table 4 - UTOPIA Output Link PHY Enable Registers

Address (Hex): 0x0011 (1 reg) Direct access Reset Value (Bin): X000000000000000		
	Type	**Description**
15	R	Reserved.
14	R/W	Reserved. Write 0 for normal operation.
13	R/W	Reserved. Write 0 for normal operation.
12	R/W	Reserved. Write 0 for normal operation.
11	R/W	16/8-bit mode selection bit for the RX UTOPIA data bus. When set the RX UTOPIA interface is operating in 8-bit mode, when reset it is operating in 16-bit mode.
10	R/W	Reserved. Write 0 for normal operation.
9	R/W	Reset UTOPIA RX state machines when set to 1.
8	R/W	Reserved. Write 0 for normal operation.
7-0	R/W	Reserved. Write 0 for normal operation.

Table 5 - UTOPIA Output Control Register

Address (Hex): 0x0012 (1 reg) Direct access 1 register which contains the User Defined Byte. This byte is inserted into the sixth byte of the header when operating in sixteen-bit mode. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:12	R	Unused. Read all 0's.
11	R/W	Reserved. Write 0 for normal operation.
10	R/W	Reserved. Write 0 for normal operation.
9	R/W	Write 0 for normal operation, 1 to tristate parity.
8	R/W	Parity Bit. EVEN parity is selected when this bit is set. ODD parity is selected when this bit is cleared.
7:0	R/W	User Defined Byte. This byte is inserted into the sixth byte of the header when cells are being output in 16-bit mode.

Table 6 - UTOPIA Output User Defined Byte

Address (Hex): 0x0040-0x0047 (8 reg) Direct access 1 register per 2 links. Link 0 is paired with link 8, link 1 with link 9 and so on Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:13	R	Unused. Read all 0's.
12:8	R/W	UTOPIA PHY Address of Link N+8.

Table 7 - UTOPIA Input Link Address Registers

Address (Hex):	0x0040-0x0047 (8 reg)
Direct access	1 register per 2 links. Link 0 is paired with link 8, link 1 with link 9 and so on
Reset Value (Hex):	0000

Bit #	Type	Description
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of Link N.

Table 7 - UTOPIA Input Link Address Registers

Address (Hex):	0x0050 (1 reg)
Direct access	1 register to enable the link's input PHY address.
Reset Value (Hex):	0000

Bit #	Type	Description
15	R/W	Enable UTOPIA PHY address of link 15. A 1 enables the PHY port Address.
14	R/W	Enable UTOPIA PHY address of link 14.A 1 enables the PHY port Address.
...	...	...
1	R/W	Enable UTOPIA PHY address of link 1. A 1 enables the PHY port Address.
0	R/W	Enable UTOPIA PHY address of link 0.A 1 enables the PHY port Address.

Table 8 - Utopia Input Link PHY Enable Registers

Address (Hex):	0x0052 (1 reg)
Direct access	1 register for all the UTOPIA Input ports.
Reset Value (Hex):	000X000000000000

Bit #	Type	Description
15:14	R	Unused. Read all 0's
13	R	Reserved.
12	R/W	Parity Bit. The incoming Parity Bit is odd parity when 0, even parity when 1.
11	R/W	Reserved. Write 0 for normal operation.
10	R/W	Reserved. Write 0 for normal operation.
9	R/W	UTOPIA loopback mode indicator. When set the Tx UTOPIA will accept cells and loop these back to the Rx UTOPIA interface. The Rx UTOPIA interface will then output these cells.
8	R/W	Reserved. Write 0 for normal operation.
7	R/W	Selects between 16- and 8-bit mode for the Utopia bus. A 0 selects a 16-bit wide bus and a 1 selects an 8-bit wide bus.
6	R/W	A 1 resets the state of the Input UTOPIA Controller. Write 0 for normal operation.
5	R/W	Reserved. Write 0 for normal operation.
4	R/W	Unassigned Cell Filter. A 1 signifies that the Unassigned[a] cells coming from the ATM layer will be discarded. The Unassigned/Idle cell counter is incremented for each cell discarded.

Table 9 - UTOPIA Input Control Register

Address (Hex):	0x0052 (1 reg)	
Direct access	1 register for all the UTOPIA Input ports.	
Reset Value (Hex):	000X000000000000	
Bit #	**Type**	**Description**
3	R/W	Idle Cell Filter. A 1 signifies that the Idle[b] cells coming from the ATM layer will be discarded. The Unassigned/Idle cell counter is incremented for each cell discarded.
2	R/W	ATM Forum Polynomial. A 1 disables the addition of the ATM Forum Polynomial calculation on the HEC calculated as per I.432. A 0 means that the coset value is included in the HEC value.
1:0	R/W	HEC Verification. 11: Enable HEC error correction if 1 bit is wrong, discard cell if more than 1 bit are wrong. 10: Discard cell if HEC is wrong, no HEC correction. 01: Enable HEC error correction if 1 bit is wrong, no correction if more than 1 bit wrong, cell is not discarded if HEC is wrong. 00: No verification of HEC.

Table 9 - UTOPIA Input Control Register (continued)

a. Unassigned Cells have a fixed header corresponding to 00000000 00000000 00000000 0000xxx0.
b. Idle Cells have a fixed header corresponding to 00000000 00000000 00000000 00000001

Address (Hex):	0x0053 (1 reg)	
Direct access	1 register to contain information about parity errors on the Tx UTOPIA data bus.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15	ROL	Indicates that the parity error counter has rolled-over. This is a sticky bit which is set by the hardware and reset by the user (by writing ’0’ to this bit).
14	ROL	Indicates that at least one parity error has occurred since this register was reset. This is a sticky bit which is set by the hardware and reset by the user (by writing ’0’ to this bit.
13	W	When written with a 1 the internal TX UTOPIA Parity Error Counter value will be transferred to the lower 12 bits of this register. When written with ’0’, no transfer is done.
13	R	Reading a 1 in this register indicates that the transfer to bits 11:0 has completed. Reading a 0 indicates that the transfer is not completed yet.
12	R/W	When this bit is set the TX UTOPIA Parity Error Counter will be reset. When this bit is reset the TX UTOPIA Parity Error Counter will operate normally.
11:0	R	TX UTOPIA Parity Error Counter. These bits contain the value of the TX UTOPIA Parity Error Counter. The counter must be loaded into the register using bit 13.

Table 10 - UTOPIA Input Parity Error Register

Address (Hex):	0x0080 (1 reg)	
Direct access	Used for initialization of the internal TX Internal Cell RAM (Idle Cell)	
Reset Value (Bin):	000000001X000000	
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0’s.
7	R	Status Bit. Goes to 0 during initialization and returns to 1 on completion of initialization.

Table 11 - TX Cell RAM Control Register

Address (Hex):	0x0080 (1 reg)	
Direct access	Used for initialization of the internal TX Internal Cell RAM (Idle Cell)	
Reset Value (Bin):	000000001X000000	
Bit #	**Type**	**Description**
6	R/W	Write 1 to this bit for normal operation. Write 0 in conjunction with bit 0 to initialize the TX Cell RAM;
5	R/W	Reserved. Write 0 for normal operation.
4:1	R/W	Reserved. Write 0's for normal operation.
0	R/W	Write 0 to initialize the internal Cell RAM.

Table 11 - TX Cell RAM Control Register

Address (Hex):	0x008B-0x0092 (8 reg)	
Direct access	1 register per 2 links. Link 0 is paired with link 8, link 1 is paired with link 9 and so on.	
Reset Value (Hex):	0101	
Bit #	**Type**	**Description**
15:12	R	Unused. Read 0's.
11:8	R/W	TX UTOPIA FIFO Length for Link N+8.
7:4	R/W	Reserved. Write 0's for normal operation.
3:0	R/W	TX UTOPIA FIFO Length for Link N.

Table 12 - TX Link UTOPIA FIFO Length Definition Register

Address (Hex): 0x00C0 - 0x00C7 (8 reg) Direct access 1 register per 2 links. Link 0 is paired with link 8, link 1 with link 9 and so on. Reset Value (Hex): 0C0C		
Bit #	**Type**	**Description**
15	R/W	Reserved. Write 1 for normal operation.
14	R/W	Reserved. Write 0 for normal operation.
13	R/W	A value of 1 enables the descrambling of the cell for the link N+8.
12	R/W	When set to 1, count all USER cells for link N+8, when cleared to 0, count Idle/Unassigned cells for link N+8.
11	R/W	A value of 1 means that the Unassigned and Idle cells are discarded upon reception for the link N+8.
10	R/W	A value of 1 enables the discard option of the cells with wrong HEC. A value of 0 will disables the discard option, all the cells will be written to the receive buffer.
9	R/W	A value of 1signifies that the ATM Forum polynomial value (coset) is not to be added to the HEC before the verification. A value of 0 means that the HEC is calculated and compared (i.e. including the coset).
8	R/W	A value of 1 enables the correction of the cells with a wrong HEC. A value of 0 disable the correction of the HEC.
7	R/W	Reserved. Write 1 for normal operation.
6	R/W	Reserved. Write 0 for normal operation.
5	R/W	A value of 1 enables the descrambling of the cell for the link N.
4	R/W	When set to 1, count all USER cells for link N, when cleared to 0, count Idle/Unassigned cells for link N.
3	R/W	A value of 1 means that the Unassigned and Idle cells are discarded upon reception for the link N.
2	R/W	A value of 1 enables the discard option of the cells with wrong HEC. A value of 0 will disables the discard option, all the cells will be written to the receive buffer.
1	R/W	A value of 1signifies that the ATM Forum polynomial value (coset) is not to be added to the HEC before the verification. A value of 0 means that the HEC as per ATM Forum is calculated and compared (i.e. including the coset).
0	R/W	A value of 1 enables the correction of the cells with a wrong HEC. A value of 0 disable the correction of the HEC.

Table 13 - RX Link Control Registers

Address (Hex): 0x00C8 (1 reg) Direct access 1 reg. for all 16 cell delineation state machines Reset Value (Hex): 000C		
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R/W	Contains the number of consecutive cell periods that the CD circuit will count before the incoming ATM cell stream to be considered in LCD state. Each count will be done on a cell by cell basis. The value of this register is multiplied by 2 before being loaded in the internal counter. (The internal counter value can be from 2 to 510). Note that a value of 0 is not allowed as an LCD condition would be generated.

Table 14 - Loss of Delineation Register

Address (Hex):	0x00C9 (1 reg)
Direct access	1 register for all 16 cell delineation state machines
Reset Value (Hex):	0067

Bit #	Type	Description
15:8	R	Unused, Read all 0's.
7:4	R/W	DELTA parameter value for the Cell Delineation register. The number of consecutive cells with correct HEC to leave the PRESYNC state to go to the SYNC state. The default value is 6.
3:0	R/W	ALPHA parameter value for the Cell Delineation register. The number of consecutive cells with incorrect HEC to leave the SYNC state to go to the HUNT state. The default value is 7.

Table 15 - Cell Delineation Register

Address (Hex):	0x00DC (1 reg)
Direct access	1 register to select the link whose CD state can be read from 0x00E4 register
Reset Value (Hex):	0000

Bit #	Type	Description
15:5	R	Unused. Read all 0's.
4	R	This bit toggles after every write to the MT90225/226 device.
3:0	R/W	Selects the RX physical link number to update the cell delineation state in Rx State Register.

Table 16 - RX Link Select Register

Address (Hex):	0x00E4 (1 reg)
Direct access	The value is updated on completion of the write action in the RX Link Select register
Reset Value (Hex):	0000

Bit #	Type	Description
15:6	R	Unused. Read all 0's.
5:4	R	Reserved.
3:2	R	Reserved.
1:0	R	Cell Delineation State: 00: Hunt 01: Presync 10: Sync. 11: Reserved.

Table 17 - RX State Register

Address (Hex): 0x00E6 (1 reg) Direct access 1 register for all links. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15	R	A 1 indicates that the Cell Delineation State Machine (CD) for the link 15 is in Synchronized State. A 0 indicates that the CD for the link 15 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the CD.
14	R	A 1 indicates that the Cell Delineation State Machine (CD) for the link 14 is in Synchronized State. A 0 indicates that the CD for the link 14 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the CD.
...	...	...
1	R	A 1 indicates that the Cell Delineation State Machine (CD) for the link 1 is in Synchronized State. A 0 indicates that the CD for the link 1 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the CD.
0	R	A 1 indicates that the Cell Delineation State Machine (CD) for the link 0 is in Synchronized State. A 0 indicates that the CD for the link 0 is in not in the Synchronized State. This bit is not latched and is reflecting the current state of the CD.

Table 18 - Cell Delineation Status Register

Note 1: A software global reset of the entire MT90225/226 component can be achieved by simultaneously writing 1s to bits [7:5].

Address (Hex): 0x0299 (1 reg) Direct access 1 register for all links. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:9	R	Unused, Read all 0's.
8	R/W	Reserved. Write 0 for normal operation.
7	R/W	Write a 1 to reset the receiver[1]. 0 means no action.
6	R/W	Write a 1 to reset the transmitter[1]. 0 means no action.
5	R/W	Write a 1 to reset counters[1]. Write 0 for normal operation.
4:3	R/W	Write 00 for normal operation.
2:0	R/W	Reserved. Write 0 for normal operation.

Table 19 - Reset Register

Address (Hex): 0x0318 - 0x031F (8 reg) Direct access 1 register per 2 links, link 0 is paired with link 8, link1 with link 9 and so on. The high byte controls link 8-15 and low byte controls links 0-7 Reset Value (Hex): 0808		
Bit #	**Type**	**Description**
15	R/W	Write 1 to count all User cells sent on the TX TDM link N+8. Write 0 to count the total number of cell sent on the TX TDM link N+8.
14	R/W	Reserved. Write 0 for normal operation.
13	R/W	Coset value. A 0 will generate HEC with Coset value. When 1, Coset is not added.
12	R/W	Cell Scrambling. A 1 enables the scrambling of the cells on the link N+8.
11	R/W	Reserved. Write 1 for normal operation.
10:8	R/W	Reserved. Write 0 for normal operation.
7	R/W	Write 1 to count all User cells sent on the TX TDM link N. Write 0 to count the total number of cells sent on the TX TDM link N.
6	R/W	Reserved. Write 0 for normal operation.
5	R/W	Coset value. A 0 will generate HEC with Coset value, when 1, Coset is not added.
4	R/W	Cell Scrambling. A 1 enables the scrambling of the cells on the link N.
3	R/W	Reserved. Write 1 for normal operation.
2:0	R/W	Reserved. Write 0 for normal operation.

Table 20 - TX Link Control Registers

Address (Hex): 0x0402 (1 reg) Direct access 1 register for all links. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15	R/W	0: Count total Cells for Link 15. 1: Count only User Cells for Link 15.
14	R/W	0: Count total Cells for Link 14. 1: Count only User Cells for Link 14.
...	...	...
1	R/W	0: Count total Cells for Link 1. 1: Count only User Cells for Link 1.
0	R/W	0: Count total Cells for Link 0. 1: Count only User Cells for Link 0.

Table 21 - UTOPIA Input Cell Counter Register

Address (Hex): 0x040E (1 reg) Direct access Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:4	R	Unused. Read all 0's.
3	R/W	Set when the UTOPIA output clock is missing or too slow. This latched bit is cleared by writing a 0.
2	R/W	Set when the UTOPIA input clock is missing or too slow. This latched bit is cleared by writing a 0.
1	R/W	Overflow of 1 or more of the TX UTOPIA FIFO.
0	R/W	Set when there is no free cell in TX Cell RAM. This latched bit is cleared by writing a 0.

Table 22 - General Status Register

Address (Hex): 0x040F (1 reg) Synchronized access Reset Value (Hex): 0080		
Bit #	**Type**	**Description**
15:12	R/W	Unused. Read all 0's.
11	R/W	Reserved. Write 0 for normal operation.
10	R/W	Counter values are latched when this bit is changed from 0 to 1 and bit 9:8 are set to 11. Writing 0 has no effect.
9:8	R/W	Write 00 for normal operation without using the latch made. Write 01 to latch the counter value at every rising edge of the signal at LatchClk pin. Write 10 to latch the counter value every 8000 rising edges of the signal at LatchClk pin. Write 11 to latch the counter value every time bit 10 of this register is written to 1.
7	R/W	Write: 0 for normal operation. Read: 1 when the transfer is done, 0 when the transfer is pending.
6	R/W	Toggle bit. Toggles with every write access to MT90225/226. Write 0 for normal operation.
5	R/W	Reserved. Write 0 for normal operation. Read value is undetermined.
4	R/W	Reserved. Write 0 for normal operation.
3	R/W	Value to write to the Enable bit. 1 to enable, 0 to mask interrupt. This value is transferred when the bit 1:0 are 10.
2	R/W	0 will enable the transfer from the uP to the selected counter. 1 will enable the transfer from the selected counter to the uP.
1:0	R/W	00: Initialize all the counters with 0. 01: Initiate a read or write of the counter value. 10: Initiate a read or write of the IRQ enable counter bit. 11: Unused.

Table 23 - Counter Transfer Command Register

Address (Hex): 0x0410 - 0x041F (16 reg) Direct access 1 register per link. The RxClk and TxClk signals must be active for correct register operation Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:13	R	Unused. Read all 0's.
12	R/W	This bit is set when the RX UTOPIA FIFO associated with a link overflows. This bit is cleared by writing 0.
11	R/W	This bit is set when the UTOPIA Input counter for all cells associated with a link overflows. This bit is cleared by writing 0.
10	R/W	This bit is set when the UTOPIA Input counter for Idle Cells associated with a link overflows. This bit is cleared by writing 0.
9	R/W	This bit is set when the UTOPIA Input counter for Unassigned Cells associated with a link overflows. This bit is cleared by writing 0.
8	R/W	This bit is set when the UTOPIA Input counter for HEC Errored Cells associated with a link overflows. This bit is cleared by writing 0.
7	R/W	This bit is set when the TX TDM Link counter for all cells associated with a link overflows. This bit is cleared by writing 0.
6	R/W	This bit is set when the TX TDM Link counter for Idle Cells associated with a link overflows. This bit is cleared by writing 0.
5	R/W	Reserved. Write 0 for normal operation.
4	R/W	Reserved. Write 0 for normal operation.
3	R/W	This bit is set when the RX TDM Link counter for all cells associated with a link overflows. This bit is cleared by writing 0.
2	R/W	This bit is set when the RX TDM Link counter for Idle Cells associated with a link overflows. This bit is cleared by writing 0.
1	R/W	This bit is set when the RX TDM Link counter for HEC Errored Cells associated with a link overflows. This bit is cleared by writing 0.
0	R/W	Reserved. Write 0 for normal operation.

Table 24 - IRQ Link Overflow Status Registers

Address (Hex): 0x0430 (1 reg) Synchronized access The value in this register is used for internal access to the counter when the transfer command is issued Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:8	R	Unused. Read all 0's.
7:0	R/W	A read accesses the MSB (byte #3) of the Counter selected in the Select Counter register. A write will hold the value to be written to the selected counter.

Table 25 - Counter Byte 3 Register

Address (Hex): 0x0431 (1 reg) Synchronized access The value in this register is used for internal access to the counter when the transfer command is issued Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:0	R/W	A read accesses the byte #2 and byte #1 of the Counter that was selected in the Select Counter register. Byte 2 is in bits 15:8 and byte 1 is in bits 7:0. A write will hold the value to be written to the selected counter.

Table 26 - Counter Bytes 2 and 1 Register

Address (Hex): 0x0432 (1 reg) Synchronized access The value in this register is used for internal access to the counter when the transfer command is issued Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:9	R	Unused. Read all 0's.
8:5	R/W	The valid bit combinations are: 1011: UTOPIA Input, counter of all cells for link 1010: UTOPIA Input, counter of Idle cells for link 1001: UTOPIA Input, counter of Unassigned cells for link 1000: UTOPIA Input, counter of cells with HEC error, single or multiple bit errors 0111: TX Link, total number of cells (or User Cells) 0110: TX Link, number of Idle cells 0011: RX Link, total number of cells 0010: RX Link, number of Idle (or User Cells) 0001: RX Link, number of cells with HEC errors Other values are not valid and should not be used.
4:0	R/W	The valid bit combinations are: 01111: Link 15 01110: Link 14 ... 00000: Link 0 Other values are not valid and should not be used.

Table 27 - Select Counter Register

Address (Hex): 0x0433 (1 reg) Direct access 1 register for all 16 links Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:0	R/W	Each bit represents a link. A '1' means that the interrupt form the corresponding link is enabled and that the level of the IRQ pin is low if the corresponding bit in the IRQ Master Register is set. A'0' means that the IRQ level is not affected by the corresponding bit.

Table 28 - IRQ Master Enable Register

Address (Hex):	0x0434 (1 reg)	
Direct access	1 register to enable interrupts from the links in TC mode. The RxClk signal must be active for correct register operation	
Reset Value (Hex):	00	
Bit #	**Type**	**Description**
15:0	R/W	When set to 1, any bit set in the IRQ Link TC Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Each bit corresponds to 1 link.

Table 29 - IRQ Link TC Overflow Enable Register

Address (Hex):	0x0435 - 0x0444 (16 reg)	
Direct access	1 Status register per link	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:12	R	Unused. Read all 0's.
11	R/W	Reserved. Write 0 for normal operation.
10	R/W	Reserved. Write 0 for normal operation.
9	R/W	A '1' indicates the end of the LCD condition. Cleared by writing a '0'.
8	R	Reserved. Write 0 for normal operation.
7	R/W	Reserved. Write 0 for normal operation.
6	R/W	Reserved. Write 0 for normal operation.
5	R/W	Reserved. Write 0 for normal operation.
4	R/W	Reserved. Write 0 for normal operation.
3	R/W	Reserved. Write 0 for normal operation.
2	R/W	Reserved. Write 0 for normal operation.
1	R/W	LCD Loss of Cell Delineation. This status bit can be cleared by writing a '0' to it.
0	R	Link Counter Overflow Interrupt. One or more counters associated with the link overflowed. This status bit can be cleared only by reading or writing to the counter(s) which is (are) the source for the IRQ.

Table 30 - IRQ Link Status Registers

Address (Hex):	0x0445 - 0x0454 (16 reg)	
Direct access	1 Enable register per link Status reg	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:12	R	Unused. Read all 0's.
11:0	R/W	Each bit set to '1' will enable the generation of the interrupt when the corresponding bit in the IRQ Link Status register is set.

Table 31 - IRQ Link Enable Registers

Address (Hex):	0x0455 (1 reg)	
Direct access	1 register for all 16 links	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15:0	R	Each bit represents a link. A '1' means that the corresponding link has a valid request for interrupt. The level of the IRQ pin is controlled by the bits in this register and the corresponding bits in the IRQ Master Enable Register. A write does not have any affect on the bits in this register. The status bit is not latched and changing the mask bit in the IRQ Master Register has a direct effect on the level of the IRQ pin.

Table 32 - IRQ Master Status Register

Address (Hex):	0x0600 - 0x060F (16 reg)	
Direct access	1 reg. per TX link.	
Reset Value (Hex):	0000	
Bit #	**Type**	**Description**
15	R	Unused. Read 0.
14:10	R/W	Clock source select These 4 bits are used to select the source for the TXCK for the link: The valid combinations are: 00000: RXCK0 00001: RXCK1 00010: RXCK2 00011: RXCK3 00100: RXCK4 00101: RXCK5 00110: RXCK6 00111: RXCK7 01000: RXCK8 01001: RXCK9 01010: RXCK10 01011: RXCK11 01100: RXCK12 01101: RXCK13 01110: RXCK14 01111: RXCK15 10000: REFCK0 10001: REFCK1 10010: REFCK2 10011: REFCK3
9	R/W	Clock and sync direction When 0, TXCK and TXSYNC are outputs. When 1, TXCK and TXSYNC are inputs.
8	R/W	Remote Loopback When 1, TXCK, TXSYNC and DSTo come from the RX pins of the same link. When 0. normal mode.
7	R/W	Link enable When 0, the TX port is in high impedance mode When 1, the TX port is active
6:5	R/W	Data rate: 11: 8.192 Mb/sec. 10: 4.096 Mb/sec. 01: 2.048 Mb/sec 00: 1.544 Mb/sec
4:3	R/W	Multiplex mode select: 00: no multiplexing, 01: multiplex on a per byte basis, 2 links to 1 link. Valid only for ST-BUS mode. 10: multiplex on a per byte basis, 4 links to 1 link. Valid only for ST-BUS mode.

Table 33 - TDM TX Link Control Register

Address (Hex): 0x0600 - 0x060F (16 reg) Direct access 1 reg. per TX link. Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
2	R/W	Clock and sync format: When 0, TDM is in Generic mode: clock is 1x data rate and sync is 1 bit long at beginning of frame. When 1, TDM is ST-BUS Format: clock 2x data rate and sync as per ST-BUS format
1	R/W	Clock polarity: When 0, the data is output/sampled at the falling edge of TXCK When 1, the data is output/sampled at the rising edge of TXCK This bit is ignored in ST-BUS Format.
0	R/W	Sync polarity: When 0, the sync pulse is active low When 1, the sync pulse is active high. This bit is ignored in ST-BUS Format.

Table 33 - TDM TX Link Control Register (continued)

Address (Hex): 0x0610 - 0x061F (16 reg) Direct access Control time slot 15:0 Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:0	R/W	Each bit controls if the corresponding time slot is used to carry ATM Traffic. When not in use, the DSTo pin is in High Z mode for the corresponding time slot. This registers controls time slots 15:0.

Table 34 - TDM TX Mapping (timeslots 15:0) Register

Address (Hex):	0x0620 - 0x062F (16 reg)
Direct access	Control time slot 31:16
Reset Value (Hex):	0000

Bit #	Type	Description
15:0	R/W	Each bit controls if the corresponding time slot is used to carry ATM Traffic. When not in use, the DSTo pin is in High Z mode for the corresponding time slot. This registers controls time slots 31:16. For T1 links, bit 8 (timeslot 24) must be zero.

Table 35 - TDM TX Mapping (timeslots 31:16) Register

Address (Hex):	0x0630 (1 reg)
Direct access	1 reg. for all 16 TXCK signals
Reset Value (Hex):	0000

Bit #	Type	Description
15	R	When 1: TXCK faulty on link 15.
14	R	When 1: TXCK faulty on link 14.
...	R	....
1	R	When 1: TXCK faulty on link 1.
0	R	When 1: TXCK faulty on link 0.

Table 36 - TXCK Status Register

Address (Hex):	0x0631 (1 reg)
Direct access	1 reg. for all 16 RXCK signals
Reset Value (Hex):	0000

Bit #	Type	Description
15	R	When 1: RXCK faulty on link 15.
14	R	When 1: RXCK faulty on link 14.
...	R	....
1	R	When 1: RXCK faulty on link 1.
0	R	When 1: RXCK faulty on link 0.

Table 37 - RXCK Status Register

Address (Hex):	0x0632 (1 reg)
Direct access	1 reg. for all 4 REFCK signals
Reset Value (Hex):	0000

Bit #	Type	Description
15:4	R	Unused. Read 0's
3	R	When 1: REFCK3 faulty
2	R	When 1: REFCK2 faulty
1	R	When 1: REFCK1 faulty
0	R	When 1: REFCK0 faulty

Table 38 - REFCK Status Register

Address (Hex):	0x0633 (1 reg)
Direct access	1 reg. for all 16 RX links
Reset Value (Hex):	0000

Bit #	Type	Description
15	R/W	TXSYNC Sync signal faulty on link 15. Cleared by writing '0'.
14	R/W	TXSYNC Sync signal faulty on link 14. Cleared by writing '0'.
...	R/W	....
1	R/W	TXSYNC Sync signal faulty on link 1. Cleared by writing '0'.
0	R/W	TXSYNC Sync signal faulty on link 0. Cleared by writing '0'.

Table 39 - TXSYNC Status Register

Address (Hex):	0x0634- 0x0635 (2 reg)
Direct access	
Reset Value (Hex):	0000

Bit #	Type	Description
15:5	R	Unused. Read all 0's.
4:0	R/W	These 5 bits are used to select the source for the signal at PLLREF0: The valid combinations are: 00000: RXCK0 01000: RXCK8 10000: RXSYNC0 11000: RXSYNC8 00001: RXCK1 01001: RXCK9 10001: RXSYNC1 11001: RXSYNC9 00010: RXCK2 01010: RXCK10 10010: RXSYNC2 11010: RXSYNC10 00011: RXCK3 01011: RXCK11 10011: RXSYNC3 11011: RXSYNC11 00100: RXCK4 01100: RXCK12 10100: RXSYNC4 11100: RXSYNC12 00101: RXCK5 01101: RXCK13 10101: RXSYNC5 11101: RXSYNC13 00110: RXCK6 01110: RXCK14 10110: RXSYNC6 11110: RXSYNC14 00111: RXCK7 01111: RXCK15 10111: RXSYNC7 11111: RXSYNC15

Table 40 - PLL Reference Control Register

Address (Hex): 0x0700 - 0x070F (16 reg) Direct access 1 reg. per RX link Reset Value (Hex): 0000		
Bit #	**Type**	**Description**
15:12	R	Unused. Read 0's.
11	W	Reserved. Write 0 for normal operation.
10	R/W	Automatic ATM cell synchronization When 1: Bit mode cell delineation is performed. To be used when no RXSYNC signal is provided. Register 0x0741 must also be initialized. When 0: Byte mode cell delineation is performed. Must be used when a valid RXSYNC signal is provided.
9	R/W	Reserved. Write 0 for normal operation.
8	R/W	Digital Loopback mode When 1, loopback mode, RXCK, RXSYNC and DSTi come from the TX pins of the same link. Both TX and RX blocks operate normally. When 0, normal mode, RXCK, RXSYNC and DSTi come from the RX pins of the link
7	R/W	Link enable: 0: RX Port is not active 1: RX port is active
6:5	R/W	Data rate: 11: 8.192 Mb/sec. 10: 4.096 Mb/sec. 01: 2.048 Mb/sec 00: 1.544 Mb/sec
4:3	R/W	Multiplex mode select: 00: no demultiplexing, 01: demultiplex on a per byte basis, 1 link to 2 links. Valid only for ST-BUS mode. 10: demultiplex on a per byte basis, 1 link to 4 links. Valid only for ST-BUS mode.
2	R/W	Clock and sync format: When 0, TDM is in Generic mode: clock is 1x data rate and sync is 1 bit long at beginning of frame. When 1, TDM is ST-BUS Format: clock 2x data rate and sync as per ST-BUS format
1	R/W	Clock polarity: When 0, the data is sampled at the rising edge of RXCK. When 1, the data is sampled at the falling edge of RXCK. This bit is ignored in ST-BUS Format.
0	R/W	Sync polarity: When 0, the sync pulse is active low. When 1, the sync pulse is active high. This bit is ignored in ST-BUS Format.

Table 41 - TDM RX Link Control Register

Address (Hex):	0x0710 - 0x071F (16 reg)
Direct access	Control time slot 15:0
Reset Value (Hex):	0000

Bit #	Type	Description
15:0	R/W	Each bit controls if the corresponding time slot is used to carry ATM Traffic. When not in use, the DSTi pin is ignored for the corresponding time slot. This registers controls time slots 15:0.

Table 42 - TDM RX Mapping (timeslots 15:0) Register

Address (Hex):	0x0720 - 0x072F (16 reg)
Direct access	Control time slot 31:16
Reset Value (Hex):	0000

Bit #	Type	Description
15:0	R/W	Each bit controls if the corresponding time slot is used to carry ATM Traffic. When not in use, the DSTi pin is ignored for the corresponding time slot. This registers controls time slots 31:16. For T1 links, bit 8 (timeslot 24) must be zero.

Table 43 - TDM RX Mapping (timeslots 31:16) Register

Address (Hex):	0x0730 (1 reg)
Direct access	1 reg. for all 16 RX links
Reset Value (Hex):	0000

Bit #	Type	Description
15	R/W	RXSYNC signal faulty on link 15. Cleared by writing ’0’.
14	R/W	RXSYNC signal faulty on link 14. Cleared by writing ’0’.
...	R/W	....
1	R/W	RXSYNC signal faulty on link 1. Cleared by writing ’0’.
0	R/W	RXSYNC signal faulty on link 0. Cleared by writing ’0’.

Table 44 - RXSYNC Status Register

Address (Hex):	0x0741 (1 reg)
Direct access	1 reg. for all RX links
Reset Value (Hex):	0000

Bit #	Type	Description
15:8	R	Unused. Read 0’s.
7:0	R/W	Must write with 54 (0x36) in Bit mode cell delineation. Not used in Byte mode cell delineation.

Table 45 - RX Automatic ATM Synchronization Register

8.0 Application Notes

8.1 Connecting the MT90225/226 to Various T1/E1/J1 Framers

Many off-the-shelf T1/E1/J1 framers require the generation of a 1.544 MHz or 2.048 MHz transmit clock reference signal at an input pin. The MT9042 can generate both of these clocks and the ST-BUS back-plane signals (C4,F0). Figure 15 provides an example implementation using existing T1/E1/J1 framers and a common 2 Mbps ST-BUS backplane.

New generation Zarlink framers only require the ST-BUS 4.096 MHz (C4) clock and a Frame Pulse (F0i) at the transmit interface. An internal PLL generates the required 1.544 MHz or 2.048 MHz transmit clock.

Figure 16 provides an example implementation based on the Zarlink MT90225 and the Zarlink MT9076 framers. Each link has independent clock in ST-BUS format.

Figure 17 and Figure 18 exemplify an ATM over T1/E1 implementation supporting the asynchronous link operation mode where the TXCLK signal is provided by the T1/E1 interface. Each T1/E1 framer uses independent clock and synchronization signals. The Tx and Rx clocks and frame pulses are fully independent.

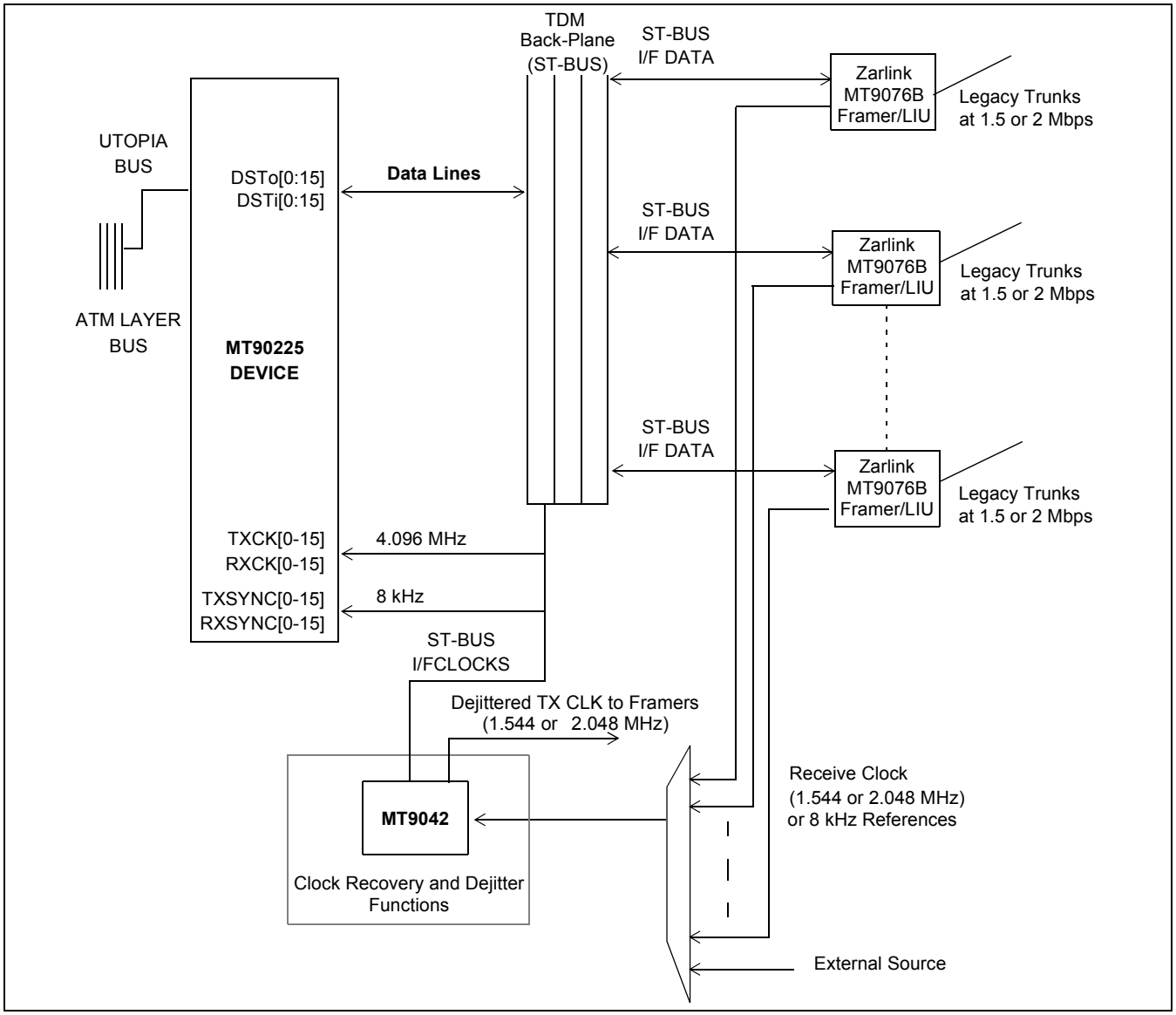


Figure 15 - MT90225 interfacing MT9076 ST-BUS mode with all links synchronous.

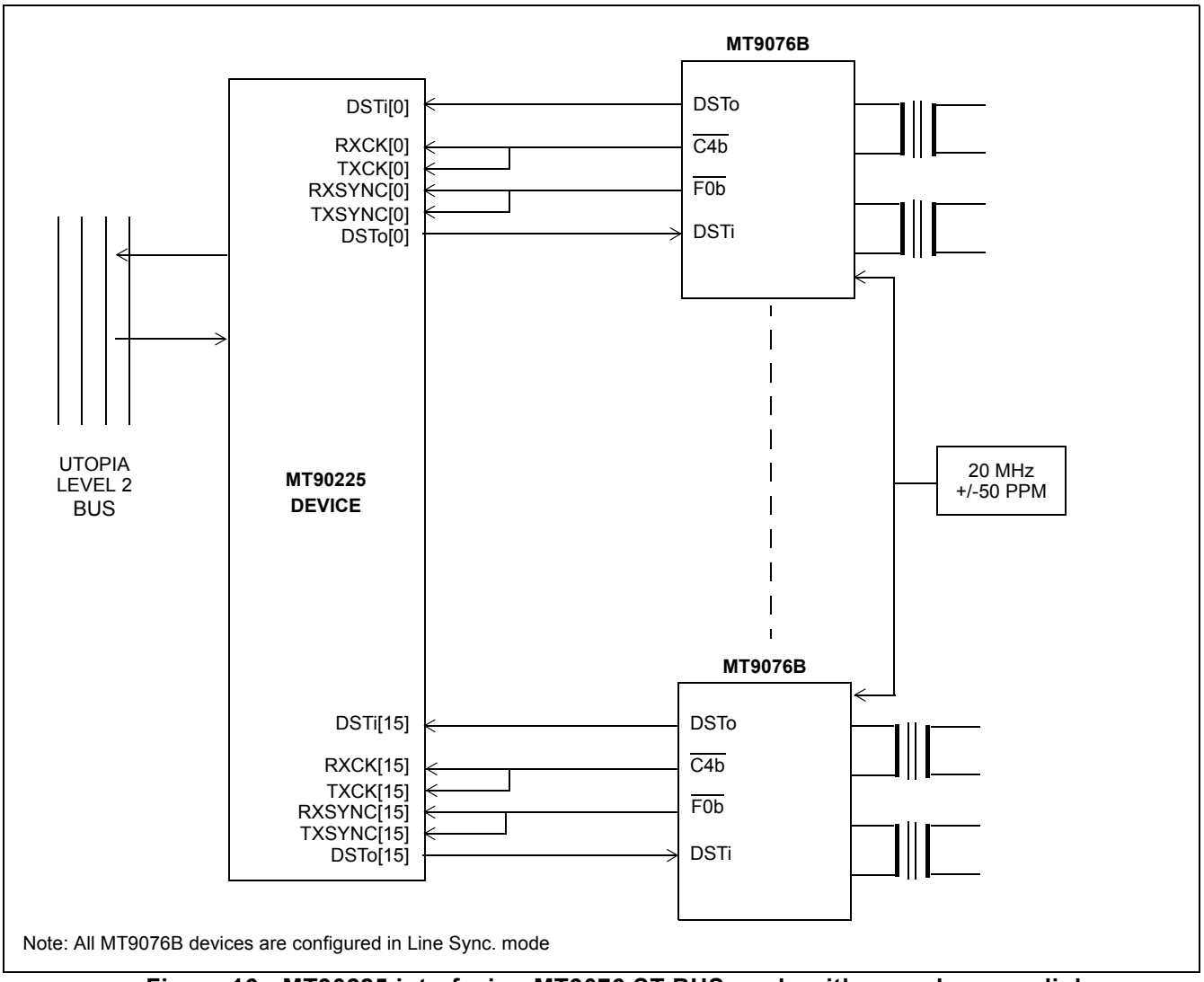


Figure 16 - MT90225 interfacing MT9076 ST-BUS mode with asynchronous links. (each link has synchronous Tx and Rx clocks)

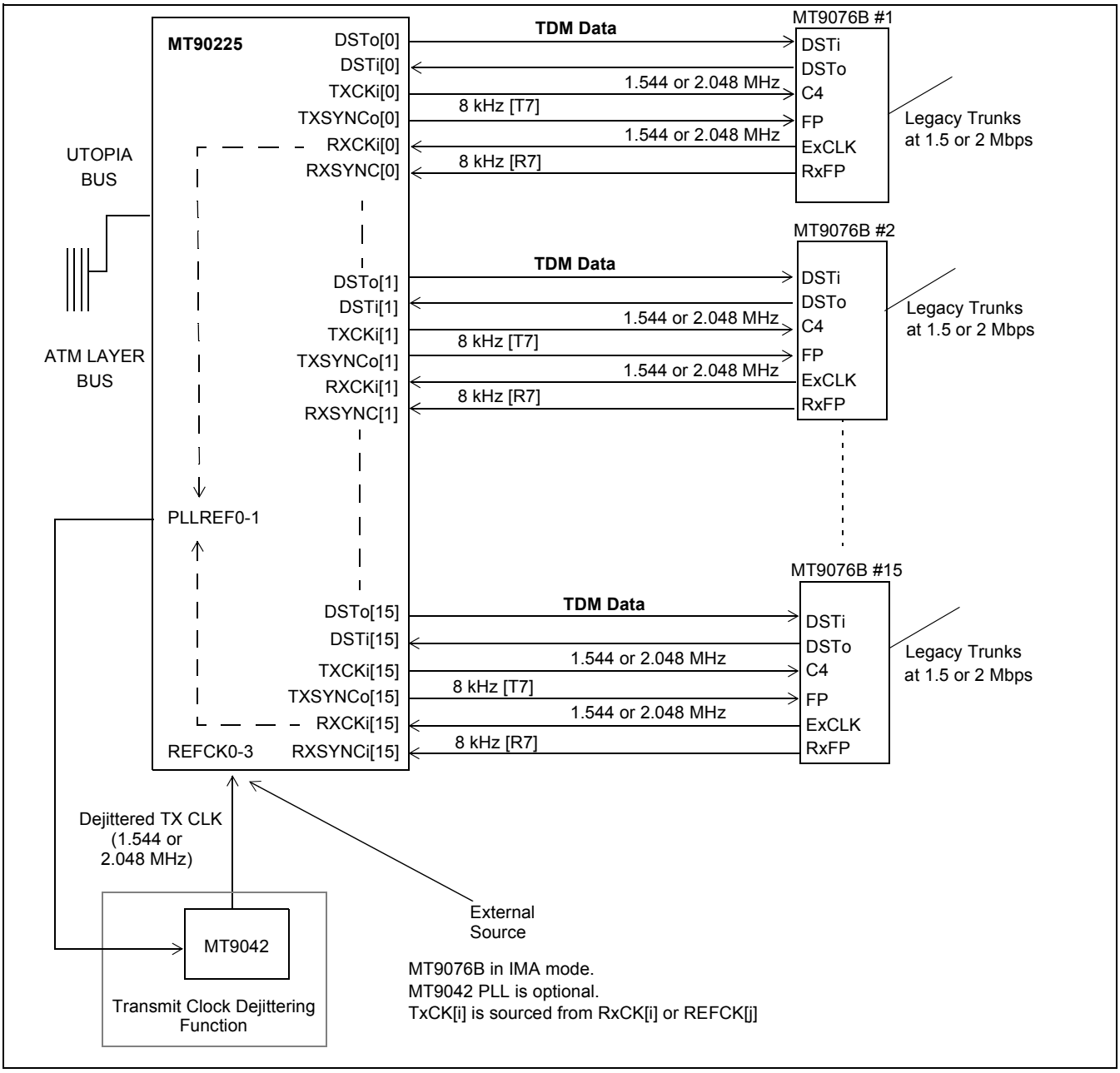
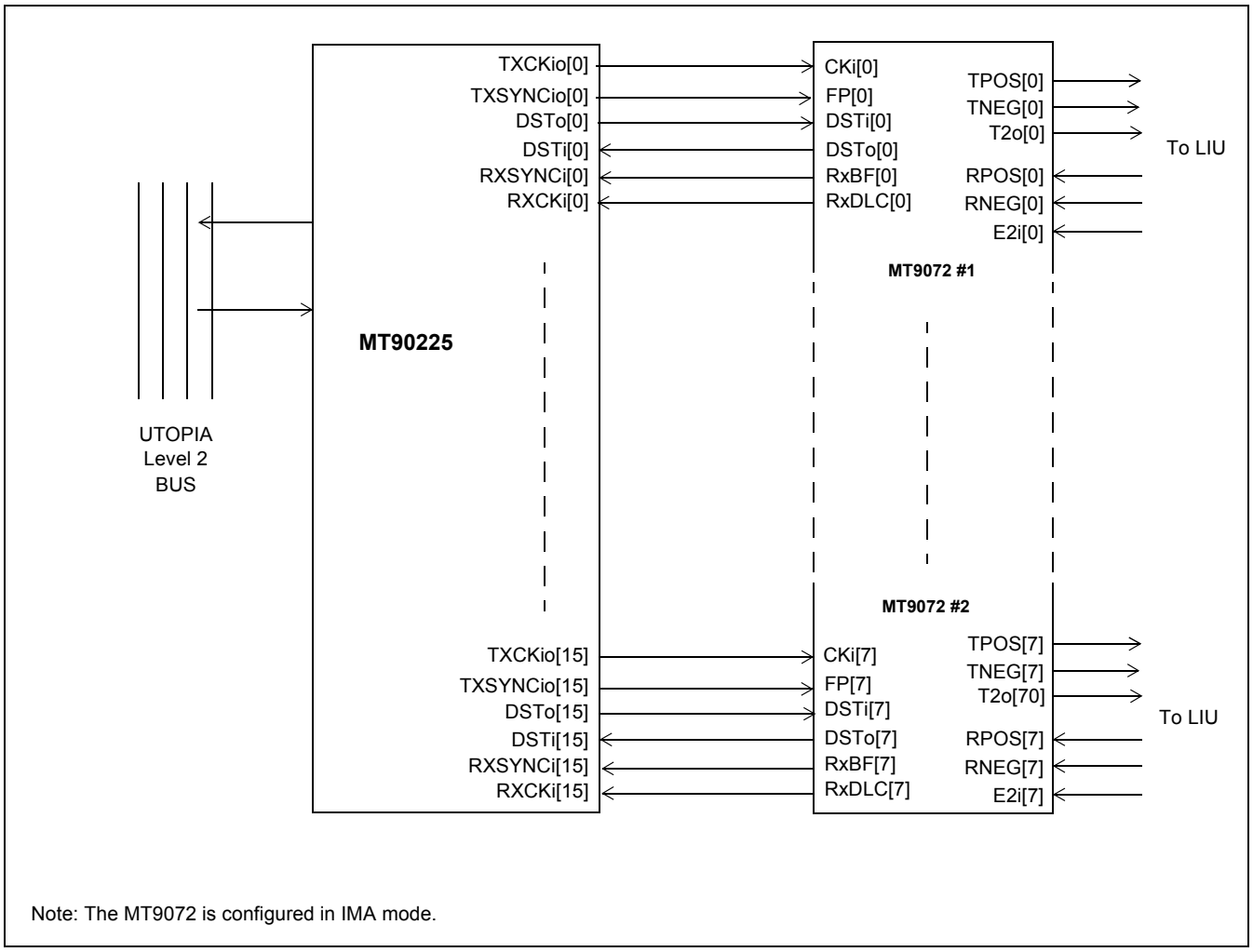


Figure 17 - MT90225 interfacing MT9076 Generic mode with asynchronous links. (each link has independent Tx and Rx clocks)



Note: The MT9072 is configured in IMA mode.

Figure 18 - MT90225 interfacing MT9072
(asynchronous links with independent Rx and Tx clocks)

9.0 AC/DC Characteristics

Absolute Maximum Conditions*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage (2.5 volt core) Supply Voltage (3.3 volt core) Supply Voltage (5.0 volt I/O)	$V_{2.5}$ $V_{3.3}$ V_{DD5}	-0.3 -0.3 -1.0	3.1 3.9 6.5	V
2	Voltage at Digital Inputs (VDD5 connected to 3.3V) Voltage at Digital Inputs (VDD5 connected to 5.0V)	$V_{I3.3}$ $V_{I5.0}$	-1.0 -1.0	3.9 6.5	V
3	Current at Digital Inputs	I_I	-10	10	µA
4	Storage Temperature	T_{ST}	-40	125	°C

* Exceeding these values may cause permanent damage. Functional Operation under these conditions is not implied.
Note: Input pins are 5 Volt compatible type

Recommended Operating Conditions - Voltages are with respect to ground (Vss) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		85	°C	
2	Supply Voltage	$V_{DD2.5}$ $V_{DD3.3}$ $V_{DD5.0}$	2.38 3.14 4.75	2.5 3.3 5.0	2.63 3.46 5.25	V	

‡ Typical figures are for design aid only.

DC Electrical Characteristics* - Voltages are with respect to ground (Vss) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current	$I_{DD2.5}$ $I_{DD3.3}$		310 29/ 20	425 133/ 80	mA	System Clock 52 MHz. TDM clock @ 2.5MHz $I_{DD3.3}$ Typical for MT90225/226 respectively with ATM traffic, no TDM Ring
2	Input High Voltage (Digital Inputs)	V_{IH}	2.0		5.5	V	When VDD5 pins connected to 5.0 VDC
3	Input Low Voltage (Digital Inputs)	V_{IL}	-0.5		0.8	V	
4	Input Leakage	I_{ILPD} I_{IL}	35 -10	115 1	222 10	µA	For pins with pull-down resistors and $V_{in} = V_{SS}$ For all remaining input pins and $V_{in} = V_{DD3.3}$ or V_{SS}
5	Input Pin Capacitance	C_{I5V} C_I			4.6 4.0	pF	5V tolerant inputs All other inputs
6	Output High Voltage (Digital Outputs)	V_{OH}	2.4		V_{DD}	V	

DC Electrical Characteristics* - Voltages are with respect to ground (Vss) unless otherwise stated. (continued)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
7	Output High Current (up_d[15:0], DSTo[15:0], TxSYNCio[15:0], TxCLK[15:0])	I_{OH}			-6	mA	Source V_{OH}=2.4 V
8	Output High Current UTOPIA	I_{OH}			-8	mA	Source V_{OH}=2.4 V
9	Output High Current (all other Digital Outputs)				-4	mA	
10	Output Low Voltage (Digital Outputs)	V_{OL}	V_{SS}		0.4	V	
11	Output Low Current (up_d[15:0], up_irq, DSTo[15:0], TxSYNCio[15:0], TxCLK[15:0])	I_{OL}	6			mA	Source V_{OL}=0.4 V
12	Output Low Current UTOPIA	I_{OL}	8			mA	Source V_{OL}=0.4 V
13	Output Low (all others)		4				
14	Output Pin Capacitance	C_{O5V} C_O			4.6 4.0	pF	For 5V tolerant outputs For all other outputs
15	High Impedance Leakage (Digital I/O)	I_{OZ}	-10	1	10	µA	V_{OH} = V_{SS} or V_{DD}

* DC Electrical Characteristics are over recommended temperature and supply voltage
‡ Typical figures are at 25°C, V_{DD}=3.3V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics - Utopia Interface Transmit Timing (≤ 50 MHz)[1]

Multi-PHY operation with up to 4 input loads of 10pF each (40 pF total)

Signal name	DIR	Item	Description	Min	Max
UTxClk	A->P	f1	TxClk frequency (nominal)	0	50 MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	2 ns
UTxData[15:0], UTxSOC, UTxEnb, UTxAddr[4:0]	A->P	tT5	Input setup to TxClk	4 ns	-
		tT6	Input hold from TxClk	1 ns	-
UTxClav[0]	A<-P	tOD	Output delay from TxClk	-	14 ns
		tT8	Output hold from TxClk	1 ns	-
		tT9	Signal going low impedance to TxClk	4 ns	-
		tT10	Signal going high impedance to TxCLK	0 ns	-
		tT11	Signal going low impedance from TxClk	1 ns	-
		tT12	Signal going high impedance from TxClk	1 ns	-

Note 1: Greater than 50MHz operation is possible with less than worst case duty cycle, jitter and rise/fall times such as 52MHz operation with 45/55% (or better) duty cycle and 2.5% (or better) jitter.

AC Electrical Characteristics - UTOPIA Interface Receive Timing (≤ 50 MHz)[1]

Multi-PHY operation with up to 4 input loads of 10pF each (40 pF total)

Signal name	DIR	Item	Description	Min.	Max.
URxClk	A->P	f1	RxClk frequency (nominal)	0	50 MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	RxClk rise/fall time	-	2 ns
URxEnb, URxAddr[4:0]	A->P	tT5	Input setup to RxClk	4 ns	-
		tT6	Input hold from RxClk	1 ns	-
URxData[15:0], URxSOC, URxClav[0], URxPAR[2]	A<-P	tOD	Output delay from RxClk	-	14 ns
		tT8	Output hold from RxClk	1 ns	-
		tT9	Signal going low impedance to RxClk	4 ns	-
		tT10	Signal going high impedance to RxClk	0 ns	-
		tT11	Signal going low impedance from RxClk	1 ns	-
		tT12	Signal going high impedance from RxClk	1 ns	-

Note 1: Greater than 50MHz operation is possible with less than worst case duty cycle, jitter and rise/fall times such as 52MHz operation with 45/55% (or better) duty cycle and 2.5% (or better) jitter.
Note 2: URxPAR is not valid for cases where URxClk low pulse is shorter than 7.9 nsec.

AC Electrical Characteristics - Utopia Interface Transmit Timing (≤ 25MHz)

Multi-PHY operation with up to 8 input loads of 10pF each (80pF total)

Signal name	DIR	Item	Description	Min.	Max.
UTxClk	A->P	f1	TxClk frequency (nominal)	0	25 MHz
		tT2	TxClk duty cycle	40%	60%
		tT3	TxClk peak-to-peak jitter	-	5%
		tT4	TxClk rise/fall time	-	4 ns
UTxData[15:0], UTxSOC, UTxEnb, UTxAddr[4:0], UTXPAR	A->P	tT5	Input setup to TxClk	10 ns	-
		tT6	Input hold from TRxClk	1 ns	-
UTxClav[0]	A<-P	tOD	Output delay from TxClk	-	27 ns
		tT8	Output hold from TxClk	1 ns	-
		tT9	Signal going low impedance to TxClk	10 ns	-
		tT10	Signal going high impedance to TxClk	0 ns	-
		tT11	Signal going low impedance from TxClk	1 ns	-
		tT12	Signal going high impedance from TRxClk	1 ns	-

AC Electrical Characteristics - UTOPIA Interface Receive Timing (≤ 25MHz)

Multi-PHY operation with up to 8 input loads of 10pF each (80pF total)

Signal name	DIR	Item	Description	Min.	Max.
URxClk	A->P	f1	RxClk frequency (nominal)	0	25 MHz
		tT2	RxClk duty cycle	40%	60%
		tT3	RxClk peak-to-peak jitter	-	5%
		tT4	RxClk rise/fall time	-	4 ns
URxEnb, URxAddr[4:0]	A->P	tT5	Input setup to RxClk	10 ns	-
		tT6	Input hold from RxClk	1 ns	-
URxData[15:0], URxSOC, URxClav[0], URXPAR	A<-P	tOD	Output delay from RxClk	-	27 ns
		tT8	Output hold from RxClk	1 ns	-
		tT9	Signal going low impedance to RxClk	10 ns	-
		tT10	Signal going high impedance to RxClk	0 ns	-
		tT11	Signal going low impedance from RxClk	1 ns	-
		tT12	Signal going high impedance from RxClk	1 ns	-

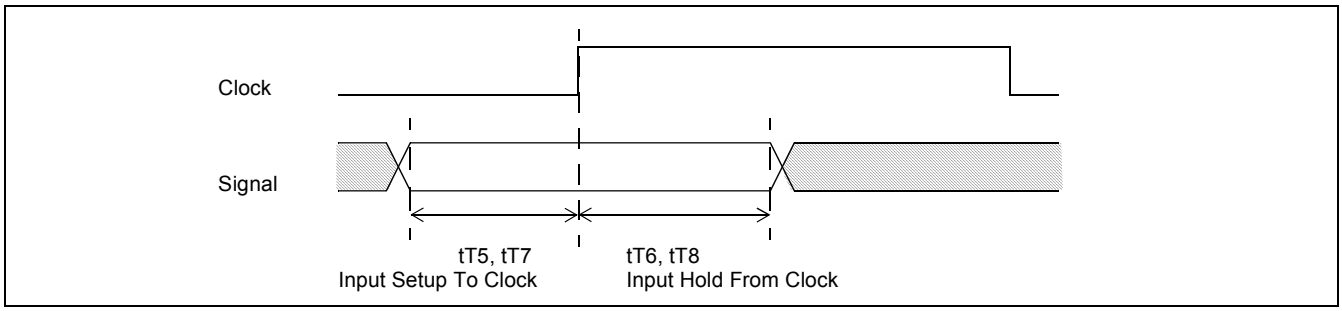


Figure 19 - Setup and Hold Time Definition

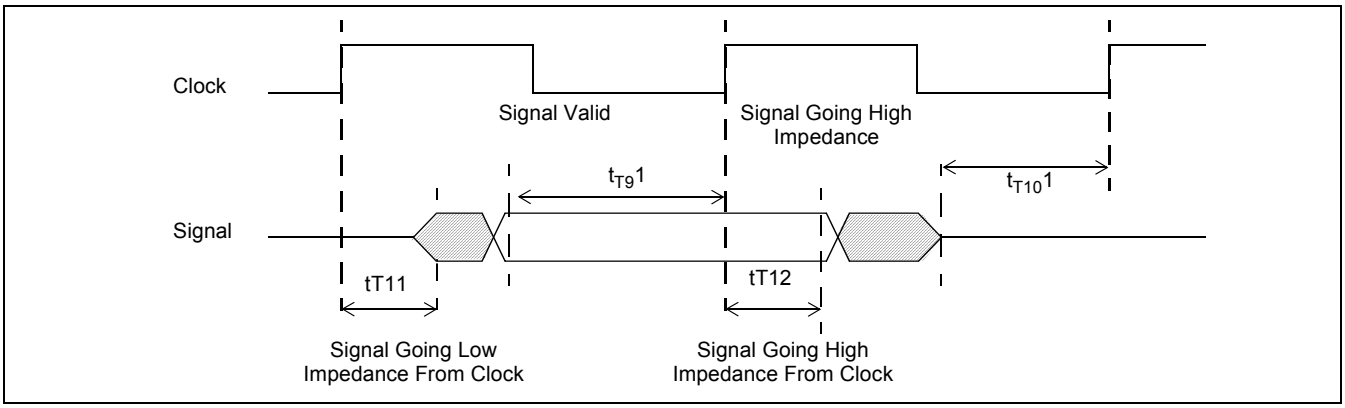


Figure 20 - Tri-State Timing

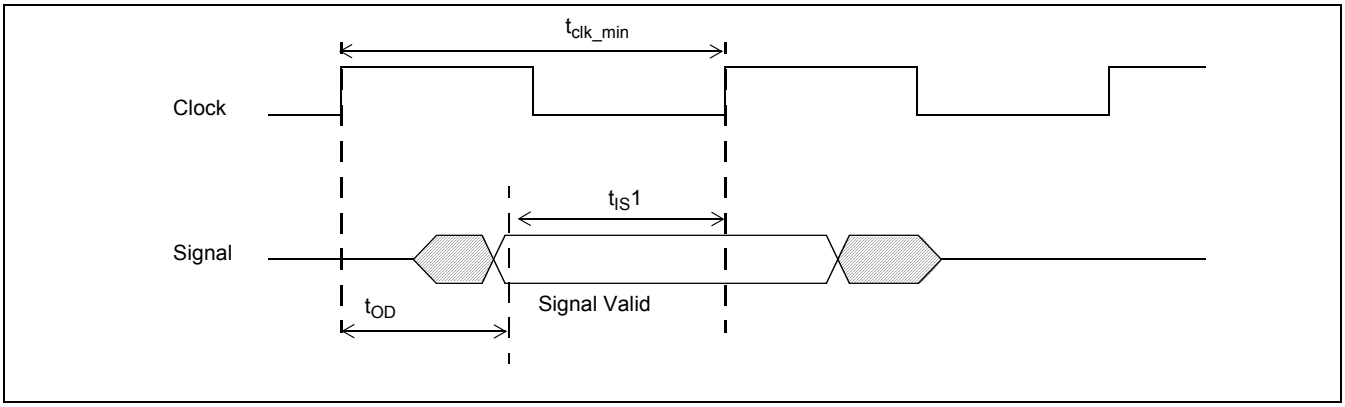


Figure 21 - Output Delay Timing

Note1: The UTOPIA specification AC Characteristics are based on the timing specification for the receiver side of a signal. In the case where the MT90225/226 is driving a signal (sending side), the input setup to the (next) clock can be derived using the worst case period of the actual clock used. t_{IS} would be equivalent to tT5 or tT7 for the device that receives the output from the MT90225/226.

$$t_{IS} = t_{clk\_min} - t_{OD}$$

9.1 CPU Interface Timing

The CPU Interface of the MT90225/226 supports both the Motorola and Intel timing modes. No Mode Select pin is required.

With Motorola devices, the Motorola R/$\overline{W}$-signal is connected to the UP_R/$\overline{W}$ pin and the $\overline{UP\_OE}$ pin is tied to ground. There is no DS signal and the $\overline{UP\_CS}$ signal is taken to access the MT90225/226.

When used with Intel devices, the READ-signal is connected to the $\overline{UP\_OE}$ pin and the WRITE-signal is connected to the UP_R/$\overline{W}$ pin.

When performing a read operation, data is placed on the bus immediately after $\overline{UP\_CS}$ is LOW UP_R/$\overline{W}$ is HIGH for the Motorola timing mode and after the $\overline{UP\_CS}$ and $\overline{UP\_OE}$ signals are LOW for Intel timing.

When performing a write operation in Motorola timing mode, the data is clocked into an MT90225/226 pre-load register on the rising edge of the UP_R/$\overline{W}$ or $\overline{UP\_CS}$ signal. In Intel timing mode, the data is clocked into MT90225/226 pre-load register on the rising edge of the UP_R/$\overline{W}$ or $\overline{UP\_CS}$ signal. Right after that transition, the data is transferred to the MT90225/226's internal register. Writing data into this register can take up 2 system clock cycles.

AC Electrical Characteristics - CPU Interface Motorola Timing - Read Cycle

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	R/W set-up time to $\overline{\text{UP\_CS}}$ falling edge	t_{WS}	1			ns	
2	Data valid after $\overline{\text{UP\_CS}}$ falling edge.	t_{ACC}			35	ns	
3	UP_AD or UP_R/$\overline{\text{W}}$ hold time after $\overline{\text{UP\_CS}}$ rising edge	t_{AH}	4			ns	
4	Data hold time after rising edge of $\overline{\text{UP\_CS}}$	t_{CH}	2			ns	
5	UP_D low impedance after falling edge of $\overline{\text{UP\_CS}}$	t_{LI}	2		20	ns	

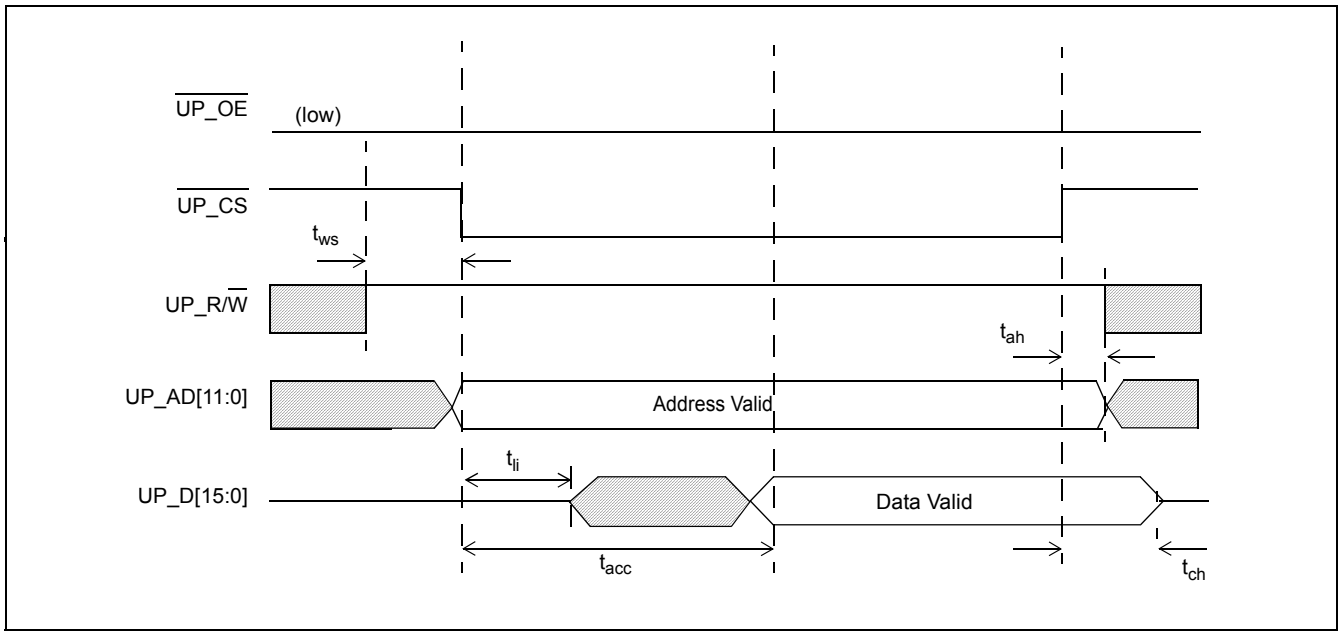


Figure 22 - CPU Interface Motorola Timing - Read Access

AC Electrical Characteristics - CPU Interface Intel Timing - Read Cycle

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	R/W set-up time to $\overline{\text{UP\_CS}}$ falling edge	t_{WS}	1			ns	
2	Data valid after both $\overline{\text{UP\_OE}}$ and $\overline{\text{UP\_CS}}$ are low.	t_{ACC}			35	ns	
3	UP_AD or UP_R/$\overline{\text{W}}$ hold time after $\overline{\text{UP\_OE}}$ rising edge	t_{AH}	4			ns	
4	Data hold time after the first rising edge of $\overline{\text{UP\_CS}}$ or $\overline{\text{UP\_OE}}$	t_{CH}	2			ns	
5	UP_D low impedance after falling edge of $\overline{\text{UP\_OE}}$	t_{LI}	2		20	ns	

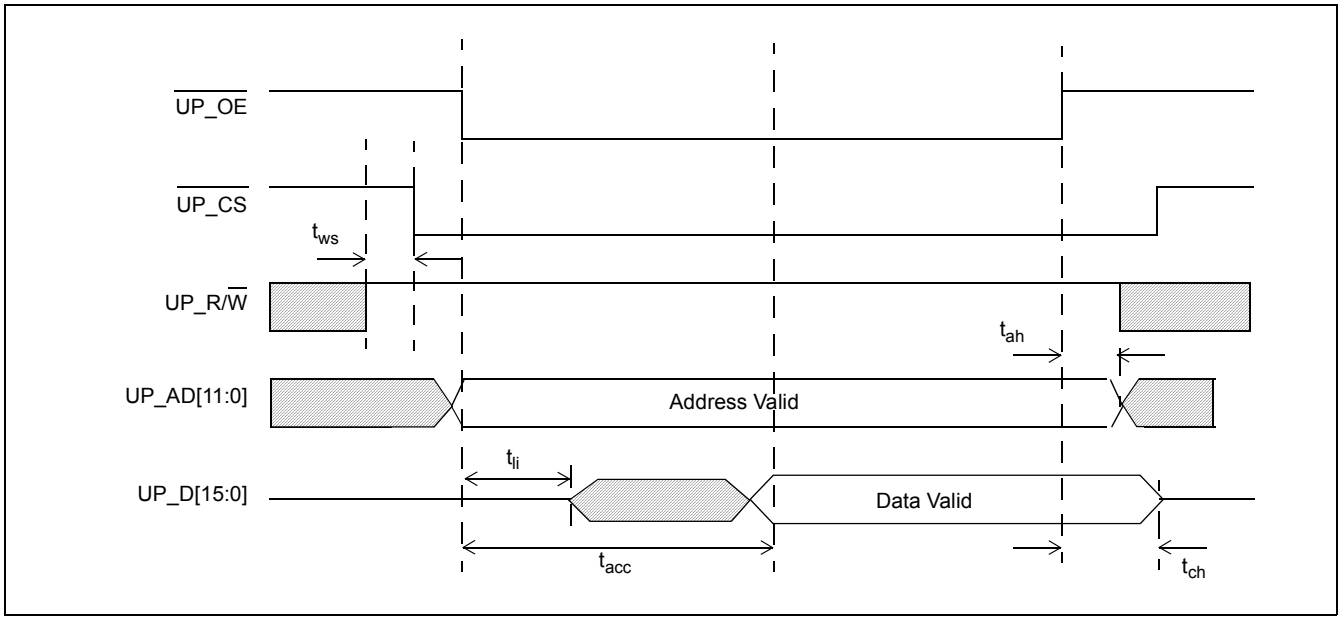


Figure 23 - CPU Interface Intel Timing - Read Access

AC Electrical Characteristics - CPU Interface Motorola Timing - Write Cycle

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	UP_R/$\overline{W}$ set-up time to $\overline{UP\_CS}$ falling edge	t_{WS}	1			ns	
2	Address and Data set up before rising edge of $\overline{UP\_CS}$	t_{SU}	10			ns	
3	UP_AD and Data hold time after $\overline{UP\_CS}$ rising edge	t_{ADH}	4			ns	
4	UP_R/$\overline{W}$ low after rising edge or $\overline{UP\_CS}$	t_{WH}	1			ns	
5	$\overline{UP\_CS}$ high before next $\overline{UP\_CS}$ low	t_{CSH}	2 (see Note 1)			cycle system clock	

Note 1 - For internal synchronization purposes, 2 system clock cycles are required between a write access and the next valid access.

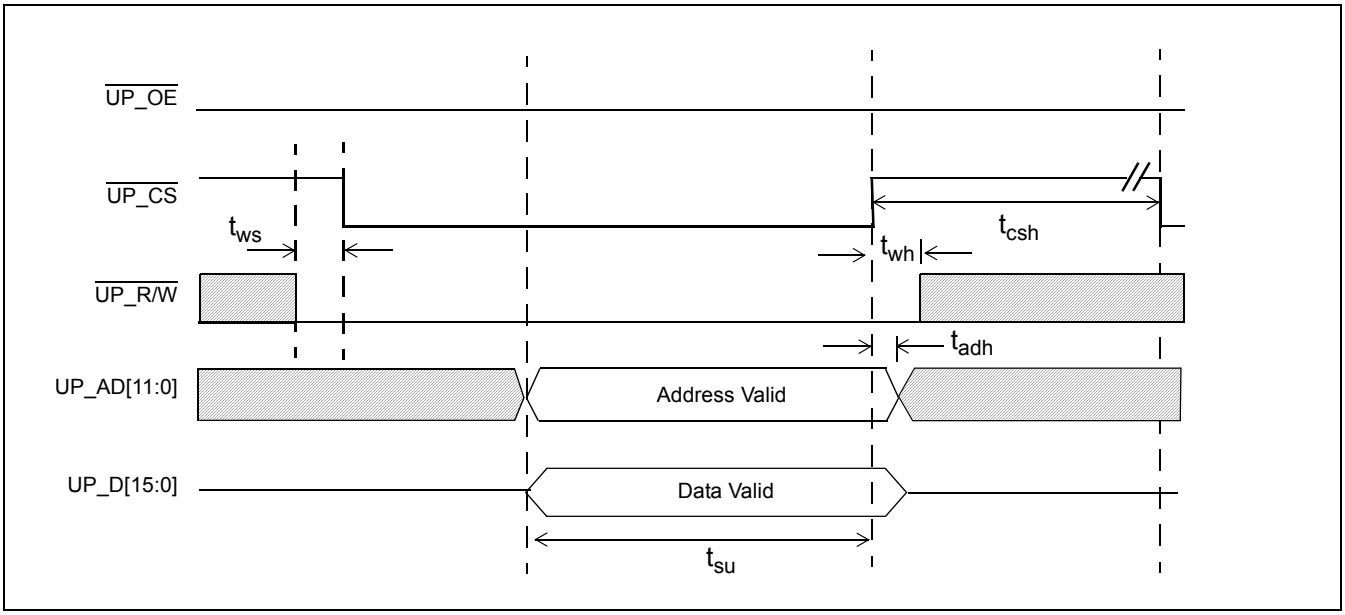


Figure 24 - CPU Interface Motorola Timing - Write Access

AC Electrical Characteristics - CPU Interface Intel Timing - Write Cycle

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	$\overline{UP\_CS}$ set-up time to UP_R/$\overline{W}$ falling edge	t_{WS}	1			ns	
2	Address and Data set up before rising edge of UP_R/$\overline{W}$	t_{SU}	10			ns	
3	UP_AD, $\overline{UP\_CS}$ and Data hold time after UP_R/$\overline{W}$ rising edge	t_{ADH}	4			ns	
4	UP_R/$\overline{W}$ low after rising edge or $\overline{UP\_CS}$	t_{CSH}	1			ns	
5	$\overline{UP\_CS}$ high before next $\overline{UP\_CS}$ low	t_{WH}	2 (see Note 1)			cycle system clock	

Note 1 - For internal synchronization purposes, 2 system clock cycles are required between a write access and the next valid access.

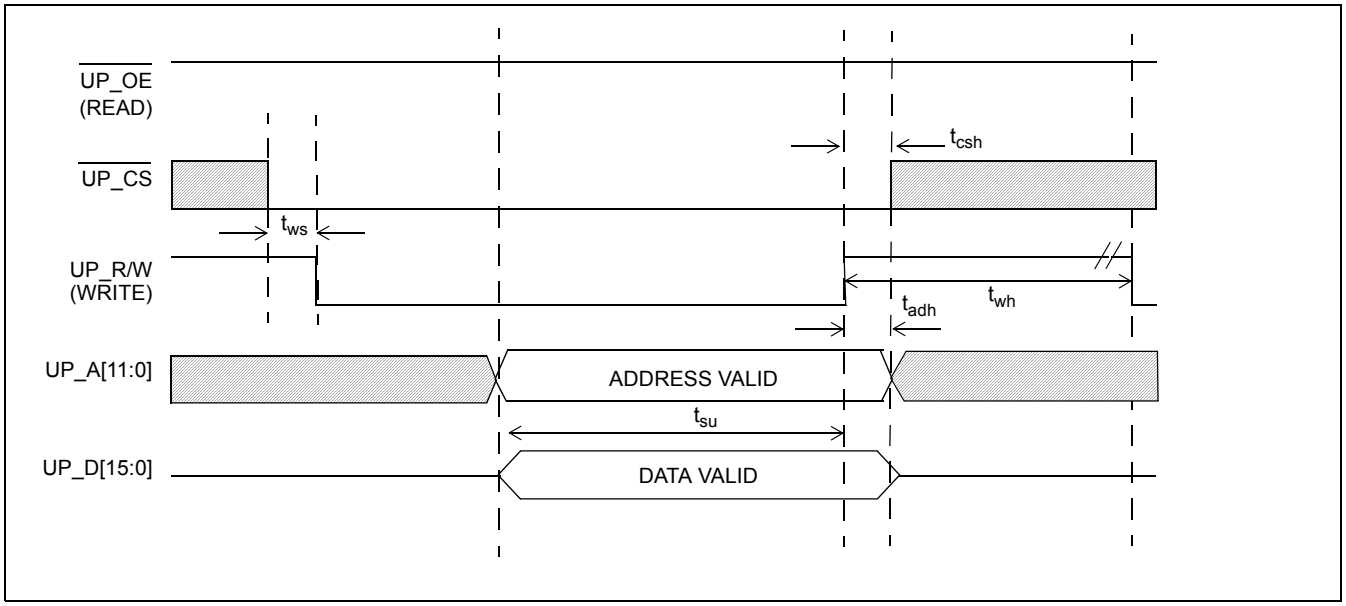


Figure 25 - CPU Interface Intel Timing - Write Access

AC Electrical Characteristics - Frame Pulse and CLK

	Characteristic	Sym	Min	Typ	Max	Units	Notes
1	Frame pulse width (ST-BUS, Generic) Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{FPW}	 26 26 26			 ns ns ns	Max width is one clock period.
2	Frame Pulse Setup Time (ST-BUS or Generic)	t_{FPS}	5			ns	
3	Frame Pulse Hold Time (ST-BUS or Generic)	t_{FPH}	10			ns	
4	Frame Pulse Output Delay	t_{FOD}			25	ns	C_L=150pF
5	CLK Period Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CP}	 190 110 55		 300 150 70	 ns ns ns	
6	CLK Pulse Width High Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CH}	 85 50 20		 150 75 40	 ns ns ns	
7	CLK Pulse Width Low Bit rate = 2.048 Mb/s Bit rate = 4.096 Mb/s Bit rate = 8.192 Mb/s	t_{CL}	 85 50 20		 150 75 40	 ns ns ns	
8	Clock Rise/Fall Time	t_r, t_f			10	ns	

AC Electrical Characteristics - Serial Streams for ST-BUS and Generic Interface

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
1	Sti Set-up Time	t_{SIS}	5			ns	
2	Sti Hold Time	t_{SIH}	10			ns	
3	Sto Delay - Active to Active	t_{SOD}			25	ns	C_L=150pF
4	STo delay - Active to High-Z	t_{DZ}			25		C_L=150pF
5	STo delay - High-Z to Active	t_{ZD}			25		C_L=150pF
6	Output Driver Enable (ODE) Delay	t_{ODE}			25	ns	C_L=150pF

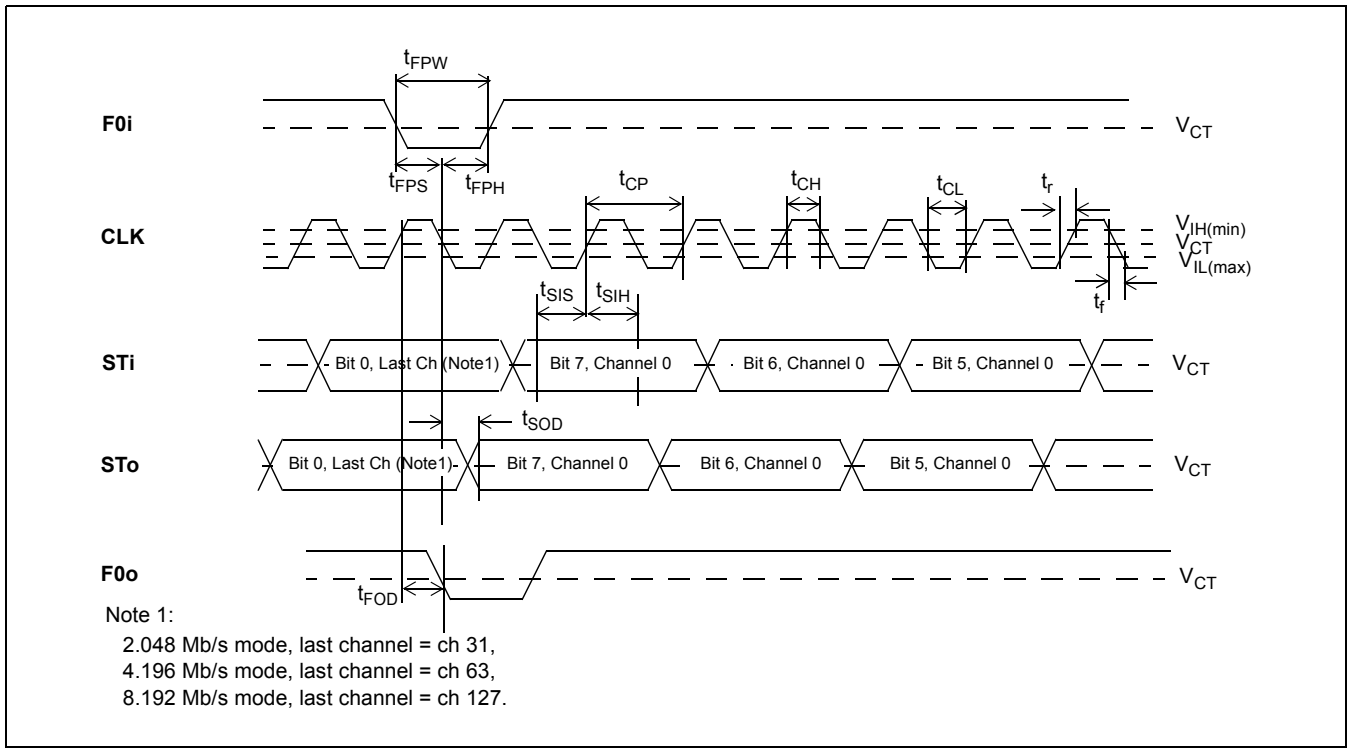
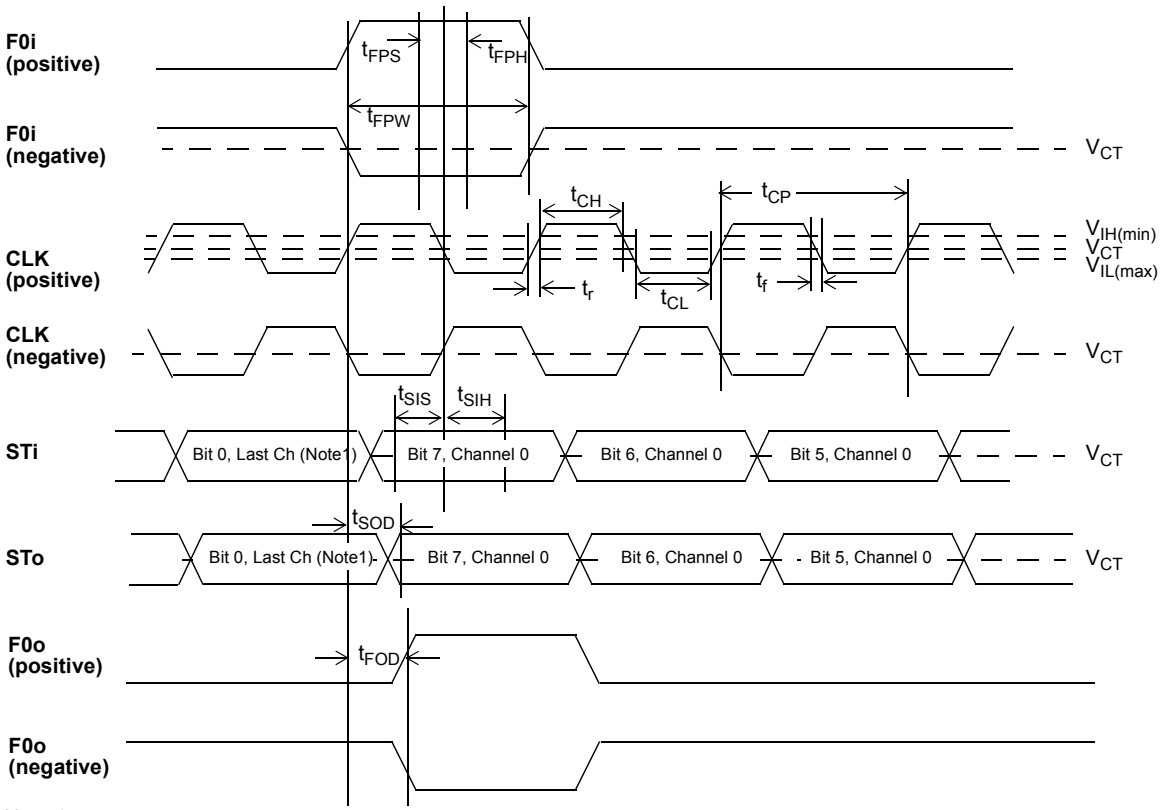


Figure 26 - ST-BUS Timing



Note 1:
2Mb/s mode, last channel = ch 31,
4Mb/s mode, last channel = ch 63,
8Mb/s mode, last channel = ch 127

Figure 27 - Generic Bus Timing

AC Electrical Characteristics - JTAG Port and RESET Pin Timing

Parameter	Symbol	Min	Typ‡	Max	Units	Test Conditions
TCK period width	t_{TCLK}	100			ns	BSDL spec's 12 MHz
TCK period width LOW	t_{TCLKL}	40			ns	
TCK period width HIGH	t_{TCLKH}	40			ns	
TDI setup time to TCK rising	t_{DISU}	2			ns	
TDI hold time after TCK rising	t_{DIH}	33			ns	
TMS setup time to TCK rising	t_{MSSU}	2			ns	
TMS hold time after TCK rising	t_{MSH}	5			ns	
TDO delay from TCK falling	t_{DOD}			20	ns	C_L = 30 pF
$\overline{TRST}$ pulse width	t_{TRST}	15			ns	
RESET pulse width	t_{RST}	2			ms	70 MCLK cycles

Note ‡: Typical figures are at 25°C, V_{DD}=3.3V, and for design aid only: not guaranteed and not subject to production testing

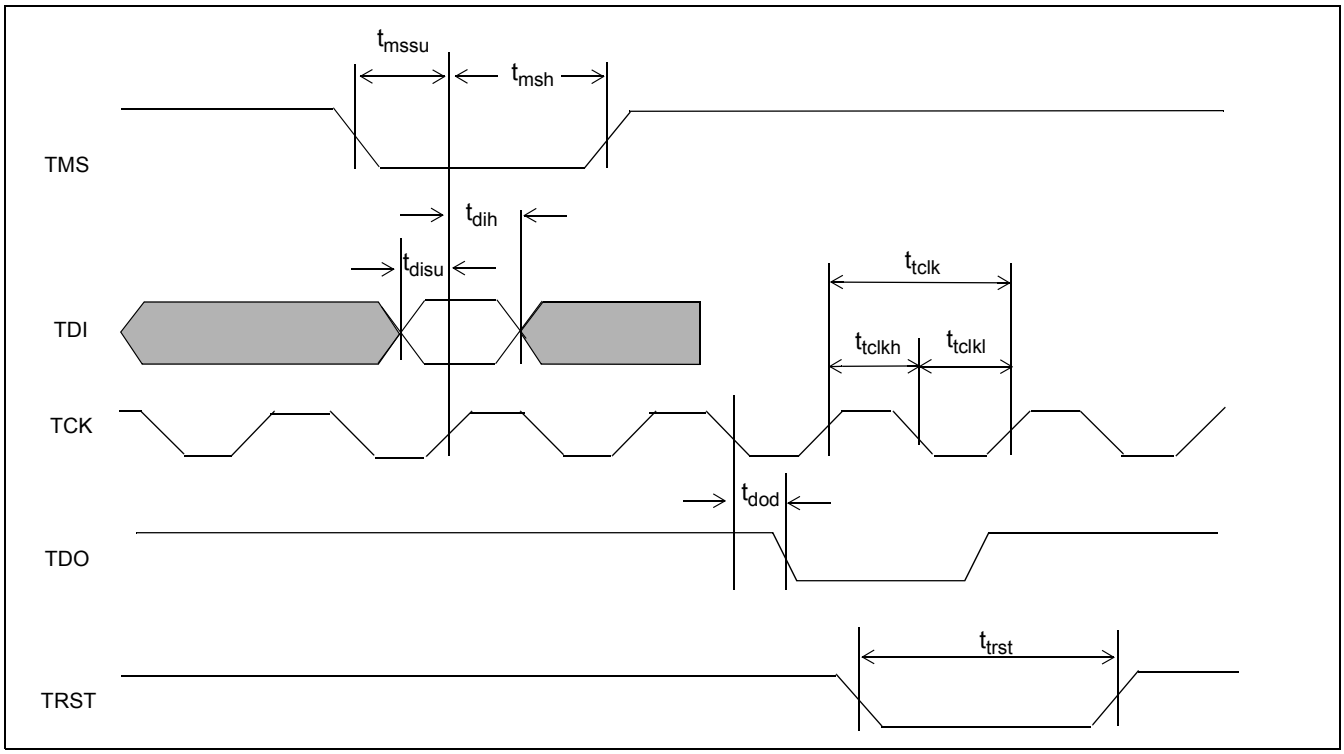


Figure 28 - JTAG Port Timing

AC Electrical Characteristics - System Clock and Reset

Parameter	Symbol	Min	Typ‡	Max	Units	Test Conditions
CLK period width	t_{CLK}	19	20	20	ns	for full operation of TDM Ring, could be longer
CLK period width LOW	t_{CLKL}		10		ns	
CLK period width HIGH	t_{CLKH}		10		ns	
CLK rising	t_{CLKR}			1.2	ns	
CLK falling	t_{CLKF}			1.2	ns	
$\overline{\text{RESET}}$ pulse width	t_{RST}	10			clk period	

Note ‡: Typical figures are at 25°C, V_{DD}=3.3V, and for design aid only: not guaranteed and not subject to production testing

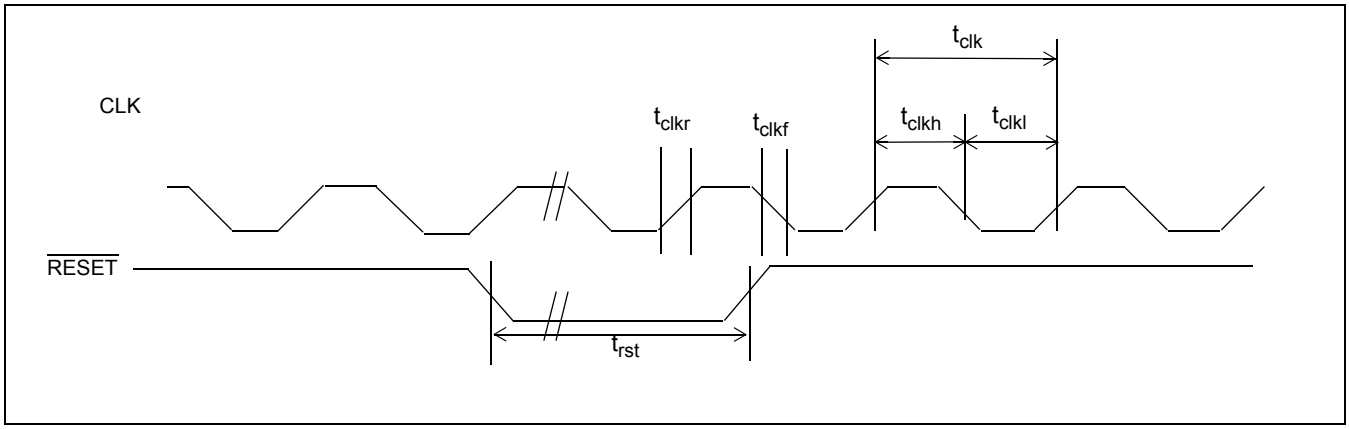


Figure 29 - System Clock and Reset

10.0 List of Abbreviations and Acronyms

AAL	ATM Adaptation Layer
ATM	Asynchronous Transfer Mode
CBR	Constant Bit Rate
CDV	Cell Delay Variation
CPE	Customer Premises Equipment
CRC	Cyclic Redundancy Check
DSU	Data Service Unit
FE	Far End
HEC	Header Error Control
I/F	Interface
IMA	Inverse Multiplexing for ATM
ISDN	Integrated Services Digital Network
LCD	Loss of Cell Delineation
LID	Link Identification
LOF	Loss Of Frame
LOS	Loss of Signal
MIB	Management Information Base
MVIP	Multi-Vendor Integration Protocol
NE	Near End
OCD	Out of Cell Delineation (anomaly)
PDH	Plesiochronous Digital Hierarchy
PHY	Physical Layer
PMD	Physical Medium Dependent
QoS	Quality of Service
RAI	Remote Alarm Indication
RDI	Remote Defect Indication
RFI	Remote Failure Indication
SAR	Segmentation and Reassembly
SOC	Start of Cell
TC	Transmission Convergence
UTOPIA	Universal Test and Operations Physical Interface for ATM
UNI	User Network Interface

11.0 ATM Glossary

Asynchronous Transfer Mode Adaptation Layer (AAL) - Standardized protocols used to translate higher layer services from multiple applications into the size and format of an ATM cell. Individual protocols are indexed as per the examples below:

AAL0 - Native ATM cell transmission proprietary protocol featuring 5-byte header and 48-byte user payload.

AAL1 - Used for the transport of constant bit rate, time-dependent traffic (e.g. voice, video); requires transfer of timing information between source and destination; maximum of 47-bytes of user data permitted in payload as an additional header byte is required to provide sequencing information.

AAL5 - Usually used for the transport of variable bit rate, delay-tolerant data traffic and signalling which requires little sequencing or error-detection support.

Active - This is a link state indicating the link is capable of passing ATM Layer cells in the specified direction.

Asynchronous 1. Not synchronous; not periodic.
2. The temporal property of being sourced from independent timing references, having different frequencies and no fixed phase relationship
3. In telecommunications, data which is not synchronized to the public network clock.
4. The condition or state of being unable to determine exactly when an event will transpire prior to its occurrence.

Asynchronous Transfer Mode (ATM) - A method of organizing information to be transferred into fixed-length cells; asynchronous in the sense that the recurrence of cells containing information from an individual user is not necessarily periodic.

Note: Although ATM cells are transmitted synchronously to maintain the clock between sender and receiver, the sender transmits data cells on an as available basis and transmits empty cells when idle. The sender is not limited to transmitting data every Nth cell.

Cell - Fixed-size information package consisting of 53 bytes (octets) of data; of these, 5 bytes represent the cell header and 48 bytes carry the user payload and required overhead.

Cell Delay Variation (CDV) - a QoS parameter that measures the peak-to-peak cell delay through the network; results from buffering and cell scheduling.

Constant Bit Rate - An ATM service category supporting a constant or guaranteed rate, with timing control and strict performance parameters. Used for services such as voice, video, or circuit emulation.

Header Error Control (HEC) - ATM equipment (usually the PHY) uses the fifth octet in the ATM cell header to check for an error and correct the contents of the header; CRC algorithm allows for single-error correction and multiple-error detection.

I.363 - ITU-T Recommendation specifying the AALs for B-ISDN.

Isochronous - The temporal property of an event or signal recurring at known periodic time intervals (e.g. 125 µs). Isochronous signals are dependent on some uniform timing, or carry their own timing information embedded as part of the signal. Examples are DS-1/T1 and E1. From the root words, “iso” meaning equal, and “chronous” meaning time.

ITU-T - International Telecommunications Union Telecommunications Standards Sector.

Loss of Cell Delineation (LCD) - The LCD defect is reported when the ***OCD*** anomaly persists for the period of time specified in ITU-T Recommendation I.432(30)¸. The LCD defect is cleared when the OCD anomaly has not been detected for the period of time specified in ITU-T Recommendation I.432.

Multi-Vendor Integration Protocol (MVIP) - MVIP standards are designed to support the inter-operability of products from different manufacturers and the portability of computer software between products from different manufacturers with the goal of facilitating new and improved applications of computer and communications equipment.

Out of Cell Delineation (OCD) Anomaly - As specified in ITU-T Recommendation I.432(30), an OCD anomaly is reported when ALPHA consecutive cells with incorrect HEC are received. It ceases to be reported when DELTA consecutive cells with correct HEC are received.

Plesiochronous - The temporal property of being arbitrarily close in frequency to some defined precision. Plesiochronous signals occur at nominally the same rate, any variation in rate being constrained within specific limits. Since they are not identical, over the long term they will be skewed from each other. This will force a switch to occasionally repeat or delete data in order to handle buffer under-flow or overflow. (In telecommunications, this is known as a frame slip).

Physical Layer (PHY) - Bottom layer of the ATM Reference Model; provides ATM cell transmission over the physical interfaces that interconnect the various ATM devices.

Quality of Service (QoS) - ATM performance parameters that characterize the transmission quality over a given VC (e.g cell delay variation; cell transfer delay, cell loss ratio).

Synchronous 1. The temporal property of being sourced from the same timing reference. Synchronous signals have the same frequency, and a fixed (often implied to be zero) phase offset.

2. A mode of transmission in which the sending and receiving terminal equipment are operating continually at the same rate and are maintained in a desired phase relationship by an appropriate means.

Universal Test and Operations Physical Interface for ATM (UTOPIA) - A PHY-level interface to provide connectivity between ATM components.

Virtual Channel (VC) - One of several logical connections defined within a virtual path (VP) between two ATM devices; provides sequential, unidirectional transport of ATM cells. Also *Virtual Circuit*.

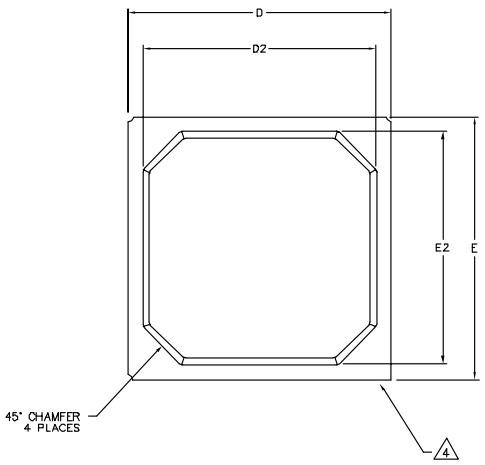
Glossary References:

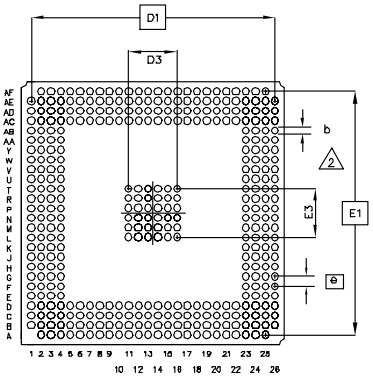
The ATM Glossary - ATM Year 97 - Version 2.1, March 1997

The ATM Forum Glossary - May 1997

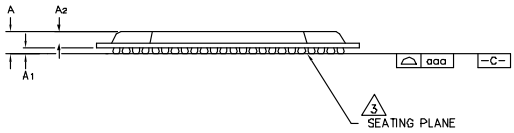
ATM and Networking Glossary
(http://www.techguide.com/comm/index.html)

Mitel Semiconductor Glossary of Telecommunications Terms - May 1995.





SYMBOL	CONTROL DIMENSIONS (mm)			NOTE
	MIN.	NOM.	MAX.	
A	1.78	2.03	2.28	
A_1	0.40	0.50	0.60	
A_2	1.10	1.17	1.25	
D	26.80	27.00	27.20	
D_1	25.00 BSC			
D_2	23.00	24.00	25.00	
D_3	5.00 BSC			
E	26.80	27.00	27.20	
E_1	25.00 BSC			
E_2	23.00	24.00	25.00	
E_3	5.00 BSC			
b	0.50	0.60	0.70	2
e	1.00 BSC			
aaa	–	–	0.20	
N	384			
	CONFORMS TO JEDEC MS-034			



NOTES: –

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C- .
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, AND MAY CONSIST OF INK, LASER MARK OR METALLIZED MARKING BUT WILL BE IN THIS CORNER INDICATED

ISSUE	1	2	3	
ACN	213450	213454	214264	
DATE	20Sep02	23Sep02	24Apr03	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code GA

Package Outline for
384 Ball PBGA (27 x 27mm)

GPD00798

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