18Mb SYNCBURST™ SRAM

MT58L1MY18F, MT58V1MV18F, MT58L512Y32F, MT58V512V32F, MT58L512Y36F, MT58V512V36F
3.3V VDD, 3.3V or 2.5V I/O; 2.5V VDD, 2.5V I/O

Features

- Fast clock and OE# access times
- Single 3.3V ±5 percent or 2.5V ±5 percent power supply
- Separate 3.3V±5 percent or 2.5V ±5 percent isolated output buffer supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual byte write control and global write
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os, and control signals
- Internally self-timed write cycle
- Burst control (interleaved or linear burst)
- Low capacitive bus loading

Options

Options	TQFP Marking
• Timing (Access/Cycle/MHz)	
6.8ns/7.5ns/133 MHz	-6.8
7.5ns/8.8ns/113 MHz	-7.5
8.5ns/10ns/100 MHz	-8.5
10ns/15ns/66 MHz	-10
• Configurations	
3.3V VDD, 3.3V or 2.5V I/O	
1 Meg x 18	MT58L1MY18F
512K x 32	MT58L512Y32F
512K x 36	MT58L512Y36F
2.5V VDD, 2.5V I/O	
1 Meg x 18	MT58V1MV18F
512K x 32	MT58V512V32F
512K x 36	MT58V512V36F
• Packages	
100-pin TQFP	T
165-ball, 13mm x 15mm FBGA	F[1]
• Operating Temperature Range	
Commercial (0ºC ≤ T_A ≤ +70ºC)	None
Industrial (-40ºC ≤ T_A ≤ +85ºC)	IT[2]

NOTE:
1. A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/numberguide.
2. Contact factory for availability of Industrial Temperature devices.

Figure 1: 100-Pin TQFP
JEDEC-Standard MS-026 BHA (LQFP)

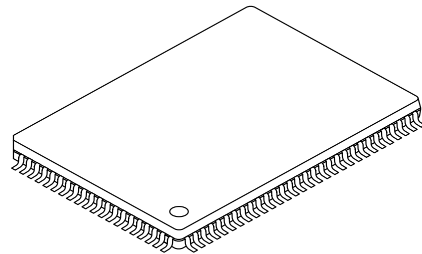
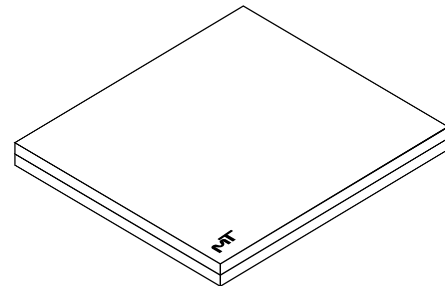


Figure 2: 165-Ball FBGA
JEDEC-Standard MO-216 (Var. CAB-1)



Part Number Example:
MT58L512Y36FT-10

General Description

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 18Mb SyncBurst SRAMs integrate a 1 Meg x 18, 512K x 32, or 512K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2#, CE2), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#), and global write (GW#).

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Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data out (Q) is enabled by OE#. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed write cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins/balls and DQPa; BWb# controls DQb pins/balls and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins/balls and DQPa; BWb# controls DQb pins/balls and DQPb; BWc# controls DQc pins/balls and DQPc; BWd# controls DQd pins/balls and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

The device is ideally suited for 486, Pentium®, 680x0 and PowerPC systems and those systems that benefit from a wide synchronous data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64-, and 72-bit-wide applications.

Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

Dual Voltage I/O

The 3.3V VDD device is tested for 3.3V and 2.5V I/O function. The 2.5V VDD device is tested for only 2.5V I/O function.

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Figure 3: Functional Block Diagram 1 Meg x 18

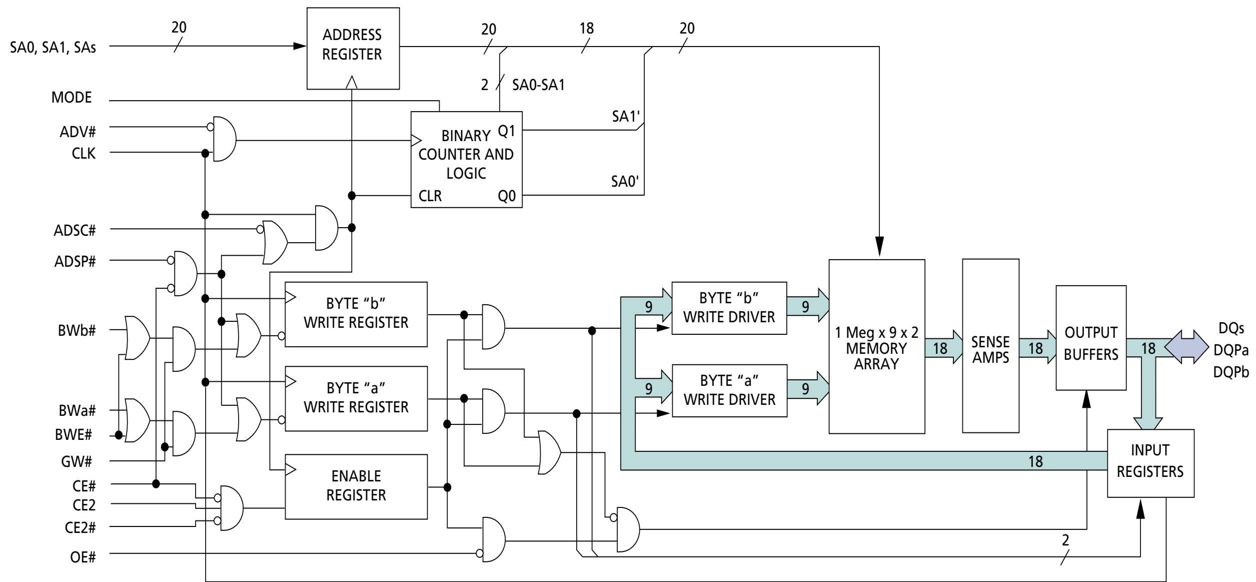
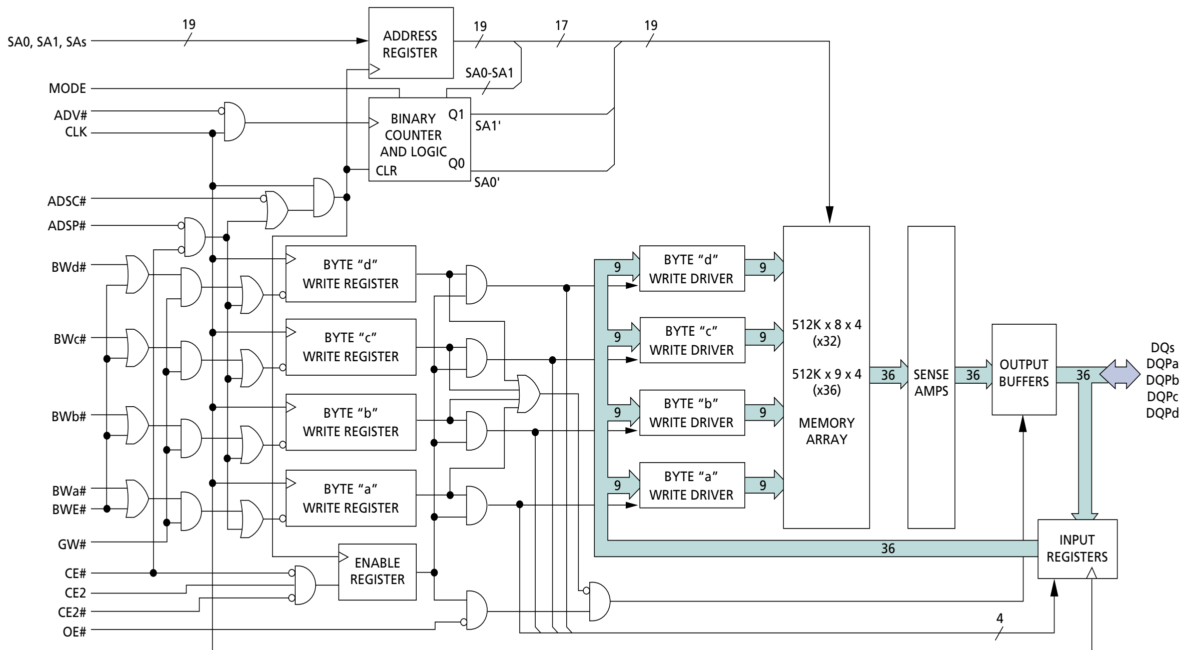


Figure 4: Functional Block Diagram 512K x 32/36



NOTE:

Functional block diagrams illustrate simplified device operation. See truth tables, pin/ball descriptions, and timing diagrams for detailed information.

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Figure 5: Pin Layout (Top View)
100-Pin TQFP

x18

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	NC	26	VSS	51	NC	76	VSS
2	NC	27	VDDQ	52	NC	77	VDDQ
3	NC	28	NC	53	NC	78	NC
4	VDDQ	29	NC	54	VDDQ	79	NC
5	VSS	30	NC	55	VSS	80	SA
6	NC	31	MODE (LBO#)	56	NC	81	SA
7	NC	32	SA	57	NC	82	SA
8	DQb	33	SA	58	DQa	83	ADV#
9	DQb	34	SA	59	DQa	84	ADSP#
10	VSS	35	SA	60	VSS	85	ADSC#
11	VDDQ	36	SA1	61	VDDQ	86	OE# (G#)
12	DQb	37	SA0	62	DQa	87	BWE#
13	DQb	38	DNU[2]	63	DQa	88	GW#
14	NC	39	DNU[2]	64	ZZ	89	CLK
15	VDD	40	VSS	65	VDD	90	VSS
16	NC	41	VDD	66	NC	91	VDD
17	VSS	42	SA	67	VSS	92	CE2#
18	DQb	43	SA	68	DQa	93	BWa#
19	DQb	44	SA	69	DQa	94	BWb#
20	VDDQ	45	SA	70	VDDQ	95	NC
21	VSS	46	SA	71	VSS	96	NC
22	DQb	47	SA	72	DQa	97	CE2
23	DQb	48	SA	73	DQa	98	CE#
24	DQPb	49	SA	74	DQPa	99	SA
25	NC	50	SA	75	NC	100	SA

x32/x36

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	NF/DQPc[1]	26	VSS	51	NF/DQPa[1]	76	VSS
2	DQc	27	VDDQ	52	DQa	77	VDDQ
3	DQc	28	DQd	53	DQa	78	DQb
4	VDDQ	29	DQd	54	VDDQ	79	DQb
5	VSS	30	NF/DQPd[1]	55	VSS	80	NF/DQPb[1]
6	DQc	31	MODE (LBO#)	56	DQa	81	SA
7	DQc	32	SA	57	DQa	82	SA
8	DQc	33	SA	58	DQa	83	ADV#
9	DQc	34	SA	59	DQa	84	ADSP#
10	VSS	35	SA	60	VSS	85	ADSC#
11	VDDQ	36	SA1	61	VDDQ	86	OE# (G#)
12	DQc	37	SA0	62	DQa	87	BWE#
13	DQc	38	DNU[2]	63	DQa	88	GW#
14	NC	39	DNU[2]	64	ZZ	89	CLK
15	VDD	40	VSS	65	VDD	90	VSS
16	NC	41	VDD	66	NC	91	VDD
17	VSS	42	SA	67	VSS	92	CE2#
18	DQd	43	SA	68	DQb	93	BWa#
19	DQd	44	SA	69	DQb	94	BWb#
20	VDDQ	45	SA	70	VDDQ	95	BWc#
21	VSS	46	SA	71	VSS	96	BWd#
22	DQd	47	SA	72	DQb	97	CE2
23	DQd	48	SA	73	DQb	98	CE#
24	DQd	49	SA	74	DQb	99	SA
25	DQd	50	SA	75	DQb	100	SA

NOTE:

1. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.
2. Pins 39 and 38 are reserved for address expansion; 36Mb and 72Mb, respectively.

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Table 1: TQFP Pin Descriptions

SYMBOL	TYPE	DESCRIPTION
ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2, and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.
BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BWs need to be asserted on the same cycle as the address. To enable the BW's functionality, the byte write enable (BWE#) input must be asserted LOW. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQa pins.
BWE#	Input	Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
CLK	Input	Clock: CLK registers address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
GW#	Input	Global Write: This active LOW input allows a full 18-, 32-, or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
MODE (LBO#)	Input	Mode: This input selects the burst sequence. A low on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. This pin has an internal pull-down and can be left unconnected.
DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, byte "a" is associated with DQa pins; byte "b" is associated with DQb pins. For the x32 and x36 versions, byte "a" is associated with DQa pins; byte "b" is associated with DQb pins; byte "c" is associated with DQc pins; byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge of CLK.

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Table 1: TQFP Pin Descriptions (continued)

SYMBOL	TYPE	DESCRIPTION
NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF I/O	No Function /Parity Data I/Os: On the x32 version, these pins are No Function (NF). On the x18 version, byte “a” parity is DQPa; byte “b” parity is DQPb. On the x36 version, byte “a” parity is DQPa; byte “b” parity is DQPb; byte “c” parity is DQPc; byte “d” parity is DQPd.
VDD	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
VDDQ	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
VSS	Supply	Ground: GND.
DNU	–	Do Not Use: These pins are internally connected to the die. They may be left floating or connected to ground to improve package heat dissipation.
NC	–	No Connect: These pins are not internally connected to the die. They may be left floating, driven by signals, or connected to ground to improve package heat dissipation.
NF	–	No Function: These pins are internally connected to the die and have the capacitance of an input pin. They may be left floating, driven by signals, or connected to ground to improve package heat dissipation.

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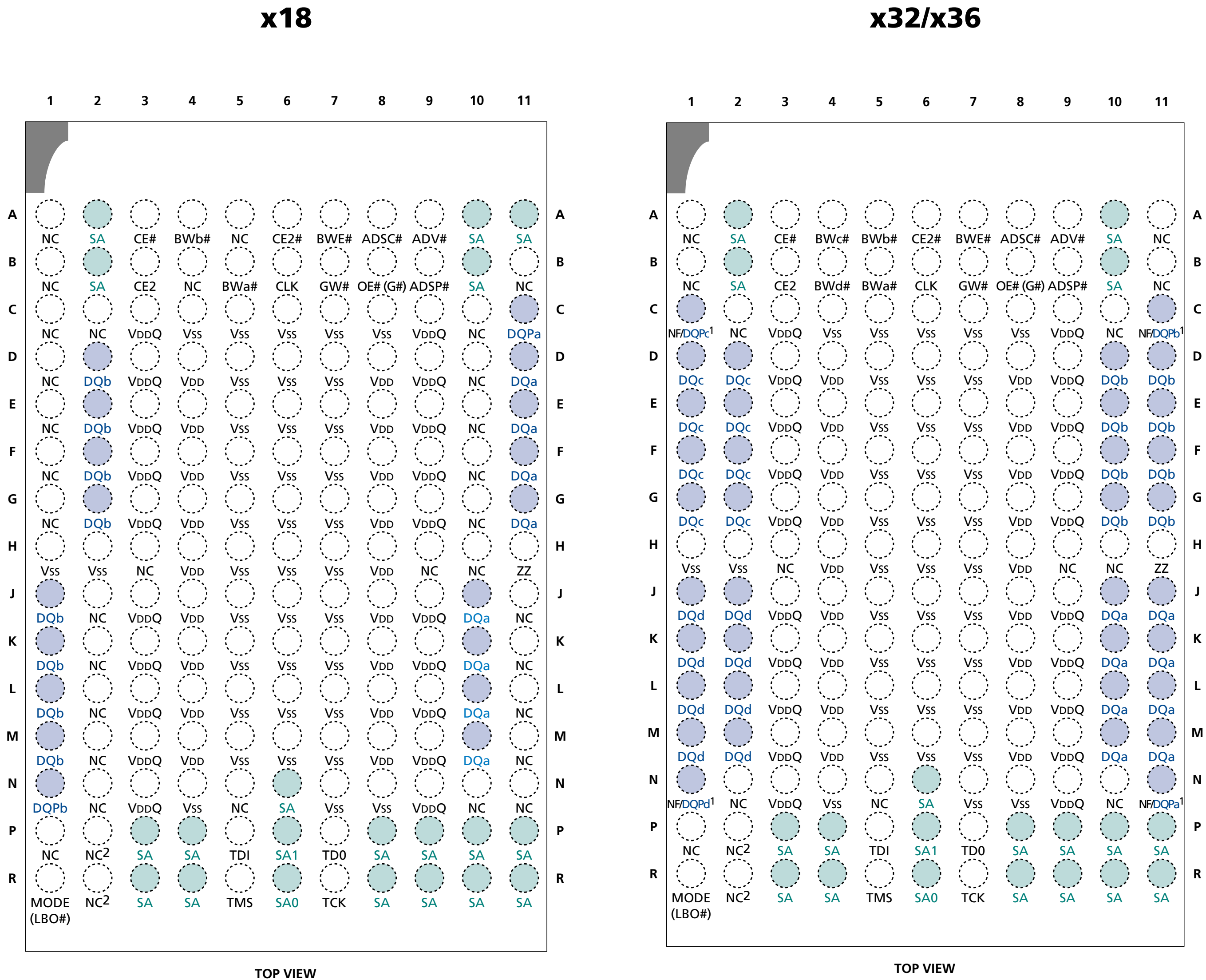
Figure 6: Ball Layout (Top View)
165-Ball FBGA



NOTE:
1. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.
2. Balls 2R and 2P are reserved for address expansion; 36Mb and 72Mb, respectively.

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Table 2: FBGA Ball Descriptions

SYMBOL	TYPE	DESCRIPTION
ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on ADV# effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.
BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BWs need to be asserted on the same cycle as the address. To enable the BW's functionality, the byte write enable (BWE#) input must be asserted LOW. BWa# controls DQa balls; BWb# controls DQb balls; BWc# controls DQc balls; and BWd# controls DQa balls.
BWE#	Input	Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
GW#	Input	Global Write: This active LOW input allows a full 18-, 32-, or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
MODE (LB0#)	Input	Mode: This input selects the burst sequence. A low on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.G# is the JEDEC-standard term for OE#.
SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
TMS TDI TCK	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 3.3V or 2.5V I/O levels. These balls may be left as No Connects if the JTAG function is not used in the circuit.
ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. This ball has an internal pull-down and can be left unconnected.
DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, byte "a" is associated with DQa pins; byte "b" is associated with DQb balls. For the x32 and x36 versions, byte "a" is associated with DQa balls; byte "b" is associated with DQb balls; byte "c" is associated with DQc balls; byte "d" is associated with DQd balls. Input data must meet setup and hold times around the rising edge of CLK.

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Table 2: FBGA Ball Descriptions (continued)

SYMBOL	TYPE	DESCRIPTION
NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF I/O	No Function/Parity Data I/Os: On the x32 version, these are No Function (NF). On the x18 version, byte "a" parity is DQPa; byte "b" parity is DQPb. On the x36 version, byte "a" parity is DQPa; byte "b" parity is DQPb; byte "c" parity is DQPc; byte "d" parity is DQPd.
TDO	Output	IEEE 1149.1 Test Outputs: JEDEC-standard 3.3V or 2.5V I/O levels.
VDD	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
VDDQ	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
VSS	Supply	Ground: GND.
NC	–	No Connect: These balls are not internally connected to the die. They may be left floating, driven by signals, or connected to ground to improve package heat dissipation.
NF	–	No Function: These balls are internally connected to the die and have the capacitance of an input pin. They may be left floating, driven by signals, or connected to ground to improve package heat dissipation.

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Table 3: Interleaved Burst Address Table (Mode = NC or HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

Table 4: Linear Burst Address Table (Mode = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

Table 5: Partial Truth Table for WRITE Commands (x18)

FUNCTION	GW#	BWE#	BWa#	BWb#
READ	H	H	X	X
READ	H	L	H	H
WRITE Byte “a”	H	L	L	H
WRITE Byte “b”	H	L	H	L
WRITE All Bytes	H	L	L	L
WRITE All Bytes	L	X	X	X

NOTE:

Using BWE# and BWa# through BWd#, any one or more bytes may be written.

Table 6: Partial Truth Table for WRITE Commands (x32/x36)

FUNCTION	GW#	BWE#	BWa#	BWb#	BWc#	BWd#
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte “a”	H	L	L	H	H	H
WRITE All Bytes	H	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

NOTE:

Using BWE# and BWa# through BWd#, any one or more bytes may be written.

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Table 7: Truth Table

Notes 1–8

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L–H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L–H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L–H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L–H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L–H	High-Z
SNOOZE Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L–H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L–H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L–H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L–H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L–H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

NOTE:
1. X means “Don’t Care.” # means active LOW. H means logic HIGH. L means logic LOW.
2. For WRITE#, L means any one or more byte write enable signals (BWa#, BWb#, BWc#, or BWd#) and BWE# are LOW or GW# is LOW. WRITE# = H for all BWx#, BWE#, GW# HIGH.
3. BWa# enables writes to DQa pins/balls and DQPa. BWb# enables writes to DQb pins/balls and DQPb. BWc# enables writes to DQc pins/balls and DQPc. BWd# enables writes to DQd pins/balls and DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
4. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, OE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP# LOW always initiates an internal READ at the L–H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L–H edge of CLK. Refer to WRITE timing diagram for clarification.

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Absolute Maximum Ratings

3.3V VDD

Voltage on VDD Supply
Relative to VSS .... -0.5V to +4.6V
Voltage on VDDQ Supply
Relative to VSS .... -0.5V to +4.6V
VIN (DQx) .... -0.5V to VDDQ + 0.5V
VIN (inputs) .... -0.5V to VDD + 0.5V
Storage Temperature (TQFP)................-55ºC to +150ºC
Storage Temperature (FBGA)................-55ºC to +125ºC
Junction Temperature .... +150ºC
Short Circuit Output Current 100mA

2.5V VDD

Voltage on VDD Supply
Relative to VSS .... -0.3V to +3.6V
Voltage on VDDQ Supply
Relative to VSS .... -0.3V to +3.6V
VIN (DQx) .... -0.3V to VDDQ + 0.3V
VIN (inputs) .... -0.3V to VDD + 0.3V
Storage Temperature (TQFP)................-55ºC to +150ºC
Storage Temperature (FBGA)................-55ºC to +125ºC
Junction Temperature .... +150ºC
Short Circuit Output Current 100mA

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Maximum Junction Temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

Table 8: 3.3V VDD, 3.3V I/O DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; VDD and VDDQ = 3.3V ±0.165V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-1.0	1.0	µA	4
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDD	ILO	-1.0	1.0	µA	
Output High Voltage	IOH = -4.0mA	VOH	2.4	–	V	1
Output Low Voltage	IOL = 8.0mA	VOL	–	0.4	V	1
Supply Voltage		VDD	3.135	3.465	V	1
Isolated Output Buffer Supply		VDDQ	3.135	VDD	V	1, 5

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Table 9: 3.3V VDD, 2.5V I/O DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; VDD = 3.3V ±0.165V and VDDQ = 2.5V ±0.125V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	VIHQ	1.7	VDDQ + 0.3	V	1, 2
	Inputs	VIH	1.7	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-1.0	1.0	µA	4
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (DQx)	ILO	-1.0	1.0	µA	
Output High Voltage	IOH = -2.0mA	VOH	1.7	–	V	1
	IOH = -1.0mA	VOH	2.0	–	V	1
Output Low Voltage	IOL = 2.0mA	VOL	–	0.7	V	1
	IOL = 1.0mA	VOL	–	0.4	V	1
Supply Voltage		VDD	3.135	3.465	V	1
Isolated Output Buffer Supply		VDDQ	2.375	2.625	V	1, 5

Table 10: 2.5V VDD, 2.5V I/O DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; VDD and VDDQ = 2.5V ±0.125V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	VIHQ	1.7	VDDQ + 0.3	V	1, 3
	Inputs	VIH	1.7	VDD + 0.3	V	1, 3
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 3
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-1.0	1.0	µA	4
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (DQx)	ILO	-1.0	1.0	µA	
Output High Voltage	IOH = -2.0mA	VOH	1.7	–	V	1
	IOH = -1.0mA	VOH	2.0	–	V	1
Output Low Voltage	IOL = 2.0mA	VOL	–	0.7	V	1
	IOL = 1.0mA	VOL	–	0.4	V	1
Supply Voltage		VDD	2.375	2.625	V	1
Isolated Output Buffer Supply		VDDQ	2.375	2.625	V	1, 5

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Table 11: TQFP Capacitance

Note 6; notes appear following parameter tables on page 17

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Control Input Capacitance	T_A = 25°C; f = 1 MHz; V_{DD} = 3.3V	C_I	4.2	5	pF
Input/Output Capacitance (DQ)		C_O	3.5	4	pF
Address Input Capacitance		C_A	4	5	pF
Clock Capacitance		C_{CK}	4.2	5	pF

Table 12: FBGA Capacitance

Note 6; notes appear following parameter tables on page 17

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Control Input Capacitance	T_A = 25°C; f = 1 MHz; V_{DD} = 3.3V	C_I	4	5	pF
Input/Output Capacitance (DQ)		C_O	4	4.5	pF
Address Input Capacitance		C_A	4	5	pF
Clock Capacitance		C_{CK}	5	5.5	pF

Table 13: TQFP Thermal Resistance

Note 6; notes appear following parameter tables on page 17

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS
Junction to Ambient (Airflow of 1m/s, two-layer board)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	28.9	°C/W
Junction to Case (Top)		θ_{JC}	4.2	°C/W

Table 14: FBGA Thermal Resistance

Note 6; notes appear following parameter tables on page 17

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS
Junction to Ambient (Airflow of 1m/s, two-layer board)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	32	°C/W
Junction to Case (Top)		θ_{JC}	1.7	°C/W
Junction to Board (Bottom)		θ_{JB}	10.4	°C/W

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Table 15: 3.3V VDD, IDD Operating Conditions and Maximum Limits (1 Meg x 18 and 512K x 32/36)

Notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; VDD and VDDQ = 3.3V ±0.165V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -6.8	MAX -7.5	MAX -8.5	MAX -10	UNITS	NOTES
Power Supply Current: Operating	Device selected; All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKC (MIN); VDD = MAX; Outputs open	IDD	200	320	290	260	230	mA	7, 8, 9
Power Supply Current: Idle	Device selected; VDD = MAX; ADSC#, ADSP#, ADV#, GW#, BWx# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; Cycle time ≥ tKC (MIN); Outputs open	IDD1	80	120	110	100	90	mA	7, 8, 9
CMOS Standby	Device deselected; VDD = MAX; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; All inputs static; CLK frequency = 0	ISB2	8	30	30	30	30	mA	8, 9
Clock Running	Device deselected; VDD = MAX; ADSC#, ADSP#, ADV#, GW#, BWx# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; Cycle time ≥ tKC (MIN)	ISB4	80	120	110	100	90	mA	8, 9
Snooze Mode	ZZ ≥ VIH	ISB2Z	8	30	30	30	30	mA	9

Table 16: 2.5V VDD, IDD Operating Conditions and Maximum Limits (1 Meg x 18 and 512K x 32/36)

Notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; VDD and VDDQ = 2.5V ±0.125V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -6.8	MAX -7.5	MAX -8.5	MAX -10	UNITS	NOTES
Power Supply Current: Operating	Device selected; All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKC (MIN); VDD = MAX; Outputs open	IDD	190	240	230	220	200	mA	7, 8, 10
Power Supply Current: Idle	Device selected; VDD = MAX; ADSC#, ADSP#, ADV#, GW#, BWx# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; Cycle time ≥ tKC (MIN); Outputs open	IDD1	80	120	110	100	90	mA	7, 8, 10
CMOS Standby	Device deselected; VDD = MAX; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; All inputs static; CLK frequency = 0	ISB2	8	30	30	30	30	mA	8, 10
Clock Running	Device deselected; VDD = MAX; ADSC#, ADSP#, ADV#, GW#, BWx# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDD - 0.2; Cycle time ≥ tKC (MIN)	ISB4	80	120	110	100	90	mA	8, 10
Snooze Mode	ZZ ≥ VIH	ISB2Z	8	30	30	30	30	mA	10

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Table 17: AC Electrical Characteristics and Recommended Operating Conditions

Note 11; notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; T_J ≤ 95°C (commercial); T_J ≤ 110°C (industrial); VDD = 3.3V ±0.165V unless otherwise noted

DESCRIPTION	SYM	-6.8		-7.5		-8.5		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock											
Clock cycle time	^tKC	7.5		8.8		10.0		15.0		ns	
Clock frequency	^fKF		133		113		100		66	MHz	
Clock HIGH time	^tKH	2.5		2.5		3.0		4.0		ns	12
Clock LOW time	^tKL	2.5		2.5		3.0		4.0		ns	12
Output Times											
Clock to output valid	^tKQ		6.8		7.5		8.5		10.0	ns	
Clock to output invalid	^tKQX	2.5		2.5		2.5		2.5		ns	13
Clock to output in Low-Z	^tKQLZ	2.5		2.5		2.5		2.5		ns	6, 13, 14,
Clock to output in High-Z	^tKQHZ		3.8		4.0		5.0		5.0	ns	6, 13, 14
OE# to output valid	^tOEQ		3.5		3.5		4.0		5.0	ns	15
OE# to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 13, 14
OE# to output in High-Z	^tOEHZ		3.5		3.5		4.0		5.0	ns	6, 13, 14
Setup Times											
Address	^tAS	1.5		1.5		1.8		2.0		ns	16, 17
Address status (ADSC#, ADSP#)	^tADSS	1.5		1.5		1.8		2.0		ns	16, 17
Address advance (ADV#)	^tAAS	1.5		1.5		1.8		2.0		ns	16, 17
Byte write enables (BWa#-BWd#, GW#, BWE#)	^tWS	1.5		1.5		1.8		2.0		ns	16, 17
Data-in	^tDS	1.5		1.5		1.8		2.0		ns	16, 17
Chip enable (CE#)	^tCES	1.5		1.5		1.8		2.0		ns	16, 17
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	16, 17
Address status (ADSC#, ADSP#)	^tADSH	0.5		0.5		0.5		0.5		ns	16, 17
Address advance (ADV#)	^tAAH	0.5		0.5		0.5		0.5		ns	16, 17
Byte write enables (BWa#-BWd#, GW#, BWE#)	^tWH	0.5		0.5		0.5		0.5		ns	16, 17
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	16, 17
Chip enable (CE#)	^tCEH	0.5		0.5		0.5		0.5		ns	16, 17

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Notes

1. All voltages referenced to V_{SS} (GND).
2. For 3.3V V_{DD}:
   Overshoot: $V_{IH} \leq +4.6V$ for $t \leq {}^{t}KC/2$ for $I \leq 20mA$
   Undershoot: $V_{IL} \geq -0.7V$ for $t \leq {}^{t}KC/2$ for $I \leq 20mA$
   Power-up: $V_{IH} \leq +3.6V$ and $V_{DD} \leq 3.135V$ for $t \leq$ 200ms
3. For 2.5V V_{DD}:
   Overshoot: $V_{IH} \leq +3.6V$ for $t \leq {}^{t}KC/2$ for $I \leq 20mA$
   Undershoot: $V_{IL} \geq -0.5V$ for $t \leq {}^{t}KC/2$ for $I \leq 20mA$
   Power-up: $V_{IH} \leq +2.65V$ and $V_{DD} \leq 2.375V$ for $t \leq$ 200ms
4. The MODE and ZZ pins/balls have an internal pull-up/pull-down and input leakage = ±10µA.
5. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be connected together.
6. This parameter is sampled.
7. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
8. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
9. Typical values are measured at 3.3V, 25°C, and 10ns cycle time.
10. Typical values are measured at 2.5V, 25°C, and 10ns cycle time.
11. Test conditions as specified with the output loading shown in Figures 11 and 12 for 3.3V I/O, and Figures 13 and 14 for 2.5V I/O unless otherwise noted.
12. Measured as HIGH above V_{IH} and LOW below V_{IL}.
13. This parameter is measured with the output loading shown in Figure 12 for 3.3V I/O and Figure 14 for 2.5V I/O.
14. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion of these parameters.
15. OE# is a "Don't Care" when a byte write enable is sampled LOW.
16. A WRITE cycle is defined by at least one byte write (BWa#–BWd#) being LOW, the byte write enable (BWE#) active, and ADSC# LOW for the required setup and hold times. A READ cycle is defined by the byte write enable (BWE#) being HIGH or ADSP# LOW for the required setup and hold times.
17. This is a synchronous device. All addresses must meet the specified setup and hold times when either ADSC# or ADSP# is LOW and chip is enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when the chip is enabled. To remain enabled, chip enable must be valid at each rising edge when either ADSC# or ADSP# is LOW.

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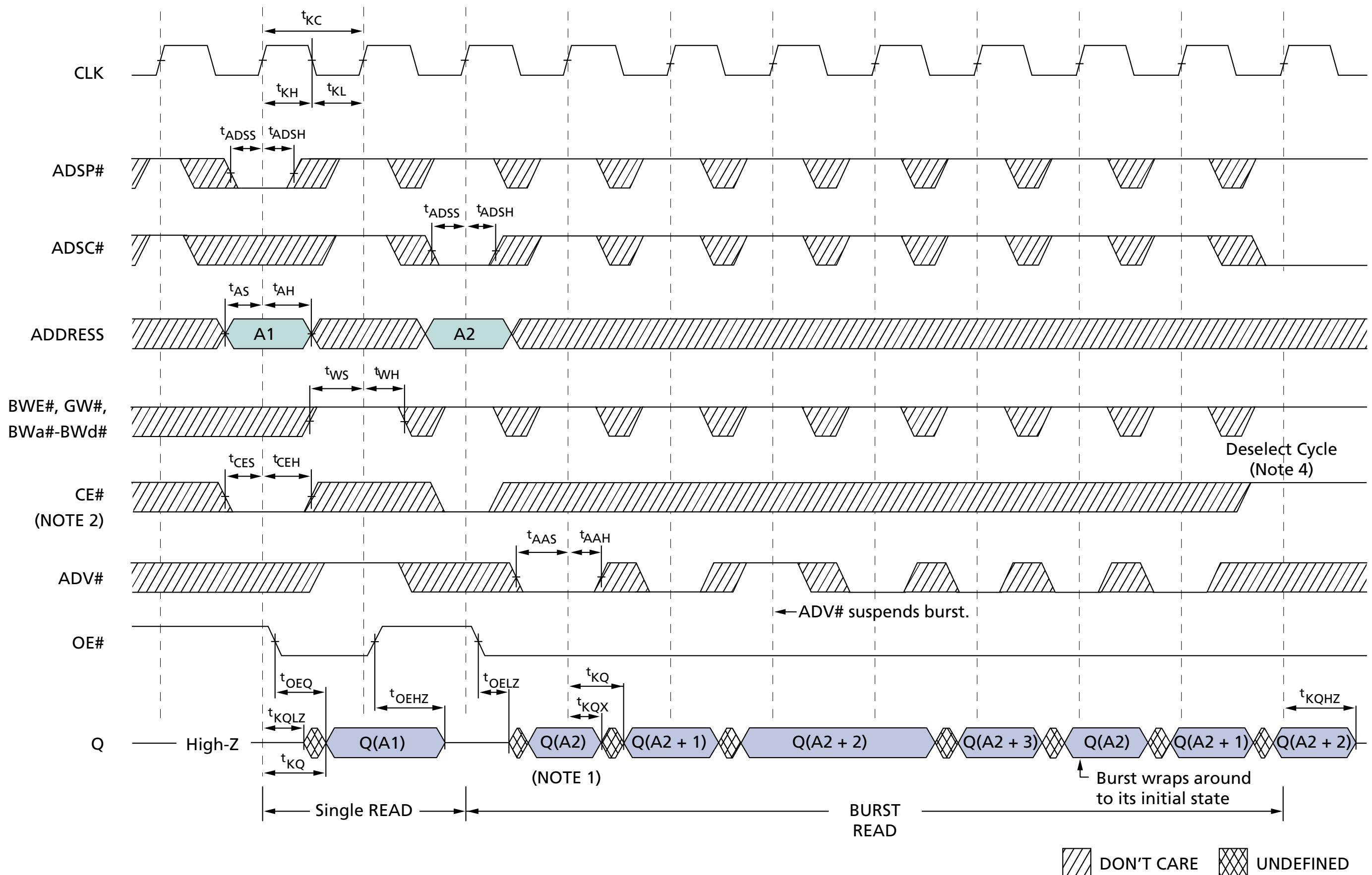
Figure 7: READ Timing



NOTE:

1. Q(A2) refers to output from address A2. Q(A2 + 1) refers to output from the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. (This note applies to whole diagram.)
4. Outputs are disabled ^{t}KQHZ after deselect.

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Figure 8:
WRITE Timing

NOTE:

1. D(A2) refers to output from address A2. D(A2 + 1) refers to output from the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV# must be HIGH to permit a WRITE to the loaded address.
5. Full-width WRITE can be initiated by GW# LOW; or GW# HIGH and BWE#, BWa#, and BWb# LOW for x18 device; or GW# HIGH and BWE#, BWa#-BWd# LOW for x32 and x36 devices.

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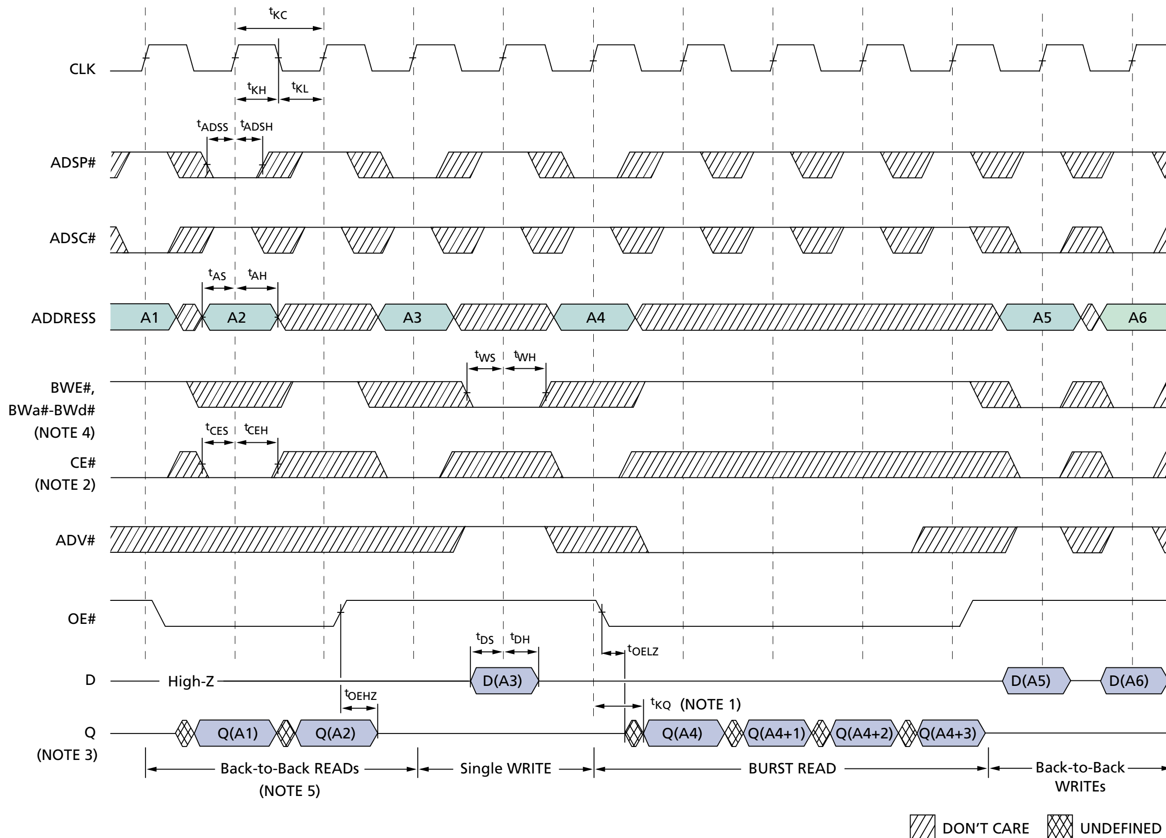
Figure 9:
READ/WRITE Timing



NOTE:

1. Q(A4) refers to output from address A4. Q(A4 + 1) refers to output from the next internal burst address following A4.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC#, or ADV# cycle is performed.
4. GW# is HIGH.
5. Back-to-back READs may be controlled by either ADSP# or ADSC#.

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SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

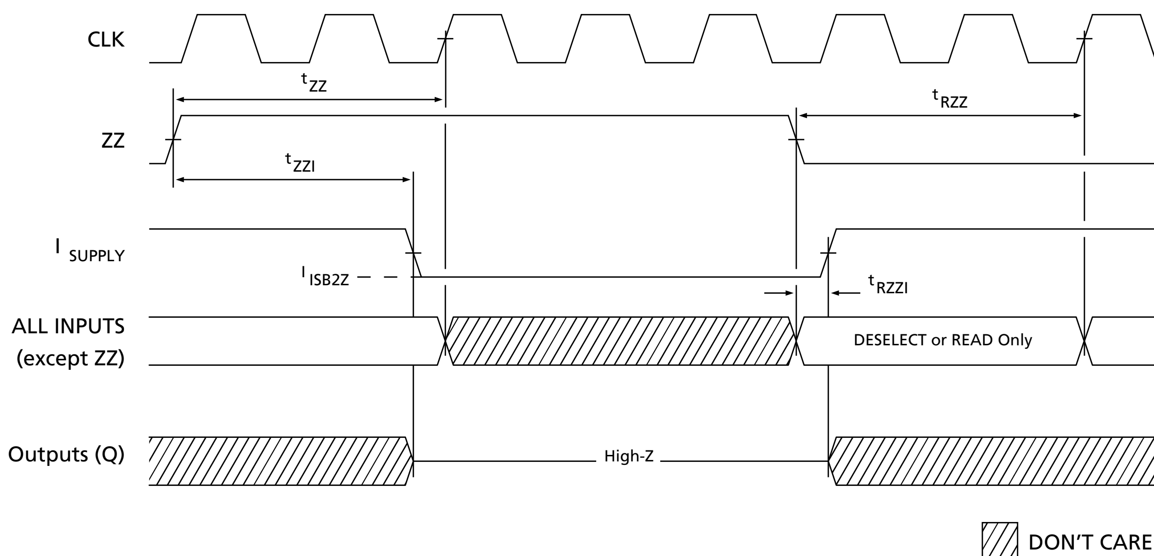
ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time ^tZZ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

Table 18: SNOOZE MODE Electrical Characteristics

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		30	mA	
ZZ active to input ignored		^tZZ		^tKC	ns	1
ZZ inactive to input sampled		^tRZZ	^tKC		ns	1
ZZ active to snooze current		^tZZI		^tKC	ns	1
ZZ inactive to exit snooze current		^tRZZI	0		ns	1

NOTE:
1. This parameter is sampled.

Figure 10: SNOOZE MODE Waveform



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3.3V VDD, 3.3V I/O AC Test Conditions

Input pulse levels ....VIH = (VDD/2.2) + 1.5V
.... VIL = (VDD/2.2) - 1.5V
Input rise and fall times.. 1ns
Input timing reference levels VDD/2.2
Output reference levels................................VDDQ/2.2
Output load ....See Figures 11 and 12

2.5V VDD, 2.5V I/O AC Test Conditions

Input pulse levels .... VIH = (VDD/2) + 1.25V
.... VIL = (VDD/2) - 1.25V
Input rise and fall times.. 1ns
Input timing reference levels VDD/2
Output reference levels................................. VDDQ/2
Output load..............................See Figures 13 and 14

3.3V VDD, 2.5V I/O AC Test Conditions

Input pulse levels ....VIH = (VDD/2.64) + 1.25V
.... VIL = (VDD/2.64) - 1.25V
Input rise and fall times.. 1ns
Input timing reference levels VDD/2.64
Output reference levels..................................VDDQ/2
Output load ....See Figures 13 and 14

3.3V I/O Output Load Equivalents

Figure 11:

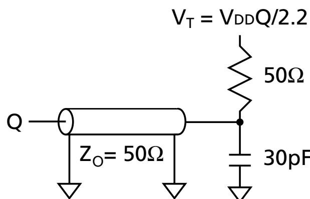
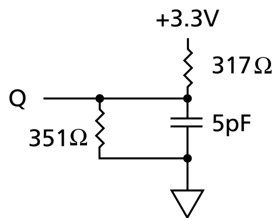


Figure 12:



2.5V I/O Output Load Equivalents

Figure 13:

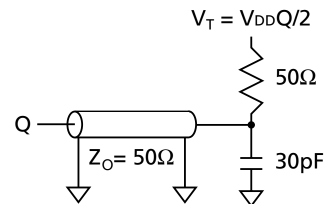
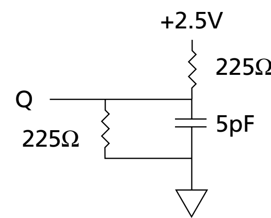


Figure 14:



NOTE:
For Figures 11 and 13, 30pF = distributive test jig capacitance.

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IEEE 1149.1 Serial Boundary Scan (JTAG)

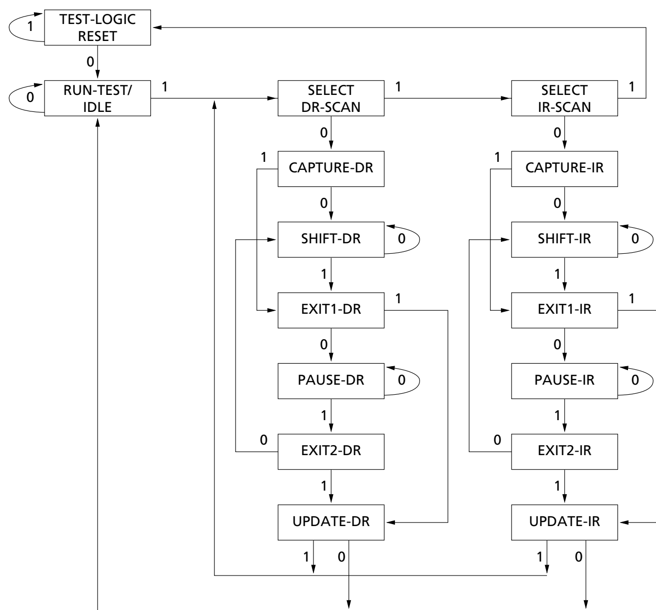
The SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-2001 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

These balls can be left floating (unconnected), if the JTAG function is not to be implemented. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Figure 15: TAP Controller State Diagram



NOTE:

The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

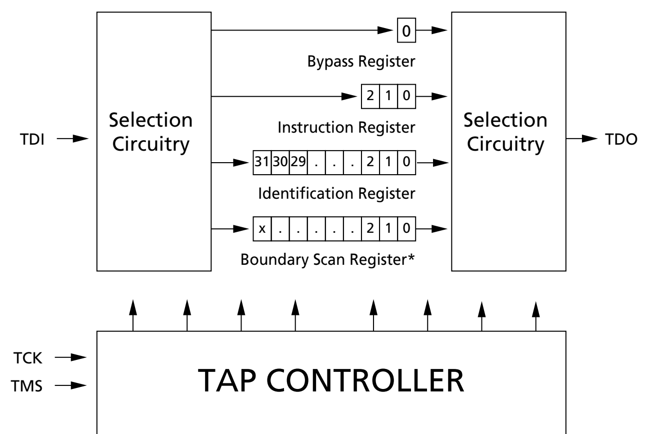
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 16.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 15.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 16.)

Figure 16: TAP Controller Block Diagram



NOTE:

X = 74 for all configurations.

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Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in Figure 16. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (Vss) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The SRAM has a 75-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1.

The TAP controller does recognize an all 0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is

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one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

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Figure 17: TAP Timing

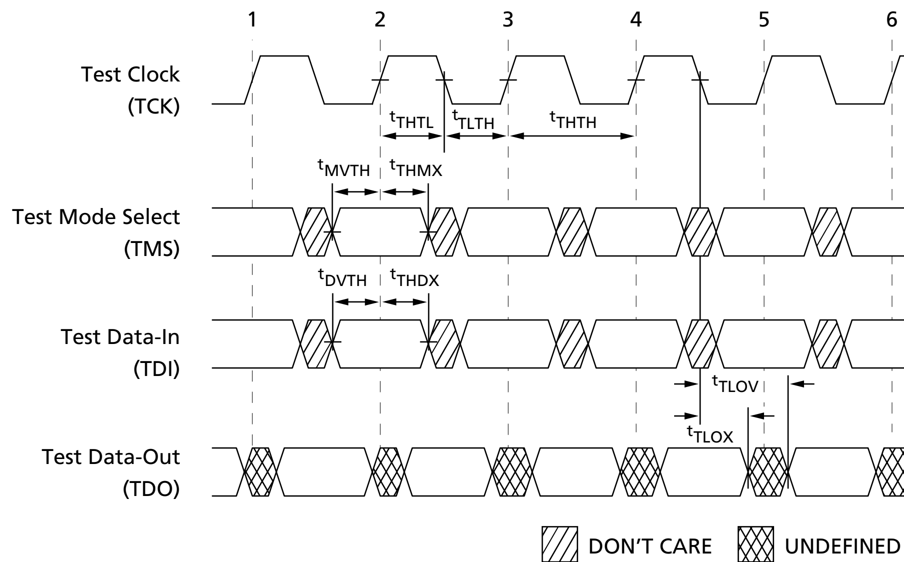

Table 19: TAP AC Electrical Characteristics

Notes 1, 2; 0°C ≤ T_A ≤ +70°C; VDD = 3.3V ±0.165V or 2.5V ± 0.125V

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

NOTE:

1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the loads in Figures 18 and 19.

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3.3V TAP AC Test Conditions

Input pulse levels.. VSS to 3.0V
Input rise and fall times 1ns
Input timing reference levels.................................. 1.5V
Output reference levels... 1.5V
Test load termination supply voltage 1.5V

2.5V TAP AC Test Conditions

Input pulse levels.. VSS to 2.5V
Input rise and fall times 1ns
Input timing reference levels............................... 1.25V
Output reference levels... 1.25V
Test load termination supply voltage 1.25V

**Figure 18:
3.3V TAP AC Output Load Equivalent**

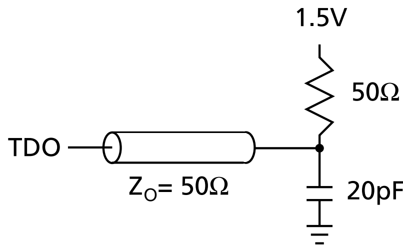

**Figure 19:
2.5V TAP AC Output Load Equivalent**

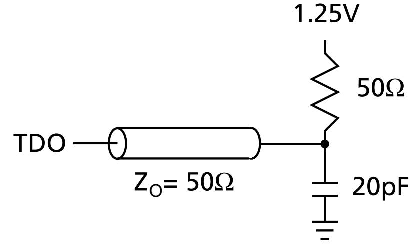

Table 20: 3.3V VDD, TAP DC Electrical Characteristics and Operating Conditions

0°C ≤ T_A ≤ +70°C; VDD = 3.3V ±0.165V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-10	10	µA	2
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDD (TDO)	ILO	-10	10	µA	2
Output Low Voltage	IOLC = 100µA	VOL1		0.7	V	1, 2
	IOLT = 2mA	VOL2		0.8	V	1, 2
Output High Voltage	IOHC = -100µA	VOH1	2.9		V	1, 2
	IOHT = -2mA	VOH2	2.0		V	1, 2

Table 21: 2.5V VDD, TAP DC Electrical Characteristics and Operating Conditions

0°C ≤ T_A ≤ +70°C; VDD = 2.5V ±0.125V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	1.7	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-10	10	µA	2
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDD (TDO)	ILO	-10	10	µA	2
Output Low Voltage	IOLC = 100µA	VOL1		0.2	V	1, 2
	IOLT = 2mA	VOL2		0.7	V	1, 2
Output High Voltage	IOHC = -100µA	VOH1	2.1		V	1, 2
	IOHT = -2mA	VOH2	1.7		V	1, 2

NOTE:
1. All voltages referenced to VSS (GND).
2. TAP control balls only. For boundary scan ball specifications, please refer to the I/O DC Electrical Characteristics and Operation Conditions tables.

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Table 22: Identification Register Definitions

INSTRUCTION FIELD	BIT CONFIGURATION	DESCRIPTION
Revision Number (31:28)	0000	Reserved for version number.
Device Depth (27:23)	00111 00110	Defines depth of 1Mb. Defines depth of 512K.
Device Width (22:18)	00011 00100	Defines width of x18 bits. Defines width of x32 or x36 bits.
Micron Device ID (17:12)	xxxxxx	Reserved for future use.
Micron JEDEC ID Code (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Table 23: Scan Register Sizes

REGISTER NAME	BIT SIZE
Instruction	3
Bypass	1
ID	32
Boundary Scan: x18, x32, x36	75

Table 24: Instruction Codes

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

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Table 25: 165-Ball FBGA Boundary Scan Order (x18)

BIT#	SIGNAL NAME	BALL ID
1	MODE (LBO#)	1R
2	SA	6N
3	SA	11P
4	SA	8R
5	SA	8P
6	SA	9R
7	SA	9P
8	SA	10R
9	SA	10P
10	SA	11R
11	ZZ	11H
12	NC	11N
13	NC	11M
14	NC	11L
15	NC	11K
16	NC	11J
17	DQa	10M
18	DQa	10L
19	DQa	10K
20	DQa	10J
21	DQa	11G
22	DQa	11F
23	DQa	11E
24	DQa	11D
25	DQPa	11C
26	NC	10F
27	NC	10E
28	NC	10D
29	NC	10G
30	SA	11A
31	SA	10B
32	SA	10A
33	ADV#	9A
34	ADSP#	9B
35	ADSC#	8A
36	OE# (G#)	8B
37	BWE#	7A
38	GW#	7B
39	CLK	6B
40	NC	11B
41	NC	1A
42	CE2#	6A
43	BWa#	5B
44	NC	5A
45	BWb#	4A
46	NC	4B
47	CE2	3B
48	CE#	3A
49	SA	2A
50	SA	2B
51	NC	1B
52	NC	1C
53	NC	1D
54	NC	1E
55	NC	1F
56	NC	1G
57	DQb	2D
58	DQb	2E
59	DQb	2F
60	DQb	2G
61	DQb	1J
62	DQb	1K
63	DQb	1L
64	DQb	1M
65	DQPb	1N
66	NC	2K
67	NC	2L
68	NC	2M
69	NC	2J
70	SA	3P
71	SA	3R
72	SA	4P
73	SA	4R
74	SA1	6P
75	SA0	6R

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Table 26: 165-Ball FBGA Boundary Scan Order (x32)

BIT#	SIGNAL NAME	BALL ID
1	MODE (LB0#)	1R
2	SA	6N
3	SA	11P
4	SA	8R
5	SA	8P
6	SA	9R
7	SA	9P
8	SA	10R
9	SA	10P
10	SA	11R
11	ZZ	11H
12	NF	11N
13	DQa	11M
14	DQa	11L
15	DQa	11K
16	DQa	11J
17	DQa	10M
18	DQa	10L
19	DQa	10K
20	DQa	10J
21	DQb	11G
22	DQb	11F
23	DQb	11E
24	DQb	11D
25	DQb	10G
26	DQb	10F
27	DQb	10E
28	DQb	10D
29	NF	11C
30	NC	11A
31	SA	10B
32	SA	10A
33	ADV#	9A
34	ADSP#	9B
35	ADSC#	8A
36	OE# (G#)	8B
37	BWE#	7A
38	GW#	7B
39	CLK	6B
40	NC	11B
41	NC	1A
42	CE2#	6A
43	BWa#	5B
44	BWb#	5A
45	BWc#	4A
46	BWd#	4B
47	CE2	3B
48	CE#	3A
49	SA	2A
50	SA	2B
51	NC	1B
52	NF	1C
53	DQc	1D
54	DQc	1E
55	DQc	1F
56	DQc	1G
57	DQc	2D
58	DQc	2E
59	DQc	2F
60	DQc	2G
61	DQd	1J
62	DQd	1K
63	DQd	1L
64	DQd	1M
65	DQd	2J
66	DQd	2K
67	DQd	2L
68	DQd	2M
69	NF	1N
70	SA	3P
71	SA	3R
72	SA	4P
73	SA	4R
74	SA1	6P
75	SA0	6R

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Table 27: 165-Ball FBGA Boundary Scan Order (x36)

BIT#	SIGNAL NAME	BALL ID
1	MODE (LB0#)	1R
2	SA	6N
3	SA	11P
4	SA	8R
5	SA	8P
6	SA	9R
7	SA	9P
8	SA	10R
9	SA	10P
10	SA	11R
11	ZZ	11H
12	DQPa	11N
13	DQa	11M
14	DQa	11L
15	DQa	11K
16	DQa	11J
17	DQa	10M
18	DQa	10L
19	DQa	10K
20	DQa	10J
21	DQb	11G
22	DQb	11F
23	DQb	11E
24	DQb	11D
25	DQb	11C
26	DQb	10F
27	DQb	10E
28	DQb	10D
29	DQPb	10G
30	NC	11A
31	SA	10B
32	SA	10A
33	ADV#	9A
34	ADSP#	9B
35	ADSC#	8A
36	OE# (G#)	8B
37	BWE#	7A
38	GW#	7B
39	CLK	6B
40	NC	11B
41	NC	1A
42	CE2#	6A
43	BWa#	5B
44	BWb#	5A
45	BWc#	4A
46	BWd#	4B
47	CE2	3B
48	CE#	3A
49	SA	2A
50	SA	2B
51	NC	1B
52	DQPc	1C
53	DQc	1D
54	DQc	1E
55	DQc	1F
56	DQc	1G
57	DQc	2D
58	DQc	2E
59	DQc	2F
60	DQc	2G
61	DQd	1J
62	DQd	1K
63	DQd	1L
64	DQd	1M
65	DQd	1N
66	DQd	2K
67	DQd	2L
68	DQd	2M
69	DQPd	2J
70	SA	3P
71	SA	3R
72	SA	4P
73	SA	4R
74	SA1	6P
75	SA0	6R

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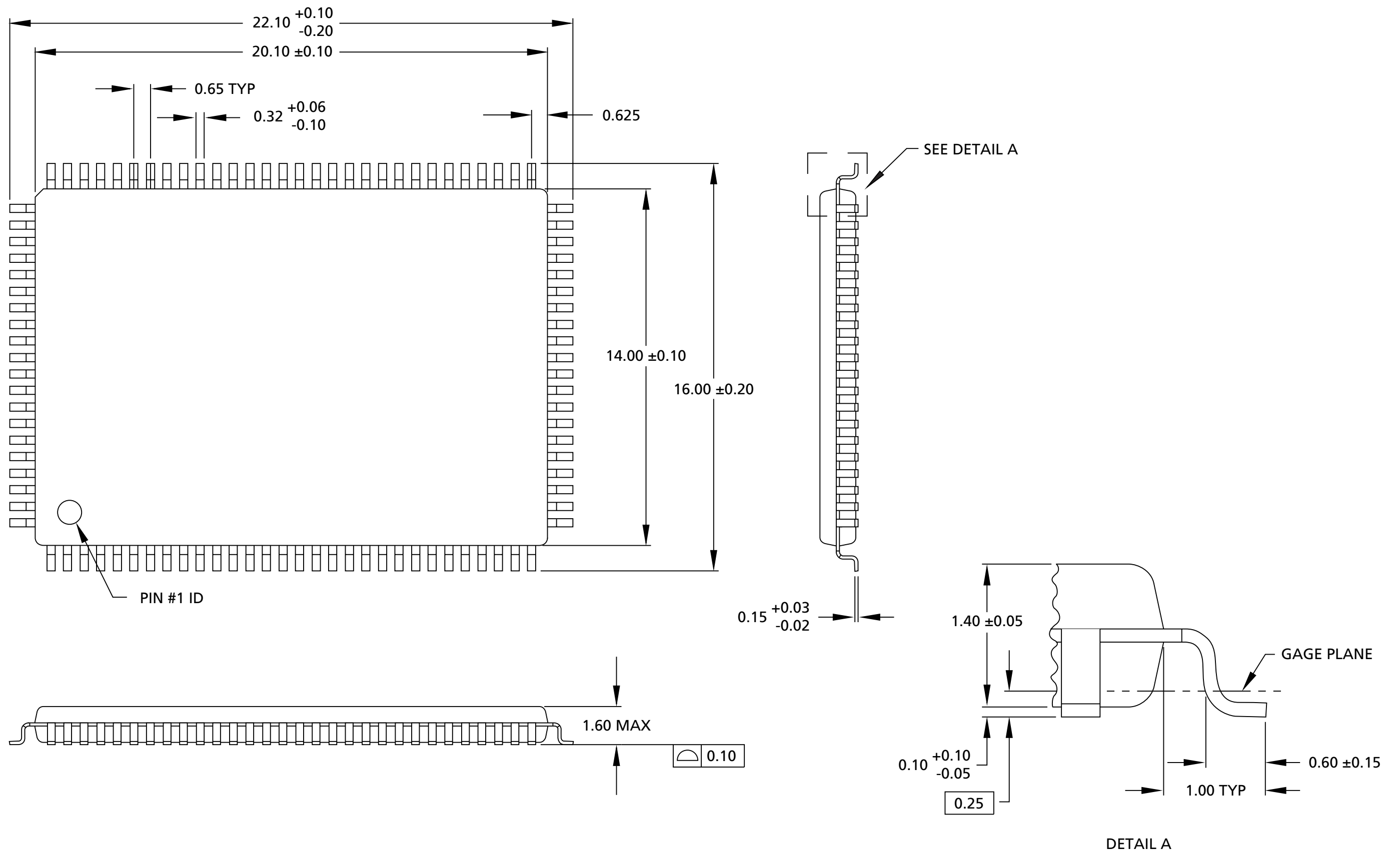
Figure 20:
100-Pin Plastic TQFP (JEDEC LQFP)



NOTE:

1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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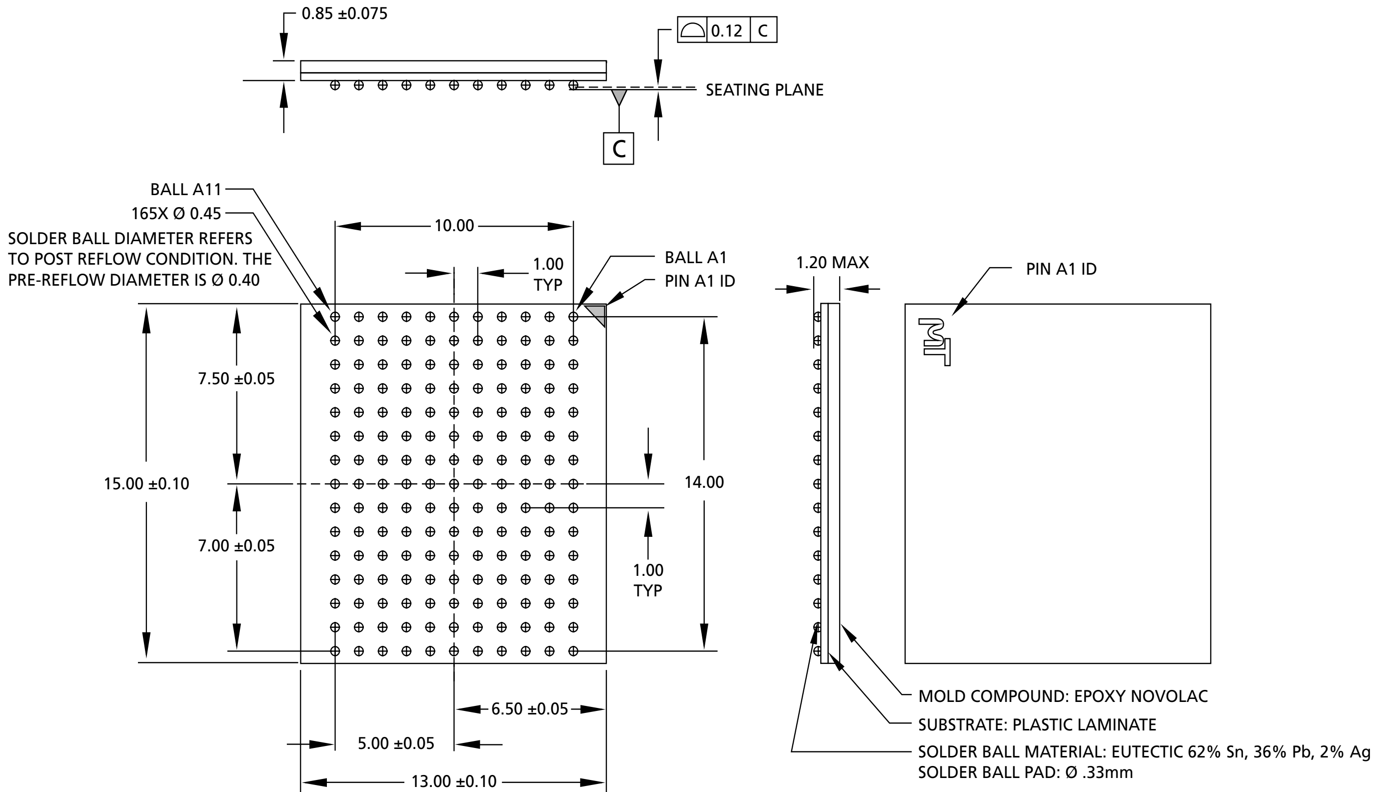
**Figure 21:
165-Ball FBGA**



NOTE:

All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Data Sheet Designation

No Marking: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Document Revision History

- Rev D; Pub. 2/03 ....2/03
  Changed designation from Preliminary to Production

- Rev C; Pub. 12/02 ....12/02
  Added T_J specifications to the AC Electrical Characteristics table
  Corrected Boundary Scan errors
  Updated TQFP and FBGA Thermal Resistance values
  Corrected grammatical errors

- Rev B; Pub. 11/02 ....11/02
  Changed designation from ADVANCE to PRELIMINARY
  Corrected grammatical errors

- New ADVANCE data sheet for 0.16µm process; Rev. A, Pub. 6 /02 ....6/02

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