256K x 36
2.5V VDD, HSTL, PIPELINED DDR SRAM

9Mb DDR SRAM

MT57V256H36E

FEATURES

- Fast cycle times: 5ns and 6ns
- 256K x 36 configuration
- Pipelined, double data rate operation
- Single +2.5V ±0.1V power supply (VDD)
- Separate isolated output buffer supply (VDDQ)
- JEDEC-standard HSTL I/O
- User-selectable trip point with VREF
- HSTL programmable impedance outputs synchronized to optional dual-data clocks
- Echo clock outputs
- JTAG boundary scan
- Fully-static design for reduced-power standby
- Clock-stop capability
- Common data inputs and data outputs
- Low-control ball count
- Internally self-timed, registered LATE WRITE cycles
- Linear burst order with four-tick burst counter
- 13mm x 15mm, 1mm pitch, 11 x 15 grid FBGA package
- Full data coherency, providing most current data

OPTIONS — MARKING[1]

- Clock Cycle Timing
  - 5ns (200 MHz) — -5
  - 6ns (167 MHz) — -6
- Configurations
  - 256K x 36 — MT57V256H36E
- Package
  - 165-ball, 13mm x 15mm FBGA — F

NOTE:

1. A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/numberguide.

Figure 1: 165-Ball FBGA

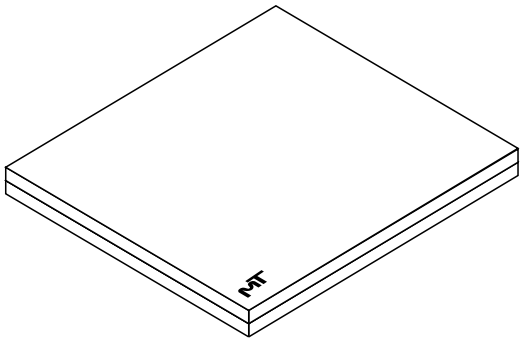


Table 1: Valid Part Numbers

PART NUMBER	DESCRIPTION
MT57V256H36EF-xx	256K x 36, HSTL, DDR, Pipelined

General Description

The Micron® DDR synchronous SRAM employs high-speed, low-power CMOS designs using an advanced 6T CMOS process.

The DDR SRAM integrates a 9Mb SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by an input clock pair (K and K#) and are latched on the rising edge of K and K#. The synchronous inputs include all addresses, all data inputs, active LOW load (LD#) and read/write (R/W#). Write data is registered on the rising edges of both K and K#. Read data is driven on the rising edge of C and C# if provided, or on the rising edge of K and K#, if C and C# are not provided.

Asynchronous inputs include impedance match (ZQ). Synchronous data outputs (Q) are closely matched to the two echo clocks (CQ and CQ#), which can be used as data receive clocks. Output data clocks (C, C#) are also provided for maximum system clocking and data synchronization flexibility.

Additional write registers are incorporated to enhance pipelined WRITE cycles and reduce READ-to-WRITE turnaround time. WRITE cycles are self-timed.

The device does not utilize internal phase-locked loops and can therefore be placed into a stopped-clock state to minimize power without lengthy restart times.

Four balls are used to implement JTAG test capabilities: test mode select (TMS), test data-in (TDI), test clock (TCK), and test data-out (TDO). JTAG circuitry is used to serially shift data to and from the SRAM. JTAG inputs use JEDEC-standard 2.5V I/O levels to shift data during this testing mode of operation.

The device can be used in HSTL systems by supplying an appropriate reference voltage (VREF). The device is ideally suited for applications requiring very rapid data transfer by operation in data-doubled mode. The device is also ideal in applications requiring the cost benefits of pipelined CMOS SRAMs and the reduced READ-to-WRITE turnaround times of Late Write SRAMs.

The SRAM operates from a +2.5V power supply, and all inputs and outputs are HSTL-compatible. The device is ideally suited for cache, network, telecom, DSP, and other applications that benefit from a very wide, high-speed data bus.

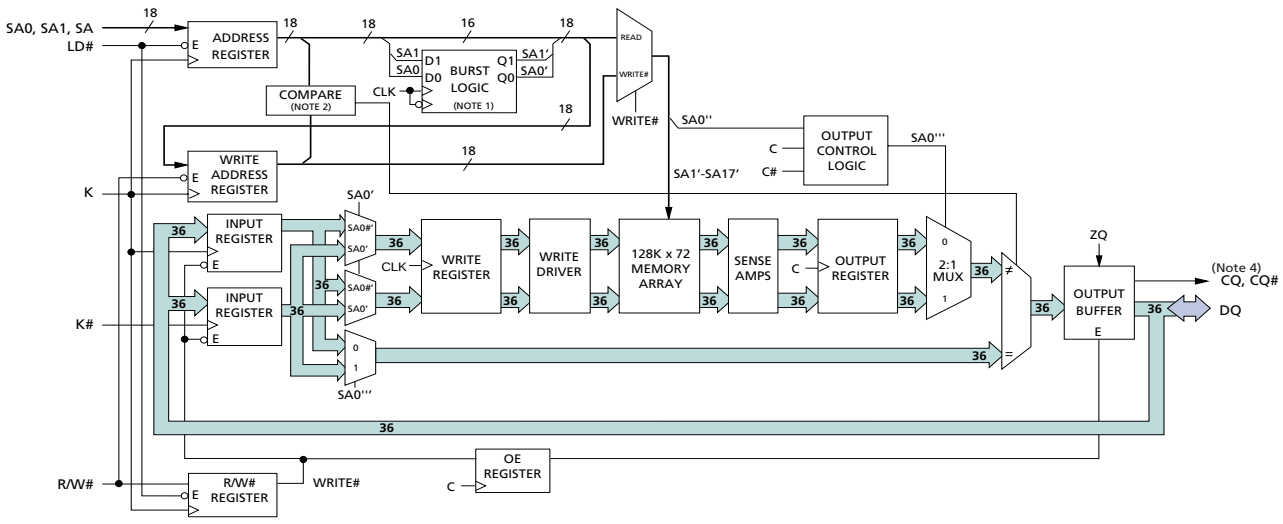
Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

DDR Operation

The DDR SRAM enables high performance operation through high-clock frequencies (achieved through pipelining) and double data rate mode of operation. At slower frequencies, the DDR SRAM requires a single NO OPERATION (NOP) cycle when transitioning from a READ to a WRITE cycle. At higher frequencies, a second NOP cycle may be required to prevent bus contention. NOP cycles are not required when switching from a WRITE to a READ.

If a READ occurs after a WRITE cycle, address and data for the WRITE are stored in registers. The write information must be stored because the SRAM cannot perform the last WORD WRITE to the array without conflicting with the READ. The data stays in this register until the next WRITE cycle occurs. On the first WRITE cycle after the READ(s), the stored data from the earlier WRITE will be written into the SRAM array. This is called a POSTED WRITE.

Figure 2:
Functional Block Diagram: 256K x 36



NOTE:

1. SA0 and SA1 are advanced in linear burst order at each K and K# rising edge.
2. The compare width is a 16-bits. The compare is performed only if a WRITE is pending and a READ cycle is requested. If the address matches, data is routed directly to the device outputs, bypassing the memory array.
3. The functional block diagram illustrates simplified device operation. See truth tables, ball descriptions, and timing diagrams for detailed information.
4. CQ and CQ# do not tri-state except during some JTAG test modes.

A READ can be made immediately to an address even if that address was written in the previous cycle. During this READ cycle, the SRAM array is bypassed, and data is read instead from the data register storing the recently written data. This is transparent to the user. This feature facilitates system data coherency.

The DDR SRAM differs in some ways from its predecessor, the Claymore DDR SRAM. Single data rate operation is not supported, hence, no SD/DD# ball is provided. Only bursts of four are supported. In addition to the echo clocks, two single-ended input clocks are available (C and C#). The SRAM synchronizes its output data to these data clock rising edges if provided. If not present, C and C# must be tied HIGH and output timing is derived from K and K#. No differential clocks are used in this device. This clocking scheme provides greater system tuning capability than Claymore SRAMs and reduces the number of input clocks required by the bus master.

Programmable Impedance Output Buffer

The DDR SRAM is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and VSS. The value of the resistor must be five times the desired impedance. For example, a 350Ω resistor is required for an output impedance of 70Ω. To ensure that output impedance is one-fifth the value of RQ (within 10 percent), the range of RQ is 175Ω to 350Ω. Alternately, the ZQ ball can be connected directly to VDDQ, which will place the device in a minimum impedance mode.

Output impedance updates may be required because variations may occur in supply voltage and temperature over time. The device samples the value of RQ. An update of the impedance is transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during an update.

The device will power up with an output impedance set at 50Ω. To guarantee optimum output driver impedance after power-up, the SRAM needs 1,024 cycles to update the impedance. The user can operate the part with fewer than 1,024 clock cycles, but optimal output impedance is not guaranteed.

Clocking

The DDR SRAM supports flexible clocking approaches. C and C# may be supplied to the SRAM to synchronize data output across multiple devices, enabling the bus master to receive all data simultaneously. If C and C# are not provided (tied HIGH) K and K# are used as the output timing reference. The echo clocks (CQ and CQ#) provide another alternative for data synchronization. The echo clocks are controlled exactly like the DQ signals except that CQ and CQ# have an additional small delay for easier data capture by the bus master. Echo clocks must be separately received for each SRAM in the system. Use of echo clocks maximizes the available data window for each SRAM in the system.

Figure 3:
Application Example

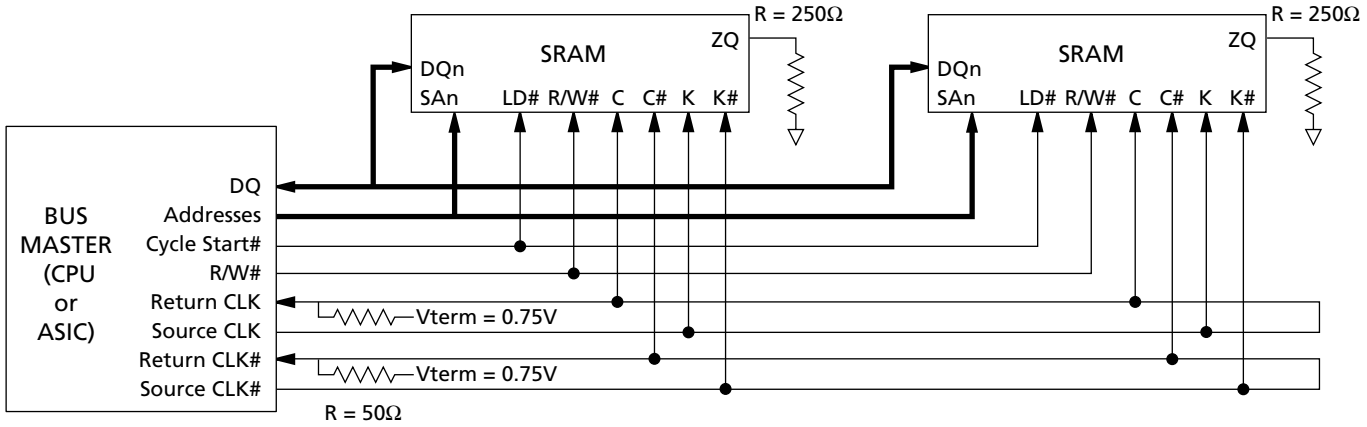


Table 2: Ball Assignment (Top View) 165-BAll FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	VSS/SA[1]	NC/SA[2]	R/W#	NC	K#	NC	LD#	NC/SA[3]	VSS/SA[4]	CQ
B	NC	DQ19	DQ18	SA	NC	K	NC	SA	NC	NC	DQ17
C	NC	NC	DQ20	VSS	SA	SA0	SA1	VSS	NC	DQ15	DQ16
D	NC	DQ22	DQ21	VSS	VSS	VSS	VSS	VSS	NC	NC	DQ14
E	NC	NC	DQ23	VDDQ	VSS	VSS	VSS	VDDQ	NC	DQ12	DQ13
F	NC	DQ25	DQ24	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ11
G	NC	DQ26	DQ27	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ10
H	NC	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	DQ28	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ9	DQ8
K	NC	NC	DQ29	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ6	DQ7
L	NC	DQ31	DQ30	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ5
M	NC	NC	DQ32	VSS	VSS	VSS	VSS	VSS	NC	DQ3	DQ4
N	NC	DQ34	DQ33	VSS	SA	SA	SA	VSS	NC	NC	DQ2
P	NC	NC	DQ35	SA	SA	C	SA	SA	NC	DQ0	DQ1
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

NOTE:
1. Expansion address: 2A for 144Mb
2. Expansion address: 3A for 36Mb
3. Expansion address: 9A for 18Mb
4. Expansion address: 10A for 72Mb

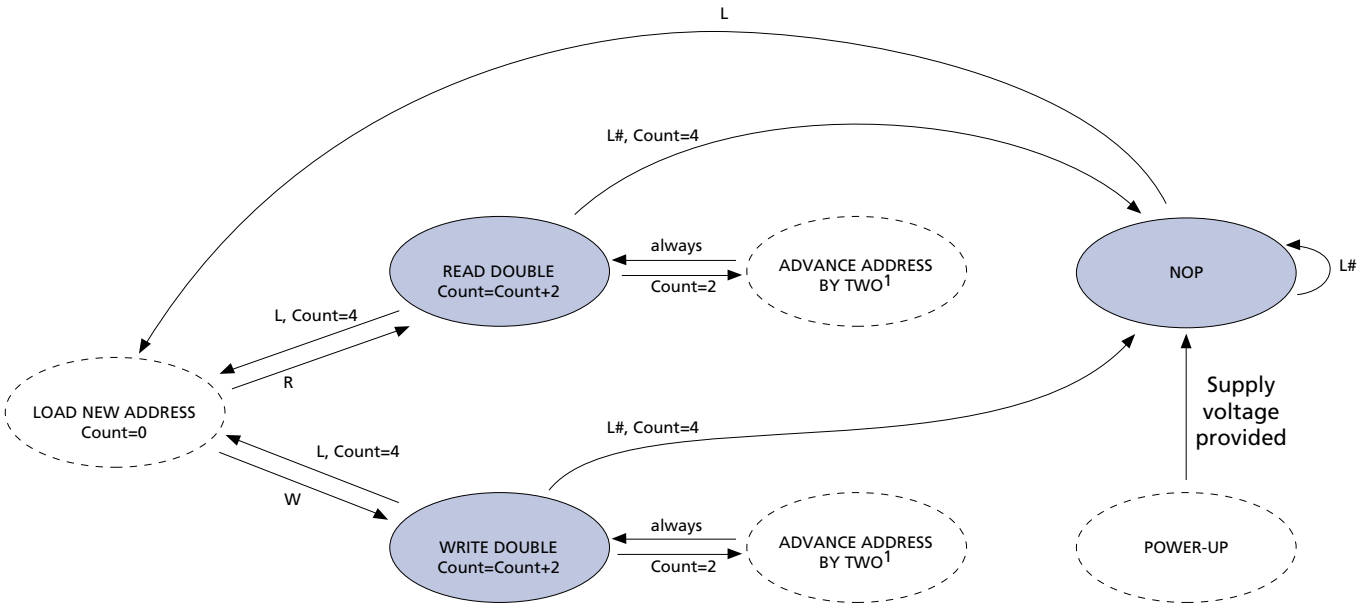
Table 3: Ball Descriptions

SYMBOL	TYPE	DESCRIPTION
SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. See Ball Assignment figures for address expansion inputs. SA0 and SA1 are used as the lowest two address bits for BURST READ and BURST WRITE operations. These inputs are ignored when device is deselected or once BURST operation is in progress.
LD#	Input	Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of four data (two clock periods of bus activity).
R/W#	Input	Synchronous Read/Write Input: When LD# is LOW, this input designates the access type (READ when R/W# is HIGH, WRITE when R/W# is LOW) for the loaded address. R/W# must meet the setup and hold times around the rising edge of K.
K K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
C C#	Input	Output Clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of C# is used as the output reference for second and fourth output data. The rising edge of C is used as the output timing reference for first and third output data. Ideally, C# is 180 degrees out of phase with C. C and C# may be tied HIGH to force the use of K and K# as the output reference clocks instead of having to provide C and C# clocks. If tied HIGH, C and C# must remain HIGH and not be toggled during device operation.
TMS TDI	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 2.5V I/O levels. These balls may be left as No Connects if the JTAG function is not used in the circuit.
TCK	Input	IEEE 1149.1 Clock Input: JEDEC-standard 2.5V I/O levels. This ball must be tied to VSS if the JTAG function is not used in the circuit.
VREF	Input	HSTL Input Reference Voltage: Nominally VDDQ/2. Provides a reference voltage for the input buffers.
ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance is set to 0.2 x RQ, where RQ is a resistor from this ball to ground. Alternately, this ball can be connected directly to VDDQ, which enables the minimum impedance mode. This ball cannot be connected directly to GND or left unconnected.
DQ_	Input/ Output	Synchronous Data I/Os: Input data must meet setup and hold times around the rising edges of K and K#. Output data is synchronized to the respective C and C# data clocks or to K and K# if C and C# are tied HIGH. See Ball Assignment figures for ball site location of individual signals.
TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level.
VDD	Supply	Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Conditions for range.
VDDQ	Supply	Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. See DC Electrical Characteristics and Operating Conditions for range.
VSS	Supply	Power Supply: GND.
NC	–	No Connect: These signals may be connected to ground to improve package heat dissipation. For upgrade to 18, 36, 72, and 144Mb DDR devices, balls 2A, 3A, 9A, and 10A are reserved for higher-order address bits, respectively.
NC/SA		These balls are reserved for higher-order address bits, respectively.

Table 4: Linear Burst Address

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

Figure 4: Bus Cycle State Diagram



NOTE:
1. SA0 and SA1 are internally advanced in accordance with the burst order table. Bus cycle is terminated after burst count = 4.
2. State transitions: L = (LD# = LOW); L# = (LD# = HIGH); R = (R/W# = HIGH); W = (R/W# = LOW).
3. State machine control timing sequence is controlled by K.

Table 5: Truth Table

Notes 1-7

OPERATION	LD#	R/W#	K	DQ	DQ	DQ	DQ
WRITE Cycle: Load address, input write data on two consecutive K and K# rising edges	L	L	L→H	DIN(A1) at K(t + 1)↑	DIN(A2) at K#(t + 1)↑	DIN(A3) at K(t + 2)↑	DIN(A4) at K#(t + 2)↑
READ Cycle: Load address, read data on two consecutive C and C# rising edges	L	H	L→H	QOUT(A1) at C(t + 1)↑	QOUT(A2) at C#(t + 1)↑	QOUT(A3) at C(t + 2)↑	QOUT(A4) at C#(t + 2)↑
NOP: No operation	H	X	L→H	High-Z	High-Z	High-Z	High-Z
STANDBY: Clock stopped	X	X	Stopped	Previous State	Previous State	Previous State	Previous State

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW. ↑ means rising edge; ↓ means falling edge.
2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges, except if C and C# are HIGH, then data outputs are delivered at K and K# rising edges.
3. All control inputs in the truth table must meet setup and hold times around the rising edge (LOW to HIGH) of K. All control inputs are registered during the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. A1 refers to the address input during a WRITE or READ cycle. A2, A3, and A4 refer to the next internal burst address in accordance with the burst sequence.
7. It is recommended that K = /K# = C =/ C# when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

ABSOLUTE MAXIMUM RATINGS

Voltage on VDD Supply Relative to VSS..... -0.5V to +3.6V
Voltage on VDDQ Supply
Relative to VSS..... -0.5V to +VDD
VIN ..... -0.5V to VDD + 0.5V
Storage Temperature ..... -55°C to +125°C
Junction Temperature ..... +125°C
Short Circuit Output Current ..... ±70mA

Table 6: DC Electrical Characteristics And Operating Conditions

Notes appear following parameter tables; 0°C ≤ T_A ≤ +70°C; +2.4V ≤ VDD ≤ +2.6V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.1	VDDQ + 0.3	V	3, 4
Input Low (Logic 0) Voltage		VIL(DC)	-0.3	VREF - 0.1	V	3, 4
Clock Input Signal Voltage		VIN	-0.3	VDDQ + 0.3	V	3, 4
Input Leakage Current	0V ≤ VIN ≤ VDDQ	ILI	-5	5	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (Q)	ILO	-5	5	µA	
Output High Voltage	|IOH| ≤ 0.1mA	VOH (LOW)	VDDQ - 0.2	VDDQ	V	3, 5, 7
	Note 1	VOH	VDDQ/2 - 0.08	VDDQ/2 + 0.08	V	3, 5, 7
Output Low Voltage	IOL ≤ 0.1mA	VOL (LOW)	VSS	0.2	V	3, 5, 7
	Note 2	VOL	VDDQ/2 - 0.08	VDDQ/2 + 0.08	V	3, 5, 7
Supply Voltage		VDD	2.4	2.6	V	3
Isolated Output Buffer Supply		VDDQ	1.4	1.6	V	3, 6
Reference Voltage		VREF	0.68	0.9	V	3

Table 7: AC Electrical Characteristics And Operating Conditions

Notes appear following parameter tables; 0°C ≤ T_A ≤ +70°C; +2.4V ≤ VDD ≤ +2.6V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH(AC)	VREF + 0.2	–	V	3, 4, 8
Input Low (Logic 0) Voltage		VIL(AC)	–	VREF - 0.2	V	3, 4, 8

Table 8: IDD Operating Conditions And Maximum Limits

Notes appear following parameter tables; 0°C ≤ T_A ≤ +70°C; VDD = MAX unless otherwise noted

				MAX			
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-5**	**-6**	**UNITS**	**NOTES**
Operating Supply Current: DDR	All inputs ≤ VIL or ≥ VIH; Cycle time ≥ ^{t}KHKH (MIN); Outputs open	IDD	550	650	550	mA	9, 10, 11
Standby Supply Current: NOP	^{t}KHKH = ^{t}KHKH (MIN); Device in NOP state; All addresses/data static	ISB1	150	225	175	mA	10, 12
Output Supply Current: DDR (Information only)	CL = 15pF	IDDQ	TBD	81	68	mA	13

Table 9: Capacitance

Note 14; notes appear following parameter tables

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	CI	4.5	5.5	pF
Input, Output Capacitance (DQ)		CO	6	7	pF
Clock Capacitance		CCK	5.5	6.5	pF

Table 10: Thermal Resistance

Note 14; notes appear following parameter tables

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ_{JA}	30.9	°C/W	15
Junction to Case (Top)		θ_{JC}	1.0	°C/W	
Junction to Balls (Bottom)		θ_{JB}	9.6	°C/W	16

Table 11: AC Electrical Characteristics And Recommended Operating Conditions

Notes 14, 17-19; notes appear following parameter tables; 0°C ≤ T_A ≤ +70°C; +2.4V ≤ VDD ≤ +2.6V

DESCRIPTION	SYMBOL	-5		-6		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Clock							
Clock cycle time (K, K#, C, C#)	^tKHKH	5.0		6.0		ns	
Clock HIGH time (K, K#, C, C#)	^tKHKL	2.0		2.4		ns	
Clock LOW time (K, K#, C, C#)	^tKLKH	2.0		2.4		ns	
Clock to clock# (K↑→K#↑, C↑→C#↑) at ^tKHKH minimum	$^tKHK\#H$	2.4		2.8		ns	
Clock# to clock (K#↑→K↑, C#↑→C↑)at ^tKHKH minimum	$^tK\#HKH$	2.4		2.8		ns	
Clock to data clock (K↑→C↑, K#↑→C#↑)	^tKHCH	0.0	1.5	0.0	2.0	ns	
Output Times							
C, C# HIGH to output valid	^tCHQV		2.4		3.0	ns	
C, C# HIGH to output hold	^tCHQX	0.8		0.8		ns	
C HIGH to output HIGH-Z	^tCHQZ		2.4		3.0	ns	20, 21
C HIGH to output LOW-Z	$^tCHQX1$	0.8		0.8		ns	20, 21
C, C# HIGH to CQ, CQ# HIGH	^tCHCQH	0.8	2.6	0.8	3.2	ns	
CQ, CQ# HIGH to output valid	^tCHCQV		0.35		0.40	ns	
CQ, CQ# HIGH to output hold	^tCQHQX	-0.35		-0.40		ns	
CQ HIGH to output HIGH-Z	^tCHQQZ		0.35		0.40	ns	20, 21
CQ HIGH to output LOW-Z	$^tCQHQX1$	-0.35		-0.40		ns	20, 21
Setup Times							
Address valid to K rising edge	^tAVKH	0.6		0.7		ns	22
Control inputs valid to K rising edge	^tIVKH	0.6		0.7		ns	22
Data-in valid to K, K# rising edge	^tDVKH	0.6		0.7		ns	22
Hold Times							
K rising edge to address hold	^tKHAX	0.6		0.7		ns	22
K rising edge to control inputs hold	^tKHIX	0.6		0.7		ns	22
K, K# rising edge to data-in hold	^tKHDX	0.6		0.7		ns	22

Notes

1. Outputs are impedance-controlled. |IOH| = (VDDQ/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
2. Outputs are impedance-controlled. IOL = (VDDQ/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
3. All voltages referenced to VSS (GND).
4. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ ^{t}KHKH/2
   Undershoot: VIL(AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
   Power-up: VIH ≤ VDDQ + 0.3V and VDD ≤ 2.4V and VDDQ ≤ 1.4V for t ≤ 200ms
   During normal operation, VDDQ must not exceed VDD. Control input signals may not have pulse widths less than ^{t}KHKL (MIN) or operate at cycle rates less than ^{t}KHKH (MIN).
5. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
6. For higher VDDQ voltages, contact factory for product information.
7. HSTL outputs meet JEDEC HSTL Class I and Class II standards.
8. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, VIL(AC) or VIH(AC)
   b. Reach at least the target AC level
   c. After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC)
9. IDD is specified with no output current and increases with faster cycle times. IDDQ increases with faster cycle times and greater output loading. Typical value is measured at 6ns cycle time.
10. Typical values are measured at VDD =2.5V, VDDQ = 1.5V, and temperature = 25°C.
11. Operating supply currents and burst mode currents are calculated with 50 percent READ cycles and 50 percent WRITE cycles.
12. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.
13. Average I/O current and power is provided for informational purposes only and is not tested. Calculation assumes that all outputs are loaded with CL (in farads), f = input clock frequency, half of outputs toggle at each transition (for example, n = 18 for x36), CO = 6pF, VDDQ = 1.5V and uses the equations: Average I/O Power as dissipated by the SRAM is:
    $P = 0.5 \times n \times f \times V_{DDQ}^2 \times (C_L + 2C_O)$. Average IDDQ = n x f x VDDQ x (CL + CO).
14. This parameter is sampled.
15. Average thermal resistance between the die and the case top surface per MIL SPEC 883 Method 1012.1.
16. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.
17. Control input signals may not be operated with pulse widths less than ^{t}KHKL (MIN).
18. Test conditions as specified with the output loading as shown in Figure 5, unless otherwise noted.
19. If C, C# are tied HIGH, then K, K# become the references for C, C# timing parameters.
20. Transition is measured ±100mV from steady state voltage.
21. ^{t}CHQXI is greater than ^{t}CHQZ at any given voltage and temperature.
22. This is a synchronous device. All addresses, data, and control lines must meet the specified setup and hold times for all latching clock edges.

AC Test Conditions

Input pulse levels	0.25V to 1.25V
Input rise and fall times	0.7ns
Input timing reference levels	0.75V
Output reference levels	VDDQ/2
ZQ for 50Ω impedance	250Ω
Output load	See Figure 5

Figure 5:
Output Load Equivalent

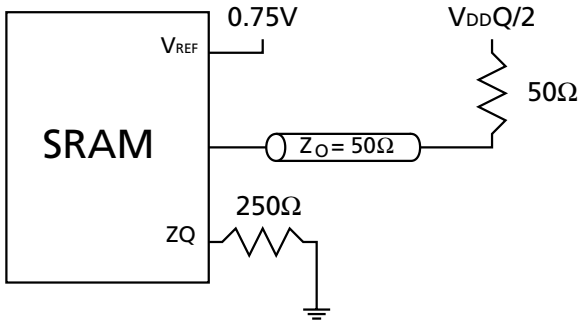
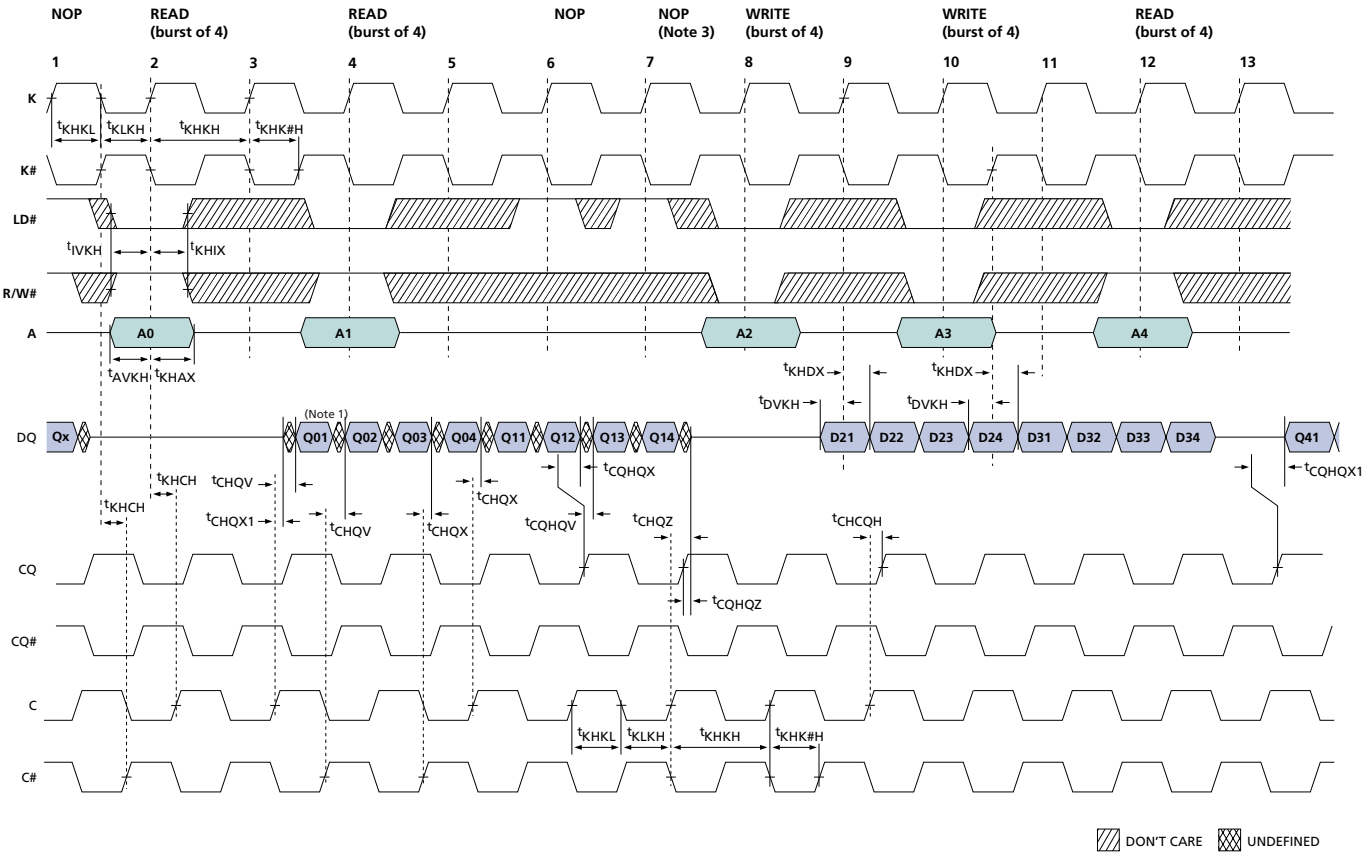


Figure 6:
READ/WRITE Timing



NOTE:

1. Q01 refers to output from address A0 + 0. Q02 refers to output from the next internal burst address following A0, etc.
2. Outputs are disabled (High-Z) one clock cycle after a NOP.
3. The second NOP cycle is not necessary for correct device operation; however, at high-clock frequencies it may be required to prevent bus contention.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The DDR SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-2001 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 1.8V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling The JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. Alternately, they may be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

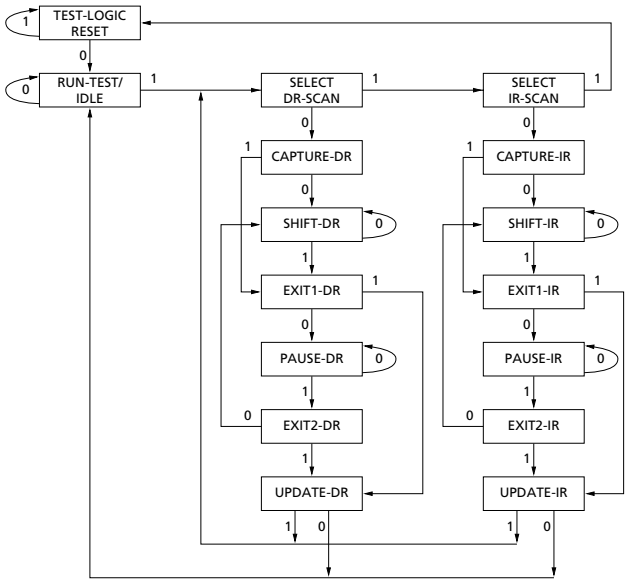
Test Access Port (TAP)
Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Figure 7:
TAP Controller State Diagram



NOTE:
The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

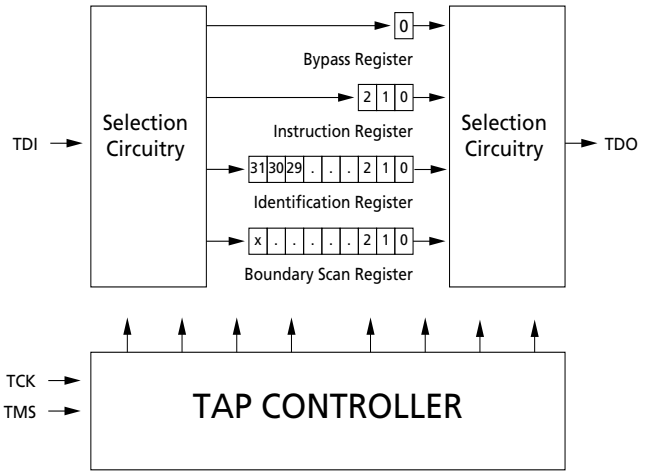
Test Data-in (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 7. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register, as illustrated in Figure 8.

Test Data-out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine illustrated in Figure 7. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register, as depicted in Figure 8.

Figure 8:
TAP Controller Block Diagram



NOTE:

X = 68 for the x36 configuration.

Performing A TAP Reset

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register at a time can be selected through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls, as shown in Figure 8. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several no connect (NC) balls are also included in the scan register to reserve balls. The SRAM has a 69-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift- DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order table shows the order in which the bits are connected. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

Tap Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not

implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register and through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, hence this device is not IEEE 1149.1 compliant.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the

instruction register, the SRAM responds as if a SAMPLE/ PRELOAD instruction has been loaded. EXTEST does not place the SRAM outputs in a High-Z state, including CQ and CQ#.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state, including CQ and CQ#.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bi-directional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the C and C# and K and K# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 9: TAP Timing

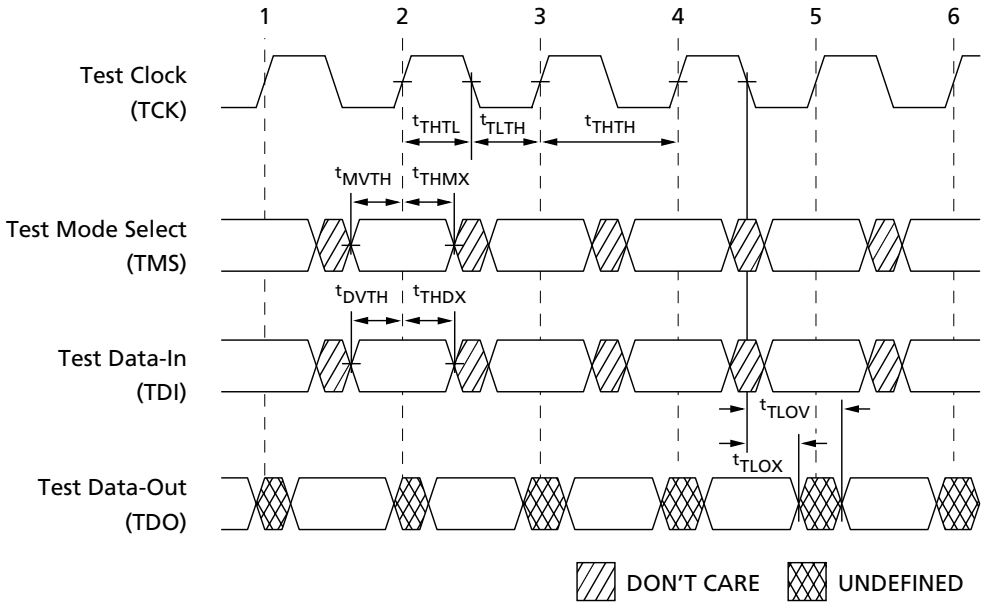


Table 12: TAP AC Characteristics

Notes 1, 2; 0°C ≤ T_A ≤ +70°C; +2.4V ≤ VDD ≤ +2.6V

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

NOTE:

1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 10.

TAP AC Test Conditions

Input pulse levels ..... VSS to 2.5V
Input rise and fall times 1ns
Input timing reference levels 1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

Figure 10: TAP AC Output Load Equivalent

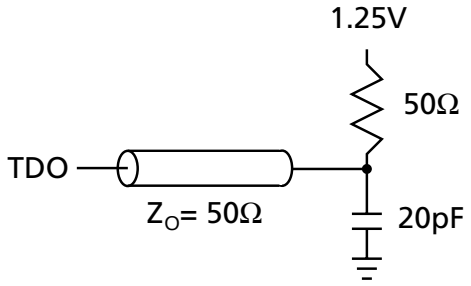


Table 13: TAP DC Electrical Characteristics And Operation Conditions

0°C ≤ T_A ≤ +70°C; +2.4V ≤ VDD ≤ +2.6V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	1.7	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled,	ILO	-5.0	5.0	µA	
	0V ≤ VIN ≤ VDDQ					
Output Low Voltage	IOLC = 100µA	VOL1		0.2	V	1
Output Low Voltage	IOLT = 2mA	VOL2		0.7	V	1
Output High Voltage	|IOHC| = 100µA	VOH1	2.1		V	1
Output High Voltage	|IOHT| = 2mA	VOH2	1.7		V	1

NOTE:

1. All voltages referenced to VSS (GND).
2. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ ^{t}KHKH/2
   Undershoot: VIL(AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
   Power-up: VIH ≤ +2.6 and VDD ≤ +2.4V and VDDQ ≤ 1.4V for t ≤ 200ms
   During normal operation, VDDQ must not exceed VDD. Control input signals (LD#, R/W#, etc.) may not have pulse widths less than ^{t}KHKL (MIN) or operate at frequencies exceeding ^{f}KF (MAX).

Table 14: Identification Register Definitions

INSTRUCTION FIELD	256K x 36	DESCRIPTION
REVISION NUMBER (31:29)	000	Reserved for version number.
DEVICE ID (28:12)	00010100011000000	Defines 256K x 36 DDR 4-word burst.
DEVICE WIDTH (22.18)	00100	Defines width of x36 bits.
MICRON JEDEC ID (17.12)	xxxxxx	Reserved for future use.
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator 0)	1	Indicates the presence of an ID register.

Table 15: Scan Register Size

REGISTER NAME	BIT SIZE (x18)
Instruction	3
Bypass	1
ID	32
Boundary Scan	69

Table 16: Instruction Codes

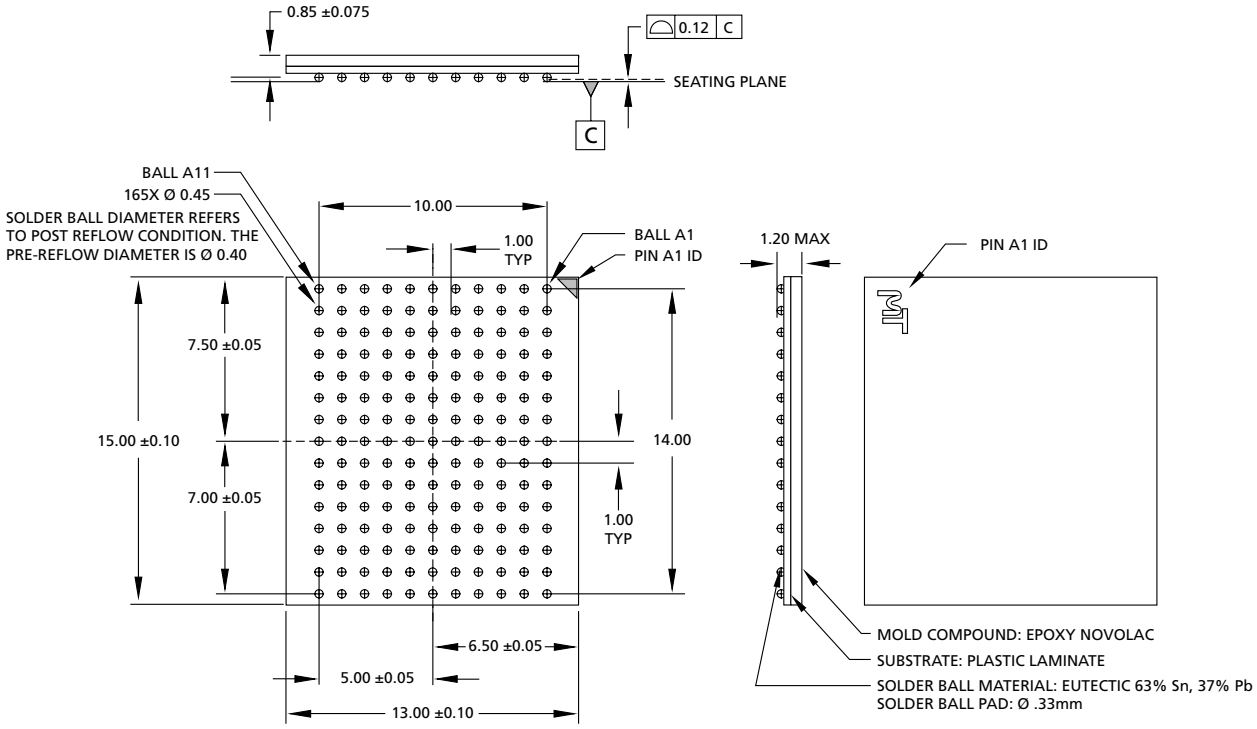
INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction is not 1149.1-compliant. This operation does not affect SRAM operations.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Table 17: Boundary Scan (Exit) Order

BIT#	SIGNAL NAME	BALL ID
1	C#	6R
2	C	6P
3	SA	6N
4	SA	7P
5	SA	7N
6	SA	7R
7	SA	8R
8	SA	8P
9	SA	9R
10	DQ0	10P
11	DQ1	11P
12	DQ2	11N
13	DQ3	10M
14	DQ4	11M
15	DQ5	11L
16	DQ6	10K
17	DQ7	11K
18	DQ8	11J
19	ZQ	11H
20	DQ9	10J
21	DQ10	11G
22	DQ11	11F
23	DQ12	10E
24	DQ13	11E
25	DQ14	11D
26	DQ15	10C
27	DQ16	11C
28	DQ17	11B
29	CQ	11A
30	GND/SA20	10A; reads as 0
31	NC/SA18	9A; reads as 1
32	SA	8B
33	SA1	7C
34	SA0	6C
35	LD#	8A

BIT#	SIGNAL NAME	BALL ID
36	NC	7B; reads as X
37	K	6B
38	K#	6A
39	NC	5A; reads as X
40	R/W#	4A
41	SA	5C
42	SA	4B
43	NC/A19	3A; reads as 1
44	GND/A21	2A; reads as 0
45	CQ#	1A
46	DQ18	3B
47	DQ19	2B
48	DQ20	3C
49	DQ21	3D
50	DQ22	2D
51	DQ23	3E
52	DQ24	3F
53	DQ25	2F
54	DQ26	2G
55	DQ27	3G
56	DQ28	3J
57	DQ29	3K
58	DQ30	3L
59	DQ31	2L
60	DQ32	3M
61	DQ33	3N
62	DQ34	2N
63	DQ35	3P
64	SA	3R
65	SA	4R
66	SA	4P
67	SA	5P
68	SA	5N
69	SA	5R

Figure 11:
165-Ball FBGA



NOTE:
All dimensions are in millimeters.

DATA SHEET DESIGNATION

Advance: This data sheet contains initial descriptions of products still under development.

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Revision History

- Updated Capacitance values, Rev. B, Pub. 1/03 ..... 1/03
  CI = 4.5 TYP; 5.5 MAX
  CO = 6 TYP; 7 MAX
  CCK = 5.5 TYP; 6.5 MAX
- Updated Thermal Resistance values:
  JA = 30.0 TYP
  JC = 1.0 TYP
  JB = 9.6 TYP
- Removed ISB (Stop Clock Current) from IDD table
- New ADVANCE data sheet for 0.16µm process, Rev. A, Pub. 10 /02 ..... 10/02