FLASH AND SRAM COMBO MEMORY

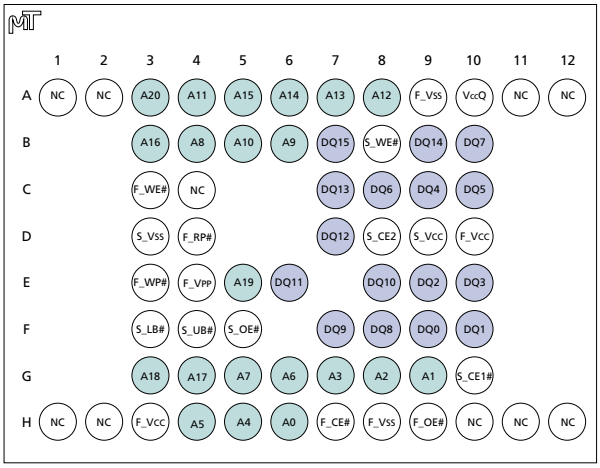
MT28C3214P2FL
MT28C3214P2NFL

Low Voltage, Extended Temperature

FEATURES

- Flexible dual-bank architecture
- Support for true concurrent operations with no latency:
  Read bank *b* during program bank *a* and vice versa
  Read bank *b* during erase bank *a* and vice versa
- Organization: 2,048K x 16 (Flash)
  256K x 16 (SRAM)
- Basic configuration:
  Flash
  Bank *a* (4Mb Flash for data storage)
  – Eight 4K-word parameter blocks
  – Seven 32K-word blocks
  Bank *b* (28Mb Flash for program storage)
  – Fifty-six 32K-word main blocks
  SRAM
  4Mb SRAM for data storage
  – 256K-words
- F_VCC, VCCQ, F_VPP, S_VCC voltages[1]
  1.65V (MIN)/1.95V (MAX) F_VCC read voltage or
  1.80V (MIN)/2.20V (MAX) F_VCC read voltage
  1.65V (MIN)/1.95V (MAX) S_VCC read voltage or
  1.80V (MIN)/2.20V (MAX) S_VCC read voltage
  1.65V (MIN)/1.95V (MAX) VCCQ or
  1.80V (MIN)/2.20V (MAX) VCCQ
  1.80V (TYP) F_VPP (in-system PROGRAM/ERASE)
  0.0V (MIN)/2.20V (MAX) F_VPP (in-system PROGRAM/ERASE)[2]
  12V ±5% (HV) F_VPP (production programming compatibility)
- Asynchronous access time[1]
  Flash access time: 100ns or 110ns @ 1.65V F_VCC
  SRAM access time: 100ns @ 1.65V S_VCC
- Page Mode read access[1]
  Interpage read access: 100ns/110ns @ 1.65V F_VCC
  Intrapage read access: 35ns/45ns @ 1.65V F_VCC
- Low power consumption
- Enhanced suspend options
  ERASE-SUSPEND-to-READ within same bank
  PROGRAM-SUSPEND-to-READ within same bank
  ERASE-SUSPEND-to-PROGRAM within same bank
- Read/Write SRAM during program/erase of Flash
- Dual 64-bit chip protection registers for security purposes
- PROGRAM/ERASE cycles
  100,000 WRITE/ERASE cycles per block

BALL ASSIGNMENT
66-Ball FBGA (Top View)



Top View
(Ball Down)

- Cross-compatible command set support
  Extended command set
  Common flash interface (CFI) compliant

NOTE: 1. These specifications are guaranteed for operation within either one of two voltage ranges, 1.65V–1.95V or 1.80V–2.20V. Use only one of the two voltage ranges for PROGRAM and ERASE operations.
2. MT28C3214P2NFL only.

OPTIONS — MARKING

- Timing
  100ns — -10
  110ns — -11
- Boot Block
  Top — T
  Bottom — B
- VPP1 Range
  0.9V–2.2V — None
  0.0V–2.2V — N
- Operating Temperature Range
  Commercial Temperature (0°C to +70°C) — None
  Extended Temperature (-40°C to +85°C) — ET
- Package
  66-ball FBGA (8 x 8 grid) — FL

Part Number Example:
MT28C3214P2FL-10 TET

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GENERAL DESCRIPTION

The MT28C3214P2FL and MT28C3214P2NFL combination Flash and SRAM memory devices provide a compact, low-power solution for systems where PCB real estate is at a premium. The dual-bank Flash is a high-performance, high-density, nonvolatile memory device with a revolutionary architecture that can significantly improve system performance.

This new architecture features:

- A two-memory-bank configuration supporting dual-bank burst operation;
- A high-performance bus interface providing a fast page data transfer; and
- A conventional asynchronous bus interface.

The device also provides soft protection for blocks by configuring soft protection registers with dedicated command sequences. For security purposes, dual 64-bit chip protection registers are provided.

The embedded WORD WRITE and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). The WSM simplifies these operations and relieves the system processor of secondary tasks. An on-chip status register, one for each bank, can be used to monitor the WSM status to determine the progress of a PROGRAM/ERASE command.

The erase/program suspend functionality allows compatibility with existing EEPROM emulation software packages.

The device takes advantage of a dedicated power source for the Flash device (F_V_{CC}) and a dedicated power source for the SRAM device (S_V_{CC}), both at 1.65V–1.95V or 1.80V–2.20V for optimized power consumption and improved noise immunity. The MT28C3214P2FL and MT28C3214P2NFL devices support two V_{PP} voltage ranges, V_{PP1} and V_{PP2}. V_{PP1} is an in-circuit voltage of 0.9V–2.2V (MT28C3214P2FL) or 0.0V–2.2V (MT28C3214P2NFL). V_{PP2} is the production compatibility voltage of 12V ±5%. The 12V ±5% V_{PP2} is supported for a maximum of 100 cycles and 10 cumulative hours. See Table 1.

The MT28C3214P2FL and MT28C3214P2NFL devices contain an asynchronous 4Mb SRAM organized as 256K-words by 16 bits. These devices are fabricated using an advanced CMOS process and high-speed/ultra-low-power circuit technology.

The MT28C3214P2FL and MT28C3214P2NFL devices are packaged in a 66-ball FBGA package with 0.80mm pitch.

DEVICE MARKING

Due to the size of the package, Micron's standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross referenced to Micron part numbers in Table 2.

ARCHITECTURE AND MEMORY ORGANIZATION

The Flash memory device contains two separate memory banks (bank *a* and bank *b*) for simultaneous READ and WRITE operations. Bank *a* is 4Mb deep and contains 8 x 4K-word parameter blocks and seven 32K-word blocks. Bank *b* is 28Mb deep, is equally sectored, and contains fifty-six 32K-word blocks.

Figures 2 and 3 show the top and bottom memory organizations.

Table 1
V_{PP} Voltage Ranges

DEVICE	VOLTAGE RANGE	
	V_{PP1}	V_{PP2}
MT28C3214P2FL	0.9V–2.2V	11.4V–12.6V
MT28C3214P2NFL	0.0V–2.2V	11.4V–12.6V

Table 2
Cross Reference for Abbreviated Device Marks

PART NUMBER	PRODUCT MARKING	SAMPLE MARKING	MECHANICAL SAMPLE MARKING
MT28C3214P2FL-10 BET	FW420	FX420	FY420
MT28C3214P2FL-10 TET	FW421	FX421	FY421
MT28C3214P2FL-11 BET	FW437	FX437	FY437
MT28C3214P2FL-11 TET	FW431	FX431	FY431
MT28C3214P2NFL-11 TET	FW439	FX439	FY439

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PART NUMBERING INFORMATION

Micron's low-power devices are available with several different combinations of features (see Figure 1). Valid combinations of features and their corresponding part numbers are listed in Table 3.

Figure 1
Part Number Chart

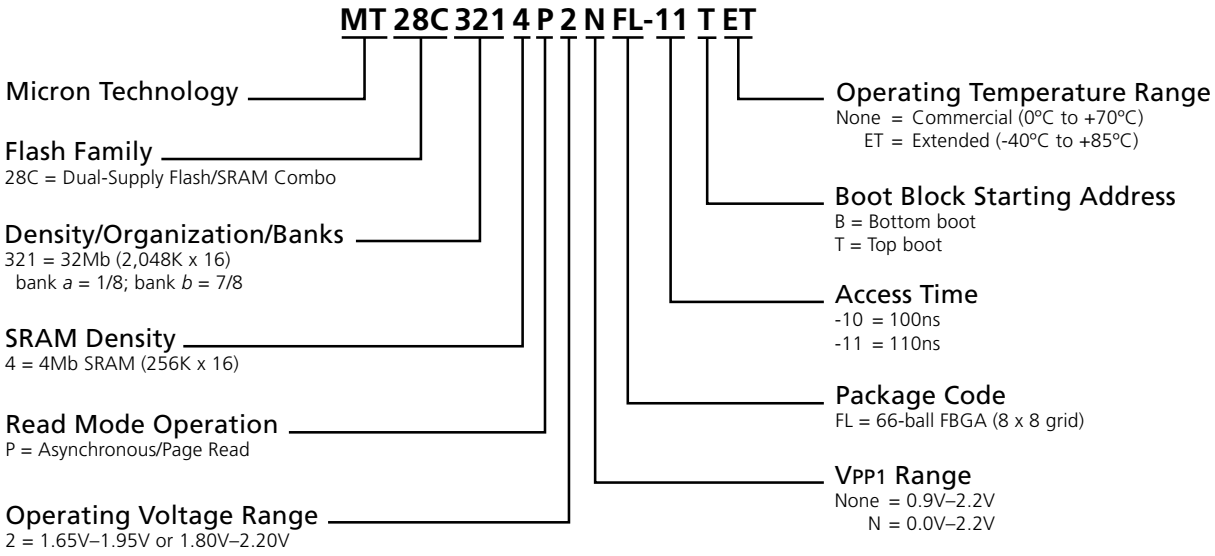

Table 3
Valid Part Number Combinations

PART NUMBER	V_{PP1} RANGE	ACCESS TIME (ns)	BOOT BLOCK STARTING ADDRESS	OPERATING TEMPERATURE RANGE
MT28C3214P2FL-10 BET	0.9V–2.2V	100	Bottom	-40°C to +85°C
MT28C3214P2FL-10 TET	0.9V–2.2V	100	Top	-40°C to +85°C
MT28C3214P2FL-11 BET	0.9V–2.2V	110	Bottom	-40°C to +85°C
MT28C3214P2FL-11 TET	0.9V–2.2V	110	Top	-40°C to +85°C
MT28C3214P2NFL-11 TET	0.0V–2.2V	110	Top	-40°C to +85°C

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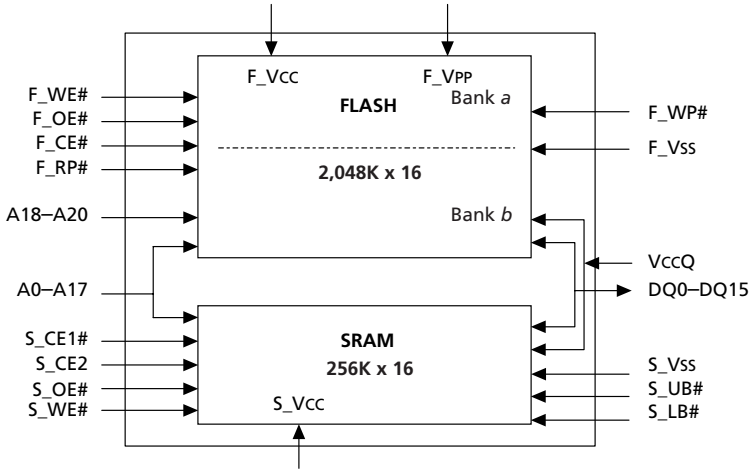
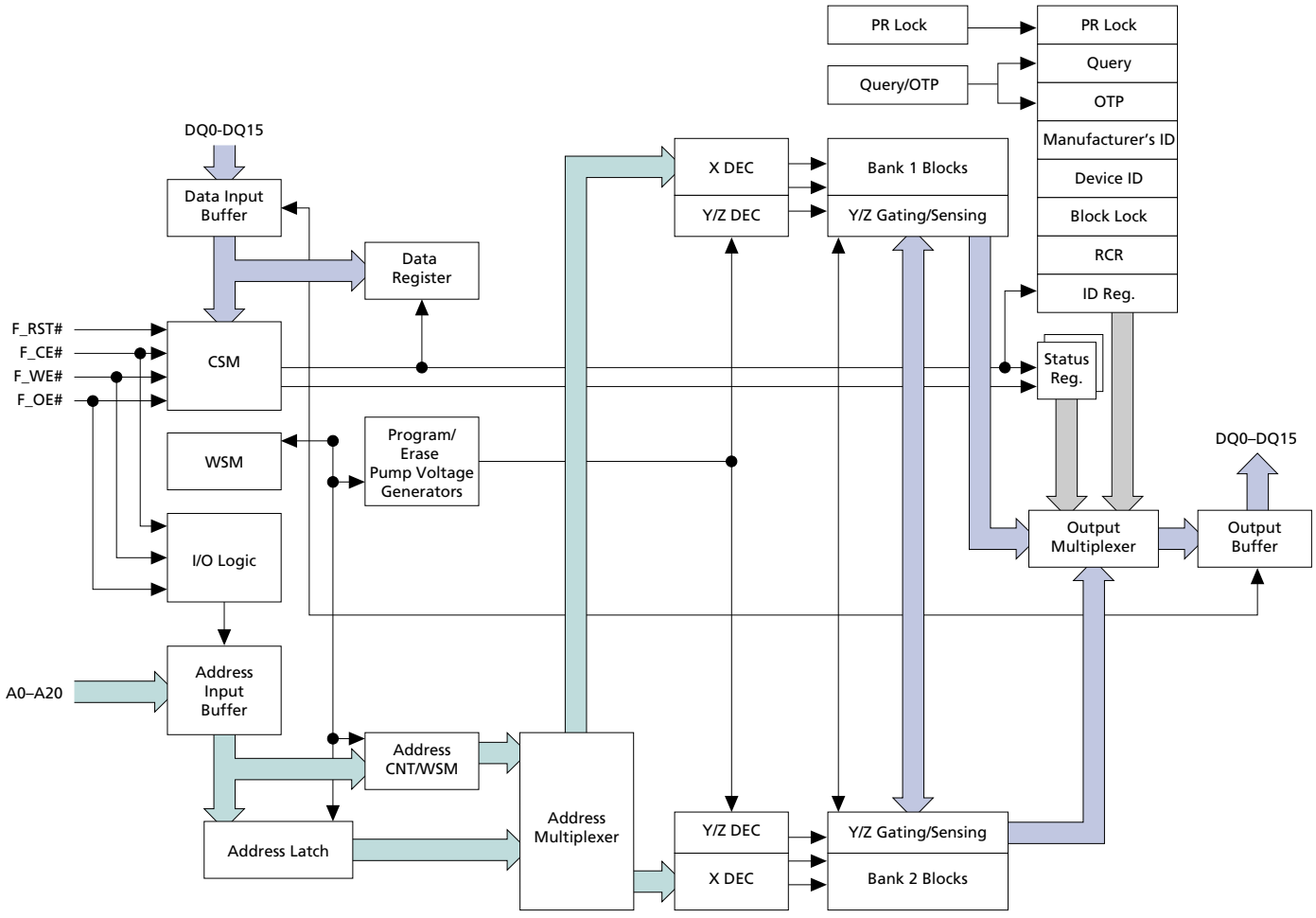
BLOCK DIAGRAM



FLASH FUNCTIONAL BLOCK DIAGRAM



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BALL DESCRIPTIONS

66-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
A3, A4, A5, A6, A7, A8, B3, B4, B5, B6, E5, G3, G4, G5, G6, G7, G8, G9, H4, H5, H6	A0–A20	Input	Address Inputs: Inputs for the addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. Flash: A0–A20; SRAM: A0–A17.
H7	F_CE#	Input	Flash Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
H9	F_OE#	Input	Flash Output Enable: Enables Flash output buffers when LOW. When F_OE# is HIGH, the output buffers are disabled.
C3	F_WE#	Input	Flash Write Enable: Determines if a given cycle is a Flash WRITE cycle. F_WE# is active LOW.
D4	F_RP#	Input	Reset. When F_RP# is a logic LOW, the device is in reset, which drives the outputs to High-Z and resets the WSM. When F_RP# is a logic HIGH, the device is in standard operation. When F_RP# transitions from logic LOW to logic HIGH, the device resets all blocks to locked and defaults to the read array mode.
E3	F_WP#	Input	Flash Write Protect. Controls the lock down function of the flexible locking feature.
G10	S_CE1#	Input	SRAM Chip Enable1: Activates the SRAM when it is LOW. HIGH level deselects the SRAM and reduces the power consumption to standby levels.
D8	S_CE2	Input	SRAM Chip Enable2: Activates the SRAM when it is HIGH. LOW level deselects the SRAM and reduces the power consumption to standby levels.
F5	S_OE#	Input	SRAM Output Enable: Enables SRAM output buffers when LOW. When S_OE# is HIGH, the output buffers are disabled.
B8	S_WE#	Input	SRAM Write Enable: Determines if a given cycle is an SRAM WRITE cycle. S_WE# is active LOW.
F3	S_LB#	Input	SRAM Lower Byte: When LOW, it selects the SRAM address lower byte (DQ0–DQ7).
F4	S_UB#	Input	SRAM Upper Byte: When LOW, it selects the SRAM address upper byte (DQ8–DQ15).
B7, B9, B10, C7, C8, C9, C10, D7, E6, E8, E9, E10, F7, F8, F9, F10	DQ0–DQ15	Input/ Output	Data Inputs/Outputs: Input array data on the second CE# and WE# cycle during PROGRAM command. Input commands to the command user interface when CE# and WE# are active. Output data when CE# and OE# are active.

(continued on next page)

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BALL DESCRIPTIONS (continued)

66-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
E4	F_V_{PP}	Input/ Supply	Flash Program/Erase Power Supply: [0.9V–2.2V or 11.4V–12.6V]. Operates as input at logic levels to control complete device protection. Provides backward compatibility for factory programming when driven to 11.4V–12.6V. A lower F_V_{PP} voltage range (0.0V–2.2V) is available on the MT28C3214P2NFL device.
D10, H3	F_V_{CC}	Supply	Flash Power Supply: [1.65V–1.95V or 1.80V–2.20V]. Supplies power for device operation.
A9, H8	F_V_{SS}	Supply	Flash Specific Ground: Do not float any ground pin.
D9	S_V_{CC}	Supply	SRAM Power Supply: [1.65V–1.95V or 1.80V–2.20V]. Supplies power for device operation.
D3	S_V_{SS}	Supply	SRAM Specific Ground: Do not float any ground pin.
A10	$V_{CC}Q$	Supply	I/O Power Supply: [1.65–1.95V or 1.80V–2.20V]. This input should be tied directly to V_{CC}.
A1, A2, A11, A12, C4, H1, H2, H10, H11, H12	NC	–	No Connect: Lead is not internally connected; it may be driven or floated.

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TRUTH TABLE – FLASH

MODES	FLASH SIGNALS				SRAM SIGNALS						MEMORY OUPUT		NOTES
	F_RP#	F_CE#	F_OE#	F_WE#	S_CE1#	S_CE2	S_OE#	S_WE#	S_UB#	S_LB#	MEMORY BUS CONTROL	DQ0–DQ15	
Read	H	L	L	H	SRAM must be High-Z						Flash	DOUT	1, 2, 3
Write	H	L	H	L							Flash	DIN	1
Standby	H	H	X	X	SRAM any mode allowable						Other	High-Z	4
Output Disable	H	L	H	H							Other	High-Z	4, 5
Reset	L	X	X	X							Other	High-Z	4, 6

TRUTH TABLE – SRAM

MODES	FLASH SIGNALS				SRAM SIGNALS						MEMORY OUPUT		NOTES
	F_RP#	F_CE#	F_OE#	F_WE#	S_CE1#	S_CE2	S_OE#	S_WE#	S_UB#	S_LB#	MEMORY BUS CONTROL	DQ0–DQ15	
Read	Flash must be High-Z												
DQ0–DQ15					L	H	L	H	L	L	SRAM	DOUT	1, 3
DQ0–DQ7					L	H	L	H	H	L	SRAM	DOUT LB	7
DQ8–DQ15					L	H	L	H	L	H	SRAM	DOUT UB	8
Write													
DQ0–DQ15					L	H	H	L	L	L	SRAM	DIN	1, 3
DQ0–DQ7					L	H	H	L	H	L	SRAM	DIN LB	9
DQ8–DQ15					L	H	H	L	L	H	SRAM	DIN UB	10
Standby	Flash any mode allowable				H	X	X	X	X	X	Other	High-Z	4
					X	L	X	X	X	X	Other	High-Z	4
Output Disable					L	H	X	X	X	X	Other	High-Z	4

NOTE:
1. Two devices may not drive the memory bus at the same time.
2. Allowable flash read modes include read array, read query, read configuration, and read status.
3. Outputs are dependent on a separate device controlling bus outputs.
4. Modes of the Flash and SRAM can be interleaved so that while one is disabled, the other controls outputs.
5. SRAM is enabled and/or disabled with the logical function: S_CE1# or S_CE2.
6. Simultaneous operations can exist, as long as the operations are interleaved such that only one device attempts to control the bus outputs at a time.
7. Data output on lower byte only; upper byte High-Z.
8. Data output on upper byte only; lower byte High-Z.
9. Data input on lower byte only.
10. Data input on upper byte only.

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Figure 2
Bottom Boot Block Device

Bank *b* = 28Mb		
Block	**Block Size (K-bytes/K-words)**	**Address Range (x16)**
70	64/32	1F8000h-1FFFFFh
69	64/32	1F0000h-1F7FFFh
68	64/32	1E8000h-1EFFFFh
67	64/32	1E0000h-1E7FFFh
66	64/32	1D8000h-1DFFFFh
65	64/32	1D0000h-1D7FFFh
64	64/32	1C8000h-1CFFFFh
63	64/32	1C0000h-1C7FFFh
62	64/32	1B8000h-1BFFFFh
61	64/32	1B0000h-1B7FFFh
60	64/32	1A8000h-1AFFFFh
59	64/32	1A0000h-1A7FFFh
58	64/32	198000h-19FFFFh
57	64/32	190000h-197FFFh
56	64/32	188000h-18FFFFh
55	64/32	180000h-187FFFh
54	64/32	178000h-17FFFFh
53	64/32	170000h-177FFFh
52	64/32	168000h-16FFFFh
51	64/32	160000h-167FFFh
50	64/32	158000h-15FFFFh
49	64/32	150000h-157FFFh
48	64/32	148000h-14FFFFh
47	64/32	140000h-147FFFh
46	64/32	138000h-13FFFFh
45	64/32	130000h-137FFFh
44	64/32	128000h-12FFFFh
43	64/32	120000h-127FFFh
42	64/32	118000h-11FFFFh
41	64/32	110000h-117FFFh
40	64/32	108000h-10FFFFh
39	64/32	100000h-107FFFh
38	64/32	0F8000h-0FFFFFh
37	64/32	0F0000h-0F7FFFh
36	64/32	0E8000h-0EFFFFh
35	64/32	0E0000h-0E7FFFh
34	64/32	0D800h-0DFFFFh
33	64/32	0D0000h-0D7FFFh
32	64/32	0C8000h-0CFFFFh
31	64/32	0C0000h-0C7FFFh
30	64/32	0B8000h-0BFFFFh
29	64/32	0B0000h-0B7FFFh
28	64/32	0A8000h-0AFFFFh
27	64/32	0A0000h-0A7FFFh
26	64/32	098000h-097FFFh
25	64/32	090000h-097FFFh
24	64/32	088000h-087FFFh
23	64/32	080000h-087FFFh
22	64/32	078000h-07FFFFh
21	64/32	070000h-077FFFh
20	64/32	068000h-067FFFh
19	64/32	060000h-067FFFh
18	64/32	058000h-05FFFFh
17	64/32	050000h-057FFFh
16	64/32	048000h-04FFFFh
15	64/32	040000h-047FFFh

Bank *a* = 4Mb		
Block	**Block Size (K-bytes/K-words)**	**Address Range (x16)**
14	64/32	038000h-03FFFFh
13	64/32	030000h-037FFFh
12	64/32	028000h-02FFFFh
11	64/32	020000h-027FFFh
10	64/32	018000h-01FFFFh
9	64/32	010000h-017FFFh
8	64/32	008000h-00FFFFh
7	8/4	007000h-007FFFh
6	8/4	006000h-006FFFh
5	8/4	005000h-005FFFh
4	8/4	004000h-004FFFh
3	8/4	003000h-003FFFh
2	8/4	002000h-002FFFh
1	8/4	001000h-001FFFh
0	8/4	000000h-000FFFh

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Figure 3
Top Boot Block Device

Bank *a* = 4Mb		
Block	**Block Size (K-bytes/K-words)**	**Address Range (x16)**
70	8/4	1FF000h-1FFFFFh
69	8/4	1FE000h-1FEFFFh
68	8/4	1FD000h-1FDFFFh
67	8/4	1FC000h-1FCFFFh
66	8/4	1FB000h-1FBFFFh
65	8/4	1FA000h-1FAFFFh
64	8/4	1F9000h-1F9FFFh
63	8/4	1F8000h-1F8FFFh
62	64/32	1F0000h-1F7FFFh
61	64/32	1E8000h-1EFFFFh
60	64/32	1E0000h-1E7FFFh
59	64/32	1D8000h-1DFFFFh
58	64/32	1D0000h-1D7FFFh
57	64/32	1C8000h-1CFFFFh
56	64/32	1C0000h-1C7FFFh

Bank *b* = 28Mb		
Block	**Block Size (K-bytes/K-words)**	**Address Range (x16)**
55	64/32	1B8000h-1BFFFFh
54	64/32	1B0000h-1B7FFFh
53	64/32	1A8000h-1AFFFFh
52	64/32	1A0000h-1A7FFFh
51	64/32	198000h-19FFFFh
50	64/32	190000h-197FFFh
49	64/32	188000h-18FFFFh
48	64/32	180000h-187FFFh
47	64/32	178000h-17FFFFh
46	64/32	170000h-177FFFh
45	64/32	168000h-16FFFFh
44	64/32	160000h-167FFFh
43	64/32	158000h-15FFFFh
42	64/32	150000h-157FFFh
41	64/32	148000h-14FFFFh
40	64/32	140000h-147FFFh
39	64/32	138000h-13FFFFh
38	64/32	130000h-137FFFh
37	64/32	128000h-12FFFFh
36	64/32	120000h-127FFFh
35	64/32	118000h-11FFFFh
34	64/32	110000h-117FFFh
33	64/32	108000h-10FFFFh
32	64/32	100000h-107FFFh
31	64/32	0F8000h-0FFFFFh
30	64/32	0F0000h-0F7FFFh
29	64/32	0E8000h-0EFFFFh
28	64/32	0E0000h-0E7FFFh
27	64/32	0D8000h-0DFFFFh
26	64/32	0D0000h-0D7FFFh
25	64/32	0C8000h-0CFFFFh
24	64/32	0C0000h-0C7FFFh
23	64/32	0B8000h-0BFFFFh
22	64/32	0B0000h-0B7FFFh
21	64/32	0A8000h-0AFFFFh
20	64/32	0A0000h-0A7FFFh
19	64/32	098000h-09FFFFh
18	64/32	090000h-097FFFh
17	64/32	088000h-08FFFFh
16	64/32	080000h-087FFFh
15	64/32	078000h-07FFFFh
14	64/32	070000h-077FFFh
13	64/32	068000h-06FFFFh
12	64/32	060000h-067FFFh
11	64/32	058000h-05FFFFh
10	64/32	050000h-057FFFh
9	64/32	048000h-04FFFFh
8	64/32	040000h-047FFFh
7	64/32	038000h-03FFFFh
6	64/32	030000h-037FFFh
5	64/32	028000h-02FFFFh
4	64/32	020000h-027FFFh
3	64/32	018000h-01FFFFh
2	64/32	010000h-017FFFh
1	64/32	008000h-00FFFFh
0	64/32	000000h-007FFFh

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FLASH MEMORY OPERATING MODES

COMMAND STATE MACHINE

Commands are issued to the command state machine (CSM) using standard microprocessor write timings. The CSM acts as an interface between external microprocessors and the internal write state machine (WSM). The available commands are listed in Table 4, their definitions are given in Table 5 and their descriptions in Table 6. Program and erase algorithms are automated by the on-chip WSM. For more specific information about the CSM transition states, see Micron technical note TN-28-33, "Command State Machine Description and Command Definition."

Once a valid PROGRAM/ERASE command is entered, the WSM executes the appropriate algorithm, which generates the necessary timing signals to control the device internally. A command is valid only if the exact sequence of WRITEs is completed. After the WSM completes its task, the write state machine status (WSMS) bit (SR7) (see Table 8) is set to a logic HIGH level (V_{IH}), allowing the CSM to respond to the full command set again.

OPERATIONS

Device operations are selected by entering a standard JEDEC 8-bit command code with conventional microprocessor timings into an on-chip CSM through I/Os DQ0–DQ7. The number of bus cycles required to activate a command is typically one or two. The first operation is always a WRITE. Control signals F_CE# and F_WE# must be at a logic LOW level (V_{IL}), and F_OE# and F_RP# must be at logic HIGH (V_{IH}). The second operation, when needed, can be a WRITE or a READ depending upon the command. During a READ operation, control signals F_CE# and F_OE# must be at a logic LOW level (V_{IL}), and F_WE# and F_RP# must be at logic HIGH (V_{IH}).

Table 7 illustrates the bus operations for all the modes: write, read, reset, standby, and output disable.

When the device is powered up, internal reset circuitry initializes the chip to a read array mode of operation. Changing the mode of operation requires that a command code be entered into the CSM. For each one of the two Flash memory partitions, an on-chip status register is available. These two registers allow the monitoring of the progress of various operations that can take place on a memory bank. One of the two status registers is interrogated by entering a READ STATUS REGISTER command onto the CSM (cycle 1), specifying an address within the memory partition boundary, and reading the register data on I/O pins DQ0–DQ7 (cycle 2). Status register bits SR0-SR7 correspond to DQ0–DQ7 (see Table 8).

COMMAND DEFINITION

Once a specific command code has been entered, the WSM executes an internal algorithm, generating the necessary timing signals to program, erase, and verify data. See Table 5 for the CSM command definitions and data for each of the bus cycles.

STATUS REGISTER

The status register allows the user to determine whether the state of a PROGRAM/ERASE operation is pending or complete. The status register is monitored by toggling F_OE# and F_CE# and reading the resulting status code on I/Os DQ0–DQ7. The high-order I/Os (DQ8–DQ15) are set to 00h internally, so only the low-

Table 4
Command State Machine Codes For Device Mode Selection

COMMAND DQ0–DQ7	CODE ON DEVICE MODE
40h/10h	Program setup/alternate program setup
20h	Block erase setup
50h	Clear status register
60h	Protection configuration setup
70h	Read status register
90h	Read protection configuration register
98h	Read query
B0h	Program/erase suspend
C0h	Protection register program/lock
D0h	Program/erase resume – erase confirm
FFh	Read array

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order I/O signals (DQ0–DQ7) need to be interpreted. Address lines select the status register pertinent to the selected memory partition.

Register data is updated and latched on the rising edge of F_OE# or F_CE#, whichever occurs first. The latest falling edge of either of these two signals updates the latch within a given READ cycle. Latching the data prevents errors from occurring if the register input changes during a status register read.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSM status. Table 8 defines the status register bits.

After monitoring the status register during a PROGRAM/ERASE operation, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

COMMAND STATE MACHINE OPERATIONS

The CSM decodes instructions for the commands listed in Table 4. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 5 for command definitions). During a PROGRAM or ERASE cycle, the CSM informs the WSM that a PROGRAM or ERASE cycle has been requested.

During a PROGRAM cycle, the WSM controls the program sequences and the CSM responds to a PROGRAM SUSPEND command only.

During an ERASE cycle, the CSM responds to an ERASE SUSPEND command only. When the WSM has completed its task, the WSMS bit (SR7) is set to a logic HIGH level and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an ERASE or PROGRAM operation only when V_{PP} is within its correct voltage range.

Table 5
Command Definitions

	FIRST BUS CYCLE			SECOND BUS CYCLE		
COMMAND	OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA
READ ARRAY	WRITE	WA	FFh			
READ PROTECTION CONFIGURATION REGISTER	WRITE	IA	90h	READ	IA	ID
READ STATUS REGISTER	WRITE	BA	70h	READ	BA	SRD
CLEAR STATUS REGISTER	WRITE	BA	50h			
READ QUERY	WRITE	QA	98h	READ	QA	QD
BLOCK ERASE SETUP	WRITE	BA	20h	WRITE	BA	D0h
PROGRAM SETUP/ALTERNATE PROGRAM SETUP	WRITE	WA	40h/10h	WRITE	WA	WD
PROGRAM/ERASE SUSPEND	WRITE	BA	B0h			
PROGRAM/ERASE RESUME – ERASE CONFIRM	WRITE	BA	D0h			
LOCK BLOCK	WRITE	BA	60h	WRITE	BA	01h
UNLOCK BLOCK	WRITE	BA	60h	WRITE	BA	D0h
LOCK DOWN BLOCK	WRITE	BA	60h	WRITE	BA	2Fh
PROTECTION REGISTER PROGRAM	WRITE	PA	C0h	WRITE	PA	PD
PROTECTION REGISTER LOCK	WRITE	LPA	C0h	WRITE	LPA	FFFDh

NOTE: 1. WA: Word address of memory location to be written, or read
2. IA: Identification code address
3. BA: Address within the block
4. ID: Identification code data
5. SRD: Data read from the status register
6. QA: Query code address
7. QD: Query code data
8. WD: Data to be written at the location WA
9. PA: Protection register address
10. LPA: Lock protection register address
11. PD: Protection register data

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Table 6
Command Descriptions

CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
10h	Alt. Program Setup	First	Operates the same as a PROGRAM SETUP command.
20h	Erase Setup	First	Prepares the CSM for an ERASE CONFIRM command. If the next command is not ERASE CONFIRM, the CSM sets both SR4 and SR5 of the status register to a "1," places the device into read status register mode, and waits for another command.
40h	Program Setup	First	A two-cycle command: The first cycle prepares for a PROGRAM operation, the second cycle latches addresses and data and initiates the WSM to execute the program algorithm. The Flash outputs status register data on the falling edge of F_OE# or F_CE#, whichever occurs first.
50h	Clear Status Register	First	The WSM can set the program status (SR4), and erase status (SR5) bits in the status register to "1," but it cannot clear them to "0." Issuing this command clears those bits to "0."
60h	Protection Configuration Setup	First	Prepares the CSM for changes to the block locking status. If the next command is not BLOCK UNLOCK, BLOCK LOCK or BLOCK LOCK DOWN, then the CSM sets both the program and erase status register bits to indicate a command sequence error.
70h	Read Status Register	First	Places the device into read status register mode. Reading the device outputs the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after a PROGRAM or ERASE operation has been initiated.
90h	Read Protection Configuration	First	Puts the device into the read protection configuration mode so that reading the device outputs the manufacturer/device codes or block lock status.
98h	Read Query	First	Puts the device into the read query mode so that reading the device outputs common Flash interface information.
B0h	Program Suspend Erase Suspend	First First	Suspends the currently executing PROGRAM/ERASE operation. The status register indicates when the operation has been successfully suspended by setting either the program suspend (SR2) or erase suspend (SR6) and the WSMS bit (SR7) to a "1" (ready). The WSM continues to idle in the suspend state, regardless of the state of all input control pins except F_RP#, which immediately shuts down the WSM and the remainder of the chip if F_RP# is driven to V_{IL}.
C0h	Program Device Protection Register	First	Writes a specific code into the device protection register.
	Lock Device Protection register	First	Locks the device protection register; data can no longer be changed.

(continued on the next page)

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Table 6
Command Descriptions (continued)

CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
D0h	Erase Confirm	First	If the previous command was an ERASE SETUP command, then the CSM closes the address and data latches, and it begins erasing the block indicated on the address pins. During programming/erase, the device responds only to the READ STATUS REGISTER, PROGRAM SUSPEND, or ERASE SUSPEND commands and outputs status register data on the falling edge of F_OE# or F_CE#, whichever occurs last.
	Program/Erase Resume	First	If a PROGRAM or ERASE operation was previously suspended, this command resumes the operation.
FFh	Read Array	First	During the array mode, array data is output on the data bus.
01h	Lock Block	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM latches the address and locks the block indicated on the address bus.
2Fh	Lock Down	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM latches the address and locks down the block indicated on the address bus.
D0h	Unlock Block	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM latches the address and unlocks the block indicated on the address bus. If the block had been previously set to lock down, this operation has no effect.
00h	Invalid/Reserved		Unassigned command that should not be used.

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CLEAR STATUS REGISTER

The internal circuitry can set, but not clear, the block lock status bit (SR1), the V_{PP} status bit (SR3), the program status bit (SR4), and the erase status bit (SR5) of the status register. The CLEAR STATUS REGISTER command (50h) allows the external microprocessor to clear these status bits and synchronize to the internal operations. When the status bits are cleared, the device returns to the read array mode.

READ OPERATIONS

The following READ operations are available: READ ARRAY, READ PROTECTION CONFIGURATION REGISTER, READ QUERY and READ STATUS REGISTER.

READ ARRAY

The array is read by entering the command code FFh on DQ0–DQ7. Control signals F_CE# and F_OE# must be at a logic LOW level (V_{IL}), and F_WE# and F_RP# must be at a logic HIGH level (V_{IH}) to read data from the array. Data is available on DQ0–DQ15. Any valid address within any of the blocks selects that address and allows data to be read from that address. Upon initial power-up, the device defaults to the read array mode.

READ CHIP PROTECTION IDENTIFICATION DATA

The chip identification mode outputs three types of information: the manufacturer/device identifier, the block locking status, and the protection register. Two bus cycles are required for this operation: the chip identification data is read by entering the command code 90h on DQ0–DQ7 to the bank containing address 00h and the identification code address on the address lines. Control signals F_CE# and F_OE# must be at a logic LOW level (V_{IL}), and F_WE# and F_RP# must be at a logic HIGH level (V_{IH}) to read data from the protection configuration register. Data is available on DQ0–DQ15. After data is read from the protection configuration register, the READ ARRAY command, FFh, must be issued to the bank containing address 00h prior to issuing other commands. See Table 10 for further details.

READ QUERY

The read query mode outputs common flash interface (CFI) data when the device is read (see Table 12). Two bus cycles are required for this operation. It is possible to access the query by writing the read query command code 98h on DQ0–DQ7. Control signals F_CE# and F_OE# must be at a logic LOW level (V_{IL}), and F_WE# and F_RP# must be at a logic HIGH level (V_{IH}) to read data from the query. The CFI data structure contains information such as block size, density, command set, and electrical specifications. To return to read array mode, write the read array command code FFh on DQ0–DQ7.

READ STATUS REGISTER

The status register is read by entering the command code 70h on DQ0–DQ7. Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a READ cycle, the address is latched and register data is updated on the falling edge of F_OE# or F_CE#, whichever occurs last.

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PROGRAMMING OPERATIONS

There are two CSM commands for programming: PROGRAM SETUP and ALTERNATE PROGRAM SETUP (see Table 4).

After the desired command code is entered (10h or 40h command code on DQ0–DQ7), the WSM takes over and correctly sequences the device to complete the PROGRAM operation. The WRITE operation may be monitored through the status register (see the Status Register section). During this time, the CSM only responds to a PROGRAM SUSPEND command until the PROGRAM operation has been completed, after which time all commands to the CSM become valid again. The PROGRAM operation can be suspended by issuing a PROGRAM SUSPEND command (B0h). Once the WSM reaches the suspend state, it allows the CSM to respond only to READ ARRAY, READ STATUS REGISTER, READ PROTECTION CONFIGURATION, READ QUERY, PROGRAM SETUP, or PROGRAM RESUME. During the PROGRAM SUSPEND operation, array data should be read from an address other than the one being programmed. To resume the PROGRAM operation, a PROGRAM RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 4 for programming operation and Figure 5 for program suspend and program resume).

Taking F_RP# to V_{IL} during programming aborts the PROGRAM operation.

ERASE OPERATIONS

An ERASE operation must be used to initialize all bits in an array block to "1s." After BLOCK ERASE confirm is issued, the CSM responds only to an ERASE SUSPEND command until the WSM completes its task.

Block erasure inside the memory array sets all bits within the address block to logic 1s. Erase is accomplished only by blocks; data at single address locations within the array cannot be erased individually. The block to be erased is selected by using any valid address within that block. Block erasure is initiated by a command sequence to the CSM: BLOCK ERASE setup (20h) followed by BLOCK ERASE CONFIRM (D0h) (see Table 5). A two-command erase sequence protects against accidental erasure of memory contents.

When the BLOCK ERASE CONFIRM command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally verification is performed to ensure that all bits are correctly erased. Monitoring of the ERASE operation is possible through the status register (see the Status Register section).

During the execution of an ERASE operation, the ERASE SUSPEND command (B0h) can be entered to direct the WSM to suspend the ERASE operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the READ ARRAY, READ STATUS REGISTER, READ QUERY, READ CHIP PROTECTION CONFIGURATION, PROGRAM SETUP, PROGRAM RESUME, ERASE RESUME and LOCK SETUP (see the Block Locking section). During the ERASE SUSPEND operation, array data must be read from a block other than the one being erased. To resume the ERASE operation, an ERASE RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 7). It is also possible that an ERASE in any bank can be suspended and a WRITE to another block in the same bank can be initiated. After the completion of a WRITE, an ERASE can be resumed by writing an ERASE RESUME command.

Table 7
Bus Operations

MODE	F_RP#	F_CE#	F_OE#	F_WE#	ADDRESS	DQ0–DQ15
Read (array, status registers, device identification register, or query)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Standby	V_{IH}	V_{IH}	X	X	X	High-Z
Output Disable	V_{IH}	V_{IH}	X	X	X	High-Z
Reset	V_{IL}	X	X	X	X	High-Z
Write	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}

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Table 8
Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check write state machine bit first to determine word program or block erase completion, before checking program or erase status bits.
SR6	ERASE SUSPEND STATUS (ESS) 1 = BLOCK ERASE Suspended 0 = BLOCK ERASE in Progress/Completed	When ERASE SUSPEND is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an ERASE RESUME command is issued.
SR5	ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful BLOCK ERASE	When this bit is set to "1," WSM has applied the maximum number of erase pulses to the block and is still unable to verify successful block erasure.
SR4	PROGRAM STATUS (PS) 1 = Error in PROGRAM 0 = Successful PROGRAM	When this bit is set to "1," WSM has attempted but failed to program a word.
SR3	VPP STATUS (VPPS) 1 = VPP Low Detect, Operation Abort 0 = VPP = OK	The VPP status bit does not provide continuous indication of the VPP level. The WSM interrogates the VPP level only after the program or erase command sequences have been entered and informs the system if VPP < 0.9V. The VPP level is also checked before the PROGRAM/ERASE operation is verified by the WSM. The MT28C3214P2NFL device allows PROGRAM or ERASE at 0V, in which case SR3 is held at "0."
SR2	PROGRAM SUSPEND STATUS (PSS) 1 = PROGRAM Suspended 0 = PROGRAM in Progress/Completed	When PROGRAM SUSPEND is issued, WSM halts execution and sets both WSM and PSS bits to "1." PSS bit remains set to "1" until a PROGRAM RESUME command is issued.
SR1	BLOCK LOCK STATUS (BLS) 1 = PROGRAM/ERASE Attempted on a Locked Block; Operation Aborted 0 = No Operation to Locked Blocks	If a PROGRAM or ERASE operation is attempted to one of the locked blocks, this is set by the WSM. The operation specified is aborted, and the device is returned to read status mode.
SR0	RESERVED FOR FUTURE ENHANCEMENT	This bit is reserved for future.

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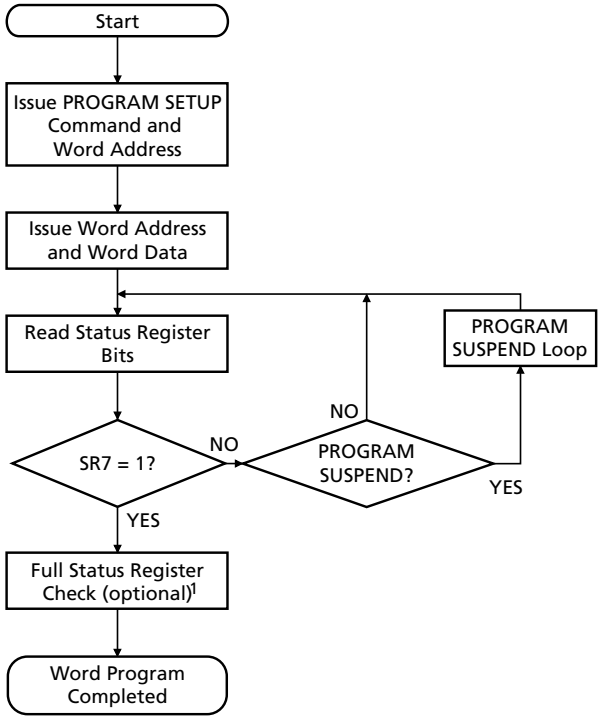
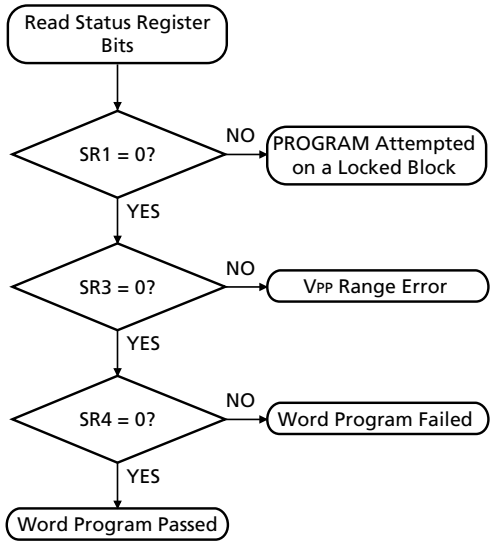
Figure 4
Automated Word Programming Flowchart



FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE PROGRAM SETUP	Data = 40h or 10h Addr = Address of word to be programmed
WRITE	WRITE DATA	Data = Word to be programmed Addr = Address of word to be programmed
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word programming operation to reset the device to read array mode.		

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect VPP low
Standby		Check SR4[3] 1 = Word program error

NOTE:
1. Full status register check can be done after each word or after a sequence of words.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR4 is cleared only by the CLEAR STATUS REGISTER command, but it does not prevent additional program operation attempts.

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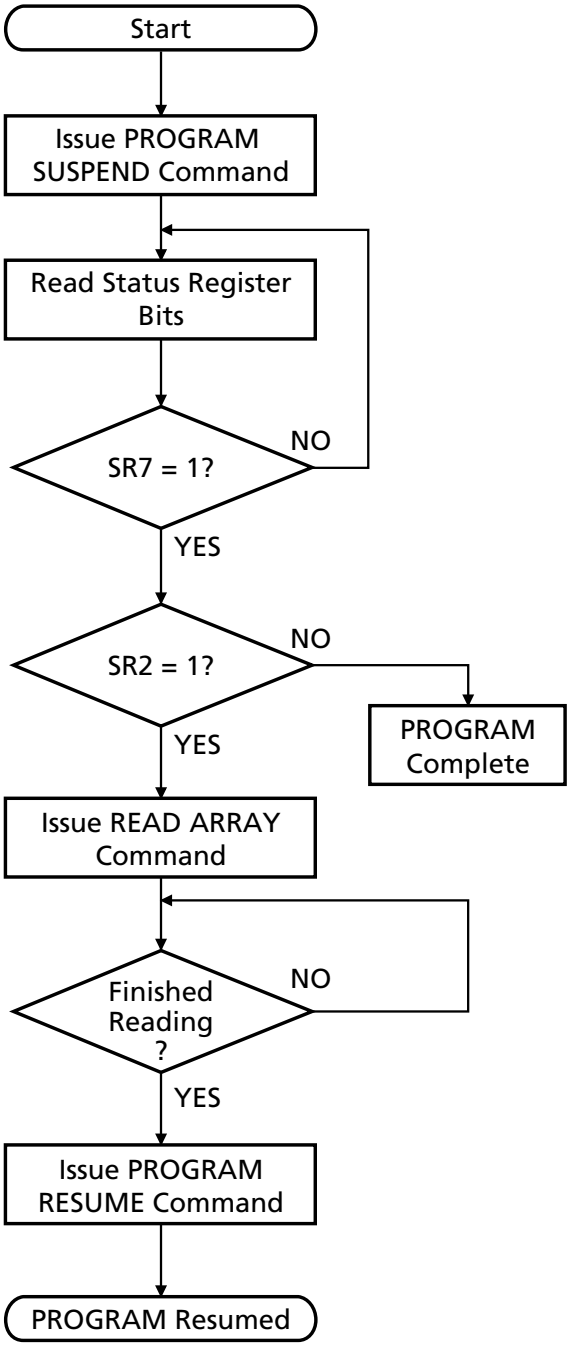
Figure 5
PROGRAM SUSPEND/
PROGRAM RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	PROGRAM SUSPEND	Data = B0h
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready
Standby		Check SR2 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being programmed.
WRITE	PROGRAM RESUME	Data = D0h

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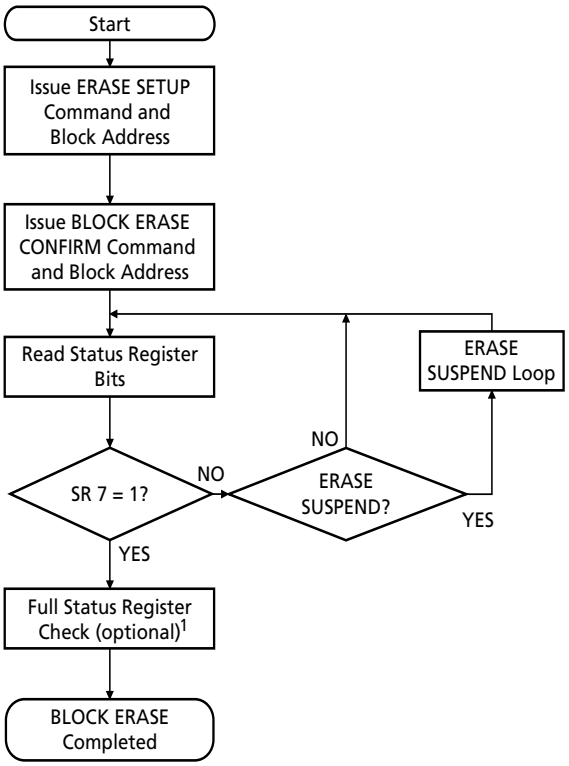
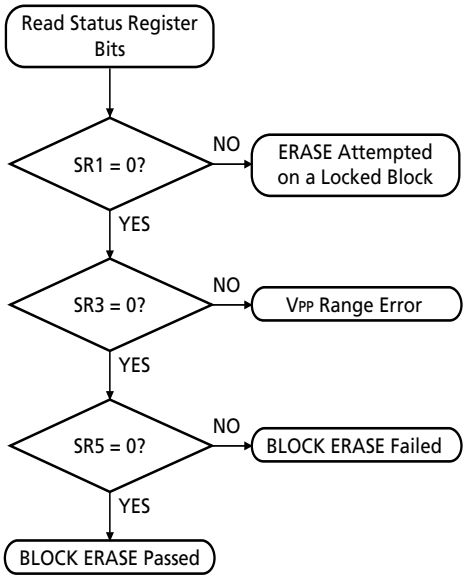
Figure 6
BLOCK ERASE Flowchart



FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE ERASE SETUP	Data = 20h Block Addr = Address within block to be erased
WRITE	ERASE	Data = D0h Block Addr = Address within block to be erased
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last BLOCK ERASE operation to reset the device to read array mode.		

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect VPP block
Standby		Check SR4 and SR5 1 = BLOCK ERASE command error
Standby		Check SR5[3] 1 = BLOCK ERASE error

NOTE: 1. Full status register check can be done after each block or after a sequence of blocks.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR5 is cleared only by the CLEAR STATUS REGISTER command in cases where multiple blocks are erased before full status is checked.

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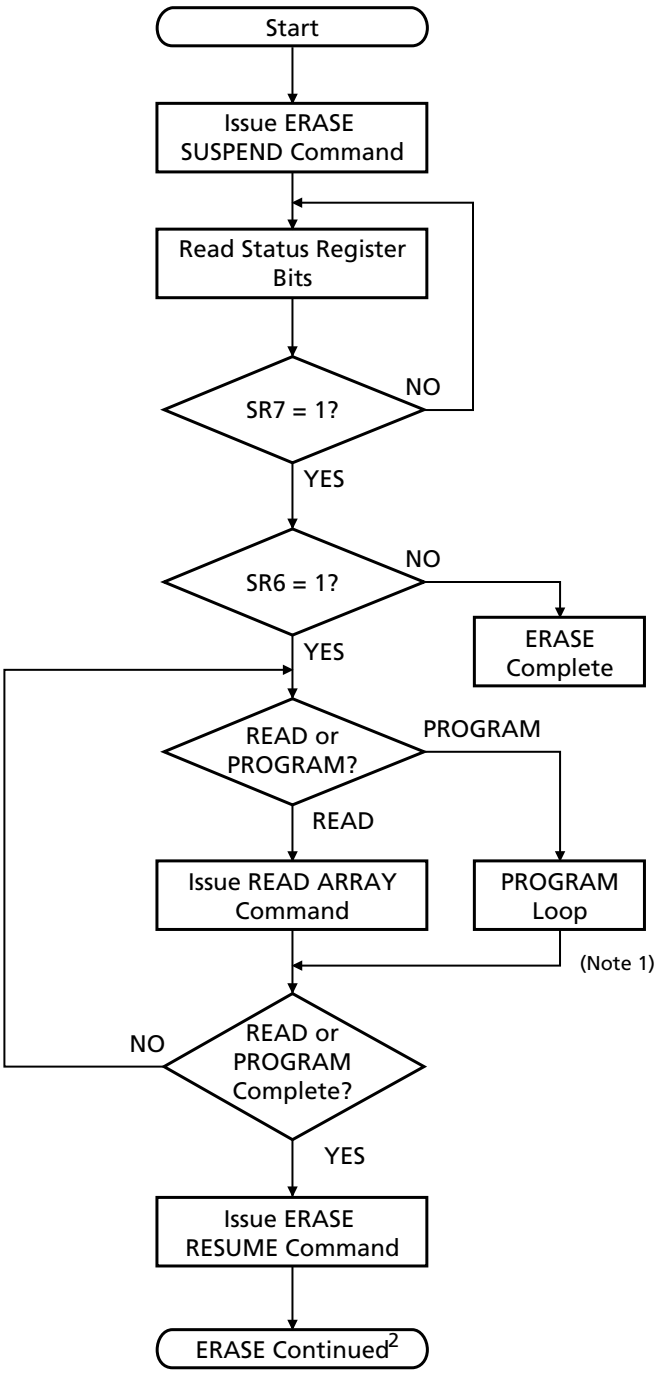
Figure 7
ERASE SUSPEND/ERASE RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE SUSPEND	Data = B0h
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready
Standby		Check SR6 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being erased.
WRITE	ERASE RESUME	Data = D0h

NOTE: 1. See BLOCK ERASE Flowchart for complete erasure procedure.
2. See Word Programming Flowchart for complete programming procedure.

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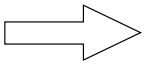
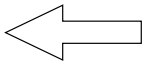
READ-WHILE-WRITE/ERASE CONCURRENCY

It is possible for the device to read from one bank while erasing/writing to another bank. Once a bank enters the WRITE/ERASE operation, the other bank automatically enters read array mode. For example, during a READ CONCURRENCY operation, if a PROGRAM/ERASE command is issued in bank *a*, then bank *a* changes to the read status mode and bank *b* defaults to the read array mode. The device reads from bank *b* if the latched address resides in bank *b* (see Figure 8). Similarly, if a PROGRAM/ERASE command is issued in bank *b*, then bank *b* changes to read status mode and bank *a* defaults to read array mode. When returning to bank *a*, the device reads program/erase status if the latched address resides in bank *a*. A correct bank address must be specified to read status register after returning from concurrent read in the other bank.

When reading the CFI area, or the chip protection register, the possible concurrent operations are reported in Figures 9a and 9b.

Figure 8
READ-While-WRITE Concurrency

Bank *a*	Bank *b*
1 - Erasing/writing to bank *a* 2 - Erasing in bank *a* can be suspended, and a WRITE to another block in bank *a* can be initiated. 3 - After the WRITE in that block is complete, an ERASE can be resumed by writing an ERASE RESUME command.	 1 - Reading from bank *b*
1 - Reading bank *a* 	1 - Erasing/writing to bank *b* 2 - Erasing in bank *b* can be suspended, and a WRITE to another block in bank *b* can be initiated. 3 - After the WRITE in that block is complete, an ERASE can be resumed by writing an ERASE RESUME command.

BLOCK LOCKING

The Flash memory of the MT28C3214P2FL or MT28C3214P2NFL device provides a flexible locking scheme which allows each block to be individually locked or unlocked with no latency.

The device offers two-level protection for the blocks. The first level allows software-only control of block locking (for data which needs to be changed frequently), while the second level requires hardware interaction before locking can be changed (code which does not require frequent updates).

Control signals F_WP#, DQ0, and DQ1 define the state of a block; for example, state [001] means F_WP# = 0, DQ0 = 0 and DQ1 = 1.

Table 9 defines all of the possible locking states.

NOTE: All blocks are software-locked upon completion of the power-up sequence.

LOCKED STATE

After a power-up sequence completion, or after a reset sequence, all blocks are locked (states [001] or [101]). This means full protection from alteration. Any PROGRAM or ERASE operations attempted on a locked block will return an error on bit SR1 of the status register. The status of a locked block can be changed to unlocked or lock down using the appropriate software commands. Writing the lock command sequence, 60h followed by 01h, can lock an unlocked block.

UNLOCKED STATE

Unlocked blocks (states [000], [100], [110]) can be programmed or erased. All unlocked blocks return to the locked state when the device is reset or powered down. An unlocked block can be locked or locked down using the appropriate software command sequence, 60h followed by D0h. (See Table 5.)

LOCKED DOWN STATE

Blocks locked down (state [011]) are protected from PROGRAM and ERASE operations, but their protection status cannot be changed using software commands

Figure 9a
Top Boot Block Device

		BANK *a*	BANK *b*
Reading the CFI or Chip Protection Register	READ	Not Supported	Not Supported
	WRITE ERASE	Not Supported	Not Supported

Figure 9b
Bottom Boot Block Device

		BANK *a*	BANK *b*
Reading the CFI or Chip Protection Register	READ	Not Supported	Supported
	WRITE ERASE	Not Supported	Supported

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Table 9
Block Locking State Transition

F_WP#	DQ1	DQ0	NAME	ERASE/PROGRAM ALLOWED	LOCK	UNLOCK	LOCK DOWN
0	0	0	Unlocked	Yes	To [001]	–	To [011]
0	0	1	Locked (Default)	No	–	To [000]	To [011]
0	1	1	Lock Down	No	–	–	–
1	0	0	Unlocked	Yes	To [101]	–	To [111]
1	0	1	Locked	No	–	To [100]	To [111]
1	1	0	Lock Down Disabled	Yes	To [111]	–	To [111]
1	1	1	Lock Down Disabled	No	–	To [110]	–

alone. A locked or unlocked block can be locked down by writing the lock down command sequence, 60h followed by 2Fh. Locked down blocks revert to the locked state when the device is reset or powered down.

The LOCK DOWN function is dependent on the F_WP# input. When F_WP# = 0, blocks in lock down [011] are protected from program, erase, and lock status changes. When F_WP# = 1, the LOCK DOWN function is disabled ([111]) and locked down blocks can be individually unlocked by a software command to the [110] state, where they can be erased and programmed. These blocks can then be relocked [111] and unlocked [110], as desired, as long as F_WP# remains HIGH. When F_WP# goes LOW, blocks that were previously locked down return to the lock down state [011] regardless of any changes made while F_WP# was HIGH. Device reset or power-down resets all locks, including those in lock down, to the locked state (see Table 9).

READING A BLOCK'S LOCK STATUS

The lock status of every block can be read in the read device identification mode. To enter this mode, write 90h to the bank containing address 00h. Subsequent READs at block address +00002 will output the lock status of that block. The lowest two outputs, DQ0 and DQ1, represent the lock status. DQ0 indicates the block lock/unlock status and is set by the LOCK command and cleared by the UNLOCK command. It is also automatically set when entering lock down. DQ1 indicates lock down status and is set by the LOCK DOWN

Table 10
Chip Protection Configuration Addressing[1]

ITEM	ADDRESS[2]	DATA
Manufacturer Code (x16)	00000h	002Ch
Device Code • Top boot configuration • Bottom boot configuration	00001h	 44A2h 44A3h
Block Lock Configuration • Block is unlocked • Block is locked • Block is locked down	XX002h	Lock DQ0 = 0 DQ0 = 1 DQ1 = 1
Chip Protection Register Lock	80h	PR Lock
Chip Protection Register 1	81h–84h	Factory Data
Chip Protection Register 2	85h–88h	User Data

NOTE: 1. Other locations within the configuration address space are reserved by Micron for future use.
2. "XX" specifies the block address of lock configuration.

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command. It can only be cleared by reset or power-down, not by software. Table 9 shows the block locking state transition scheme. The READ ARRAY command, FFh, must be issued to the bank containing address 00h prior to issuing other commands.

LOCKING OPERATIONS DURING ERASE SUSPEND

Changes to block lock status can be performed during an ERASE SUSPEND by using the standard locking command sequences to unlock, lock, or lock down. This is useful in the case when another block needs to be updated while an ERASE operation is in progress.

To change block locking during an ERASE operation, first write the ERASE SUSPEND command (B0h), then check the status register until it indicates that the ERASE operation has been suspended. Next, write the desired lock command sequence to block lock, and the lock status will be changed. After completing any desired LOCK, READ, or PROGRAM operations, resume the ERASE operation with the ERASE RESUME command (D0h).

If a block is locked or locked down during an ERASE SUSPEND on the same block, the locking status bits are changed immediately. When the ERASE is resumed, the ERASE operation completes.

A locking operation cannot be performed during a PROGRAM SUSPEND.

STATUS REGISTER ERROR CHECKING

Using nested locking or program command sequences during ERASE SUSPEND can introduce ambiguity into status register results.

Following protection configuration setup (60h), an invalid command produces a lock command error (SR4 and SR5 are set to "1") in the status register. If a lock command error occurs during an ERASE SUSPEND, SR4 and SR5 are set to "1" and remain at "1" after the ERASE SUSPEND command is issued. When the ERASE is complete, any possible error during the ERASE cannot be detected via the status register because of the previous locking command error.

A similar situation happens if an error occurs during a program operation error nested within an ERASE SUSPEND.

CHIP PROTECTION REGISTER

A 128-bit protection register can be used to fullfill the security considerations in the system (preventing device substitution).

The 128-bit security area is divided into two 64-bit segments. The first 64 bits are programmed at the manufacturing site with a unique 64-bit number. The other segment is left blank for customers to program as desired. (See Figure 10).

READING THE CHIP PROTECTION REGISTER

The chip protection register is read in the device identification mode. To enter this mode, load the 90h command to the bank containing address 00h. Once in this mode, READ cycles from addresses shown in Table 10 retrieve the specified information. To return to the read array mode, write the READ ARRAY command (FFh). The READ ARRAY command, FFh, must be issued to the bank containing address 00h prior to issuing other commands.

PAGE READ MODE

The initial portion of the page mode cycle is the same as the asynchronous access cycle. Holding CE# LOW and toggling addresses A0–A1 allows random access of other words in the page.

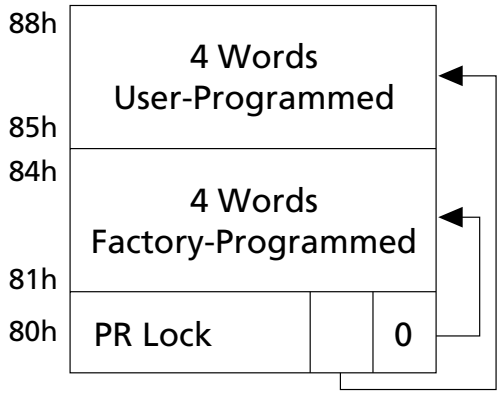
The page size can be customized at the factory to four or eight words as required; but if no specification is made, the normal size is four words.

ASYNCHRONOUS READ CYCLE

When accessing addresses in a random order or when switching between pages, the access time is given by ^{t}AA.

When F_CE# and F_OE# are LOW, the data is placed on the data bus and the processor can read the data.

Figure 10
Protection Register Memory Map



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STANDBY MODE

Icc supply current is reduced by applying a logic HIGH level on F_CE# and F_RP# to enter the standby mode. In the standby mode, the outputs are placed in High-Z. Applying a CMOS logic HIGH level on F_CE# and F_RP# reduces the current to I_{CC2} (MAX). If the device is deselected during an ERASE operation or during programming, the device continues to draw current until the operation is complete.

AUTOMATIC POWER SAVE (APS) MODE

Substantial power savings are realized during periods when the Flash array is not being read and the device is in the active mode. During this time the device switches to the automatic power save (APS) mode. When the device switches to this mode, I_{CC} is reduced to I_{CC2}. The low level of power is maintained until another operation is initiated. In this mode, the I/Os retain the data from the last memory address read until a new address is read. This mode is entered automatically if no addresses or control signals toggle.

V_{PP}/V_{CC} PROGRAM AND ERASE VOLTAGES

The MT28C3214P2FL Flash memory provides in-system programming and erase with V_{PP} in the 0.9V–2.2V range (V_{PP1}). In addition to the flexible block locking, the V_{PP} programming voltage can be held LOW for absolute hardware write protection of all blocks in the Flash device. When V_{PP} is below V_{PPLK}, any PROGRAM or ERASE operation results in an error, prompting the corresponding status register bit (SR3) to be set.

The MT28C3214P2NFL Flash memory provides in-system programming and erase with V_{PP} in the 0.0V–2.2V range (V_{PP1}).

V_{PP} at 12V ±5% (V_{PP2}) is supported for a maximum of 100 cycles and 10 cumulative hours. The device can withstand 100,000 WRITE/ERASE operations when $V_{PP} = V_{CC}$.

During WRITE and ERASE operations, the WSM monitors the V_{PP} voltage level. WRITE/ERASE operations are allowed only when V_{PP} is within the ranges specified in Table 11.

When V_{CC} is below V_{LKO} or V_{PP} is below V_{PPLK}, any WRITE/ERASE operation is prevented.

DEVICE RESET

To correctly reset the device, the RST# signal must be asserted (RST# = V_{IL}) for a minimum of ^{t}RP. After reset, the device can be accessed for a READ operation with a delayed access time of ^{t}RWH from the rising edge of RST#. The circuitry used for generating the RST# signal needs to be common with the rest of the system reset to ensure that correct system initialization occurs. Please refer to the timing diagram for further details.

POWER-UP SEQUENCE

The following power-up sequence must be observed to properly initialize the device:

- RST# must be at V_{IL}.
- Power on V_{CC}/V_{CC}Q ($V_{CC} \geq V_{CC}$Q at all times).
- Wait 2µS after V_{CC} reaches V_{CC} (MIN).
- Take RST# from V_{IL} to V_{IH}.
- The RST# transition from V_{IL} to V_{IH} must be less than 10µS.

Table 11
V_{PP} Ranges (V)

DEVICE	IN-SYSTEM		IN-FACTORY	
	MIN	MAX	MIN	MAX
MT28C3214P2FL	0.9	2.2	11.4	12.6
MT28C3214P2NFL	0.0	2.2	11.4	12.6

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FLASH ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage to Any Pin Except V_{CC} and V_{PP}
with Respect to V_{SS} ..... -0.5V to +2.45V
V_{PP} Voltage (for BLOCK ERASE and PROGRAM
with Respect to V_{SS}) ..... -0.5V to +13.5V**
V_{CC} and $V_{CC}Q$ Supply Voltage
with Respect to V_{SS} ..... -0.3V to +2.45V
Output Short Circuit Current 100mA
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Cycle ..... 260°C for 10s

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

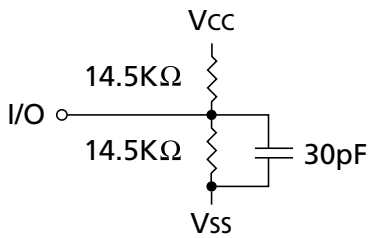
**Maximum DC voltage on V_{PP} may overshoot to +13.5V for periods <20ns.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Operating temperature	^{t}A	-40	+85	°C	
V_{CC} supply voltage	F_V_{CC}, S_V_{CC}	1.65	2.2	V	
I/O supply voltage (V_{CC} = 1.65V–1.95V)	$V_{CC}Q$	1.65	1.95	V	1
I/O supply voltage (V_{CC} = 1.80V–2.20V)	$V_{CC}Q$	1.80	2.20	V	1
V_{PP} voltage (MT28C3214P2FL only)	V_{PP1}	0.9	2.2	V	
V_{PP} voltage (MT28C3214P2NFL only)	V_{PP1}	0.0	2.2	V	
V_{PP} in-factory programming voltage	V_{PP2}	11.4	12.6	V	2
Data retention supply voltage	S_V_{DR}	1.0	–	V	
Block erase cycling		–	100,000	Cycles	

NOTE: 1. Use only one of the two I/O supply voltage ranges, 1.65V–1.95V or 1.80V–2.20V.
2. 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 10 cumulative hours.

Figure 11
Output Load Circuit



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COMBINED DC CHARACTERISTICS[1]

DESCRIPTION	CONDITIONS	SYMBOL	Vcc = 1.65V–1.95V or 1.80V–2.20V VccQ = 1.65V–1.95V or 1.80V–2.20V MIN	TYP	MAX	UNITS	NOTES
Input low voltage		V_{IL}	-0.4	–	0.4	V	
Input high voltage		V_{IH}	VccQ - 0.4V	–	VccQ + 0.3V	V	
Output low voltage I_{OL} = 100µA (Flash)		V_{OL}	–	–	0.10	V	
Output low voltage I_{OL} = 100µA (SRAM)		V_{OL}	0.3	–	0.3	V	
Output high voltage I_{OH} = 100µA (Flash)		V_{OH}	VccQ - 0.1V	–	–	V	
Output high voltage I_{OH} = 100µA (SRAM)		V_{OH}	VccQ - 0.3V	–	–	V	
V_{PP} lock out voltage		V_{PPLK}	–	–	0.4	V	
V_{PP} during PROGRAM/ERASE operations (MT28C3214P2FL only)		V_{PP1}	0.9	–	2.2	V	
		V_{PP2}	11.4	–	12.6	V	2
V_{PP} during PROGRAM/ERASE operations (MT28C3214P2NFL only)		V_{PP1}	0.0	–	2.2	V	
		V_{PP2}	11.4	–	12.6	V	2
Vcc PROGRAM/ERASE lock voltage		V_{LKO}	1.0	–	–	V	
Input leakage current		I_L	–	–	1	µA	
Output leakage current		I_{OZ}	–	–	1	µA	
F_Vcc asynchronous read current at 95ns		I_{CC1}	–	–	15	mA	
F_Vcc page mode read current at 35ns		I_{CC2}	–	–	5	mA	
F_Vcc plus S_Vcc standby current		I_{CC3}	–	25	60	µA	
F_Vcc program current		$I_{CC4}+I_{PP3}$	–	–	55	mA	
F_Vcc erase current		$I_{CC5}+I_{PP4}$	–	–	65	mA	
F_Vcc/S_Vcc erase suspend current		I_{CC6}	–	–	60	µA	
F_Vcc/S_Vcc program suspend current		I_{CC7}	–	–	60	µA	
Read-while-write current		I_{CC8}	–	–	80	mA	

NOTE: 1. All currents are in RMS unless otherwise noted.
2. 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 10 cumulative hours.
3. Operating current is a linear function of operating frequency and voltage. Operating current can be calculated using the formula shown with operating frequency (f) expressed in MHz and operating voltage (V) in volts. Example: When operating at 2 MHz at 2V, the device will draw a typical active current of 0.8*2* 2 = 3.2mA in the page access mode. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

(continued on the next page)

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COMBINED DC CHARACTERISTICS[1] (continued)

DESCRIPTION	CONDITIONS	SYMBOL	Vcc = 1.65V–1.95V or 1.80V–2.20V VccQ = 1.65V–1.95V or 1.80V–2.20V			UNITS	NOTES
			MIN	TYP	MAX		
S_Vcc read/write operating supply current – page access mode	VIN = VIH or VIL chip enabled, IOL = 0	ICC9	–	12	25	mA	3
S_Vcc read/write operating supply current – word access mode	VIN = VIH or VIL chip enabled, IOL = 0	ICC10	–	3	8	mA	3
VPP read current	VPP ≤ VCC	IPP1	–	–	1	µA	
	VPP ≥ VCC		–	–	200	µA	
VPP standby current	VPP ≤ VCC	IPP2	–	–	1	µA	
	VPP ≥ VCC		–	–	200	µA	
VPP erase suspend current	VPP = VPP1	IPP5	–	–	1	µA	
	VPP = VPP2		–	–	200	µA	
VPP program suspend current	VPP = VPP1	IPP6	–	–	1	µA	
	VPP = VPP2		–	–	200	µA	

NOTE:
1. All currents are in RMS unless otherwise noted.
2. 12V VPP is supported for a maximum of 100 cycles and may be connected for up to 10 cumulative hours.
3. Operating current is a linear function of operating frequency and voltage. Operating current can be calculated using the formula shown with operating frequency (f) expressed in MHz and operating voltage (V) in volts. Example: When operating at 2 MHz at 2V, the device will draw a typical active current of 0.8*2* 2 = 3.2mA in the page access mode. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

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FLASH READ CYCLE TIMING REQUIREMENT

Vcc = 1.65V–1.95V

PARAMETER	SYMBOL	-10 Vcc = 1.65V–1.95V MIN	-10 Vcc = 1.65V–1.95V MAX	-11 Vcc = 1.65V–1.95V MIN	-11 Vcc = 1.65V–1.95V MAX	UNITS
Address to output delay	^{t}AA		100		110	ns
CE# LOW to output delay	^{t}ACE		100		110	ns
Page address access	^{t}APA		35		45	ns
OE# LOW to output delay	^{t}AOE		30		30	ns
F_RP# HIGH to output delay	^{t}RWH		200		200	ns
F_RP# LOW pulse width	^{t}RP	125		125		ns
CE# or OE# HIGH to output High-Z	^{t}OD		25		25	ns
Output hold from address, CE# or OE# change	^{t}OH	0		0		ns
READ cycle time	^{t}RC		100		110	ns

FLASH READ CYCLE TIMING REQUIREMENT

Vcc = 1.80V–2.20V

PARAMETER	SYMBOL	-10 Vcc = 1.80V–2.20V MIN	-10 Vcc = 1.80V–2.20V MAX	-11 Vcc = 1.80V–2.20V MIN	-11 Vcc = 1.80V–2.20V MAX	UNITS
Address to output delay	^{t}AA		95		100	ns
CE# LOW to output delay	^{t}ACE		95		100	ns
Page address access	^{t}APA		35		45	ns
OE# LOW to output delay	^{t}AOE		30		30	ns
F_RP# HIGH to output delay	^{t}RWH		150		150	ns
F_RP# LOW pulse width	^{t}RP	100		100		ns
CE# or OE# HIGH to output High-Z	^{t}OD		25		25	ns
Output hold from address, CE# or OE# change	^{t}OH	0		0		ns
READ cycle time	^{t}RC		95		100	ns

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FLASH WRITE CYCLE TIMING REQUIREMENTS

PARAMETER	SYMBOL	-10/-11 Vcc = 1.65V–1.95V or 1.80V–2.20V MIN	MAX	UNITS
Reset HIGH recovery to WE# going LOW	^{t}RS	150		ns
CE# setup to WE# going LOW	^{t}CS	0		ns
Write pulse width	^{t}WP	50		ns
Data setup to WE# going HIGH	^{t}DS	50		ns
Address setup to WE# going HIGH	^{t}AS	50		ns
CE# hold from WE# HIGH	^{t}CH	0		ns
Data hold from WE# HIGH	^{t}DH	0		ns
Address hold from WE# HIGH	^{t}AH	9		ns
Write pulse width HIGH	^{t}WPH	30		ns
WP# setup to WE# going HIGH	^{t}RHS	200		ns
V_{PP} setup to WE# going HIGH	^{t}VPS	200		ns
Write recovery before READ	^{t}WOS	50		ns
WP# hold from valid SRD	^{t}RHH	0		ns
V_{PP} hold from valid SRD	^{t}VPH	0		ns
WE# HIGH to data valid	^{t}WB		^{t}AA+50	ns

FLASH ERASE AND PROGRAM CYCLE TIMING REQUIREMENTS

PARAMETER	-10/-11 Vcc = 1.65V–1.95V or 1.80V–2.20V TYP	MAX	UNITS
4KW parameter block program time	0.1	0.3	s
32KW parameter block program time	0.8	2.4	s
Word program time	8	185	µs
4KW parameter block erase time	1	4	s
32KW parameter block erase time	1.5	5	s
Program suspend latency	5	10	µs
Erase suspend latency	5	20	µs

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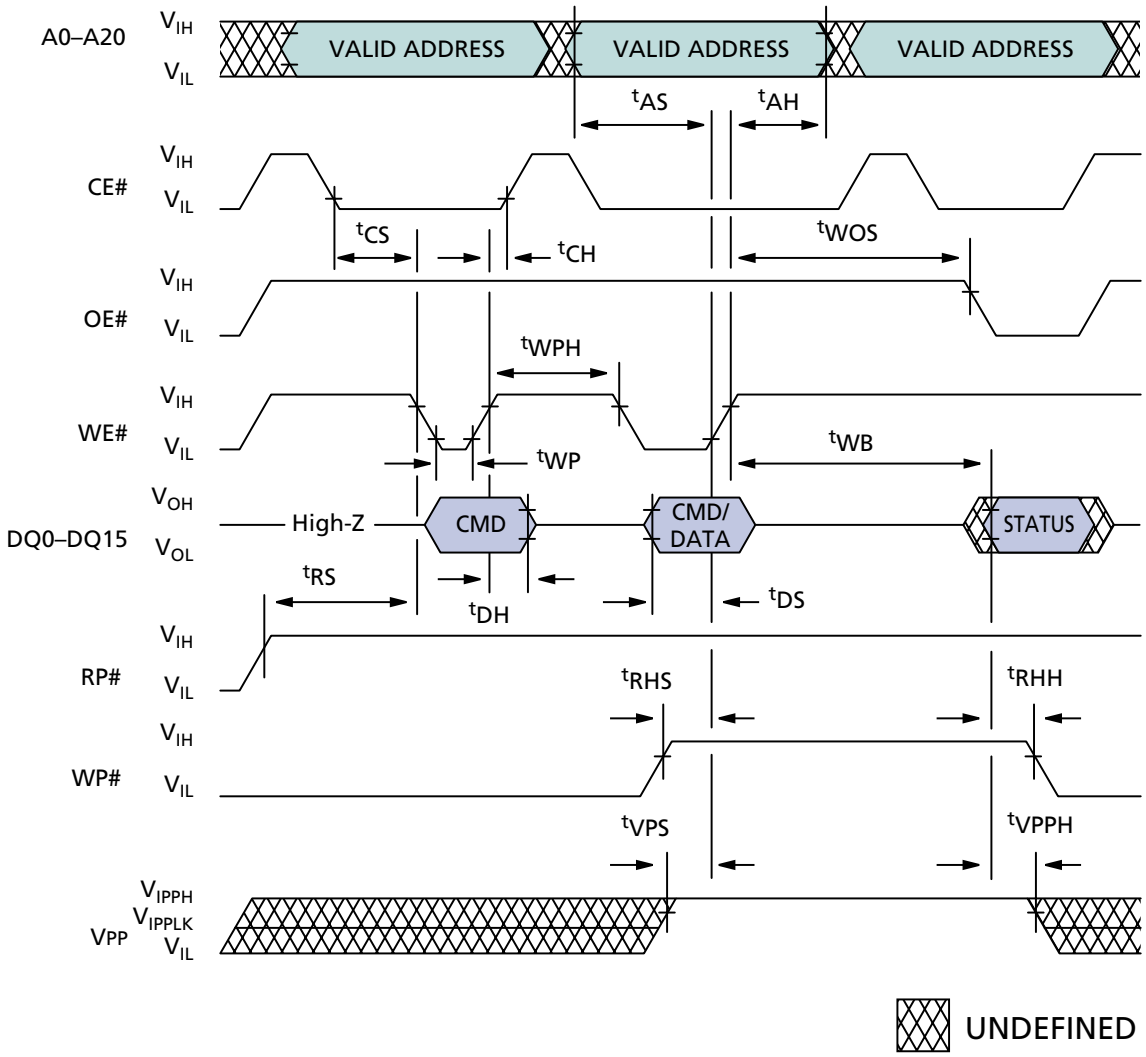
TWO-CYCLE PROGRAMMING/ERASE OPERATION



WRITE TIMING PARAMETERS

SYMBOL	-10/-11 Vcc = 1.65V–1.95V or 1.80V–2.20V MIN	MAX	UNITS
tRS	150		ns
tCS	0		ns
tWP	50		ns
tDS	50		ns
tAS	50		ns
tCH	0		ns
tDH	0		ns

SYMBOL	-10/-11 Vcc = 1.65V–1.95V or 1.80V–2.20V MIN	MAX	UNITS
tAH	9		ns
tRHS	200		ns
tVPS	200		ns
tWOS	50		ns
tRHH	0		ns
tVPH	0		ns
tWB		tAA+50	ns

NOTE: 1. The WRITE cycles for the WORD PROGRAMMING command are followed by a READ ARRAY DATA cycle.

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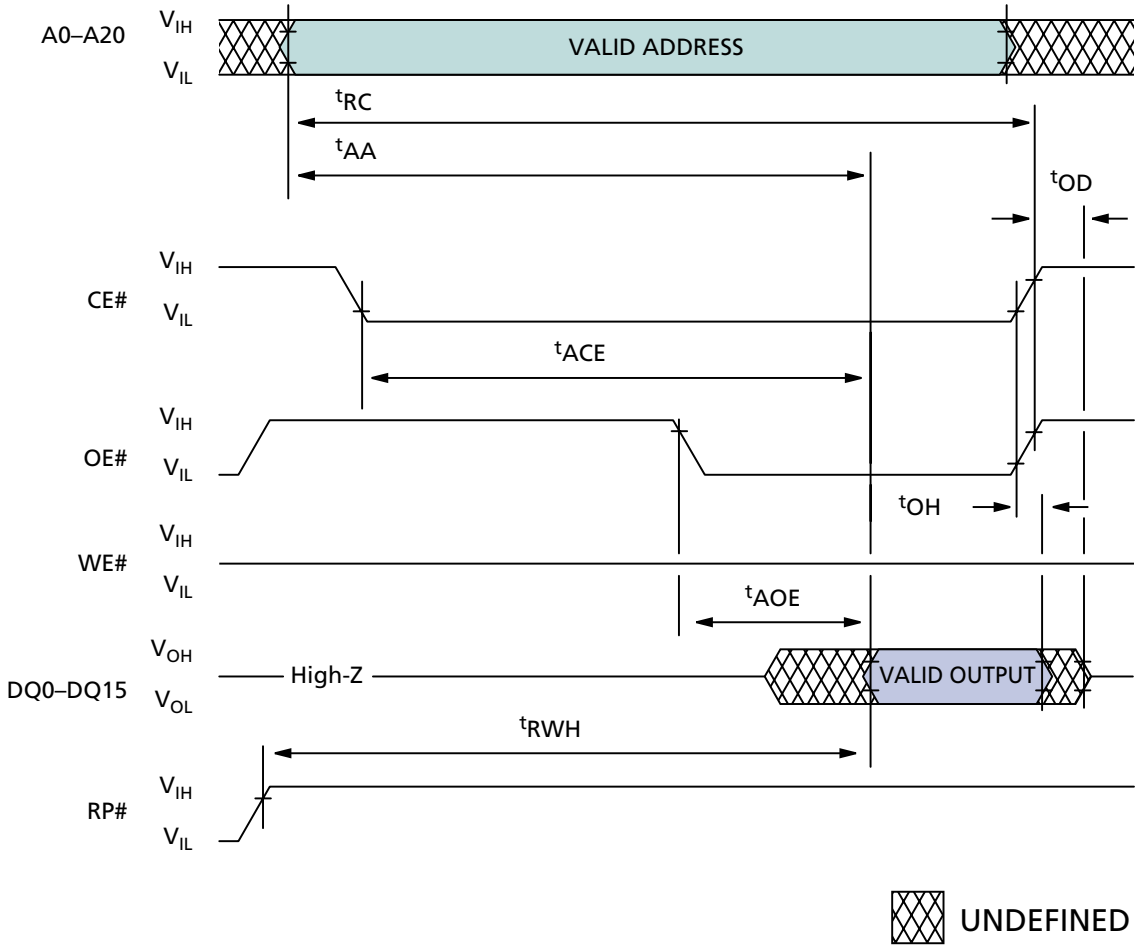
SINGLE ASYNCHRONOUS READ OPERATION



READ TIMING PARAMETERS
(Vcc = 1.65V–1.95V)

SYMBOL	-10 Vcc = 1.65V–1.95V MIN	-10 Vcc = 1.65V–1.95V MAX	-11 Vcc = 1.65V–1.95V MIN	-11 Vcc = 1.65V–1.95V MAX	UNITS
tAA		100		110	ns
tACE		100		110	ns
tAOE		30		30	ns
tRWH		200		200	ns
tOD		25		25	ns
tOH	0		0		ns
tRC		100		110	ns

READ TIMING PARAMETERS
(Vcc = 1.80V–2.20V)

SYMBOL	-10 Vcc = 1.80V–2.20V MIN	-10 Vcc = 1.80V–2.20V MAX	-11 Vcc = 1.80V–2.20V MIN	-11 Vcc = 1.80V–2.20V MAX	UNITS
tAA		95		100	ns
tACE		95		100	ns
tAOE		30		30	ns
tRWH		150		150	ns
tOD		25		25	ns
tOH	0		0		ns
tRC		95		100	ns

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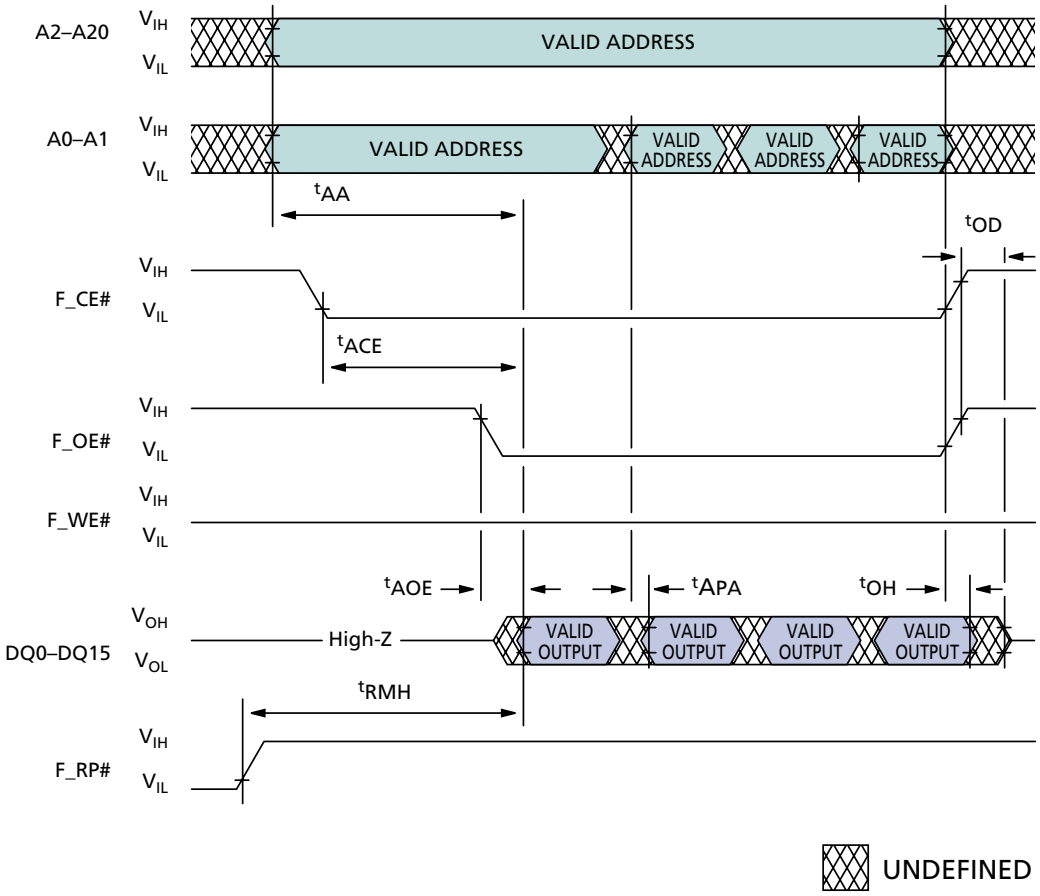
ASYNCHRONOUS PAGE MODE READ OPERATION



READ TIMING PARAMETERS
(Vcc = 1.65V–1.95V)

	-10		-11		
	Vcc = 1.65V–1.95V		Vcc = 1.65V–1.95V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		100		110	ns
tACE		100		110	ns
tAPA		35		45	ns
tAOE		30		30	ns
tRWH		200		200	ns
tOD		25		25	ns
tOH	0		0		ns

READ TIMING PARAMETERS
(Vcc = 1.80V–2.20V)

	-10		-11		
	Vcc = 1.80V–2.20V		Vcc = 1.80V–2.20V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		95		100	ns
tACE		95		100	ns
tAPA		35		45	ns
tAOE		30		30	ns
tRWH		150		150	ns
tOD		25		25	ns
tOH	0		0		ns

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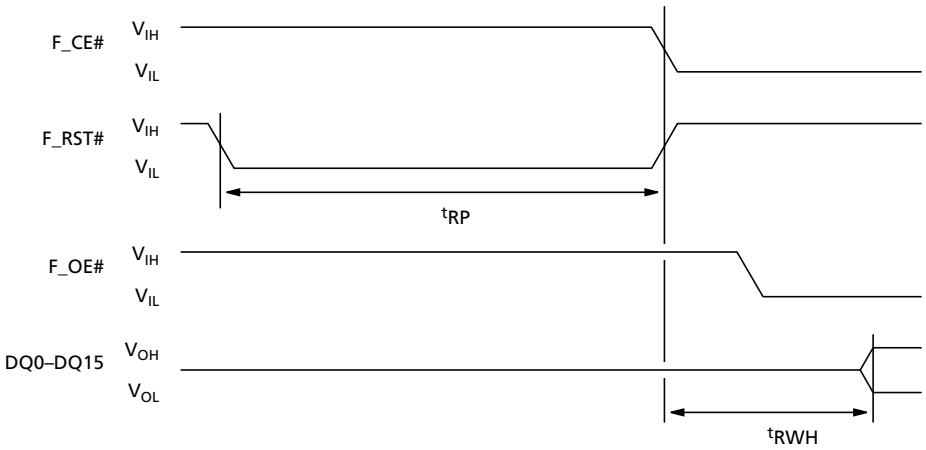
RESET OPERATION



READ TIMING PARAMETERS
(Vcc = 1.65V–1.95V)

SYMBOL	-10 Vcc = 1.65V–1.95V MIN	-10 Vcc = 1.65V–1.95V MAX	-11 Vcc = 1.65V–1.95V MIN	-11 Vcc = 1.65V–1.95V MAX	UNITS
^{t}RWH		200		200	ns
^{t}RP	125		125		ns

READ TIMING PARAMETERS
(Vcc = 1.80V–2.20V)

SYMBOL	-10 Vcc = 1.80V–2.20V MIN	-10 Vcc = 1.80V–2.20V MAX	-11 Vcc = 1.80V–2.20V MIN	-11 Vcc = 1.80V–2.20V MAX	UNITS
^{t}RWH		150		150	ns
^{t}RP	100		100		ns

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Table 12
CFI

OFFSET	DATA	DESCRIPTION
00	2Ch	Manufacturer Code
01	A2h	Top Boot Block Device Code
	A3h	Bottom Boot Block Device Code
02–0F	reserved	Reserved
10, 11	0051,0052	"QR"
12	0059	"Y"
13, 14	0003, 0000	Primary OEM Command Set
15, 16	0039, 0000	Address for Primary Extended Table
17, 18	0000, 0000	Alternate OEM Command Set
19, 1A	0000, 0000	Address for OEM Extended Table
1B	0017	V_{CC} MIN for Erase/Write; Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
1C	0022	V_{CC} MAX for Erase/Write; Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
1D	00B4	V_{PP} MIN for Erase/Write; Bit7–Bit4 Volts in Hex; Bit3–Bit0 100mV in BCD
1E	00C6	V_{PP} MAX for Erase/Write; Bit7–Bit4 Volts in Hex; Bit3–Bit0 100mV in BCD
1F	0003	Typical timeout for single byte/word program, 2^n µs, 0000 = not supported
20	0000	Typical timeout for maximum size multiple byte/word program, 2^n µs, 0000 = not supported
21	0009	Typical timeout for individual block erase, 2^n ms, 0000 = not supported
22	0000	Typical timeout for full chip erase, 2^n ms, 0000 = not supported
23	000C	Maximum timeout for single byte/word program, 2^n µs, 0000 = not supported
24	0000	Maximum timeout for maximum size multiple byte/word program, 2^n µs, 0000 = not supported
25	0003	Maximum timeout for individual block erase, 2^n ms, 0000 = not supported
26	0000	Maximum timeout for full chip erase, 2^n ms, 0000 = not supported
27	0016	Device size, 2^n bytes
28	0001	Bus Interface x8 = 0, x16 = 1, x8/x16 = 2
29	0000	Flash device interface description 0000 = async
2A, 2B	0000, 0000	Maximum number of bytes in multi-byte program or page, 2^n
2C	0003	Number of erase block regions within device (4K words and 32K words)
2D, 2E	0037, 0000	Top boot block device erase block region information 1, 8 blocks …
	0007, 0000	Bottom boot block device erase block region information 1, 8 blocks …
2F, 30	0000, 0001	Top boot block device …of 8KB
	0020, 0000	Bottom boot block device …of 8KB
31, 32	0006, 0000	7 blocks of ….
33, 34	0000, 0001	……64KB
35, 36	0007, 0000	Top boot block device 56 blocks of
	0037, 0000	Bottom boot block device 56 blocks of

(continued on the next page)

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Table 12
CFI (continued)

OFFSET	DATA	DESCRIPTION
37, 38	0020, 0000	Top boot block device……64KB
	0000, 0001	Bottom boot block device……64KB
39, 3A	0050, 0052	"PR"
3B	0049	"I"
3C	0030	Major version number, ASCII
3D	0031	Minor Version Number, ASCII
3E 3F 40 41	00E6 0002 0000 0000	Optional Feature and Command Support Bit 0 Chip erase supported no = 0 Bit 1 Suspend erase supported = yes = 1 Bit 2 Suspend program supported = yes = 1 Bit 3 Chip lock/unlock supported = no = 0 Bit 4 Queued erase supported = no = 0 Bit 5 Instant individual block locking supported = yes = 1 Bit 6 Protection bits supported = yes = 1 Bit 7 Page mode read supported = yes = 1 Bit 8 Synchronous read supported = yes = 1 Bit 9 Simultaneous operation supported = yes = 1
42	0001	Program supported after erase suspend = yes
43, 44	0003,0000	Bit 0 Block Lock Status active = yes; Bit 1 Block Lock Down active = yes
45	0018	V_{CC} supply optimum; Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
46	00C0	V_{PP} supply optimum; Bit7–Bit4 Volts in Hex; Bit3–Bit0 100mV in BCD
47	0001	Number of protection register fields in JEDEC ID space
48, 49	0080, 0000	Lock bytes LOW address, lock bytes HIGH address
4A, 4B	0003, 0003	2^n factory programmed bytes, 2^n user programmable bytes
4C	0002	Background Operation 0000 = Not used 0001 = 4% block split 0002 = 12% block split 0003 = 25% block split 0004 = 50% block split
4D	0000	Burst Mode Type 0000 = No burst mode 00x1 = 4 words max 00x2 = 8 words max 00x3 = 16 words max 001x = Linear burst, and/or 002x = Interleaved burst, and/or 004x = Continuous burst
4E	0002	Page Mode Type 0000 = No page mode 0001 = 4-word page 0002 = 8-word page 0003 = 16-word page 0004 = 32-word page
4F	0004	SRAM density, 4Mb (256K x 16)

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SRAM OPERATING MODES

SRAM READ ARRAY

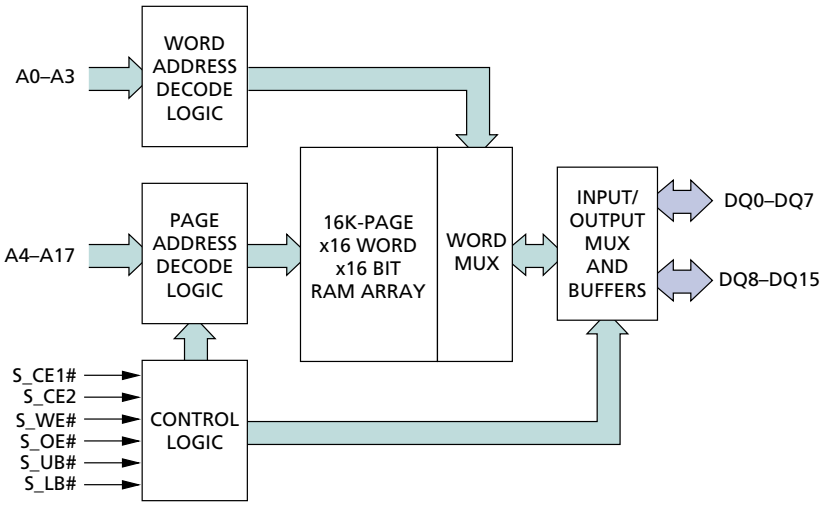
The operational state of the SRAM is determined by S_CE1#, S_CE2, S_WE#, S_OE#, S_UB#, and S_LB#, as indicated in the Truth Table. To perform an SRAM READ operation, S_CE1#, and S_OE#, must be at VIL, and S_CE2 and S_WE# must be at VIH. When in this state, S_UB# and S_LB# control whether the lower byte is read (S_UB# VIH, S_LB# VIL), the upper byte is read (S_UB# VIL, S_LB# VIH), both upper and lower bytes are read (S_UB# VIL, S_LB# VIL), or neither are read (S_UB# VIH, S_LB# VIH) and the device is in a standby state.

While performing an SRAM READ operation, current consumption may be reduced by reading within a 16-word page. This is done by holding S_CE1# and S_OE# at VIL, S_WE# and S_CE2 at VIH, and toggling addresses A0-A3. S_UB# and S_LB# control the data width as described above.

SRAM WRITE ARRAY

In order to perform an SRAM WRITE operation, S_CE1# and S_WE# must be at VIL, and S_CE2 and S_OE# must be at VIH. When in this state, S_UB# and S_LB# control whether the lower byte is written (S_UB# VIH, S_LB# VIL), the upper byte is written (S_UB# VIL, S_LB# VIH), both upper and lower bytes are written (S_UB# VIL, S_LB# VIL), or neither are written (S_UB# VIH, S_LB# VIH) and the device is in a standby state.

SRAM FUNCTIONAL BLOCK DIAGRAM



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TIMING TEST CONDITIONS

Input pulse levels	0.1V Vcc to 0.9V Vcc
Input rise and fall times	5ns
Input timing reference levels	0.5V
Output timing reference levels	0.5V
Operating Temperature	-40°C to +85°C

SRAM READ CYCLE TIMING

DESCRIPTION	SYMBOL	-10/-11				UNITS
		Vcc = 1.65V–1.95V		Vcc = 1.80V–2.20V		
		MIN	MAX	MIN	MAX	
Read cycle time	^{t}RC		100		85	ns
Address access time	^{t}AA		100		85	ns
Chip enable to valid output	^{t}CO		100		85	ns
Output enable to valid output	^{t}OE		35		35	ns
Byte select to valid output	^{t}LB, ^{t}UB		100		85	ns
Chip enable to Low-Z output	^{t}LZ	0		0		ns
Output enable to Low-Z output	^{t}OLZ	0		0		ns
Byte select to Low-Z output	^{t}LBZ, ^{t}UBZ	0		0		ns
Chip enable to High-Z output	^{t}HZ	0	15	0	15	ns
Output disable to High-Z output	^{t}OHZ	0	15	0	15	ns
Byte select disable to High-Z output	$^{t}LBHZ$, $^{t}UBHZ$	0	15	0	15	ns
Output hold from address change	^{t}OH	5		5		ns

SRAM WRITE CYCLE TIMING

DESCRIPTION	SYMBOL	-10/-11				UNITS
		Vcc = 1.65V–1.95V		Vcc = 1.80V–2.20V		
		MIN	MAX	MIN	MAX	
Write cycle time	^{t}WC		100		85	ns
Chip enable to end of write	^{t}CW		100		85	ns
Address valid to end of write	^{t}AW		100		85	ns
Byte select to end of write	^{t}LBW, ^{t}UBW		100		85	ns
Address setup time	^{t}AS	0		0		ns
Write pulse width	^{t}WP	50		50		ns
Write recovery time	^{t}WR	0		0		ns
Write to High-Z output	^{t}WHZ	0	15	0	15	ns
Data to write time overlap	^{t}DW	50		50		ns
Data hold from write time	^{t}DH	0		0		ns
End write to Low-Z output	^{t}OW	0		0		ns

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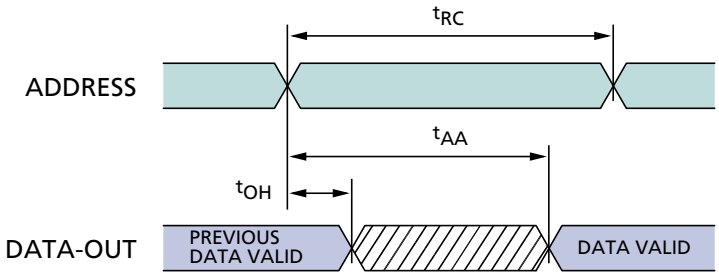
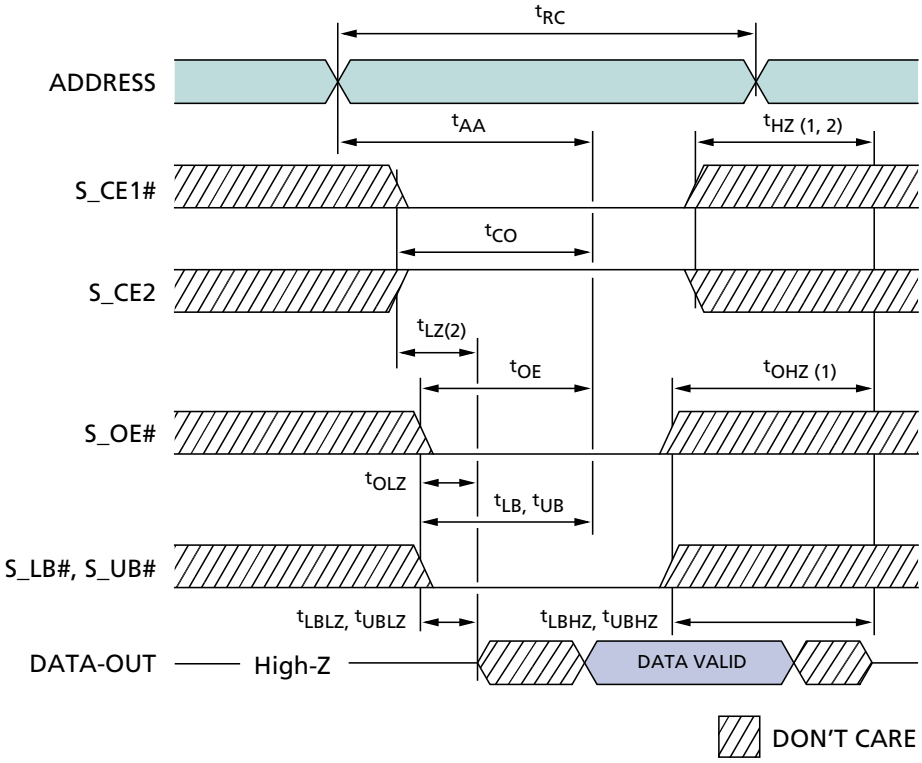
READ CYCLE 1

(S_CE1# = S_OE# = V_{IL}; S_CE2, S_WE# = V_{IH})



READ CYCLE 2

(S_WE# = V_{IH})



READ TIMING PARAMETERS

SYMBOL	-10/-11				UNITS
	Vcc = 1.65V–1.95V		Vcc = 1.80V–2.20V		
	MIN	MAX	MIN	MAX	
tRC		100		85	ns
tAA		100		85	ns
tCO		100		85	ns
tOE		35		35	ns
tLB, tUB		100		85	ns
tLZ	0		0		ns

SYMBOL	-10/-11				UNITS
	Vcc = 1.65V–1.95V		Vcc = 1.80V–2.20V		
	MIN	MAX	MIN	MAX	
tOLZ	0		0		ns
tHZ	0	15	0	15	ns
tOHZ	0	15	0	15	ns
tLBHZ, tUBHZ	0	15	0	15	ns
tOH	5		5		ns

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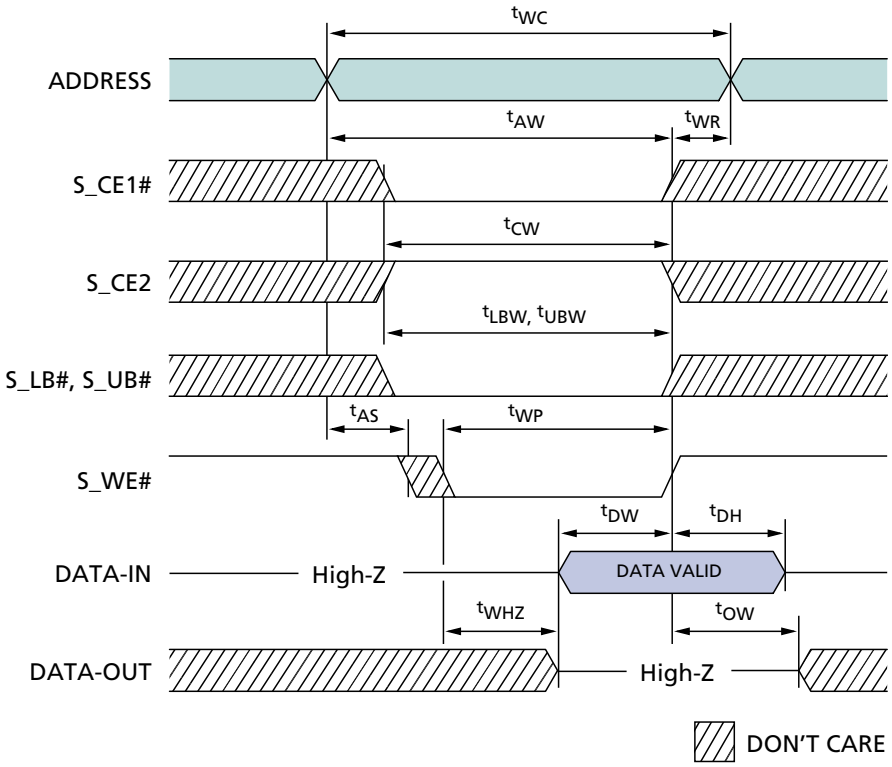
WRITE CYCLE
(S_WE# CONTROL)



WRITE TIMING PARAMETERS

SYMBOL	-10/-11 Vcc = 1.65V–1.95V MIN	-10/-11 Vcc = 1.65V–1.95V MAX	-10/-11 Vcc = 1.80V–2.20V MIN	-10/-11 Vcc = 1.80V–2.20V MAX	UNITS
tWC		100		85	ns
tCW		100		85	ns
tAW		100		85	ns
tLBW, tUBW		100		85	ns
tAS	0		0		ns
tWP	50		50		ns

SYMBOL	-10/-11 Vcc = 1.65V–1.95V MIN	-10/-11 Vcc = 1.65V–1.95V MAX	-10/-11 Vcc = 1.80V–2.20V MIN	-10/-11 Vcc = 1.80V–2.20V MAX	UNITS
tWR	0		0		ns
tWHZ	0	15	0	15	ns
tDW	50		50		ns
tDH	0		0		ns
tOW	0		0		ns

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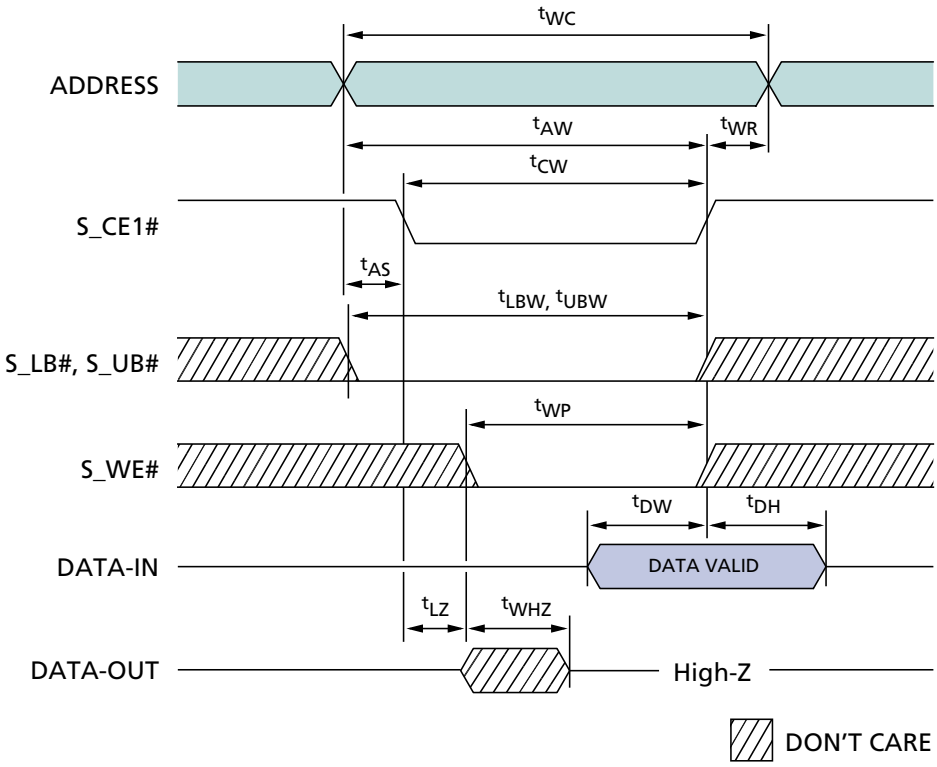
WRITE CYCLE 2
(S_CE1# CONTROL)



WRITE TIMING PARAMETERS

SYMBOL	-10/-11 Vcc = 1.65V–1.95V MIN	-10/-11 Vcc = 1.65V–1.95V MAX	-10/-11 Vcc = 1.80V–2.20V MIN	-10/-11 Vcc = 1.80V–2.20V MAX	UNITS
tWC		100		85	ns
tCW		100		85	ns
tAW		100		85	ns
tLBW, tUBW		100		85	ns
tAS	0		0		ns
tWP	50		50		ns

SYMBOL	-10/-11 Vcc = 1.65V–1.95V MIN	-10/-11 Vcc = 1.65V–1.95V MAX	-10/-11 Vcc = 1.80V–2.20V MIN	-10/-11 Vcc = 1.80V–2.20V MAX	UNITS
tWR	0		0		ns
tWHZ	0	15	0	15	ns
tDW	50		50		ns
tDH	0		0		ns
tOW	0		0		ns

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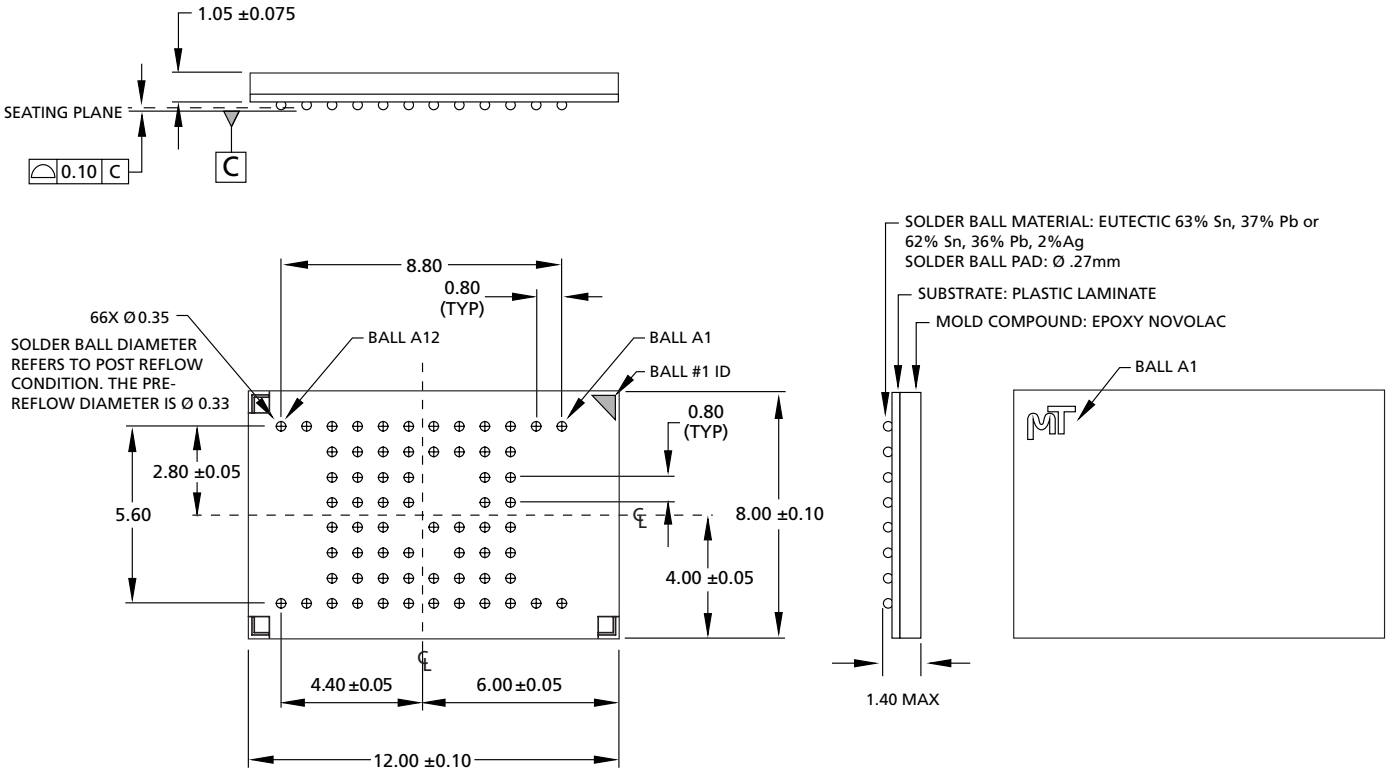
66-BALL FBGA



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.27mm per side.

DATA SHEET DESIGNATION

This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992
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REVISION HISTORY

Rev. 4, Pub. 4/02 ..... 4/02
- Removed the ^{t}CBPH parameter.
- Updated the chip protection mode and register information.
- Updated the block locking information.

Rev. 4, Pub. 9/01 ..... 9/01
- Added minimum spec for SRAM output high voltage (V_{OH})
- Removed CSM Table

Rev. 3, Pub. 6/01 ..... 6/01
- Data sheet designation change (removed “Advance”)

Rev. 2, Pub. 5/01, Advance 5/01
- Added V_{PP1} range
- Added second V_{CC} range

Initial published release, Rev. 1, Advance 11/00

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