256Mb MULTIBANK BURST FLASH
32Mb/64Mb ASYNC/PAGE CellularRAM COMBO

FLASH AND CellularRAM™ COMBO MEMORY

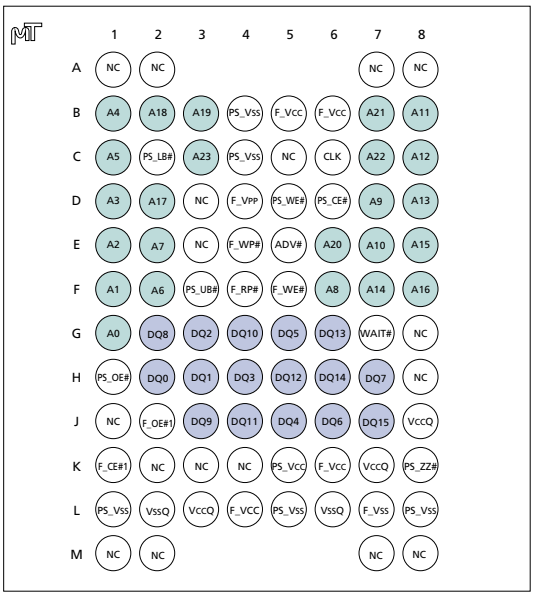
MT28C256532W18S
MT28C256564W18S

Low Voltage, Wireless Temperature

Features

- Stacked die Combo package
  Includes two 128Mb Flash devices
  Choice of either one 32Mb or one 64Mb CellularRAM™ device
- Basic configuration
  Flash
    Flexible multibank architecture
    8 Meg x 16 Async/Page/Burst interface
    Support for true concurrent operations with no latency
  CellularRAM
    Low-power, high-density design
    2 Meg x 16 or 4 Meg x 16 configurations
    Async/Page
- F_VCC, VCCQ, F_VPP, PS_VCC voltages
  1.70V (MIN)/1.95V (MAX) F_VCC, PS_VCC
  1.70V (MIN)/2.24V (MAX) VCCQ
  1.80V (TYP) F_VPP (in-system PROGRAM/ERASE)
  12V ±5% (HV) F_VPP (in-house programming and accelerated programming algorithm [APA] activation)
- Asynchronous access time
  Flash/CellularRAM access time: 60ns @ 1.70V VCC
- Page Mode read access
  Interpage read access: 60ns @ 1.8V F_VCC, PS_VCC
  Intrapage read access: 20ns @ 1.8V F_VCC, PS_VCC
- Burst Mode Read Access
  Max Operating Frequency: 66 MHz
  Flash Initial Latency: 60ns @ 1.8V F_VCC/66 MHz
  CellularRAM Initial Latency: 60ns @ 1.8V PS_VCC/66 MHz
  ^{t}ACLK: 11ns @ 1.8V Vcc
- Enhanced suspend options
  ERASE-SUSPEND-to-READ within same bank
  PROGRAM-SUSPEND-to-READ within same bank
  ERASE-SUSPEND-to-PROGRAM within same bank
- Each Flash contains two 64-bit chip protection registers for security purposes
- Flash PROGRAM/ERASE cycles
  100,000 WRITE/ERASE cycles per block
- Cross-compatible command set support
  Extended command set
  Common Flash interface (CFI) compliant

Figure 1: 88-Ball FBGA



Top View
(Ball Down)

Options

	Marking
• Timing	
60ns	-60
70ns	-70
• Burst Frequency	
66 MHz	6
54 MHz	5
• Boot Block Configuration	
Top/Top	TT
Top/Bottom	TB
Bottom/Top	BT
Bottom/Bottom	BB
• Operating Voltage Range	
PS_VCC 1.70V–1.95V	18
• Operating Temperature Range	
Wireless Temperature (-25°C to +85°C)	WT
• Package	
88-ball FBGA	FT
(8 x 10 grid with eight support balls)	

Part Number Example:

MT28C256564W18S-705 BBWT

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General Description

The MT28C256532W18S/MT28C256564W18S combination Flash and CellularRAM is a high-performance, high-density, memory solution that can significantly improve system performance. The Flash architecture features a multipartition configuration that supports READ-while-PROGRAM/ERASE operations with no latency. An 8Mb partition size enables optimal design flexibility.

Two Flash devices are stacked to achieve the 256Mb density. Both Flash die share a dedicated CE# and OE# control.

The MT28C256532W18S/MT28C256564W18S stacked Flash device enables soft protection for blocks, as read only, by configuring soft protection registers with dedicated command sequences. For security purposes, two user-programmable 64-bit chip protection registers are provided for each Flash device.

The embedded WORD PROGRAM and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). An on-chip device status register can be used to monitor the WSM status and determine the progress of the PROGRAM/ERASE tasks.

Each Flash device has a read configuration register (RCR) that defines how the Flash interacts with the memory bus. For device specifications and additional documentation concerning Flash and CellularRAM features, please refer to the MT28F1284W18 data sheet at www.micron.com/flash and the MT45W2MW16PFA and MT45W4MW16PFA data sheets at http://www.micron.com/cellularram.

The CellularRAM architecture features high-speed CMOS, dynamic random-access memories developed for low-power portable applications The CellularRAM device is available in either 32Mb or 64Mb densities.

To operate seamlessly on a burst Flash bus, CellularRAM products have incorporated a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

The refresh configuration register (CR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated any time during normal operation. Special attention has been focused on standby current consumption during self-refresh.

CellularRAM products include three system-accessible mechanisms used to minimize standby current. Partial array refresh (PAR) limits refresh to the portion of the memory array being used. Temperature compensated refresh (TCR) is used to adjust the refresh rate according to the ambient temperature. The refresh rate can be decreased to lower temperatures to minimize current consumption during standby. Deep sleep mode halts the refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are adjusted through the CR.

Please refer to Micron's Web site www.micron.com/flash for the latest MT28F1284W18 Flash data sheet sheet and http://www.micron.com/cellularram for the latest MT45W2MW16PFA and MT45W4MW16PFA CellularRAM data sheet.

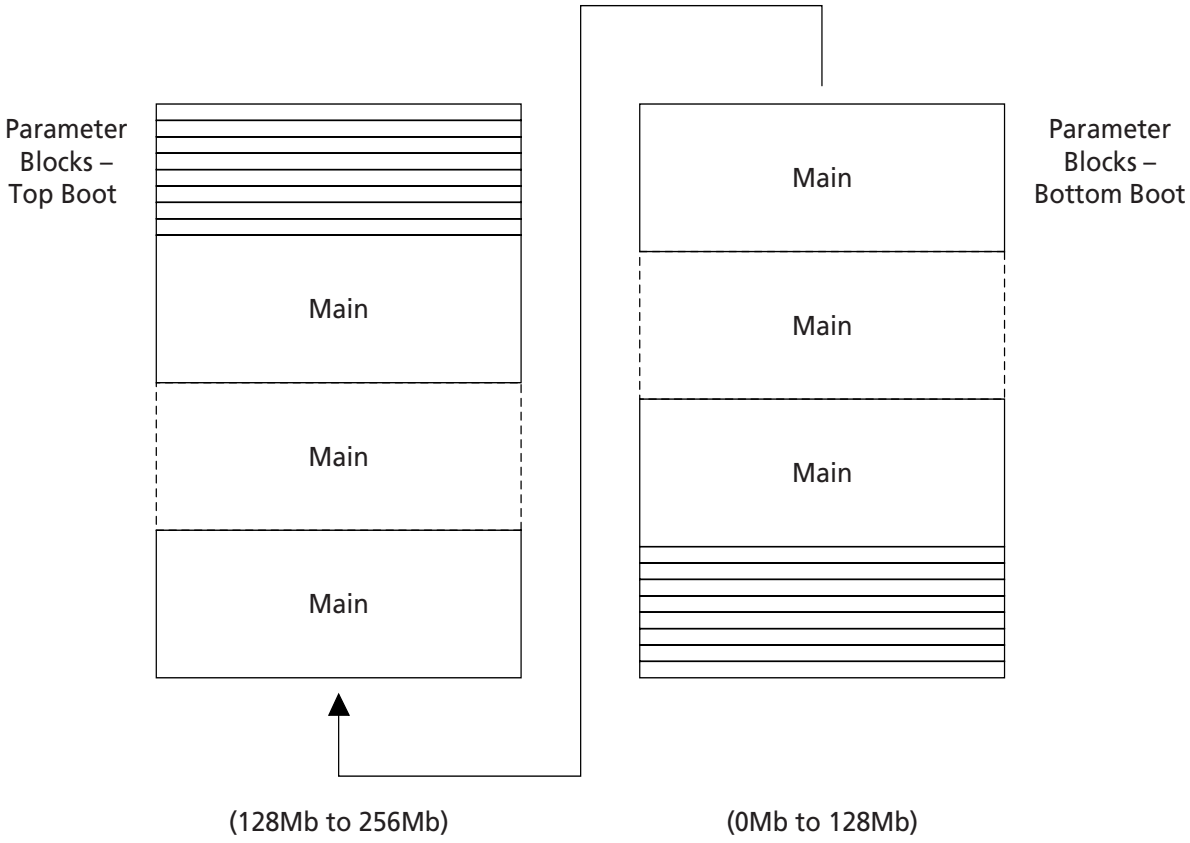
Flash Configurations

Each Flash memory implements a multibank architecture (16 banks of 8Mb each) to allow concurrent operations. Any address within a block address range selects that block for the required READ, PROGRAM, or ERASE operation.

Each Flash memory features eight 8K-word sectors (8 x 65,536 bits), designated as parameter blocks, and the remaining part is organized in main blocks of 64K words each (524,288 bits). The parameter blocks are addressed either by the low order addresses (bottom boot) or by the higher order addresses (top boot).

The two Flash devices can be supplied with any combination of top or bottom boot (e.g., top/top, bottom/bottom, top/bottom, or bottom/top). Please see Figures 2 and 3 for more information.

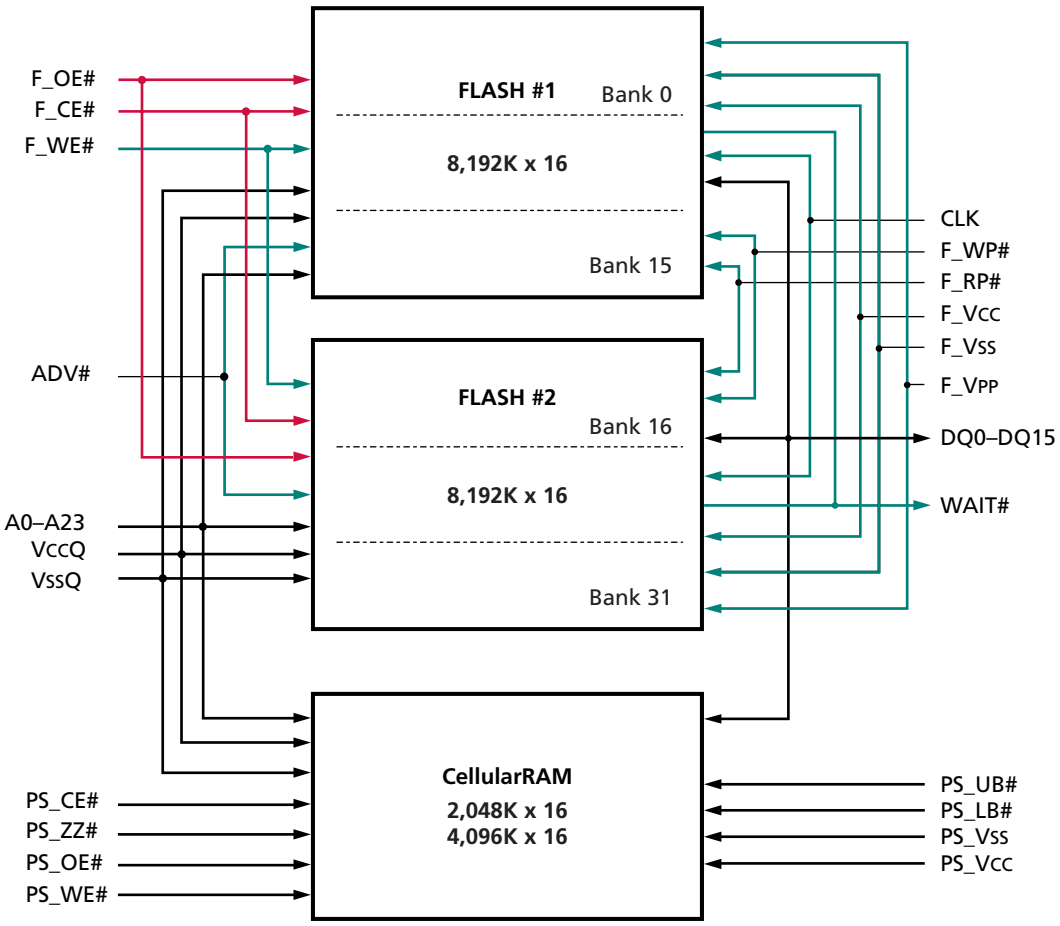
Figure 2: Flash Memory Map



NOTE:

Figure 2 shows a BT (bottom/top) dual Flash configuration.

Figure 3: Block Diagram



Device Marking

Due to the size of the package, the Micron® standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers in Table 1.

Table 1: Cross-Reference for Abbreviated Device Marks

PRODUCT PART NUMBER	PRODUCT MARKING	SAMPLE MARKING	MECHANICAL MARKING
MT28C256532W18SFT-705 BTWT	FW636	FX636	FY636
MT28C256532W18SFT-705 TTWT	FW641	FX641	FY641

Part Numbering Information

Micron's low-power devices are available with several different combinations of features (see Figure 4). Valid combinations of features and their corresponding part numbers are listed in Table 2.

Figure 4: Part Number Chart

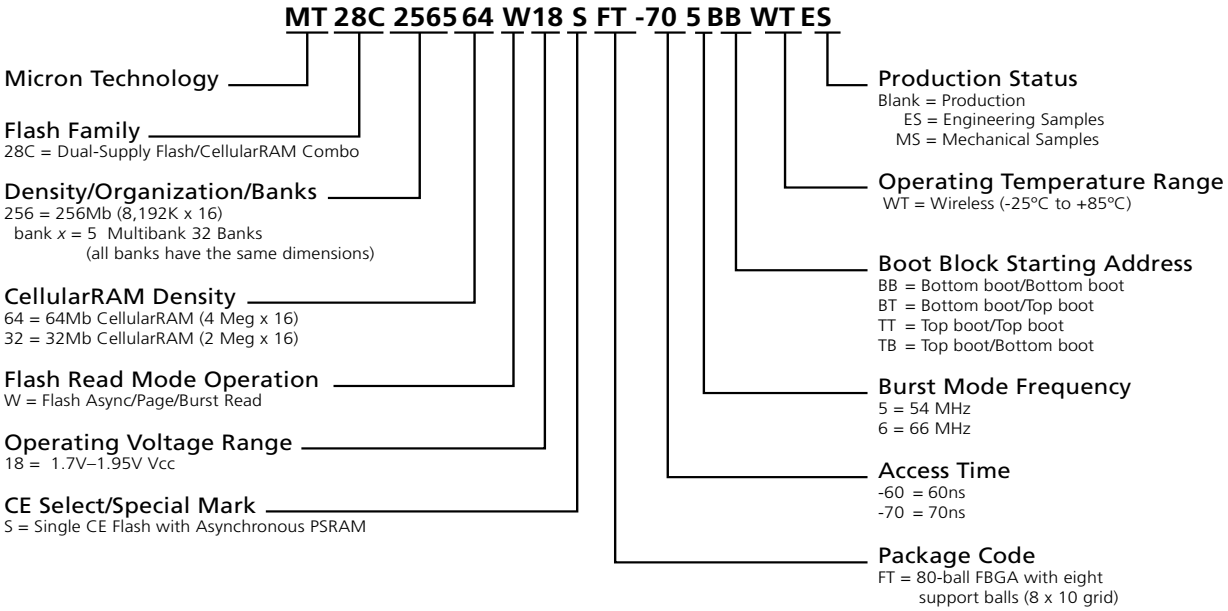


Table 2: Valid Part Number Combinations

PART NUMBER	ACCESS TIME (ns)	BOOT BLOCK STARTING ADDRESS	BURST FREQUENCY (MHz)
MT28C256532W18SFT-705 BTWT	-70	Bottom/Top	54
MT28C256532W18SFT-705 TTWT	-70	Top/Top	54

Table 3: Ball Descriptions

88-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTIONS
B1, B2, B3, B7, B8, C1, C3, C7, C8, D1, D2, D7, D8, E1, E2, E6, E7, E8, F1, F2, F6, F7, F8, G1	A0–A23	Input	Addresses: Flash: A0–A23 CellularRAM: A0–A21 (64Mb) CellularRAM: A0–A20 (32Mb)
K1	F_CE#	Input	Flash Chip Enable
J2	F_OE#	Input	Flash Output Enable
F5	F_WE#	Input	Flash Write Enable
E4	F_WP#	Input	Flash Write Protect
C2	PS_LB#	Input	CellularRAM Lower Byte Control
F3	PS_UB#	Input	CellularRAM Upper Byte Control
D5	PS_WE#	Input	CellularRAM Write Enable
H1	PS_OE#	Input	CellularRAM Output Enable
D6	PS_CE#	Input	CellularRAM Chip Enable
K8	PS_ZZ#	Input	CellularRAM Deep Sleep Mode and Configuration Mode
E5	ADV#	Input	Flash Address Valid (Burst operation only)
C6	CLK	Input	Flash Clock (Burst operation only)
F4	F_RP#	Input	Flash Reset
G2, G3, G4, G5, G6, H2, H3, H4, H5, H6, H7, J3, J4, J5, J6, J7	DQ0–DQ15	I/O	Flash/CellularRAM Data Input/Output
G7	WAIT#	Output	Flash/ WAIT#
L7	F_V_{SS}	Supply	Flash Core Ground
D4	F_V_{PP}	Supply	Flash V_{PP}
K6	F_V_{CC}	Supply	Flash Core Power Supply
L5	PS_V_{SS}	Supply	CellularRAM Core Ground
K5	PS_V_{CC}	Supply	CellularRAM Core Power supply
K7	$V_{CC}Q$	Supply	Flash/CellularRAM I/O supply
L6	$V_{SS}Q$	Supply	Flash/CellularRAM I/O ground
A1, A2, A7, A8, C5, D3, E3, G8, H8, J1, K2, K3, K4, M1, M2, M7, M8	NC	–	No Connect

Boot Configurations

The possible configurations for Flash die are shown in Table 4 below. This table shows the possible configurations of the two Flash devices for either top boot or bottom boot.

Table 4: Possible Boot Configurations for Flash Die

CONFIGURATION	F_CE1#	ORDER CODE
Top/Top	Top	TT
Bottom/Top	Bottom	BT
Top/Bottom	Top	TB
Bottom/Bottom	Bottom	BB

MultiChip Packaging Considerations

Multichip packaging presents unique challenges when controlling complex memory devices.

The MT28C256532W18 and MT28C256564W18 devices combine two Micron Flash devices with a single CellularRAM device.

Unique IDs, State Machines, and Registers

Each Flash device has a separate command state machine (CSM) and status register (SR) and read configuration register (RCR). The RCR settings are separate and can be different for the upper and lower device. Each Flash device has its own OTP, CFI, and device code. Depending on the boot configuration of each Flash device, the OTP, CFI, and device code information may differ.

The CellularRAM device has a refresh configuration register (CR) that defines how the device performs self refresh.

Command Codes

All Flash command codes are independent within each device. Care must be taken when crossing the array boundary between the upper and lower Flash device and the CellularRAM device to ensure that only one device is enabled at one time.

In a two-cycle command sequence such as word program (0x40/data), it is required that both commands be issued to the same device.

It is not recommended that READ and ERASE operations occur simultaneously on two devices.

READ Operation

Page and burst read modes are limited to the address boundaries of each device. A new page/ burst operation must be started when crossing a device boundary.

Flash Reset

The reset control is shared by both Flash die. Bringing RST# conrol LOW will reset both the upper and lower device.

Power Consumption

Multiple chip packaging requires that power calculations consider the active operation of the upper and lower Flash device as well as that of the CellularRAM device. Total power consumed will be the sum of the currents associated with the state of each device. Table 10 on page 14 shows the power consumption specifications.

Table 5: Truth Table

		FLASH SIGNALS			SHARED SIGNALS			CellularRAM SIGNALS					MEMORY OUPUT	
	MODES	F_CE#	F_OE#	F_WE#	F_RP#	ADV#	WAIT#	PS_CE#	PS_CRE#	PS_OE#	PS_UB/LB	PS_WE#	MEMORY BUS CONTROL	D0–D15
FLASH F_CE#	Read	L	L	H	H	L	Valid	CellularRAM must be in High-Z					Flash	DOUT
	Write	L	H	L	H	L	Valid						Flash	DIN
	Standby	H	X	X	H	X	X	CellularRAM any mode allowable					Other	High-Z
	Output Disable	L	H	H	H	X	X						Other	High-Z
	Reset	X	X	X	L	X	X						None	High-Z
CellularRAM	Read	Flash must be in High-Z			X	L	Valid	L	H	L	L	H	PSRAM	DOUT
	Write				X	L	Valid	L	H	H	L	L	PSRAM	DIN
	Standby	Flash any mode allowable			X	X	X	H	H	X	X	X	Other	High-Z
	Output Disable				X	X	X	L	H	H	X	X	Other	High-Z
	Deep Sleep Mode				X	X	X	H	L	X	X	X	Other	High-Z

Flash Electrical Specifications

Table 6: Absolute Maximum Ratings[1]

PARAMETERS/CONDITIONS	MIN	MAX	UNITS	NOTES
Voltage to any ball except VCC, VCCQ, and VPP	-0.5	+2.45	V	
VPP Voltage	-0.2	+14	V	2
VCC Supply Voltage	-0.2	+2.45	V	
VCCQ Supply Voltage	-0.2	+2.45	V	
Output Short Circuit Current		100	mA	
Operating Temperature Range	-25	+85	°C	
Storage Temperature Range	-55	+125	°C	
Soldering Cycle		+260°C for 10s		

NOTE:

1. Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum DC voltage on VPP may overshoot to +14V for periods < 20ns.

Table 7: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Temperature	T_A	-25	–	+85	°C
VCC Supply Voltage	VCC	1.70	–	1.95	V
I/O Supply Voltage	VCCQ	1.70	–	2.24	V
Input/Output Capacitance: DQs	CIO	–	4.0	6.5	pF
VPP Voltage	VPP1	0.9	–	1.95	V
VPP In-factory Programming Voltage	VPP2	11.4	–	12.6	V
Block Erase Cycling (VPP = VPP1)		–	–	100,000	Cycles
Block Erase Cycling (VPP = VPP2)		–	–	1,000	Cycles
Time for VPP at VPP2	^tPPH	–	–	100	Hours

Table 8: Capacitance

T_A = +25°C; f = 1 MHz

PARAMETER/CONDITION	SYMBOL	TYP	MAX	UNITS
Input Capacitance	CIN	TBD	TBD	pF
Output Capacitance	COUT	TBD	TBD	pF

Table 9: AC Characteristics

PARAMETER	SYMBOL	-70/-60		UNITS
		MIN	MAX	
CE# hold from WE# HIGH	^tCH	10		ns

NOTE:

This parameter overrides the value given in the discrete Flash data sheet.

Table 10: DC Characteristics

Notes appear following table; all currents are in RMS unless otherwise noted

PARAMETER	CONDITIONS	SYM	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage		V_{IL}			0.4	V	1
Input High Voltage		V_{IH}	V_{CCQ} - 0.4		V_{CCQ}	V	1
Output Low Voltage I_{OL} = 100µA		V_{OL}			0.1	V	
Output High Voltage I_{OH} = -100µA		V_{OH}	V_{CCQ} - 0.1			V	
V_{PP} Lockout Voltage		F_V_{PPLK}	0.4			V	
V_{CC} Lock		F_V_{LKO}	1.0			V	
VccQ Lock		F_V_{ILKOQ}	TBD			V	
Input Load Current		F_I_{LI}			±1	µA	
Output Leakage Current		F_I_{LO}			±1	µA	
V_{CC} Standby Current with 32Mb PSRAM with 64Mb PSRAM		F_I_{CCS}			140 150	µA	
Asynchronous Read Current		F_I_{CCR}	2	4	TBD	mA	
Page Read Current		F_I_{CCR}	3	6	TBD	mA	
V_{CC} Burst Read Current 4-word Burst Read Current at 54 MHz 4-word Burst Read Current at 66 MHz		F_I_{CCR}	 2 3	 4 5	TBD	mA	2, 3, 5
V_{CC} Burst Read Current 8-word Burst Read Current at 54 MHz 8-word Burst Read Current at 66 MHz		F_I_{CCR}	 2 3	 4 5	TBD	mA	2, 3, 5
V_{CC} Burst Read Current 16-word Burst Read Current at 54 MHz 16-word Burst Read Current at 66 MHz		F_I_{CCR}	 2 3	 4 5	TBD	mA	2, 3, 5
V_{CC} Continuous Burst Read Current Continuous Burst Read Current at 54 MHz Continuous Burst Read Current at 66 MHz		F_I_{CCR}	 5 7	 8 9	TBD	mA	2, 3, 5
F_V_{CC} Program Current F_V_{PP} = F_V_{PP1}, Program in Progress F_V_{PP} = F_V_{PP2}, Program in Progress		F_I_{CCW}		 18 8	 25 15	mA	
F_V_{CC} Block Erase Current F_V_{PP} = F_V_{PP1}, Block Erase in Progress F_V_{PP} = F_V_{PP2}, Block Erase in Progress		F_I_{CCE}		 18 8	 30 15	mA	
F_V_{CC} Program Suspend Current		F_I_{CCWS}		7	25	µA	4
F_V_{CC} Erase Suspend Current		F_I_{CCES}		7	25	µA	4
F_V_{CC} Automatic Power Save Current		F_I_{CCAPS}		7	25	µA	
F_V_{PP} Standby Current F_V_{PP} Program Suspend Current		F_I_{PPS} F_I_{PPWS}		0.2 0.2	5 5	µA	
F_V_{PP} Erase Suspend Current F_V_{PP} Read Current		F_I_{PPES} F_I_{PPR}		0.2 2	5 15	µA	

Table 10: DC Characteristics (continued)

Notes appear following table; all currents are in RMS unless otherwise noted

PARAMETER	CONDITIONS	SYM	MIN	TYP	MAX		UNITS	NOTES
F_VPP Program Current F_VPP = F_VPP1, Program in Progress F_VPP = F_VPP2, Program in Progress		F_IPPW		0.05 8	0.10 22		mA	
F_VPP Erase Current F_VPP = F_VPP1, Erase in Progress F_VPP = F_VPP2, Erase in Progress		F_IPPE		0.05 8	0.10 22		mA	
Read Operating Current Asynchronous Random READ Asynchronous Page READ	VIN = VCC or 0V Chip Enabled, IOUT = 0	PS_ICC1			(-60) 25 15	(-70) 21 13	mA	6, 7
Write Operating Current	VIN = VCC or 0V Chip Enabled, IOUT = 0	PS_ICC2 (-60) (-70)			25 21		mA	6, 7

NOTE:

1. VIL may decrease to -0.4V and VIH may increase to VCCQ + 0.3V for durations not to exceed 20ns.
2. APS mode reduces ICC to approximately ICCS levels.
3. Test conditions: VCC = VCC (MAX), CE# = VIL, OE# = VIH. All other inputs = VIH or VIL.
4. ICCES and ICCWS values are valid when the device is deselected. Any READ operation performed while in suspend mode will have an additional current draw of suspend current (ICCES or ICCWS).
5. Synchronous clock = 54 MHz/burst length = continuous is worst case for VCC burst read current.
6. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
7. This device assumes a standby mode if the chip is disabled (CE# HIGH). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling), regardless of the state of CE#, UB#, and LB#. In order to achieve low standby current all inputs must be either VCC or VSS.

Table 11: CFI

OFFSET	DATA	DESCRIPTION
00	2Ch	Manufacturer code
01	44C6h	Top boot block device code
	44C7h	Bottom boot block device code
02 – 0F	reserved	Reserved
10, 11	0051, 0052	"QR"
12	0059	"Y"
13, 14	0003, 0000	Primary OEM command set
15, 16	0039, 0000	Address for primary extended table
17, 18	0000, 0000	Alternate OEM command set
19, 1A	0000, 0000	Address for OEM extended table
1B	0017	V_{CC} MIN for Erase/Write; Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
1C	0019	V_{CC} MAX for Erase/Write; Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
1D	00B4	V_{PP} MIN for Erase/Write; Bit 7–bit 4 volts in hex; Bit 3–bit 0 100mV in BCD
1E	00C6	V_{PP} MAX for Erase/Write; Bit 7–bit 4 Volts in hex; Bit 3–bit 0 100mV in BCD
1F	0004	Typical timeout for single byte/word program, 2^nµs, 0000 = not supported
20	0000	Typical timeout for maximum size multiple byte/word program, 2^nµs, 0000 = not supported
21	000A	Typical timeout for individual block erase, 2^ns, 0000 = not supported
22	0000	Typical timeout for full chip erase, 2^ns, 0000 = not supported
23	0004	Maximum timeout for single byte/word program, 2^nµs, 0000 = not supported
24	0000	Maximum timeout for maximum size multiple byte/word program, 2^nµs, 0000 = not supported
25	0002	Maximum timeout for individual block erase, 2^ns, 0000 = not supported
26	0000	Maximum timeout for full chip erase, 2^ns, 0000 = not supported
27	0017	Device size, 2^n bytes
28	0001	Bus interface x8 = 0, x16 = 1, x32 = 2, x64 = 3
29	0000	Flash device interface description 0000 = async
2A, 2B	0000, 0000	Maximum number of bytes in multibyte program or page, 2^n
2C	0002	Number of erase block regions within device (4K words and 32K words)
2D, 2E	007E, 0000	Top boot block device erase block region information 1
	0007, 0000	Bottom boot block device erase block region information 1
2F, 30	0000, 0001	Top boot block device erase block region information 1
	0020, 0000	Bottom boot block device erase block region information 1
31, 32	0007, 0000	Top boot block device erase block region information 2
	007E, 0000	Bottom boot block device erase block region information 2
33, 34	0020, 0000	Top boot block device erase block region information 2
	0000, 0001	Bottom boot block device erase block region information 2
35, 36	0000, 0000	Reserved for future erase block region information
37, 38	0000, 0000	Reserved for future erase block region information
39, 3A	0050, 0052	"PR"
3B	0049	"I"
3C	0031	Major version number, ASCII
3D	0033	Minor version number, ASCII

Table 11: CFI (continued)

OFFSET	DATA	DESCRIPTION
3E 3F 40 41	00E6 0003 0000 0000	Optional Feature and Command Support Bit 0 Chip erase supported no = 0 Bit 1 Suspend erase supported = yes = 1 Bit 2 Suspend program supported = yes = 1 Bit 3 Chip lock/unlock supported = no = 0 Bit 4 Queued erase supported = no = 0 Bit 5 Instant individual block locking supported = yes = 1 Bit 6 Protection bits supported = yes = 1 Bit 7 Page mode read supported = yes = 1 Bit 8 Synchronous read supported = no = 0 Bit 9 Simultaneous operation supported = yes = 1
42	0001	Program supported after erase suspend = yes
43, 44	0003, 0000	Bit 0 block lock status active = yes; Bit 1 block lock down active = yes
45	0018	V_{CC} supply optimum, 00 = not supported, Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
46	00C0	V_{PP} supply optimum, 00 = not supported, Bit 7–bit 4 volts in BCD; Bit 3–bit 0 100mV in BCD
47	0001	Number of protection register fields in JEDEC ID space
48, 49	0080, 0000	Lock bytes LOW address, lock bytes HIGH address
4A, 4B	0003, 0003	2^n factory programmed bytes, 2^n user programmable bytes
4C	0004	Page mode read capability
4D	0004	Number of synchronous mode read configuration fields that follow
4E	0001	Synchronous mode read capability configuration 1
4F	0002	Synchronous mode read capability configuration 2
50	0007	Synchronous mode read capability configuration 3
51	0000	Synchronous mode read capability configuration 4
52	Top: 0002 Bot :0002	Number of device hardware partition regions within the device
53	Top: 000F Bot: 0001	Number of identical partitions within the partition region
54	Top: 0000 Bot: 0000	Number of identical partitions within the partition region
55	Top: 0011 Bot: 0011	Number of identical partitions within the partition region
56	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in program mode
57	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in erase mode
58	Top: 0001 Bot: 0002	Types of erase block regions in this partition region
59	Top: 0007 Bot: 0007	Partition region 1 erase block type 1 information
5A	Top: 0000 Bot: 0000	Partition region 1 erase block type 1 information
5B	Top: 0000 Bot: 0020	Partition region 1 erase block type 1 information
5C	Top: 0001 Bot: 0000	Partition region 1 erase block type 1 information

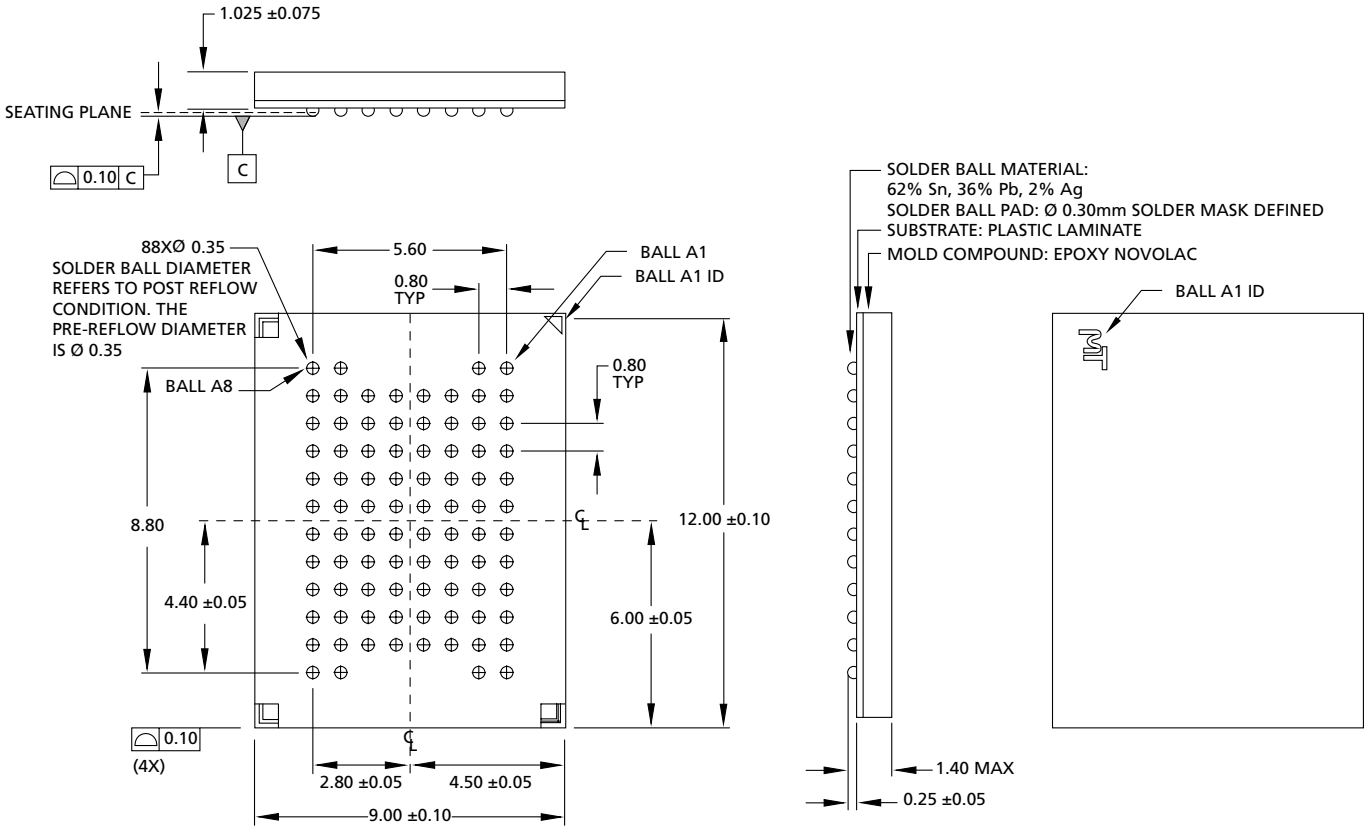
Table 11: CFI (continued)

OFFSET	DATA	DESCRIPTION
5D	Top: 0064 Bot: 0064	Partition 1 (erase block type 1)
5E	Top: 0000 Bot: 0000	Partition 1 (erase block type 1)
5F	Top: 0001 Bot: 0001	Partition 1 (erase block type 1) bits per cell; internal ECC
60	Top: 0003 Bot: 0003	Partition 1 (erase block type 1) page mode and synchronous mode capabilities
Bot: 61	Bot: 0006	Partition region 1 erase block type 2 information
Bot: 62	Bot: 0000	Partition region 1 erase block type 2 information
Bot: 63	Bot: 0000	Partition region 1 erase block type 2 information
Bot: 64	Bot: 0001	Partition region 1 erase block type 2 information
Bot: 65	Bot: 0064	Partition region 1 (erase block type 2)
Bot: 66	Bot: 0000	Partition region 1 (erase block type 2)
Bot: 67	Bot: 0001	Partition region 1 (erase block type 2) bits per cell
Bot: 68	Bot: 0003	Partition region 1 (erase block type 2) page mode and synchronous mode capabilities
Top: 61 Bot: 69	Top: 0001 Bot: 000F	Number of identical partitions within the partition region
Top: 62 Bot: 6A	Top: 0000 Bot: 0000	Number of identical partitions within the partition region
Top: 63 Bot: 6B	Top: 0011 Bot: 0011	Number of PROGRAM/ERASE operations allowed in a partition
Top: 64 Bot: 6C	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in program mode
Top: 65 Bot: 6D	Top: 0000 Bot: 0000	Simultaneous PROGRAM/ERASE operations allowed in other partitions while a partition in this region is in erase mode
Top: 66 Bot: 6E	Top: 0002 Bot: 0001	Types of erase block regions in this partition region
Top: 67 Bot: 6F	Top: 0006 Bot: 0007	Partition region 2 erase block type 1 information
Top: 68 Bot: 70	Top: 0000 Bot: 0000	Partition region 2 erase block type 1 information
Top: 69 Bot: 71	Top: 0000 Bot: 0000	Partition region 2 erase block type 1 information
Top: 6A Bot: 72	Top: 0001 Bot: 0001	Partition region 2 erase block type 1 information

Table 11: CFI (continued)

OFFSET	DATA	DESCRIPTION
Top: 6B	Top: 0064	Partition 2 (erase block type 1)
Bot: 73	Bot: 0064	
Top: 6C	Top: 0000	Partition 2 (erase block type 1)
Bot: 74	Bot: 0000	
Top: 6D	Top: 0001	Partition 2 (erase block type 1) bits per cell
Bot: 75	Bot: 0001	
Top: 6E	Top: 0003	Partition 2 (erase block type 1) page mode and synchronous mode capabilities
Bot: 76	Bot: 0003	
Top: 6F	Top: 0007	Partition region 2 erase block type 2 information
Top: 70	Top: 0000	Partition region 2 erase block type 2 information
Top: 71	Top: 0020	Partition region 2 erase block type 2 information
Top: 72	Top: 0000	Partition region 2 erase block type 2 information
Top: 73	Top: 0064	Partition 2 (erase block type 2)
Top: 74	Top: 0000	Partition 2 (erase block type 2)
Top: 75	Top: 0001	Partition 2 (erase block type 2) bits per cell
Top: 76	Top: 0003	Partition 2 (erase block type 2) page mode and synchronous mode capabilities
77		TBD
78	32Mb: 0020	PSRAM Density
	64Mb: 0040	
79 – 7H		Reserved

Figure 5: 88-Ball FBGA



NOTE:
1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.27mm per side.

Data Sheet Designation

Advance: This data sheet contains initial descriptions of products still under development.

For additional documentation concerning Flash and CellularRAM features, functional descriptions, programming, and timing, please refer to the MT28F644W18 data sheet at www.micron.com/flash and the MT45W2MW16FPA and MT45W4MW16FPA data sheets at http://www.micron.com/cellularram.

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Revision History

- Original document, Rev. A 6/03