

PHOTO IC COUPLER

MT25300, MT25310

J-41-83

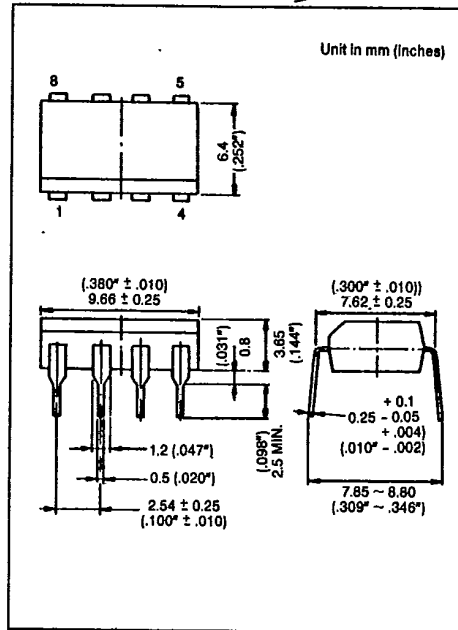
APPLICATIONS

- DIGITAL LOGIC ISOLATION
- LINE RECEIVER
- POWER SUPPLY CONTROL
- SWITCHING POWER SUPPLY
- TRANSISTOR INVERTER

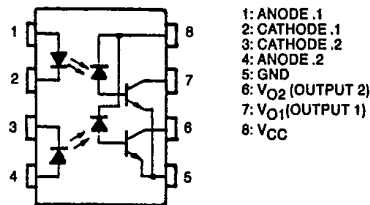
The MARKTECH MT25300 and MT25310 dual photocouplers consist of a pair of GaAlAs light emitting diodes and integrated photodetector. This unit is 8-lead DIP package. Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

FEATURES

- TTL Compatible
- Switching Speed : $t_{pHL}, t_{pLH} = 0.3\mu s$ (Typ.)
(@ $R_L = 1.9k\Omega$)
- Guaranteed Performance Over Temp. : $0 \sim 70^\circ C$
- Isolation Voltage : $2500 V_{rms}$ Min.



PIN CONFIGURATION (TOP VIEW)



SCHEMATIC

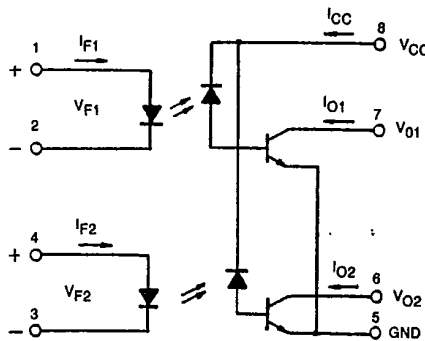


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RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{CC}	0	—	12	V
Forward Current, Each Channel	I _F	—	16	25	mA
Operating Temperature	T _{opr}	-25	—	85	°C

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Each channel, Note 1)	I _F	25	mA
	Pulse Forward Current (Each channel, Note 2)	I _{FP}	50	mA
	Total Pulse Forward Current (Each channel, Note 3)	I _{FPT}	1	A
	Reverse Voltage (Each channel)	V _R	5	V
	Diode Power Dissipation (Each channel, Note 4)	P _D	45	mW
DETECTOR	Output Current (Each channel)	I _O	8	mA
	Peak Output Current (Each channel)	I _{OP}	16	mA
	Supply Voltage	V _{CC}	-0.5 ~ 15	V
	Output Voltage (Each channel)	V _O	-0.5 ~ 15	V
	Output Power Dissipation (Each channel, Note 5)	P _O	35	mW
Operating Temperature Range		T _{opr}	-55 ~ 100	°C
Storage Temperature Range		T _{stg}	-55 ~ 125	°C
Lead Solder Temperature (10 sec.) **		T _{sold}	260	°C
Isolation Voltage (AC, 1 min., R.H. ≤ 60%, Note 7)		BV _S	2500	V _{rms}

Note 1: Derate 0.8mA above 70°C.

Note 2: 50% duty cycle, 1ms pulse width. Derate 1.6mA/°C above 70°C.

Note 3: Pulse width 1μs, 300pps.

Note 4: Derate 0.9mW/°C above 70°C.

Note 5: Derate 1mW/°C above 70°C.

** 1.6mm below seating plane.

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ELECTRICAL CHARACTERISTICS Over Recommended Temperature ($T_a=0^{\circ}\text{C} \sim 70^{\circ}\text{C}$, Unless otherwise noted).

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.**	MAX.	UNIT
Current Transfer Ratio (Each channel)	MT25300	$I_F=16\text{mA}$, $V_O=0.4\text{V}$	7	30	—	%
	MT25310	$V_{CC}=4.5\text{V}$, $T_a=25^{\circ}\text{C}$ (Note 6)	19	30	—	
	MT25300	$I_F=16\text{mA}$, $V_O=0.5\text{V}$	5	—	—	%
	MT25310	$V_{CC}=4.5\text{V}$ (Note 6)	15	—	—	
Logic Low Output Voltage (Each channel)	MT25300	$I_F=16\text{mA}$, $I_O=1.1\text{mA}$ $V_{CC}=4.5\text{V}$	—	0.1	0.4	V
	MT25310	$I_F=16\text{mA}$, $I_O=2.4\text{mA}$ $V_{CC}=4.5\text{V}$	—	0.1	0.4	V
Logic High Output Current (Each channel)	I_{OH}	$I_F=0\text{mA}$, $V_O=V_{CC}=5.5\text{V}$ $T_a=25^{\circ}\text{C}$	—	3	500	nA
		$I_F=0\text{mA}$, $V_O=V_{CC}=15\text{V}$	—	—	50	μA
Logic Low Supply Current	I_{CCL}	$I_{F1}=I_{F2}=16\text{mA}$ $V_{O1}=V_{O2}=\text{Open}$, $V_{CC}=15\text{V}$	—	160	—	μA
Logic High Supply Current	I_{CCH}	$I_{F1}=I_{F2}=0\text{mA}$, $V_{O1}=V_{O2}=\text{Open}$, $V_{CC}=15\text{V}$	—	0.05	4	μA
Input Forward Voltage (Each channel)	V_F	$I_F=16\text{mA}$, $T_a=25^{\circ}\text{C}$	—	1.65	1.7	V
Temperature Coefficient of Forward Voltage (Each channel)	$\frac{\Delta V_F}{\Delta T_a}$	$I_F=16\text{mA}$	—	-2	—	mV/ $^{\circ}\text{C}$
Input Reverse Breakdown Voltage (Each channel)	BV_R	$I_R=10\mu\text{A}$, $T_a=25^{\circ}\text{C}$	5	—	—	V
Input Capacitance (Each channel)	C_{IN}	$f=1\text{MHz}$, $V_F=0$	—	60	—	pF
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity=45% $t=5\text{s}$, $V_{I-O}=3000\text{V}_{dc}$, $T_a=25^{\circ}\text{C}$ (Note 7)	—	—	1.0	μA
Resistance (Input-Output)	R_{I-O}	$V_{I-O}=500\text{V}_{dc}$ (Note 7)	—	10^{12}	—	Ω
Capacitance (Input-Output)	C_{I-O}	$f=1\text{MHz}$ (Note 7)	—	0.6	—	pF
Input-Input Leakage Current	I_{I-I}	Relative Humidity=45% $t=5\text{s}$, $V_{I-I}=500\text{V}$ (note 8)	—	0.005	—	μA
Resistance (Input-Input)	R_{I-I}	$V_{I-I}=500\text{V}_{dc}$ (Note 8)	—	10^{11}	—	Ω
Capacitance (Input-Input)	C_{I-I}	$f=1\text{MHz}$ (Note 8)	—	0.25	—	pF

**All typicals $T_a=25^{\circ}\text{C}$.

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SWITCHING SPECIFICATIONS

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=5\text{V}$, $I_F=16\text{mA}$)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to Logic Low at Output (Each channel)	MT25300	t_{pHL}	1	$R_L=4.1\text{k}\Omega$	—	0.3	1.5	μs
	MT25310			$R_L=1.9\text{k}\Omega$	—	0.2	0.8	
Propagation Delay Time to Logic High at Output (Each channel)	MT25300	t_{pLH}	1	$R_L=4.1\text{k}\Omega$	—	0.5	1.5	μs
	MT25310			$R_L=1.9\text{k}\Omega$	—	0.3	0.8	
Common Mode Transient Immunity at Logic High Level Output (Each channel, Note 9)	MT25300	C_{MH}	2	$I_F=0\text{mA}$, $V_{CM}=400\text{Vp-p}$ $R_L=4.1\text{k}\Omega$	—	1000	—	$\text{V}/\mu\text{s}$
	MT25310			$I_F=0\text{mA}$, $V_{CM}=400\text{Vp-p}$ $R_L=1.9\text{k}\Omega$	—	1000	—	
Common Mode Transient Immunity at Logic Low Level Output (Each Channel, Note 9)	MT25300	C_{ML}	2	$V_{CM}=400\text{Vp-p}$ $R_L=4.1\text{k}\Omega$, $I_F=16\text{mA}$	—	-1000	—	$\text{V}/\mu\text{s}$
	MT25310			$V_{CM}=400\text{Vp-p}$ $R_L=1.9\text{k}\Omega$, $I_F=16\text{mA}$	—	-1000	—	
Bandwidth (Each channel, Note 10)		BW	3	$R_L=100\Omega$	—	2	—	MHz

Note 6: DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.

Note 7: Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.

Note 8: Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

Note 9: Common mode transient immunity in Logic High level is the maximum tolerable (Positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm} , to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0\text{V}$).

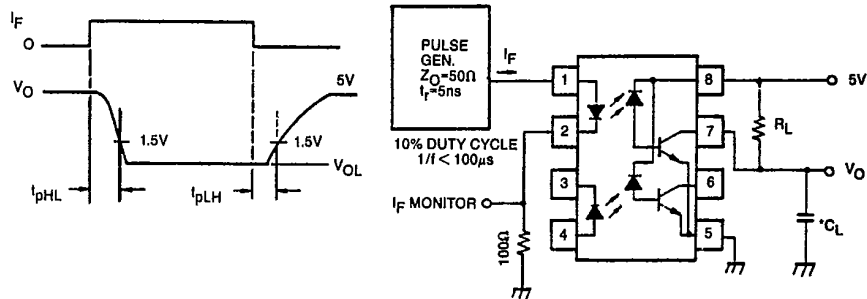
Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm} , to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8\text{V}$).

Note 10: The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

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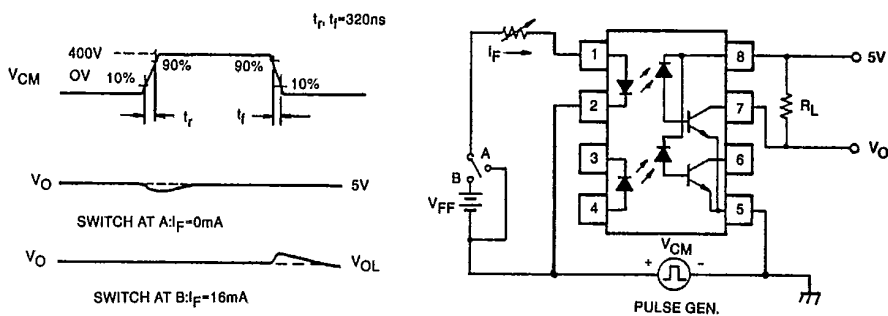
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TEST CIRCUIT 1: SWITCHING TIME, t_{pHL} , t_{pLH}



* C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 2: TRANSIENT IMMUNITY AND TYPICAL WAVEFORM



TEST CIRCUIT 3: FREQUENCY RESPONSE

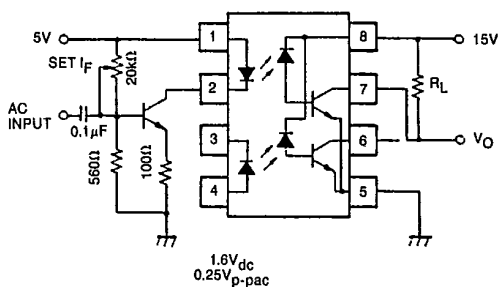
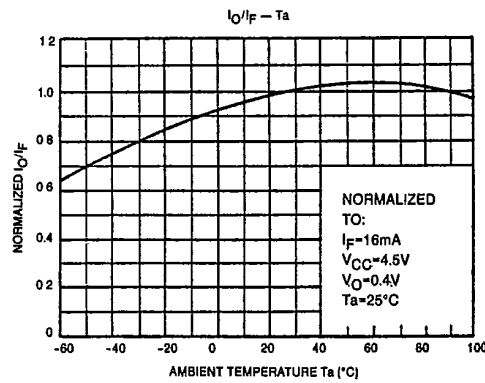
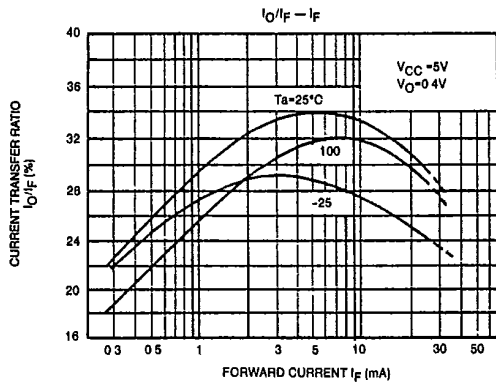
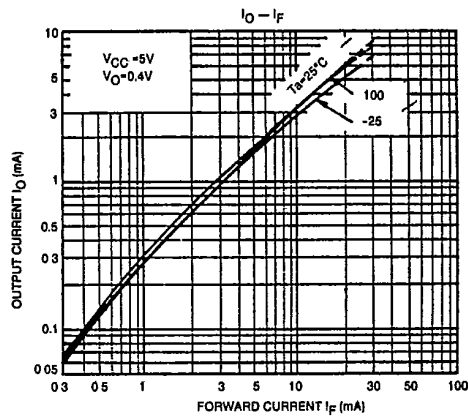
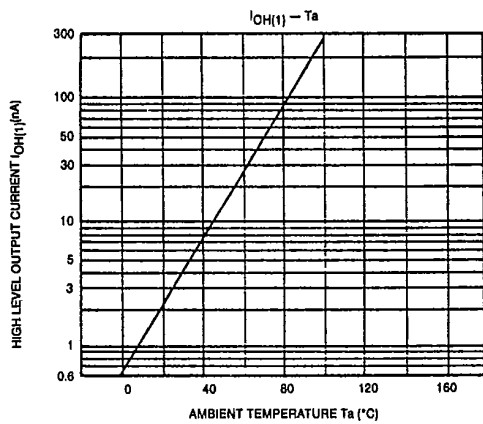
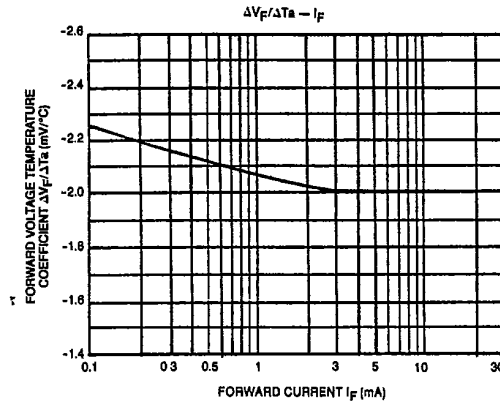
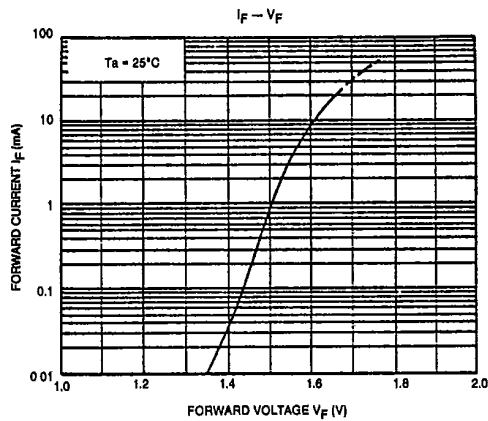


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