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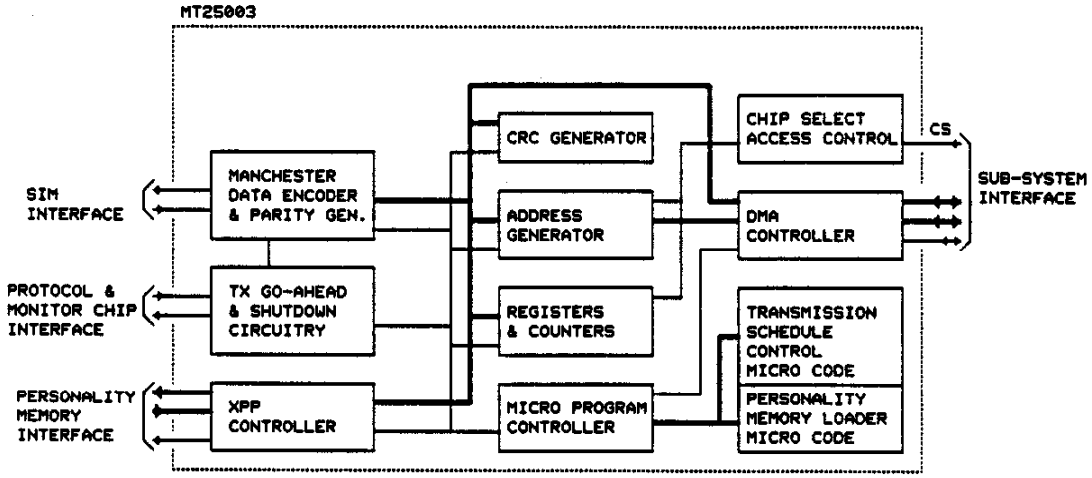
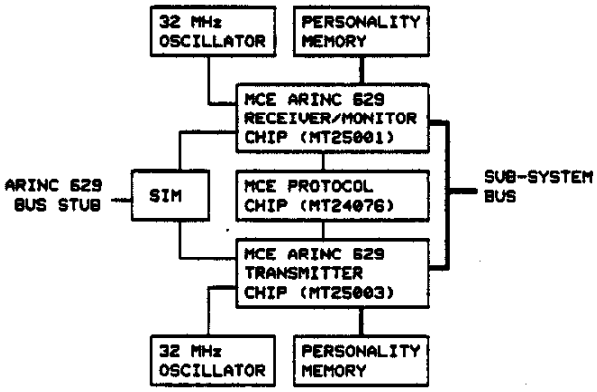
MT25003 ARINC629 TRANSMITTER

DEVICE INTERNAL ORGANISATION



ARINC 629 INTERFACE ORGANISATION



FEATURES

COMPATIBLE WITH BP AND CP MODE DATABUS SYSTEMS.

ENHANCED SUB-SYSTEM ADDRESSING MODES FOR EFFICIENT DATA HANDLING.

LEVEL 3 MESSAGE QUEUING FOR EFFICIENT BUS UTILISATION.

124 PIN PGA PACKAGE.

GENERATES AND APPENDS CRC WORD TO SELECTED WORDSTRINGS.

SUPPORTS PERSONALITY MEMORY PROGRAMMING VIA THE SUB-SYSTEM BUS AND THE ARINC 629 DATABUS.

USE WITH MCE RECEIVER AND PROTOCOL CHIPS FOR FULL FUNCTION ARINC 629 TERMINALS.

LOW POWER CMOS TECHNOLOGY.

1.0 GENERAL DESCRIPTION

This device can be used with the MCE RX/MONITOR chip and PROTOCOL chip to realise a full function ARINC 629 terminal. It implements the transmission functions defined in ARINC 629 with a number of additional features. It is compatible with the standard ARINC 629 Serial Interface Module (SIM).

The device will respond to an external TX Go-Ahead signal (TXGO) and performs all the actions to transmit a message at level 1, level 2, level 3 backlog, or level 3 new (only level 1 is used in Basic Protocol systems).

At level 1, the device supports Block Schedule mode, Alternate (block) Schedule mode and Independent Schedule mode. There is also a Synchronise function (forces the schedule counters to a specified point in the transmission schedule) and an Initialise function (forces the schedule counters to the start of the transmission schedule). Block/Independent schedule selection is made by XPP programming. Initialise, Sync and Alternate schedule action may be selected by a discrete input signal to the chip or by writing to an internal configuration register.

At level 2, the device logs a transmission request from the sub-system (by a discrete input or by writing an internal register) and uses an XPP cell specified by an internal register. At the next level 2 TX Go-Ahead, the message is transmitted and the request is cleared.

At level 3, the device logs a transmission request and uses a specified XPP cell (similar to level 2). At the next level 3 TX Go-Ahead, the message is transmitted and the request is cleared. If the message has not been sent at the end of level 3, the request is changed into a level 3 backlog request. If level 3 message queuing is enabled, an internal queue pointer register is used to access a transmission request control block (in sub-system memory). When a message has been sent, a new level 3 request is logged automatically for the next entry in the queue. In this way, a message will be transmitted at each level 3 transmission opportunity as long as there are entries remaining in the queue. Entries can be appended to the queue by the sub-system at any time.

At all levels, the top 4 bits of the transmitted label are the value of the CID (channel identifier) strap input pins. The remainder of the message content is controlled by data in the transmitter personality program (XPP). An address field in XPP is used by the device to fetch the message data from sub-system memory using DMA transfers on the sub-system bus. Other fields in XPP control features including direct/indirect address selection, wordstring length, generation & appending of the CRC word, and level 3 queue operations.

The device continuously monitors an input signal from the associated RX/Monitor and protocol chips. When this input indicates a transmission error has been detected, the current transmission is quickly terminated. When this happens, the schedule counters and level 3 queue are left in a tidy state. At power-on reset and after responding to an error, the device (re)loads bus access protocol parameters from XPP into the associated protocol chip.

The device includes a special serial input channel to load XPP data from an associated RX/Monitor chip. This channel is only operational when the transmit function is disabled and allows the XPP to be programmed over the ARINC 629 databus. This feature is described in detail in the RX/Monitor chip datasheet. XPP data can also be accessed through the sub-system databus by processor initiated read/write cycles.

2.0 DEVICE OPERATION

2.1 Initialisation

A low going pulse on the reset input (PWRSTN) sets internal registers to their default states and initialises the internal timing circuits. The state of the transmit enable input (TXE) (from the RX/Monitor chip) determines subsequent actions. Whilst TXE is low (Transmitter Disabled), the device will only respond to data on the XPP serial data loader input (SRTX). When TXE changes from low to high, the device will execute the following initialisation sequence to prepare the terminal for transmission. Three bus access protocol parameters are read from an XPP control cell and strobed into the associated Protocol chip. The four CID input pins select which one of 16 control cells is used. This allows selection of a different set of parameters for each value of CID. The Block/Independent schedule mode bit is read from control cell 0 in XPP and the Initialise schedule function is set. The device then waits for a TX Go-Ahead. Initialisation takes approximately 3μS from TXE=>1.

2.2 Starting a Message Transmission

The transmitter continuously receives LVL0 and LVL1 inputs from the protocol chip indicating the current level of operation in the bus access protocol. The transmitter chip responds by setting its REQSTN output low when there is a transmit request pending at the indicated level. REQSTN will always be low during level 1 unless level 1 transmissions are inhibited by configuration register bit setting (see section 4.1). When conditions for transmission are satisfied (TX Go-Ahead), each of the dual Protocol circuits places a high-going pulse on one of the TXGO1 & TXGO2 inputs. These two inputs must be simultaneously high to start the transmitter. The transmitter immediately sets TXHB low and TXO high for the pre-pre-sync pulse at the start of the first wordstring. LVL0 & LVL1 inputs are latched. The message that follows is a function of level, schedule mode and the XPP program.

2.3 Level 1 Transmission

At level 1, a message can contain up to 31 wordstrings, each defined by a different XPP cell. This device implements Block schedule, Alternate (block) schedule and Independent schedule modes as defined in the ARINC 629 standard. Block or Independent schedule mode is selected by a bit in XPP control cell 0 and is consequently fixed for any particular XPP program. The operation of Sync and Initialise functions and mode changing is designed to be clean and easily controlled.

To initiate a Synchronise frame, the discrete input SYNCN or the Sync bit in the configuration register is briefly asserted (by the sub-system). The Sync request is recognised at the start of the next level 1 transmission. The schedule counters are now set to the values in the SYNC words of the control cells and the Sync message is transmitted. The chip sets the Sync bit in the status register at the start of the Sync message transmission and clears it at the start of the next (non-sync) level 1 transmission. If the Sync request is continuously asserted, Sync messages will be transmitted at every level 1 Go-Ahead until the request is removed. If Sync is requested with Alternate schedule mode, then the ALT values from the control cells are loaded into the schedule counters instead of the SYNC values.

An initialise frame is requested by briefly asserting the INITN input or Init configuration register bit. The initialise request is serviced in the same way as described above for the Sync request. In this case however, the schedule counters are reset to zero instead of the SYNC values. If Alternate schedule is selected at the same time as Initialise, then the schedule counters are set to the ALT values in the control cells.

Note that Alternate schedule cannot be selected with Independent schedule mode, the Alternate schedule request will be ignored.

Switching between Block schedule mode and Alternate schedule mode by toggling the ALTN input or configuration register bit forces the execution of an Initialise cycle each time the mode is changed. This ensures the terminal never tries to transmit a string from an undefined XPP cell after a mode change.

2.4 Level 2 Transmission

The device internal register L2XPPCELL is used to control level 2 transmission. This register may be written at any time by a sub-system controlled (CS) write cycle. Writing to this register with the most significant bit (bit 15) set to zero requests a level 2 transmission. Bits 0-9 contain the XPP cell address of the requested message (bits 0-4 map onto XX0-4, bits 5-9 map onto XY0-4). The sub-system may set bit 15 to one to cancel the request before transmission. Bit 15 is automatically set to one when the device begins its level 2 transmission. The state of bit 15 may be examined by reading the status register (see section 4.2). Take care to avoid changing the data in the L2XPPCELL register whilst the device is transmitting at level 2.

During power-on reset, the L2XPPCELL register is initialised to point to the default L2XPP cell (XY4-0 = 00010, XX4-0 = 11111). This cell can never be used by level 1 schedules. A discrete input (L2RQN) may be pulsed low to set L2XPPCELL bit 15 = 1. This mechanism may be used by simple systems (which have no way of writing to the L2XPPCELL register) to request a single level 2 message defined by the default L2XPP cell.

All level 2 messages comprise a single wordstring only. Before transmission, a bit in the XPP cell (LVL23) is checked to ensure this message is permitted at level 2 (or level 3). This prevents a faulty sub-system requesting level 2 transmission of a wordstring which should only form part of the level 1 schedule. This mechanism allows the system designer to partition XPP cells into periodic (level 1) messages and aperiodic (level 2/3) messages.

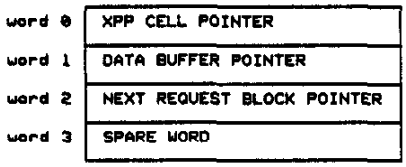
2.5 Level 3 Transmission

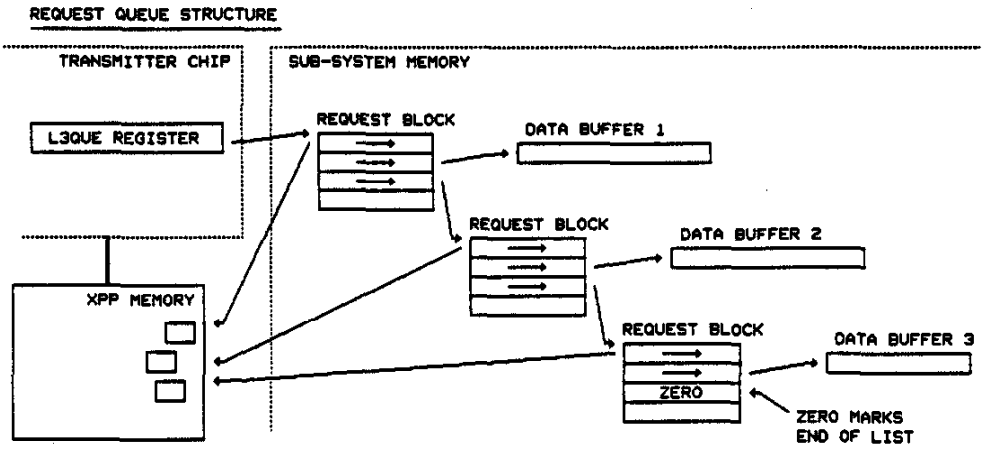
Simple (non-queued) level 3 transmission is very similar to level 2. In this case L3XPPCELL is the internal register used to control transmission. L3RQN is the discrete request input and the default L3XPP cell address is XY4-0 = 00011, XX4-0 = 11111. Requests not serviced at the end of level 3 are automatically changed into backlog requests for the next minor frame.

There is a special XPP cell address reserved for use with an optional level 3 protocol modification. If a level 3 TX Go-Ahead is received when there is no request logged, then the transmission uses the cell address XY4-0 = 00000, XX4-0 = 11111. This cell should be programmed with the "Level 3 Sync" message. This function is not used when standard ARINC 629 CP protocol is selected.

Level 3 queue operation uses the following additional elements. An XPP cell bit (L3QUEN) is set low to indicate this (level 3) transmission is part of a queue of messages. An internal register (L3QUE) holds the address of the current level 3 transmission request block in sub-system memory. Each request block is a four word area of sub-system memory loaded by the sub-system. Request blocks are linked by pointers to form the request chain. This is shown in the diagram below.

REQUEST BLOCK LAYOUT (4 x 16 BIT WORDS)





Notes

1) Request blocks must start on a 4 word (i.e., 8 byte) address boundary.
2) All pointers are 16 bit word addresses, i.e. map onto address bits A1-A16.
3) The top 3 address bits (A17-A19, i.e. above the 64k word boundary) of the request block address are taken from the (internal) configuration register. This means all request blocks reside in the same 64k word page of sub-system memory.
4) The top 3 address bits of the data buffer are taken from the BADR field of XPP. This means all buffers used with a particular XPP cell must reside in the same 64k word page of memory.
5) Address mapping of the XPP cell pointer is: bit0-bit4 -> XX0-XX4
   bit5-bit9 -> XY0-XY4.
6) The spare word in the request block is available for sub-system use.
7) A 'word' in sub-system memory is 16 bits. Bit 0 is least significant bit.
8) The L3QUEN and Indirect address bits must be set in all of the XPP cells used by the queue.

To start the queue, the sub-system takes the following actions.

1) A request block and data buffer must be prepared for each message as shown above.
2) The L3QUE register must be loaded with the (word) address of the first request block in the queue.
3) The L3XPPCELL register must be loaded with a copy of the XPPCELL word in the first request block. Note bit 15 must be zero to log the request.

The sub-system may add entries to the queue at any time. It is advisable for the sub-system to check the queue is not empty (i.e., L3QUE register not zero) after adding an entry in case the last queue entry was completed as the new entry was added. Request blocks and buffers may be re-used after the requests have been processed. When all requests have been processed, the L3QUE register is set to zero and the queue stops. When further requests arrive, the queue must be started again as described above.

The transmitter chip updates its internal registers at the end of each level 3 transmission. The pointer to the next request block is read into the L3QUE register. If this value is not zero, the new XPPCELL address is read into the L3XPPCELL register. If an error occurs during level 3 transmission, the action depends on the L3SKIP bit in the current XPP cell. Either the queue is stopped with the failed request block pointer in L3QUE, or the failed message is skipped and the device transmits the next message in the queue at the next opportunity. If an error is encountered during queue pointer manipulation, then the queue will always stop. In every case, an XERFN error output will be generated and the appropriate status register error bit will be set.

3.0 XPP Controlled Functions

3.1 Sub-System Memory Addressing

Data for transmission is fetched from the sub-system memory by DMA transfer controlled by the transmitter chip. Direct and Indirect address modes are available, selected by the Indirect address bit (IND) in the XPP cell. With direct address mode, the address taken from the BADR,MADR,LADR fields of the XPP cell is the sub-system word address (A19-A1) of the first dataword transmitted. With indirect addressing, the sub-system location specified by the address in XPP contains a 16 bit pointer to the first dataword to be transmitted. The pointer and the data both use the same top 3 address bits (A17-A19) taken from the BADR field in the XPP cell.

Note that with indirect addressing, it is important the sub-system processor initialises indirect address pointers before enabling the ARINC 629 terminal. Indirect addressing allows the system designer to use any number of alternative buffering schemes, and avoids the danger of transmitting invalid data when the sub-system starts to update a data buffer during transmission.

3.2 Cyclic Redundancy Check Word Generation

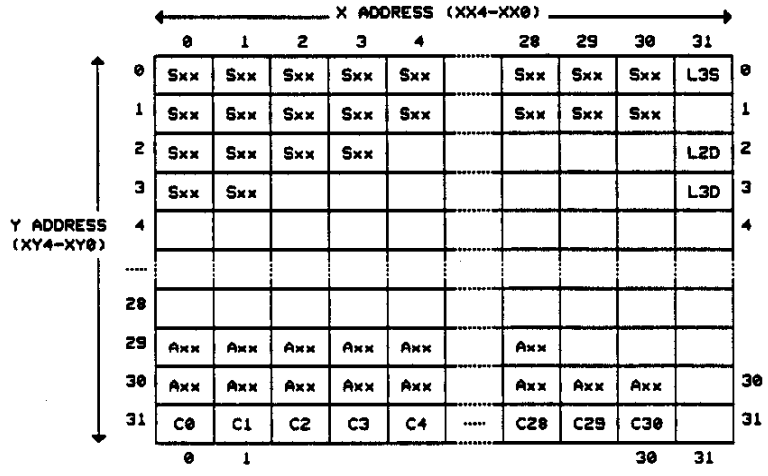
The CRC enable (CRCEN) bit in the XPP cell controls the operation of the on-chip CRC generator. When enabled, a CRC code word is inserted in the last word of the wordstring. Note the wordstring length is not increased by this action, but the number of datawords fetched from the sub-system is reduced by one. The device uses the CRC algorithm defined in the ARINC 629 standard.

The CRC writeback (CRCWB) bit in the XPP cell enables the CRC word to be written back to sub-system memory in the location following the last transmitted dataword. This allows use of the CRC generator with Compare and Writeback monitor modes described in the RX/Monitor chip datasheet.

3.3 XPP Memory Layout

XPP memory layout is as defined in the ARINC 629 standard with a number of minor extensions. Cells are allocated for default level 2 & 3 messages. Other level 2 & 3 messages may be programmed into any other unused cells. Additional data is stored in the control cells. Control cell 0 contains a Block/Independent schedule select bit. Control cells 0-15 contain 16 sets of bus access protocol parameters corresponding to the 16 values of the CID strap inputs on the transmitter. This data duplicates the parameters held in RPP. Note that independent CID strap inputs are used on the transmit and receive chips so that the parameters held in XPP and RPP are totally independent.

XPP MEMORY LAYOUT - EACH BLOCK REPRESENTS AN 8 BYTE CELL



C0-C30 - CONTROL CELLS 0-30.
Sxx - LEVEL 1 SCHEDULE CELLS (EXAMPLE).
Axx - ALTERNATE SCHEDULE CELLS (EXAMPLE).
L2D - LEVEL 2 DEFAULT MESSAGE CELL.
L3D - LEVEL 3 DEFAULT MESSAGE CELL.
L3S - LEVEL 3 SYNC MESSAGE CELL (MODIFIED CP ONLY)
ANY UNUSED CELLS MAY BE USED FOR LEVEL 2 & 3 MESSAGES.

3.4 XPP Cell Format

byte 0 byte 1

xxxx	MLBL	LLBL		
MADR		LADR		
XWM		XWC		
XIV		AXWM	xx	BADR

byte 6 byte 7

xxxx, xx Unused bit fields.

MLBL 12 bit label for transmission (the top 4 bits of the transmitted
LLBL 16 bit label word are taken from the CID strap inputs).

BADR 3 bit sub-system block address (A19-A17). This field supplies high order sub-system address bits to extend the addressing range beyond 64k words. Wordstring buffers must not cross block boundaries.

MADR 16 bit sub-system word address (A16-A1).
LADR

XWM 8 bit control field:- EOM,DATA,VWS,XIVE,XIVL,LVL23,CRCWB,CRCEN

EOM (bit 7) =0 to indicate this is the last wordstring in a message (level 1 only). This is described in the ARINC 629 standard.

DATA (bit 6) =0 to indicate at least one dataword follows the label in this wordstring.

VWS (bit 5) =0 to indicate this wordstring is variable length wordstring format as defined in the ARINC 629 standard.

XIVE (bit 4) =0 to enable the generation of an interrupt strobe (XIVSN) output at the start of message transmission.

XIVL (bit 3) =0 to enable the generation of an interrupt strobe (XIVSN) output at the end of message transmission.

LVL23 (bit2) =0 to permit this XPP cell to be used for messages transmitted at levels 2 and 3.

CRCWB (bit 1) =0 to enable the transmitter chip to write-back the generated CRC word to sub-system memory at the end of the transmit data buffer. This can only be used when CRCEN=0.

CRCEN (bit 0) =0 to enable CRC check word generation and insertion in the transmitted wordstring.

XWC 8 bit data word count for the wordstring. The values 1-255 (true logic) indicate 1-255 datawords follow the label. The value 0 indicates 256 datawords follow the label. This field is not used with variable length wordstring format (VWS).

XIV 8 bit interrupt vector. This value is placed on the IV0-7 outputs during wordstring transmission.

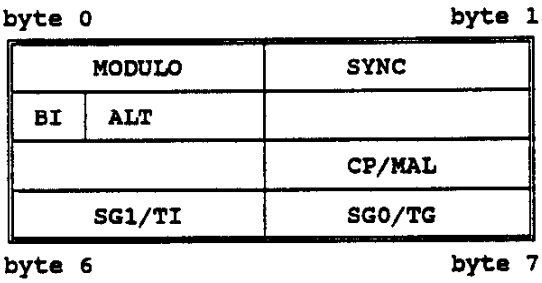
AXWM 3 bit auxiliary control field:- IND,L3QUEN,L3SKIP

IND (bit 7) =0 to select indirect addressing.

L3QUEN (bit 6) =0 to select level 3 queue operation.

L3SKIP (bit 5) =0 to skip a failed level 3 queued message and continue with the next message in the queue.

3.5 XPP Control Cell Format



MODULO	Maximum schedule counter value in block or independent schedule modes as defined in the ARINC 629 standard.
SYNC	Value to force into the schedule counter when Sync operation is selected.
ALT	Alternate schedule start value as defined in the ARINC 629 standard. Only used in first control cell.
BI (bit 7)	Block/Independent schedule select bit. 0=Block, 1=Independent. Only used in first control cell.
CP/MAL	Bus access protocol parameter. Bit 7 selects BP or CP mode, 0=CP, 1=BP. Bits 6-0 select the MAL (maximum aperiodic message length) for CP mode.
SG1/TI	Bus access protocol parameter. Bit 7 is SG1. Bits 6-0 are TI6-TI0.
SG0/TG	Bus access protocol parameter. Bit 7 is SG0. Bits 6-0 are TG6-TG0.

The first 16 control cells contain sets of bus access protocol parameters for the corresponding 16 values of the CID strap inputs. The transmitter chip controls the process of loading one of these sets of parameters into the protocol chip. The parameters are described more fully in the protocol chip data sheet and the ARINC 629 standard.

4.0 Accessing Internal Registers and Personality Memory from the Sub-System

These are accessed by sub-system processor controlled read/write cycles with CSN (chip select) asserted. Address decodes are:

A19-A4	A3-A1	
XXXXXX	000	Read status register, Write Configuration Register.
XXXXXX	001	Read Interrupt Vector Register.
XXXXXX	010	Write L2XPPCELL Register.
XXXXXX	011	Write L3XPPCELL Register.
XXXXXX	100	Read/Write L3QUE (level 3 queue pointer) Register.
XXXXXX	101	Read/Write Sub-System Address Register.
XXXXXX	110	Read CRC Register.
XXXXXX	111	Read/Write a Byte to XPP memory.

Notes: Write to Sub-System address register and Read/Write to personality memory is conditional on configuration register setting.

Definitions of internal register bit fields follow.

4.1 Configuration Register Bits

This register is write-only. Note: In this device, data inputs D4,D5,D6 must be stable before the leading edge of the data strobe (NDSO) or else spurious ALT, SYNC or INIT schedule cycles may be generated.

Bit 0 — 0 = Disable Transmit function,
1 = Enable Transmit function
(Bit0 = 1 at reset).

Bit 1 — 0 = Disable all writes to XPP memory,
1 = Enable writing to XPP memory
(Bit1 = 1 at reset).

Bit 2 — 0 = Inhibit the transmit request (REQSTN) output at level 1,
1 = Enable the transmit request output at level 1 (normal operation)
(Bit2 = 1 at reset).

Bit 3 — 1 = Force a minimum of one wait state for sub-system DMA transfers
(Bit3 = 0 at reset).

Bit 4 — 1 = Select the Alternate transmission schedule (ALT) at level 1. This function may also be selected by the discrete input signal ALTN. (Bit4 = 0 at reset).

Bit 5 — 1 = Select Synchronise schedule (SYNC) action at level 1. This function may also be selected by the discrete input signal SYNCN. (Bit5 = 0 at reset).

Bit 6 — 1 = Select Initialise schedule (INIT) action at level 1. This function may also be selected by the discrete input INITN.
(Bit6 = 0 at reset).

Bit 7 — 0 = Normal chip operation,
1 = Chips test mode (Bit7 = 0 at reset).

Bits 8-10 — These are the top 3 address bits (A17-A19) appended to the 16 bit L3QUE register when accessing level 3 request blocks.
(Bits 8-10 = 0 at reset).

Bits 11-15 — Reserved.

4.2 Status Register Bits

This register is read-only.

Bit 0 Transmitter Active. Set to 1 throughout message transmission and transmit error recovery.

Bit 1 SYNC Active. Set to 1 from the start of level 1 Sync message transmission until the start of the next level 1 transmission.

Bit 2 1 = level 2 Request Pending. This is the inverse of bit 15 (the request bit) of the L2XPPCELL register. It is set when a request is issued, and reset when the requested message transmission begins.

Bit 3 1 = level 3 Request Pending. This is the inverse of bit 15 (the request bit) of the L3XPPCELL register. It is set when a request is issued, and reset when the requested message transmission begins.

Bit 4 LVL0
Bit 5 LVL1 These two bits reflect the current bus access protocol level. They are a copy of the LVL0 and LVL1 input signals from the associated protocol chip coded as follows.

LVL1	LVL0	
0	0	level 1
0	1	level 2
1	1	level 3 backlog
1	0	level 3 new

Bit 6 1 = DMA Data Error. The DMA cycle(s) to fetch datawords from sub-system memory were not completed quickly enough. Also set by CRC word write-back DMA cycle failure. DMA cycles must be serviced within 4μS.

Bit 7 1 = DMA Queue Error. A DMA cycle to access the level 3 queue request block was not completed quickly enough. DMA cycles must be serviced within 4μS.

Bit 8 1 = XPP Access Error. The sub-system has issued a level 2/3 request referencing an XPP cell which has not been enabled for use at level 2/3. That is, LVL23 = 1 in the XPP cell.

Bit 9 INIT Active. Set to 1 from the start of level 1 Init message transmission until the start of the next level 1 transmission.

Bits 10-15 Not defined.

Note: Bits 6-8 (the Error Flags) are set when an error is detected and cleared after the status register is next read. Ther error strobe (XERFN) is asserted when one of the error bits is set. Other error conditions are detected in the RX/Monitor chip. These other conditions set a status register bit in the RX/Monitor chip and generate a monitor error strobe pulse (MONERRN).

4.3 Interrupt Vector Register

This register is read-only. It is a copy of bytes 6 & 7 of the current XPP cell entry.

Bits 0-2 BADR - subsystem block address (A17-19).

Bits 3-4 Not used by the transmitter - These bits may be programmed in XPP for use by the sub-system.

Bits 5-7 AXWM field from XPP as defined in section 3.4.

Bits 8-15 XIV - 8 bit interrupt vector.

4.4 L2XPPCELL and L3XPPCELL Registers

These registers are write-only. They are used to issue level 2 and level 3 transmission requests. The formats are described in section 2.4.

4.5 Level 3 Queue (L3QUE) Register

This register may be written and read. It is the bottom 16 bits (A16-A1) of the word address of the next level 3 queue request block in sub-system memory. The least significant 2 bits of this register are always zero when read. Its use is defined in section 2.5.

4.6 Sub-System Address Register

During transmission this register contains the address of the last word sent or about to be sent. This register may be read after an error to discover whereabouts in a wordstring the error occurred. It is also used as the personality memory address register for loading/readback via the sub-system interface. The chip transmit function must be disabled (by zeroing bit 0 of the configuration register) before the address register can be written from the sub-system.

4.7 CRC Register

This register is read-only. The internally generated cyclic redundancy code (CRC) may be read from this register at the end of a wordstring transmission. The register contents remain valid only until the end of the label word transmission of the next wordstring.

4.8 Read/Write to XPP

Any attempt to read or write personality memory is ignored until the transmit function is disabled (configuration register bit0 = 0). Configuration register bit1 (write enable) must be set to one before data can be written to XPP. Data is accessed one byte at a time. Only the least significant 8 data lines (D0-7) are used, D8-15 are dont care on write and indeterminate on read. The personality memory address is taken from the sub-system address register and incremented after each read or write. XPP address lines map onto address register bits as follows.

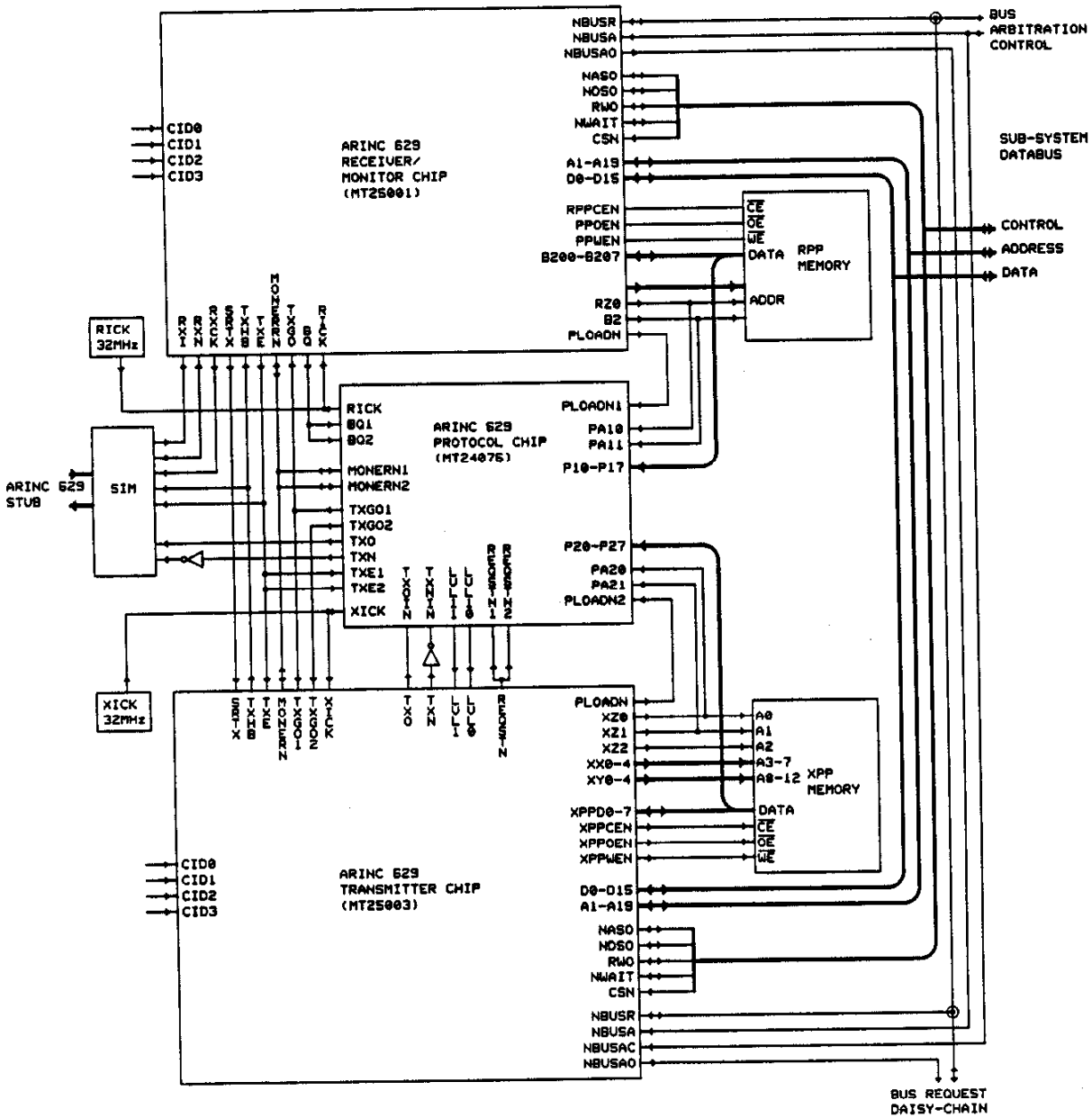
Sub-System Address Register	>>	XPP Address
bit12 - bit8	>>	XY4 - XY0
bit 7 - bit 3	>>	XX4 - XX0
bit 2 - bit 0	>>	XZ2 - XZ0

5.0 Writing XPP via the ARINC 629 Databus

XPP can be loaded with data received from the ARINC 629 databus. This function is controlled by the associated RX/Monitor chip and fully described in the datasheet for that device. This function is only enabled when the transmitter configuration register is set to enable the transmit chip and enable XPP write. Data and commands are received from the RX/Monitor chip over a serial datalink (SRTX). This function may be disabled by tying the SRTX input to zero (0v).

6.0 ARINC 629 Terminal Hardware Configuration

The following diagram shows all the connections between the three MCE chips in a complete ARINC 629 terminal. Typical connections to personality memory, SIM and sub-system are also shown.



7.0 Device Interfaces and Signal Descriptions

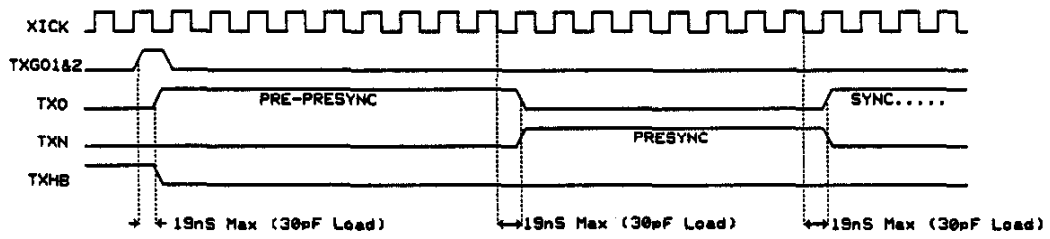
7.1 SIM Interface

The chip generates complementary manchester encoded data and a transmit enable output to drive a SIM (serial interface module). The transmission starts asynchronously as soon as TX Go-Ahead conditions (TXGO1&2 inputs) are satisfied. A strap input option (DELTXHB) modifies the timing of the transmit enable signal to either allow or forbid the generation of a doublet at the (current mode) SIM output at the end of a wordstring.

Note: This device generates a zero parity bit on all transmitted words. The manchester encoded data (TXO & TXN) should be routed through the protocol chip (MT24076) where the correct parity bit will be added. This is shown in the interconnection diagram (section 6.0).

Signals

TXO,TXN	outputs	Transmitted Manchester encoded data (2M Bit/sec.).
TXHB	output	Active low transmit enable output. This signal is taken low for the duration of each wordstring transmission.
DELTXHB	input	Strap this input to VSS (0v) to force TXHB high immediately a wordstring ends. Strap this input to VDD (+5v) to hold TXHB low for 8 clock cycles (250nS) after the end of a wordstring. DELTXHB should be strapped to VSS to conform to the latest supplement of ARINC 629, current mode bus.



Notes

1) The pre-presync pulse ends 9 clock cycles after the -ve XICK edge on which TXGO is detected.

2) To guarantee TXGO detection in a specific clock cycle, it should be stable from 8nS before until 12nS after the XICK -ve edge.

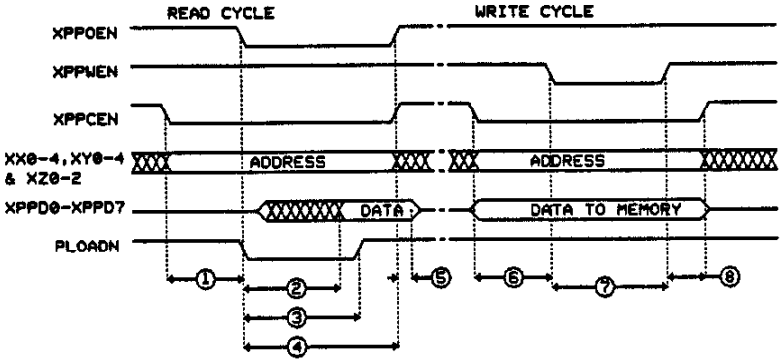
3) At the start and end of a wordstring, TXHB changes within 20nS of the XICK -ve edge on which TXO/TXN changes (30pF load). When DELTXHB=1, TXHB remains low for 8 XICK clock cycles after the end of the wordstring.

7.2 Personality Memory Interface

Standard three line memory control signals (CE, OE and WE) are provided for XPP. The interface is designed to work with 250nS memory chips. Timing of internally generated read/write cycles is shown below. Timing of cycles initiated via the sub-system (chip select) interface imposes less severe constraints on the memory chips. Address, data and control signals are high impedance during power-on reset. Data and control signals have high value internal pullup resistors to prevent them floating during reset, but an external pullup resistor may be needed on the write enable signal with some system/memory arrangements.

Signals

XY4-XY0, XX4-XX0	output	XPP cell address lines.
XZ2-XZ0	output	XPP byte address lines.
XPPD7-XPPD0	bi-dir	XPP data lines.
XPPCEN	output	Active low XPP chip enable control signal.
XPPOEN	output	Active low XPP output enable control signal.
XPPWEN	output	Active low XPP write enable control signal.
PLOADN	output	This active low signal indicates protocol parameter data is being read from XPP. It is used to strobe this data into the associated protocol chip. Timing is shown below.



PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM
1	CE TO OE	120nS	130nS
2	OE TO DATA VALID		150nS
3	OE TO END OF PLOAD	170nS	
4	OE WIDTH	245nS	255nS
5	DATA HOLD AFTER OE	0nS	60nS
6	SETUP BEFORE WE	115nS	130nS
7	WE WIDTH	180nS	195nS
8	HOLD AFTER WE	40nS	

7.3 Monitor/Control Interface

This interface comprises signals needed to start and stop transmissions and to control XPP loading from the ARINC 629 databus.

Signals

TXE	input	Active high transmitter enable input from the RX/Monitor chip. Used for hard shutdown of transmitter after repeated errors. Also used for transmitter disable during XPP loading via the ARINC 629 databus.
MONERRN	input	Active low input indicates an error has been detected by monitoring logic and transmission should be stopped. Minimum pulse width nominally 500nS.
LVL1,LVL0	inputs	Signals from associated protocol chip define current level of operation. See sections 2.2 & 4.2.
REQSTN	output	Active low output indicates there is a transmission request pending at the current level of operation. This signal is used by the associated protocol chip.
TXGO1,TXGO2	input	TX Go-Ahead inputs from associated protocol chip. Active high pulse (min width 150nS) simultaneously on both inputs signals start of transmission.
SRTX	input	Serial input channel from associated RX/Monitor chip used for loading XPP data. Tie this input to VSS (0v) if not used.

7.4 Sub-System Interface

This interface can operate in two modes.
1) DMA mode where the bus is acquired and controlled by the terminal chip to transfer wordstrings to/from sub-system memory.
2) Processor controlled mode to read/write XPP and status registers on the chip.

A number of signals are bi-directional to support both modes.

Strap inputs SSIMOD0-1 configure bus timing and control signals for compatibility with VME, Multibus or Zbus systems. A configuration register bit may be set to force a minimum of one wait state in each DMA cycle. This allows more time for slow memory sub-systems to generate the DTACK/READY/WAIT signal.

Signals

A1-19	bi-dir	19 Active high Word address lines (8 blocks of 64k words).
D0-15	bi-dir	16 bit active high data to/from sub-system memory/processor.
NASO	bi-dir	AS/ or ALE or AS/ Control signal (VME/Multibus/Zbus mode).
NDSO	bi-dir	DS/ or READ/ or DS/ Control signal (VME/Multibus/Zbus mode).
RWO	bi-dir	R/W or WRITE/ or R/W Control signal (VME/Multibus/Zbus mode).
NWAIT	bi-dir	DTACK/ or READY/ or WAIT/ Control signal (VME/Multibus/Zbus). This is an open drain output stage.

(Note: / after a signal indicates active low)

NBUSR	bi-dir	Active low bus request for DMA. This is an open drain output stage.
NBUSA	input	Active low bus acknowledge for DMA.
NBUSAC	input	Active low bus acknowledge look-ahead for DMA cycle coupling to associated RX/Monitor chip.
NBUSAO	output	Active low bus acknowledge out for DMA request chain.

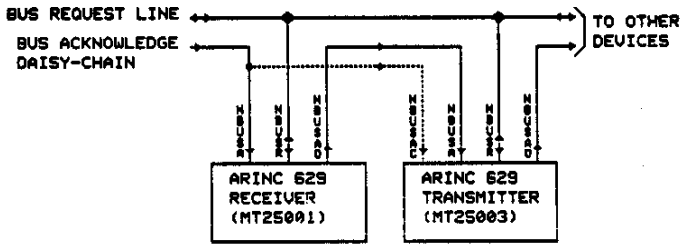
XIVSN	output	Active low transmitted wordstring interrupt strobe. Pulse width is 500nS nominal.
XERFN	output	Active low error interrupt strobe. Pulse width is 500nS nominal. XERFN is asserted whenever a sub-system interface DMA access error or XPP error is detected, i.e., whenever any of bits 6-8 of the status register become set.
IVREN	input	Active low interrupt vector enable. Enables the tri-state outputs IV0-7.
IV0-7	output	8 bit interrupt vector. Tristate outputs.
CSN	input	Active low chip select for sub-system controlled read/writes.
IOCK	output	General purpose 8MHz clock synchronised to sub-system interface DMA cycles.

7.4.1 Sub-system Bus Acquisition

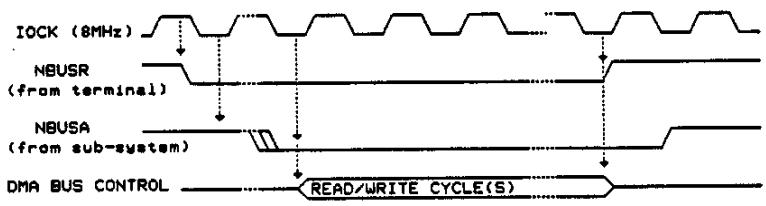
The terminal device uses the same sequence of actions to gain control of the sub-system bus in each of the three bus configurations.

a) The terminal waits for NBUSR=1 and NBUSA=1 or
NBUSR=0 and NBUSA=1 and NBUSAC=0 .
b) The terminal pulls NBUSR low (open drain) to request the bus.
c) The terminal waits for the sub-system to relinquish control of the bus and set NBUSA=0.
d) The terminal executes one or more read/write cycles.
e) The terminal releases the bus and stops driving NBUSR low.
f) The sub-system sets NBUSA=1 and takes control of the bus.

The second condition in step (a) allows the transmitter device to issue a request when the associated receiver device is executing a DMA cycle. The transmitter device will then take control of the bus immediately the receiver has finished its cycle. The NBUSAC input monitors the NBUSA input of the associated receiver chip to detect this condition. The bus request chain connections are shown below. If the NBUSAC input is not used it should be tied to VDD (+5v).



Whenever NBUSA=0 and the terminal is not requesting the bus, NBUSAO is set low. These two signals can be used in a bus-grant daisy chain. The delay from NBUSA to NBUSAO is less than 30nS. For proper terminal operation, bus requests should be serviced within 4μS. The sequence of operation is shown graphically below.

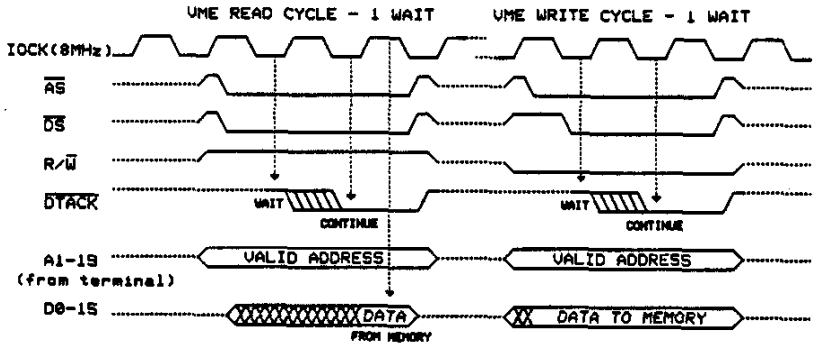


When indirect addressing is selected, the first word of a string requires two DMA cycles. A read cycle is executed to fetch the indirect address and then another read cycle to read the first data word. In this case, the terminal issues Bus Request, Bus Acknowledge is received, and then the terminal executes the two DMA cycles with a 125nS gap between before releasing Bus Request.

7.4.2 Terminal controlled (DMA) read/write cycles

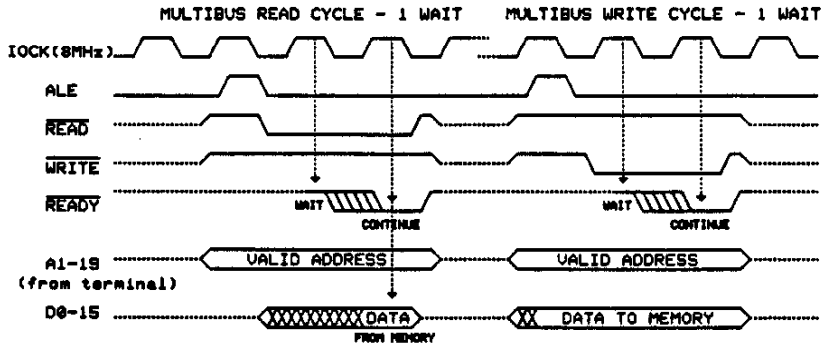
The diagrams below show waveforms and timing parameters for each of the 3 bus configurations. These cycles are executed after the terminal has gained control of the bus as described above. Timing parameters are given relative to the strobe signals for asynchronous interface design, and relative to IOCK which may be used to externally synchronise bus operations.

VMEBUS Configuration



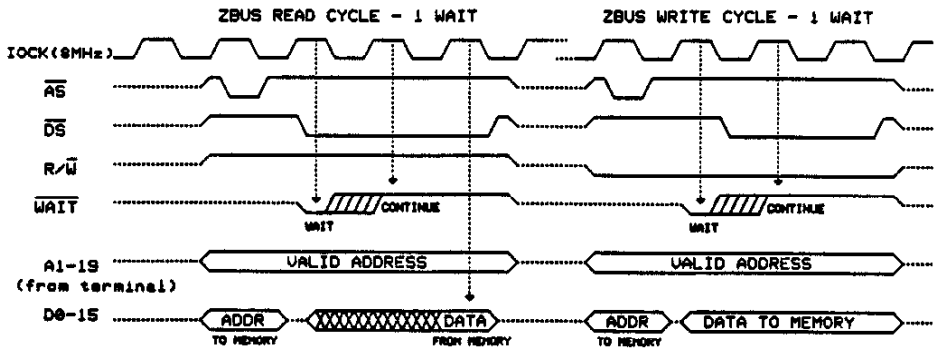
Parameter	Minimum	Maximum
NBUSA low to AS/, DS/ & RW/ driven	6.5nS	172nS
AS/, DS/ & RW/ high impedance to NBUSR high	50nS	
Address valid to AS/ low	10nS	
Address valid to DS/ low (read)	10nS	
Address valid to DS/ low (write)	70nS	
DS/ low to Data valid (read), Add 125nS per wait state		110nS
DS/ low pulse width (write), Add 125nS per wait state	115nS	
DS/ high to Data dont care (read)	0nS	
DS/ high to Address changing	5nS	
Data valid to DS/ low (write)	60nS	
DS/ high to Data changing (write)	5nS	
AS/ low to DTACK/ stable		45nS
IOCK pulse width (high)	55nS	65nS
IOCK pulse width (low)	60nS	70nS
NBUSA setup time before IOCK low	10nS	
IOCK high to AS/ low	0nS	20nS
IOCK low to AS/ high	0nS	25nS
IOCK high to DS/ low (read)	0nS	25nS
IOCK low to DS/ low (write)	0nS	25nS
IOCK low to DS/ high	0nS	25nS
DTACK/ setup time before IOCK low	10nS	
DTACK/ hold time after IOCK low	40nS	
Data setup time before IOCK high (read)	5nS	
Data hold time after IOCK high (read)	50nS	
IOCK high to Data valid (write)		10nS
IOCK high to Address valid & control sigs driven		0nS
IOCK low to busses & control sigs high impedance	15nS	45nS

MULTIBUS Configuration



Parameter	Minimum	Maximum
NBUSA low to READ/ & WRITE/ driven	6.5nS	172nS
READ/ & WRITE/ high impedance to NBUSR high	50nS	
Address valid to ALE high	10nS	
ALE high pulse width	55nS	
Address valid to DS/ low (write)	70nS	
ALE low to READ/ low	-5nS	
ALE low to WRITE/ low	25nS	
READ/ low to Data valid, Add 125nS per wait state	50nS	
WRITE/ low pulse width, Add 125nS per wait state	80nS	
READ/ high to Data dont care	0nS	
READ/ high to Address changing	5nS	
Data valid to WRITE/ low	90nS	
WRITE/ high to Data and Address changing	5nS	
ALE low to READY/ stable		40nS
IOCK pulse width (high)	55nS	65nS
IOCK pulse width (low)	60nS	70nS
NBUSA setup time before IOCK low	10nS	
IOCK high to ALE high	0nS	20nS
IOCK low to ALE low	0nS	20nS
IOCK low to READ/ low	0nS	25nS
IOCK low to WRITE/ low	30nS	50nS
IOCK low to READ/ high	0nS	25nS
IOCK low to WRITE/ high	0nS	25nS
READY/ setup time before IOCK high	15nS	
READY/ hold time after IOCK high	35nS	
Data setup time before IOCK high (read)	5nS	
Data hold time after IOCK high (read)	50nS	
IOCK high to Data valid (write)		10nS
IOCK high to Address valid & control sigs driven		0nS
IOCK low to busses & control sigs high impedance	15nS	45nS

ZBUS Configuration



NOTES ON ZBUS CYCLES:

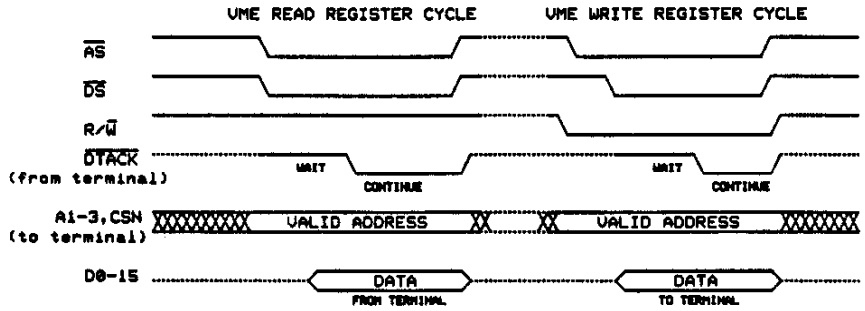
ADDRESS BITS A1-A16 ARE DRIVEN ONTO D0-15 DURING THE ADDRESS PHASE OF ZBUS CYCLES.

Parameter	Minimum	Maximum
NBUSA low to AS/, DS/ & RW/ driven	6.5nS	172nS
AS/, DS/ & RW/ high impedance to NBUSR high	50nS	
AS/ low to Multiplexed Address valid on D0-15		5nS
AS/ high to Multiplexed Address invalid on D0-15	15nS	
AS/ low pulse width	55nS	
AS/ high to DS/ low (read)	55nS	
AS/ high to DS/ low (write)	115nS	
DS/ low to Data valid (read), Add 125nS per wait state	110nS	
DS/ low pulse width (write), Add 125nS per wait state	115nS	
DS/ high to Data dont care (read)	0nS	
DS/ high to Address changing	5nS	
Data valid to DS/ low (write)	55nS	
AS/ high to WAIT/ stable		45nS
IOCK pulse width (high)	55nS	65nS
IOCK pulse width (low)	60nS	70nS
NBUSA setup time before IOCK low	10nS	
IOCK high to AS/ low	0nS	20nS
IOCK low to AS/ high	0nS	25nS
IOCK high to DS/ low (read)	0nS	25nS
IOCK low to DS/ low (write)	0nS	25nS
IOCK low to DS/ high	0nS	25nS
WAIT/ setup time before IOCK high	15nS	
WAIT/ hold time after IOCK high	35nS	
Data setup time before IOCK high (read)	5nS	
Data hold time after IOCK high (read)	50nS	
IOCK high to Data valid (write)		10nS
IOCK high to Address valid & control sigs driven		0nS
IOCK high to Multiplexed Address valid on D0-15		15nS
IOCK low to busses & control sigs high impedance	15nS	45nS

7.4.3 Sub-system controlled read/write cycles

The diagrams below show waveforms and timing parameters for sub-system controlled cycles in each of the 3 bus configurations. These cycles are used to access internal registers and the personality memory. Cycles which access personality memory differ only in that they have more wait states.

VMEBUS Configuration

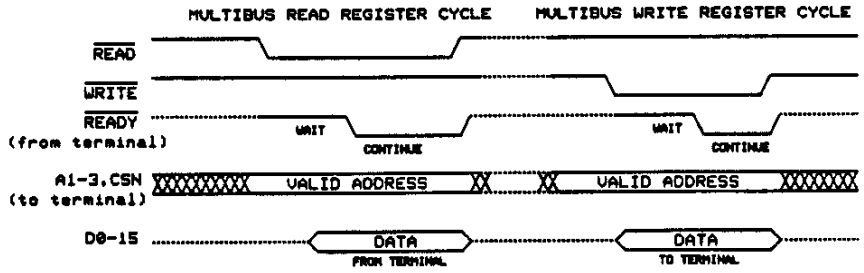


Note: DATA must be stable before DS/ goes low when loading the configuration register.

Parameter	Minimum	Maximum
A1-3, CSN & RW setup before DS/ high to low edge	20nS	
DS/ low to DTACK/ low (register access)	100nS	170nS
DS/ low to DTACK/ low (memory access)	319nS	389nS
DS/ low to D0-15 valid (register read)		55nS
DS/ low to D0-15 valid (memory read)		75nS + Taoe
DS/ low to D0-15 valid (write)		0nS
DS/ high to A1-3, CSN & RW dont care hold time	5nS	
DS/ high to D0-15 High-Z hold time (read)	0nS	25nS
DS/ high to D0-15 dont care hold time (write)	0nS	

Taoe is the personality memory Output Enable Access time.

MULTIBUS Configuration

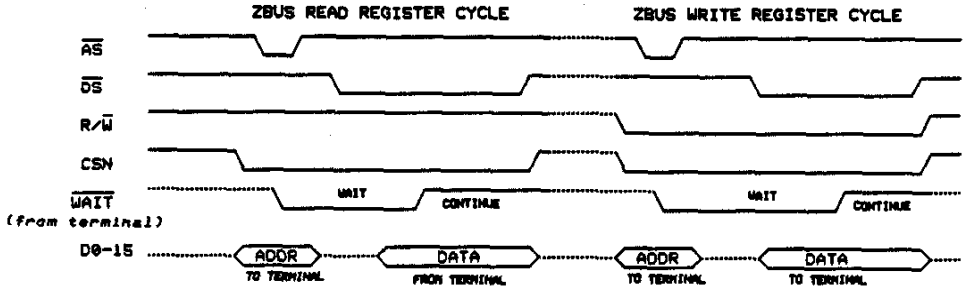


Note: DATA must be stable before WRITE/ goes low when loading the configuration register.

Parameter	Minimum	Maximum
A1-3 & CSN setup before RD/ or WR/ high to low edge	20nS	
RD/ or WR/ low to READY/ low (register access)	100nS	170nS
RD/ or WR/ low to READY/ low (memory access)	319nS	389nS
RD/ low to D0-15 valid (register read)		55nS
RD/ low to D0-15 valid (memory read)		75nS + Taoe
WR/ low to D0-15 valid (write)		0nS
RD/ or WR/ high to A1-3 & CSN dont care hold time	5nS	
RD/ high to D0-15 High-Z hold time (read)	0nS	25nS
WR/ high to D0-15 dont care hold time (write)	0nS	

Taoe is the personality memory Output Enable Access time.

ZBUS Configuration



NOTE: ADDRESS BITS A1-3 MUST BE DRIVEN ONTO D1-3 IN THE ADDRESS PHASE OF ZBUS CYCLES.

Note: DATA must be stable before DS/ goes low when loading the configuration register.

Parameter	Minimum	Maximum
Address setup time before AS/ low to high edge	12nS	
Address hold time after AS/ low to high edge	5nS	
AS/ (low going) pulse width	20nS	
CSN & RW setup before DS/ high to low edge	20nS	
CSN low to WAIT/ low		50nS
DS/ low to WAIT/ high (register access)	100nS	165nS + Tpu
DS/ low to WAIT/ high (memory access)	319nS	384nS + Tpu
DS/ low to D0-15 valid (register read)		55nS
DS/ low to D0-15 valid (memory read)		75nS + Taoe
DS/ low to D0-15 valid (write)		0nS
DS/ high to CSN & RW dont care hold time	5nS	
DS/ high to D0-15 High-Z hold time (read)	0nS	25nS
DS/ high to D0-15 dont care hold time (write)	0nS	

Tpu is the time taken for the (external)pullup resistor to pull up this signal.
Taoe is the personality memory Output Enable Access time.

7.5 Miscellaneous Signals

XICK	input	32MHz clock. Minimum pulse high or low time = 12.5nS.
PWRSTN	input	Active low power-up/system reset. This signal should be held low for at least 4.0µS to ensure complete initialisation.
CID0-CID3	input	This system channel identifier.
SSIMOD1,0	input	Sub-system interface configuration straps: 11 = VME bus mode. 10 = Multibus mode. 00 = Zbus mode.
ALTN	input	Active low input selects level 1 Alternate transmission schedule.
SYNCN	input	Active low input requests the schedule counters are to be set to Sync values for the next level 1 message. Minimum pulse width = 20nS.
INITN	input	Active low input requests the schedule counters are to be set to Initial values for the next level 1 message. Minimum pulse width = 20nS.
L2RQN	input	Active low level 2 message request input. A low going pulse of at least 20nS will log a request. The XPP cell address currently held in the L2XPPCELL register will be used to define the message.
L3RQN	input	Active low level 3 message request input. A low going pulse of at least 20nS will log a request. The XPP cell address currently held in the L3XPPCELL register will be used to define the message.

8.0 General Electrical Characteristics

All timing parameters are specified for the following conditions unless otherwise stated:

Ambient temperature range -55°C to 125°C
VDD voltage range 4.5v to 5.5v
Output load Capacitance 50pF
Falling edge measurements are made to Vol=0.8v
Rising edge measurements are made to Voh=2.0v

All inputs and outputs are TTL compatible.

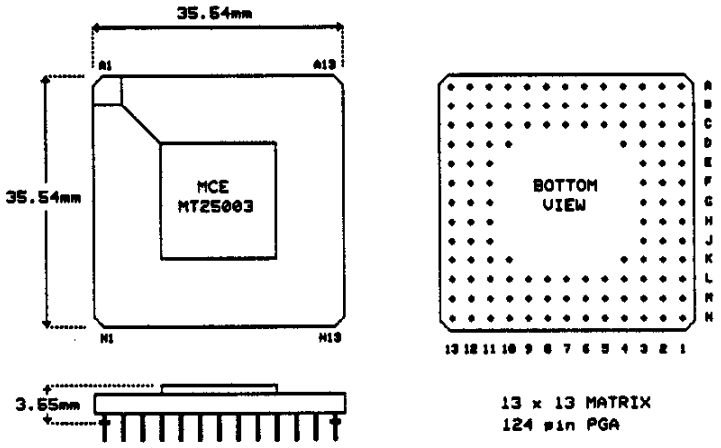
All outputs have 4mA drive except NWAIT, NBUSR, TXO, TXN & TXHB which have 8mA drive.

NWAIT & NBUSR are open drain output stages.

The following signals have internal high value (50KΩ approx.) pullup resistors:
XPPD0-XPPD7, XPPOEN, XPPCEN, XPPWEN, D0-D15, IVREN, CID0-CID3, PWRSTN, NDSO, NASO, RWO, NBUSR, NBUSAC, SSIMOD0, SSIMOD1, CSN, NWAIT, MONERRN, DELTXHB, ALTN, SYNCN, INITN, L2RQN, L3RQN.

The following signals have internal high value (50KΩ approx.) pulldown resistors:
SRTX, TXGO1, TXGO2.

8.1 Package Outline



8.2 PIN ASSIGNMENTS (124 Pin PGA Package)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	XPPCEN	C8	XX4	G11	IV5	L7	IV0
A2	XPPOEN	C9	XX3	G12	D5	L8	D1
A3	XPPWEN	C10	XX2	G13	D9	L9	VDD (+5V)
A4	XPPD0	C11	XX1			L10	IV1
A5	XPPD1	C12	XX0	H1	NBUSR	L11	VSS (0V)
A6	XPPD2	C13	XZ2	H2	NBUSAO	L12	IV2
A7	XPPD3			H3	NBUSA	L13	D13
A8	XPPD4	D1	TXHB				
A9	XPPD5	D2	TXGO1	H11	VSS (0V)	M1	A18
A10	XPPD6	D3	TXE	H12	IV4	M2	A19
A11	XPPD7	D4	not used	H13	D10	M3	L3RQN
A12	not used					M4	L2RQN
A13	XZ0	D10	not used	J1	NASO	M5	PWRSTN
		D11	VSS (0V)	J2	ALTN	M6	A1
B1	LVL1	D12	DELTXHB	J3	VDD (+5V)	M7	A2
B2	PLOADN	D13	XICK			M8	A3
B3	REQSTN			J11	VDD (+5V)	M9	A4
B4	CID1	E1	MONERRN	J12	D4	M10	A5
B5	CID0	E2	SRTX	J13	D11	M11	A6
B6	SSIMOD1	E3	TXN			M12	D2
B7	SSIMOD0			K1	INITN	M13	D14
B8	XY0	E11	VDD (+5V)	K2	XERFN		
B9	XY1	E12	IV7	K3	VSS (0V)	N1	A17
B10	XY2	E13	D7	K4	not used	N2	A16
B11	XY3					N3	A15
B12	XY4	F1	VSS (0V)	K10	not used	N4	A14
B13	XZ1	F2	TXO	K11	IV3	N5	A13
		F3	NBUSAC	K12	D3	N6	A12
C1	LVL0			K13	D12	N7	VSS (0V)
C2	TXGO2	F11	IV6			N8	A11
C3	VSS (0V)	F12	D6	L1	CSN	N9	A10
C4	CID3	F13	D8	L2	NWAIT	N10	A9
C5	VDD (+5V)			L3	SYNCN	N11	A8
C6	CID2	G1	RWO	L4	XIVSN	N12	A7
C7	VSS (0V)	G2	NDSO	L5	IVREN	N13	D15
		G3	IOCK	L6	D0		

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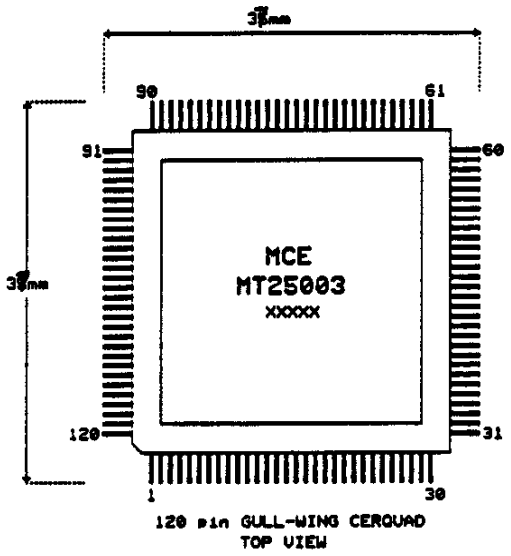
MT25003 ARINC 629 Transmitter Chip - 120 pin Gull-Wing Package Option.



Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS (0v)	31	VSS (0v)	61	VSS (0v)	91	VSS (0v)
2	XIVN	32	IV3	62	XX2	92	TXE
3	SYNCN	33	D15	63	XX1	93	XPPCEN
4	L3RQN	34	IV2	64	XY3	94	TXGO2
5	A16	35	D14	65	unused	95	LVL1
6	A15	36	D13	66	XPPD7	96	LVL0
7	L2RQN	37	D3	67	XY2	97	TXGO1
8	A14	38	D12	68	XPPD6	98	TXHB
9	PWRSTN	39	D4	69	XY1	99	SRTX
10	A13	40	D11	70	XPPD5	100	MONERRN
11	IVREN	41	VDD (+5v)	71	XX3	101	TXN
12	A1	42	IV4	72	XY0	102	TXO
13	A12	43	D10	73	XPPD4	103	VSS (0v)
14	D0	44	VSS (0v)	74	XX4	104	NBUSAC
15	VSS (0v)	45	D9	75	XPPD3	105	RWO
16	A2	46	D5	76	SSIMOD0	106	NDSO
17	IV0	47	IV5	77	VSS (0v)	107	IOCK
18	A11	48	D8	78	XPPD2	108	NBUSR
19	A3	49	D6	79	SSIMOD1	109	NBUSAO
20	D1	50	IV6	80	CID2	110	NBUSA
21	A10	51	D7	81	XPPD1	111	NASO
22	A4	52	IV7	82	CID0	112	ALTN
23	A9	53	XICK	83	XPPD0	113	INITN
24	A5	54	DELTXHB	84	CID1	114	XERFN
25	A8	55	XZ2	85	XPPWEN	115	CSN
26	A7	56	XZ1	86	XPPOEN	116	A18
27	A6	57	XX0	87	REQSTN	117	NWAIT
28	D2	58	XZ0	88	PLOADN	118	A17
29	IV1	59	XY4	89	CID3	119	A19
30	VDD (+5v)	60	VDD (+5v)	90	VDD (+5v)	120	VDD (+5v)