Micro Circuit Engineering
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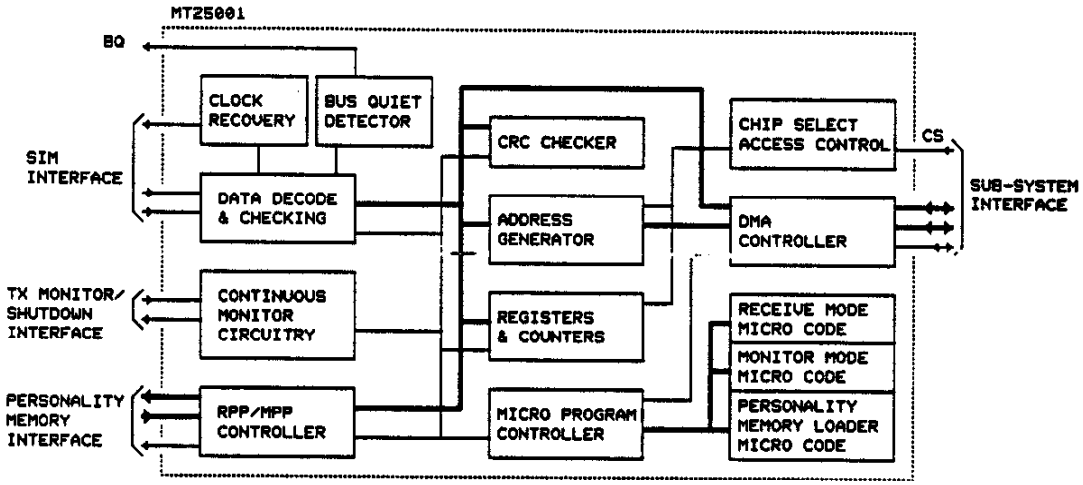
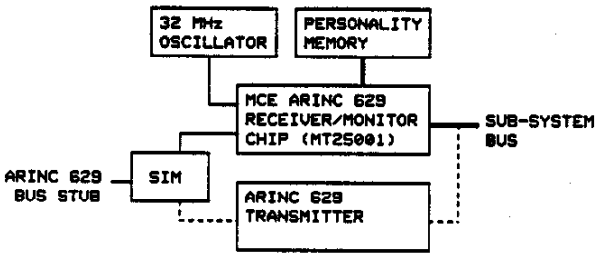
Smiths Industries Public Limited Company

MT25001 ARINC629 RECEIVER/MONITOR

DEVICE INTERNAL ORGANISATION



ARINC 629 INTERFACE ORGANISATION



FEATURES

USE ALONE FOR LOW-COST READ-ONLY TERMINAL APPLICATIONS.

COMPATIBLE WITH BP AND CP MODE DATABUS SYSTEMS.

POWERFUL SUB-SYSTEM ADDRESSING MODES FOR EFFICIENT DATA HANDLING.

124 PIN PGA PACKAGE.

USE WITH TX/PROTOCOL CHIPS FOR FULL FUNCTION TERMINAL APPLICATIONS.

TRANSMISSION MONITORING CAPABILITY EXCEEDS REQUIREMENTS OF ARINC 629 FOR HIGHER DATA INTEGRITY.

SUPPORTS PERSONALITY MEMORY PROGRAMMING VIA THE SUB-SYSTEM BUS AND THE ARINC629 DATABUS.

LOW POWER CMOS TECHNOLOGY.

1.0 GENERAL DESCRIPTION

This device can be used alone as a read-only ARINC 629 terminal or as part of a full function terminal. It implements the receive and transmission monitoring functions defined in ARINC 629 with a number of additional features. It is compatible with the standard ARINC 629 Serial Interface Module (SIM).

In receive mode, the device will:-

Decode incoming labels, rejecting any containing errors.

Determine from its personality program whether this wordstring is to be received or ignored.

For wordstrings of interest, the destination address in sub-system memory is computed from the label/extension, this terminals CID (channel identifier), and the personality program.

Datawords following the label are decoded, checked for errors and transferred to the sub-system by DMA (direct memory access).

Options include an interrupt to the sub-system at the start and/or end of the wordstring transfer, CRC (cyclic redundancy code) checking of wordstrings including label, direct/indirect address modes and automatic double buffering of data.

When used as part of a transmit/receive terminal, the device will:-

Continuously monitor the transmitter for spurious transmissions.

Detect when the transmitter is active and switch into monitor mode.

Use the personality program to check each monitored message as follows:-

The label/extension value is legal for this terminal.

Wordstring coding, parity, and sync pattern is legal.

Each wordstring contains the correct number of datawords.

The number of wordstrings in a message does not exceed the programmed limit.

When an error is detected, the device will issue a soft shutdown signal to stop the transmission.

If errors are detected in seven consecutive transmissions, the device will issue a hard shutdown signal to the transmitter.

The above monitoring actions fulfil all the requirements specified in the ARINC 629 standard. The following enhanced monitoring functions may be selected for any wordstrings:-

CRC checking of a monitored wordstring (label + datawords).

Word-by-word comparison of monitored data with expected values read from the sub-system.

Write-back monitored data to the sub-system (e.g., for local wrap-around testing).

The device has two functions to support personality memory loading and checking. Normal receive/monitoring is disabled during these operations. The sub-system processor may read and write personality memory by addressing the device as a peripheral and accessing internal registers. Personality memory may also be loaded via the ARINC 629 databus using a special command and data sequence. This sequence does not interfere with normal bus operation and provides a high degree of protection against operating with a corrupt personality program.

2.0 Receive Mode

The chip uses a receive personality program (RPP) to control the following:

Selective reception of wordstrings based on label value and label extension (source channel ID).
Selection of destination address and address mode in sub-system memory for received data.
Signalling wordstring received by interrupt & vector to the sub-system processor.
Enabling/disabling hardware CRC checking.

Full multiple personality operation (i.e., modification of sub-system address by received label extension, this system channel identifier and offset pointer) is possible using RPP alone or with an additional multiple personality program memory (MPP).

RPP bits select addressing mode for each wordstring. The sub-system address may be direct, indirect or indirect with automatic double buffering. Indirect addressing allows the sub-system processor to use multiple buffers for any wordstring. The processor switches between buffers by changing the indirect address pointer value in sub-system memory. This may be necessary to avoid the sub-system using data at the same time as the data is being updated, and consequently seeing inconsistent values. In automatic double buffering mode, the receiver/monitor device manages the buffers to ensure the sub-system always has available the latest complete good wordstring data without the need for interrupts or other processor action. When automatic double buffering is selected for a wordstring, the following actions take place. At system start-up, the sub-system must initialise a pair of indirect address pointers pointing to a pair of data buffers. The first pointer is located at the usual indirect address mode pointer address and the second pointer at the next higher word address. New data received from the databus is written to a buffer using the first pointer, whilst the sub-system reads data in the other buffer using the second pointer. When the new data has been received complete and error-free, the receiver/monitor chip exchanges the two pointers in a single indivisible operation. The sub-system can now read the new data and the other buffer is made available for the next update. If the sub-system is reading data when the pointers are swopped it can continue to use the old data up until the start of the next update. There is a restriction on the use of CRC checking with automatic double buffering (ADB) in this device. Errors in received data detected by the CRC checker will not inhibit the pointer exchange. An error status register bit and receive error strobe (RERFN) will be set to indicate this condition. All other types of receive error inhibit pointer exchange.

A strap input selects whether the chip is enabled (for receive) or disabled when the chip comes out of reset. When indirect addressing is used, the sub-system processor should initialise indirect pointers before enabling the chip to prevent wordstrings being transferred to random addresses in sub-system memory. In other cases, especially simple systems with no sub-system processor, the chip may be initialised enabled ready to receive data.

RPP bits control receive interrupt generation for each wordstring. An interrupt strobe may be generated at the start or end of wordstring reception (or both). The interrupt vector (in RPP) may be used to determine which wordstring generated the interrupt.

Errors detected whilst receiving data will cause the RERFN output to be asserted. The source of the error may be determined by reading internal registers on the chip.

3.0 Monitor Mode

The chip may be used with an MCE ARINC 629 transmitter chip, or as a monitor for any '629 terminal device. It automatically switches into monitor mode when it detects the transmitter is active. The RPP may be programmed to check for errors and terminate transmission when errors are detected. Basic checks are always performed. Additional checks may be selectively enabled for any wordstring. The MONERRN output is asserted whenever an error is detected. This may be used to interrupt the sub-system processor. The source of the error may be determined by reading internal registers. The chip can additionally accept error inputs from a transmitter chip and access protocol chip and generate a hard shutdown signal (TXE) if too many errors occur as defined in the ARINC 629 standard. In addition TXE shutdown occurs whenever the chip is disabled to prevent unmonitored transmission.

The following conditions are always checked and transmission should be terminated (by MONERRN) on any of these errors:

Transmitted wordstrings too long or message too long (babbling).
Illegal label/label extension being transmitted (impersonation). Invalid word coding/parity/sync pattern.

When basic check mode with CRC checking is enabled:

A CRC check on the wordstring (including label) is performed. A transmission error is reported if the check fails.

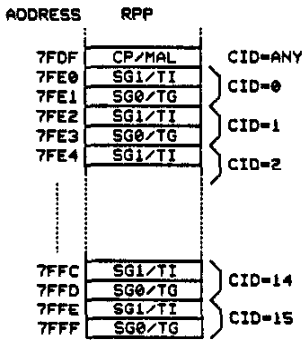
When compare check mode is enabled:
The value of each transmitted data word is compared against data read from the sub-system memory via an interface which is independent of the transmitter. Transmission is terminated if data values do not agree. The data for comparison may be read from the same memory location as the transmitted data, or from a different location or even a different sub-system.

When write-back check mode is enabled:
The value of each monitored word is written back to sub-system memory via an interface which is independent of the transmitter. The destination address is as programmed in RPP. It should be different from the location of the transmitted data and may be in a different sub-system. It is the responsibility of the sub-system processor to check this data.

Either CRC Checking, Compare, or Write-back checking may be selectively enabled for each wordstring by RPP programming. In each case the transmitted data is picked off at the bus coupler, returned through the SIM, decoded and checked in the receiver/monitor chip.

4.0 Protocol Parameter Loading

Bus access protocol timing parameters (TI, SG, TG etc) are stored in the four highest addressed RPP cells (32 bytes). When the chip comes out of reset in the enabled state or when the chip detects a monitoring error, these parameters are read. The receiver/monitor chip does not use these parameters, but their values may be strobed into an associated protocol chip using the PLOADN signal. There are 16 parameter sets stored in RPP. Only the one corresponding to the value of the chip CID (channel identifier) inputs is used. The format of these words is shown below.



Note: The CP/MAL word occupies the highest offset vector location which cannot therefore be programmed for use as an offset vector. These parameters are described more fully in the protocol chip datasheet.

5.0 Personality Memory Loading

The RPP/MPP memory may be (E)PROM, EEPROM or RAM. When writable memory is used (EEPROM or RAM), the RPP/MPP may be written via the sub-system interface (by the sub-system processor) or via the ARINC 629 databus using a special loading sequence. When the chip is held in reset, the personality memory busses and control signals are tri-stated so the memory could be accessed by external hardware during this time. Personality memory contents can also be read via the sub-system bus.

5.1 Access via the Sub-System

Before loading, the chip receive function must be disabled, and the personality memory load/read-back function enabled. This is done by writing values into the chip configuration register. Also, the first address (in RPP or MPP) to be read or written must be loaded into the chip address register. Personality memory may now be read or written one byte at a time, the address being incremented automatically after each operation. The following section on Chip Select read/write operations details addresses used to access internal registers and RPP/MPP memory. Figure 4 shows the mapping of RPP/MPP address lines onto address register bits for loading/read-back.

After loading, the personality memory load/read-back function should be disabled and then the chip receive function may be re-enabled.

5.2 Access via the ARINC 629 Databus

A specific sequence of command and data wordstrings received over the databus will switch the chip into a mode where it can load received data into its personality memory. This sequence is designed to avoid interference with normal bus traffic, and to minimise the probability of unintentional or incorrect programming of personality memory. The chip will only switch back to normal receive/monitor operation when the appropriate command sequence is received and it has received the personality memory data complete and without error. Detailed loading information is included in Appendix 1.

5.3 Disable-on-Reset Strap

The 'disable on reset' strap input controls how the chip behaves when the power-on-reset signal is removed.

First consider a system with no sub-system processor or where the processor is not permitted to write to the terminal configuration register for integrity reasons.

Tieing this strap input to 'disable' ensures the terminal will start-up in a state where it will not receive any data (or permit any transmissions) until it has received a valid set of personality memory data over the '629 databus. This prevents the chip trying to receive data before the RPP/MPP has been loaded with a valid program.

Tieing this strap input to 'enable' allows the terminal to start-up ready to receive data and monitor transmissions. It simultaneously inhibits any personality memory loading via the databus. This arrangement is appropriate for systems with fixed personality programs.

Now consider a system with a sub-system processor which is permitted to write to the terminal configuration register. The strap input will still control whether the terminal comes out of reset with its receive/monitor function enabled or disabled, but its effect can be subsequently overridden by writing to the configuration register. It is useful to set the strap input to 'disable' in systems which use indirect addressing. This will prevent the terminal receiving data and writing it to random locations in memory before the processor has initialised the address pointers. The processor can enable the terminal after software initialisation by writing to the configuration register.

6.0 Accessing Internal Registers and Personality Memory from the Sub-System

These are accessed by sub-system processor controlled read/write cycles with CSN (chip select) asserted. Address decodes are:

A19-A4	A3-A1	
XXXXXX	000	Read status register, Write Configuration Register.
XXXXXX	001	Read Interrupt Vector Register.
XXXXXX	010	Read EXT/Label Register.
XXXXXX	011	Read/Write Sub-System Address Register.
XXXXXX	1X0	Read/Write a Byte to RPP memory.
XXXXXX	1X1	Read/Write a Byte to MPP memory.

Notes: Write to Sub-System address register and Read/Write to personality memory is conditional on configuration register setting.

Definitions of internal register bit functions follow.

6.1 Configuration Register Bits

Bit 0 0 = Master Disable Receiver/Monitor function,
1 = Enable Rx/Mon when permitted by Bit 1
(Bit0 = 1 at reset).

Bit 1 1 = Enable Personality memory loading and Disable Rx/Mon function
(Bit1 = 'Disable-on-reset' strap at reset).

Bit 2 0 = Select personality memory access from sub-system,
1 = Select personality memory load via '629 Bus
(Bit2 = 1 at reset).

Bit 3 1 = Force a minimum of one wait state for sub-system DMA transfers
(Bit3 = 0 at reset).

Bit 4 1 = Permit monitored transmitter to send special command and data wordstrings under label FFC for personality memory loading
(Bit4 = 0 at reset).

Bit 5 0 = Normal chip operation,
1 = Chip Test Mode (Bit5 = 0 at reset).

Bits 6-15 Reserved.

Note: Bit 1 is also set to 1 whilst loading personality memory data via the ARINC 629 bus and reset to 0 when loading is successfully completed.

6.2 Status Register Bits

Bits 0-2 Monitor Error Counter Value 0-7, TX shutdown when count=7.
Bit 3 1 = Monitor has detected an error, reset when status read.
Bit 4 1 = Receiver has detected an error, reset when status read.
Bit 5 1 = String Active i.e., a wordstring is being received.
Bit 6 1 = The chip receive/monitor function is enabled (i.e. the device is enabled and not in personality memory programming mode).
Bits 7-15 Not defined.

Note: Monitor error status (bit 3) is set whenever the monitor error strobe (MONERRN) is asserted (low). This happens whether MONERRN is driven low from within this chip or from an external source.

6.3 Interrupt Vector Register

This is a copy of bytes 4 & 5 of the current RPP cell entry.

Bits 0-2 BADR - subsystem block address (A17-19).
Bit 3 0 = Enable automatic double buffering mode.

Bit 4 0 = Late Interrupt enable.
Bits 5-6 Monitor mode/CRC enable bits.
Bit 7 0 = Indirect sub-system address mode enable.
Bits 8-15 RIV - 8 bit interrupt vector.

6.4 EXT/Label Register

This register contains the last label extension + label received or monitored.

6.5 Sub-System Address Register

During receive (and monitor compare or writeback) this register contains the address of the last word written or about to be written (or read in compare mode). This register may be read after an error to discover whereabouts in a wordstring the error occurred. It is also used as the personality memory address register for loading/readback via the sub-system interface. The chip receive/monitor function must be disabled and personality memory loading via the sub-system must be enabled before the address register can be written from the sub-system.

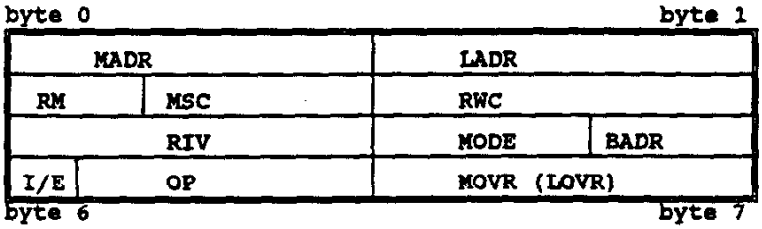
6.6 Read/Write to RPP/MPP

Any attempt to read or write personality memory is ignored until configuration register bits are set to disable the receive/monitor function and enable personality memory access. Data is accessed one byte at a time. Only the least significant 8 data lines (D0-7) are used, D8-15 are dont care on write and indeterminate on read. The personality memory address is taken from the sub-system address register and incremented after each read or write. Figure 4 defines the mapping of address register onto memory address lines.

7.0 RPP Memory Format

The receive personality program (RPP) memory contains an 8 byte cell corresponding to each of the 4096 label values. B0-B11 address the cell (these address bits take the same values as the label) and RZ0-RZ2 address a byte (0-7) within the cell. The cell contents determines the device response to each label received or monitored. This is described fully in the ARINC 629 standard.

RPP Cell Format



BADR — 3 bit sub-system block address (A19-A17). This field supplies high order sub-system address bits to extend the addressing range beyond 64K words. Wordstring addresses must not cross block boundaries.

MADR
LADR — 16 bit sub-system word address (A16-A1).

RM — 3 bit control field (DAT, VWS, RIVE).
DAT=0 indicates this wordstring contains datawords following the label.
VWS=0 indicates the first dataword contains the wordstring wordcount (i.e., variable wordstring format).
RIVE=0 specifies an interrupt should be generated at the start of receiving this wordstring (early interrupt).

MSC — 5 bit message counter used in monitor mode. The value 1F (hex) in this field indicates this wordstring must not be transmitted by this terminal. When this wordstring is the first string in a (level 1) message, this field is set to the ones complement of the maximum number of wordstrings which may be transmitted in the message. For monitored wordstrings which are not the first string in a message, this field may be set to any value except 1F.

RWC — 8 bit dataword count for the wordstring. It specifies the exact number of datawords expected (in receive or monitor mode) except when variable wordstring format is used, when it specifies the maximum permissible wordcount. RWC is the ones complement of the word count for counts from 1-255. The value FF (hex) specifies 256 datawords.

RIV — 8 bit interrupt vector.

MODE — 5 bit control field (IND, MON(2), RIVL, ADB).

IND Direct/indirect bit. This controls whether the sub-system memory address generated from ADR & OVR is the destination of the first data word in a string (direct) or contains a 16 bit pointer to the first data word (indirect). The indirect pointer and the data both share the same block address (BADR). 1=Direct, 0=Indirect.

MON This 2 bit field specifies basic monitoring (11), compare check mode (01), write-back check mode (10) or basic monitoring with CRC checking (00). Setting this field to (00) also enables CRC checking on received wordstrings.

RIVL Late interrupt enable bit (0=Enable Interrupt). When enabled, generates an interrupt at the end of receiving an error-free wordstring.

ADB Automatic Double Buffering Enable bit (0=Enable). Indirect addressing (IND=0) must be selected when ADB is enabled.

I/E — 1 bit internal/external MPP control bit. Determines whether the offset vector (OVR) is read from RPP or MPP. 1 = select MPP, 0 = select RPP.

OP — 7 bit offset pointer. This is used in forming the offset vector address as described in the ARINC 629 standard.

MOVR, LOVR — 16 bit offset value (2 bytes in consecutive cells, lower address contains most significant byte).

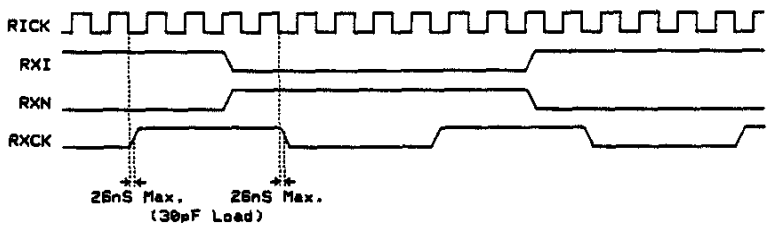
8.0 Receiver/Monitor Chip Interfaces

8.1 SIM Interface

The chip receives asynchronous complementary manchester encoded data from a SIM and returns a regenerated twice data rate clock.

Signals

RXI,RXN	inputs	Received Manchester encoded data (2M Bit/sec.).
RXCK	output	4MHz clock regenerated from data.



RXI/RXN may be asynchronous - they are sampled on the falling edge of RICK.

RXCK is phase-locked to RXI/RXN transitions by the clock recovery circuit.

The interval between consecutive transitions on RXI/RXN may vary by up to ±62.5nS without loss of data or RXCK phase lock.

8.2 Personality Memory Interface

This interface has been designed to minimise the chip pin count and provide a simple interface for most applications whilst maintaining the full flexibility of multiple personality address configurations. In most applications, a separate MPP should be unnecessary. The RPP alone provides room for 2000 offset values. The multiple personality feature supplies a 16 bit offset value to be added to the sub-system address of any wordstring. The offset value is a function of this system channel identifier (CID), the received wordstring source channel identifier (EXT - the label extension field), and an offset pointer for each label in the RPP. The MPP is a look-up table of offset values. It can contain a maximum of 32000 offset values addressed by 4 CID bits plus 4 EXT bits plus 7 offset pointer bits. When offset values are stored in the RPP, only 11 address lines are available for the look-up table which means 4 of the 15 offset address bits must be discarded. It is anticipated that 2 CID bits, 4 EXT bits and 5 offset pointer bits will be sufficient for most applications and these are internally wired to the RPP offset value table. If a different configuration is required, up to 4 of these bits may be replaced by any of the 4 discarded bits using an external multiplexer and the RDOFFS select signal supplied. All 15 offset address bits may be connected to a separate MPP when needed. Standard three line memory control signals (CE, OE and WE) are provided for RPP and MPP. Figure 1 shows connections for the standard RPP system, figure 2 shows a RPP with special offset value address configuration, and figure 3 shows a fully configured system with RPP and MPP.

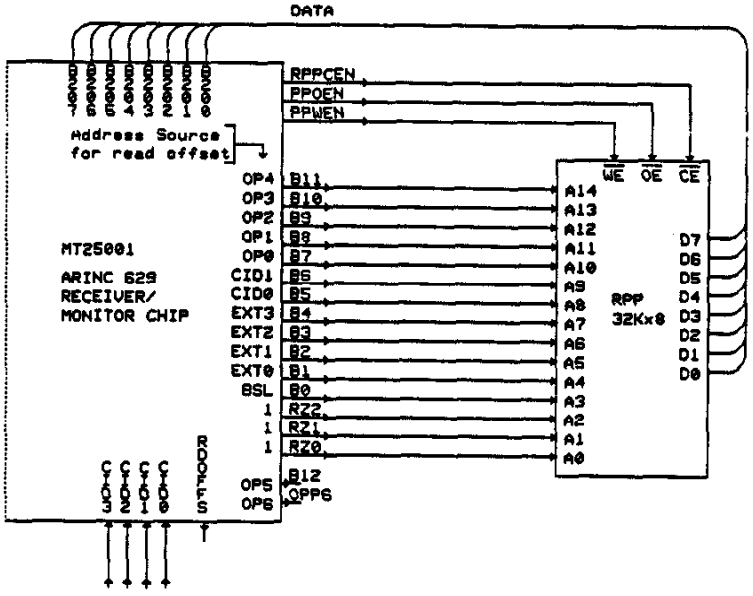


Fig 1. STANDARD RPP CONNECTIONS

ADDRESS REGISTER	RPP	MPP
BIT 15	--	OP3
BIT 14	B11	OP2
BIT 13	B10	OP1
BIT 12	B9	OP0
BIT 11	B8	CID3
BIT 10	B7	CID2
BIT 9	B6	CID1
BIT 8	B5	CID0
BIT 7	B4	EXT3
BIT 6	B3	EXT2
BIT 5	B2	EXT1
BIT 4	B1	EXT0
BIT 3	B0	Byte
BIT 2	RZ2	OP6
BIT 1	RZ1	OP5
BIT 0	RZ0	OP4

Fig 4. RPP/MPP MAPPING INTO SUB SYSTEM ADDRESS SPACE

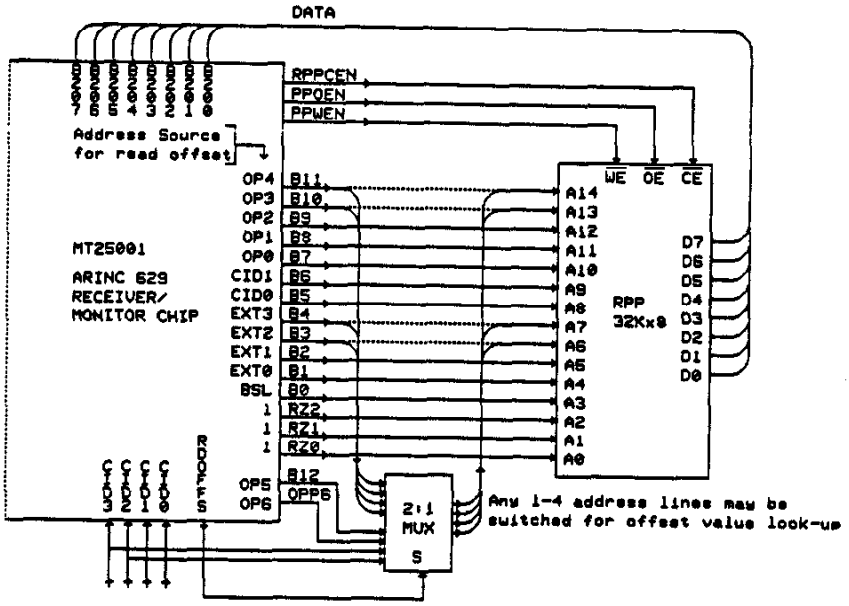


Fig 2. RPP CONNECTIONS FOR SPECIAL OFFSET VALUE ADDRESSING

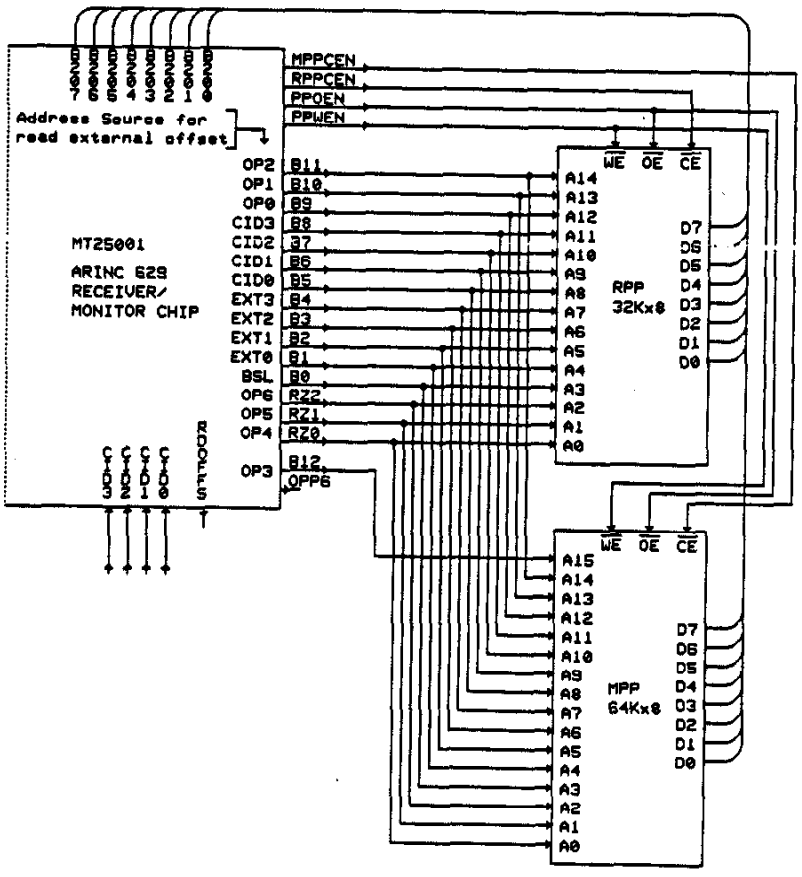
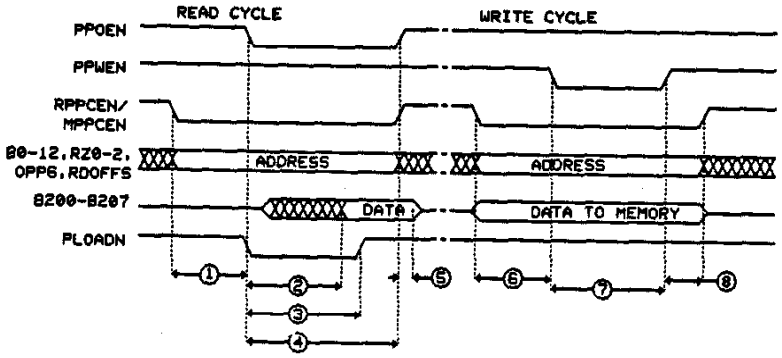


Fig 3. FULL RPP/MPP CONNECTION SCHEME

Signals

B00-B11	output	RPP cell address lines.
RZ0-RZ2	output	RPP byte address lines. (B00-B11 and RZ0-RZ2 also double as MPP address lines for external offset value look-up - see figure 3.)
B200-B207	bi-dir	RPP/MPP data lines.
RPPCEN	output	Active low RPP chip enable control signal.
MPPCEN	output	Active low MPP chip enable control signal.
PPOEN	output	Active low RPP/MPP output enable control signal.
PPWEN	output	Active low RPP/MPP write enable control signal. This pin should have an external pullup resistor or other means of preventing the memory write signal floating during reset.
RDOFFS	output	Read offset selector to control special offset address configuration multiplexer. 0 = reading RPP, 1 = reading offset.
B12,OPP6	output	Extra address bits for special offset address configuration multiplexer and MPP address (see figure 3).

The interface is designed to work with 250nS memory chips. Timing of internally generated read/write cycles is shown below. Timing of cycles initiated via the sub-system (chip select) interface imposes less severe constraints on the memory chips.



PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM
1	CE TO OE	120nS	130nS
2	OE TO DATA VALID		150nS
3	OE TO END OF PLOAD	170nS	
4	OE WIDTH	245nS	255nS
5	DATA HOLD AFTER OE	0nS	60nS
6	SETUP BEFORE WE	115nS	130nS
7	WE WIDTH	180nS	195nS
8	HOLD AFTER WE	40nS	

8.3 Monitor/Control Interface

This interface comprises signals needed to monitor a transmitter chip and control transmission shutdown.

Signals

TXHB	input	From monitored transmitter. Asserted when transmitter is not active (including between wordstrings in a message).
TXGO	input	From monitored transmitter. Active high pulse (min width 150nS) indicates start of transmission.
MONERRN	bi-dir	Active low signal. Output indicates error has been detected during transmission monitoring and transmission should be stopped. Input indicates error has been detected by another part of the terminal and the error counter will be incremented. The minimum pulse width should be greater than 500nS. This is an open drain output.
TXE	output	Active high transmit enable signal to SIM. Used for hard shutdown of transmitter after repeated errors. Also shutdown during personality memory loading.

8.4 Sub-System Interface

This interface can operate in two modes.
1) DMA mode where the bus is acquired and controlled by the terminal chip to transfer wordstrings to/from sub-system memory.
2) Processor controlled mode to read/write RPP/MPP and status registers on the chip.

A number of signals are bi-directional to support both modes.

Strap inputs SSIMOD0-1 configure bus timing and control signals for compatibility with VME, Multibus or Zbus systems. A configuration register bit may be set to force a minimum of one wait state in each DMA cycle. This allows more time for slow memory sub-systems to generate the DTACK/READY/WAIT signal.

Signals

A1-19	bi-dir	19 Active high Word address lines (8 blocks of 64k words).
D0-15	bi-dir	16 bit active high data to/from sub-system memory/processor.
NASO	bi-dir	AS/ or ALE or AS/ Control signal (VME/Multibus/Zbus mode).
NDSO	bi-dir	DS/ or READ/ or DS/ Control signal (VME/Multibus/Zbus mode).
RWO	bi-dir	R/W or WRITE/ or R/W Control signal (VME/Multibus/Zbus mode).
NWAIT	bi-dir	DTACK/ or READY/ or WAIT/ Control signal (VME/Multibus/Zbus). This is an open drain output stage.

(Note: / after a signal indicates active low)

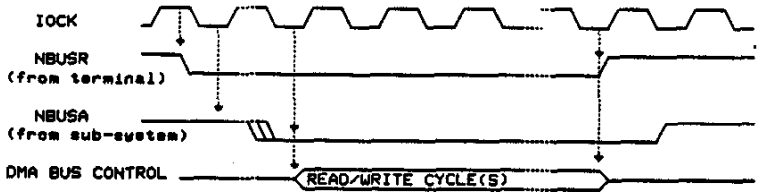
NBUSR	bi-dir	Active low bus request for DMA. This is an open drain output stage.
NBUSA	input	Active low bus acknowledge for DMA.
NBUSAO	output	Active low bus ack out for DMA request chain.
RIVSN	output	Active low received wordstring interrupt strobe. Pulse width is 500nS nominal.
IVREN	input	Active low interrupt vector enable. Enables the tri-state outputs IV0-7.
IV0-7	output	8 bit interrupt vector. Tristate outputs.
CSN	input	Active low chip select for sub-system controlled read/writes.
IOCK	output	General purpose 8MHz clock synchronised to sub-system interface DMA cycles.

8.4.1 Sub-system Bus Acquisition

The terminal device uses the same sequence of actions to gain control of the sub-system bus in each of the three bus configurations.

a) The terminal waits for NBUSR=1 and NBUSA=1.
b) The terminal pulls NBUSR low (open drain) to request the bus.
c) The terminal waits for the sub-system to relinquish control of the bus and set NBUSA=0.
d) The terminal executes one or more read/write cycles.
e) The terminal releases the bus and stops driving NBUSR low.
f) The sub-system sets NBUSA=1 and takes control of the bus.

Whenever NBUSA=0 and the terminal is not requesting the bus, NBUSAO is set low. These two signals can be used in a bus-grant daisy chain. The delay from NBUSA to NBUSAO is less than 30nS. For proper terminal operation, bus requests should be serviced within 4μS. The sequence of operation is shown graphically below.



When indirect addressing is selected, the first word of a string requires two DMA cycles. A read cycle is executed to fetch the indirect address and then a write cycle to write the first data word (or a read cycle for the first data word in compare monitor mode). In this case, the terminal issues Bus Request, Bus Acknowledge is received, and then the terminal executes the two DMA cycles ((read+write) or (read+read)) with a 125nS gap between before releasing Bus Request.

When automatic double buffering (ADB) is selected, at the end of receiving a string the buffer pointers are updated as follows. The terminal issues Bus Request, Bus Acknowledge is received, and then the terminal executes four DMA cycles (read+read+write+write) with a 125nS gap between each before releasing Bus Request. In both cases the sub-system interface design must allow this DMA sequence to complete within 4μS.

8.4.2 Terminal controlled (DMA) read/write cycles

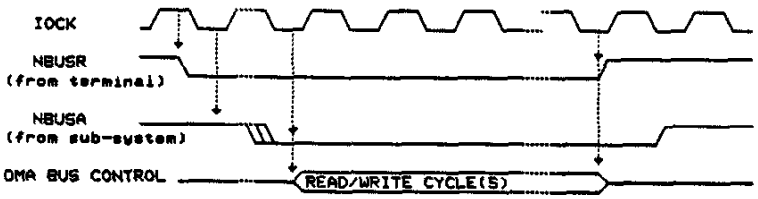
The diagrams below show waveforms and timing parameters for each of the 3 bus configurations. These cycles are executed after the terminal has gained control of the bus as described above. Timing parameters are given relative to the strobe signals for asynchronous interface design, and relative to IOCK which may be used to externally synchronise bus operations.

8.4.1 Sub-system Bus Acquisition

The terminal device uses the same sequence of actions to gain control of the sub-system bus in each of the three bus configurations.

a) The terminal waits for NBUSR=1 and NBUSA=1.
b) The terminal pulls NBUSR low (open drain) to request the bus.
c) The terminal waits for the sub-system to relinquish control of the bus and set NBUSA=0.
d) The terminal executes one or more read/write cycles.
e) The terminal releases the bus and stops driving NBUSR low.
f) The sub-system sets NBUSA=1 and takes control of the bus.

Whenever NBUSA=0 and the terminal is not requesting the bus, NBUSAO is set low. These two signals can be used in a bus-grant daisy chain. The delay from NBUSA to NBUSAO is less than 30nS. For proper terminal operation, bus requests should be serviced within 4µS. The sequence of operation is shown graphically below.



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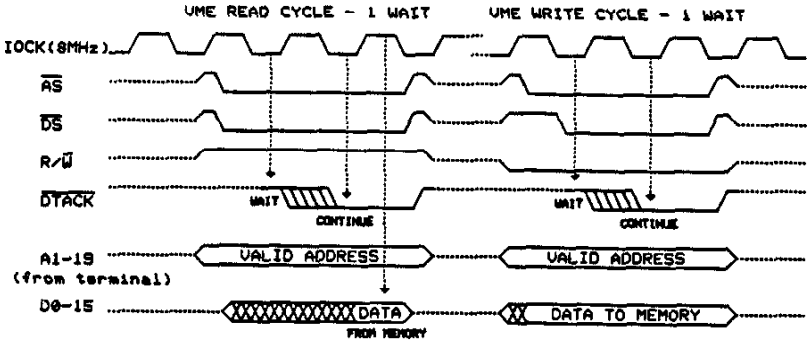
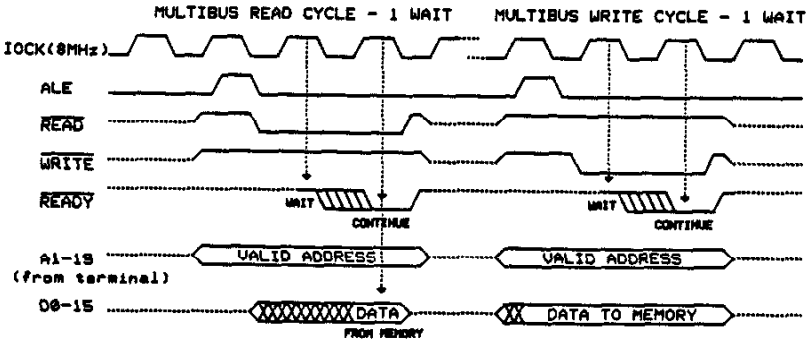
VMEBUS Configuration



Parameter	Minimum	Maximum
NBUSA low to AS/, DS/ & RW/ driven	6.5nS	172nS
AS/, DS/ & RW/ high impedance to NBUSR high	50nS	
Address valid to AS/ low	10nS	
Address valid to DS/ low (read)	10nS	
Address valid to DS/ low (write)	70nS	
DS/ low to Data valid (read), Add 125nS per wait state		110nS
DS/ low pulse width (write), Add 125nS per wait state	115nS	
DS/ high to Data dont care (read)	0nS	
DS/ high to Address changing	5nS	
Data valid to DS/ low (write)	60nS	
DS/ high to Data changing (write)	5nS	
AS/ low to DTACK/ stable		45nS
IOCK pulse width (high)	55nS	65nS
IOCK pulse width (low)	60nS	70nS
NBUSA setup time before IOCK low	10nS	
IOCK high to AS/ low	0nS	20nS
IOCK low to AS/ high	0nS	25nS
IOCK high to DS/ low (read)	0nS	25nS
IOCK low to DS/ low (write)	0nS	25nS
IOCK low to DS/ high	0nS	25nS
DTACK/ setup time before IOCK low	10nS	
DTACK/ hold time after IOCK low	40nS	
Data setup time before IOCK high (read)	5nS	
Data hold time after IOCK high (read)	50nS	
IOCK high to Data valid (write)		10nS
IOCK high to Address valid & control sigs driven		0nS
IOCK low to busses & control sigs high impedance	15nS	45nS

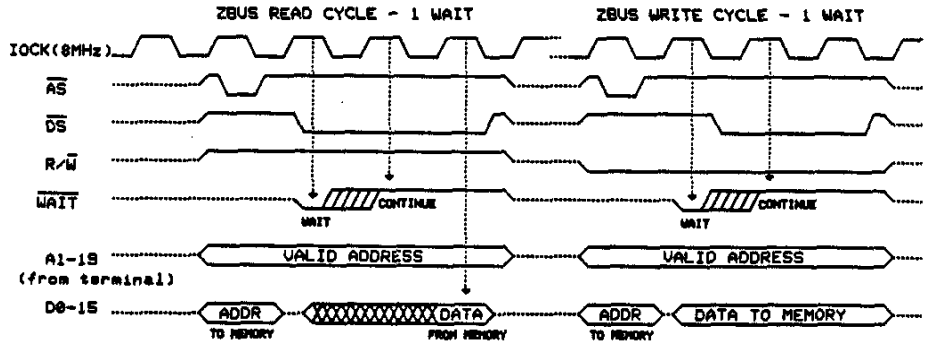
MULTIBUS Configuration



Parameter	Minimum	Maximum
NBUSA low to READ/ & WRITE/ driven	6.5nS	172nS
READ/ & WRITE/ high impedance to NBUSR high	50nS	
Address valid to ALE high	10nS	
ALE high pulse width	55nS	
Address valid to DS/ low (write)	70nS	
ALE low to READ/ low	-5nS	
ALE low to WRITE/ low	25nS	
READ/ low to Data valid, Add 125nS per wait state	50nS	
WRITE/ low pulse width, Add 125nS per wait state	80nS	
READ/ high to Data dont care	0nS	
READ/ high to Address changing	5nS	
Data valid to WRITE/ low	90nS	
WRITE/ high to Data and Address changing	5nS	
ALE low to READY/ stable		40nS
IOCK pulse width (high)	55nS	65nS
IOCK pulse width (low)	60nS	70nS
NBUSA setup time before IOCK low	10nS	
IOCK high to ALE high	0nS	20nS
IOCK low to ALE low	0nS	20nS
IOCK low to READ/ low	0nS	25nS
IOCK low to WRITE/ low	30nS	50nS
IOCK low to READ/ high	0nS	25nS
IOCK low to WRITE/ high	0nS	25nS
READY/ setup time before IOCK high	15nS	
READY/ hold time after IOCK high	35nS	
Data setup time before IOCK high (read)	5nS	
Data hold time after IOCK high (read)	50nS	
IOCK high to Data valid (write)		10nS
IOCK high to Address valid & control sigs driven		0nS
IOCK low to busses & control sigs high impedance	15nS	45nS

ZBUS Configuration

Note there is a limitation on using Automatic Double Buffering address mode with ZBUS configuration in that the multiplexed address is not available on D0-15 in some cycles. The separate address bus A1-19 may be used instead.



NOTES ON ZBUS CYCLES:

ADDRESS BITS A1-A16 ARE DRIVEN ONTO D0-15 DURING THE ADDRESS PHASE OF ZBUS CYCLES.

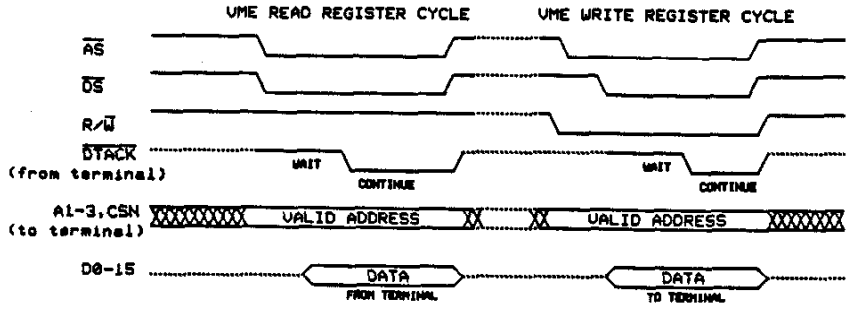
ADDRESS BITS ARE NOT OUTPUT ON D0-15 DURING SOME AUTOMATIC DOUBLE BUFFERING ADDRESS MODE CYCLES. THE ADDRESS ON A1-19 SHOULD BE USED INSTEAD.

Parameter	Minimum	Maximum
NBUSA low to AS/, DS/ & RW/ driven	6.5nS	172nS
AS/, DS/ & RW/ high impedance to NBUSR high	50nS	
AS/ low to Multiplexed Address valid on D0-15		5nS
AS/ high to Multiplexed Address invalid on D0-15	15nS	
AS/ low pulse width	55nS	
AS/ high to DS/ low (read)	55nS	
AS/ high to DS/ low (write)	115nS	
DS/ low to Data valid (read), Add 125nS per wait state	110nS	
DS/ low pulse width (write), Add 125nS per wait state	115nS	
DS/ high to Data dont care (read)	0nS	
DS/ high to Address changing	5nS	
Data valid to DS/ low (write)	55nS	
AS/ high to WAIT/ stable		45nS
IOCK pulse width (high)	55nS	65nS
IOCK pulse width (low)	60nS	70nS
NBUSA setup time before IOCK low	10nS	
IOCK high to AS/ low	0nS	20nS
IOCK low to AS/ high	0nS	25nS
IOCK high to DS/ low (read)	0nS	25nS
IOCK low to DS/ low (write)	0nS	25nS
IOCK low to DS/ high	0nS	25nS
WAIT/ setup time before IOCK high	15nS	
WAIT/ hold time after IOCK high	35nS	
Data setup time before IOCK high (read)	5nS	
Data hold time after IOCK high (read)	50nS	
IOCK high to Data valid (write)		10nS
IOCK high to Address valid & control sigs driven		0nS
IOCK high to Multiplexed Address valid on D0-15		15nS
IOCK low to busses & control sigs high impedance	15nS	45nS

8.4.3 Sub-system controlled read/write cycles

The diagrams below show waveforms and timing parameters for sub-system controlled cycles in each of the 3 bus configurations. These cycles are used to access internal registers and the personality memory. Cycles which access personality memory differ only in that they have more wait states.

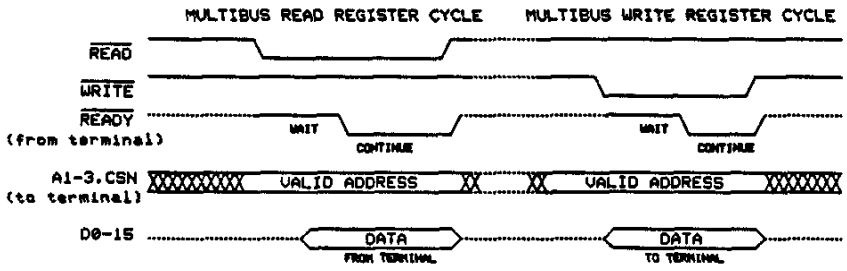
VMEBUS Configuration



Parameter	Minimum	Maximum
A1-3, CSN & RW setup before DS/ high to low edge	20nS	
DS/ low to DTACK/ low (register access)	100nS	170nS
DS/ low to DTACK/ low (memory access)	319nS	389nS
DS/ low to D0-15 valid (register read)		55nS
DS/ low to D0-15 valid (memory read).		75nS + Taoe
DS/ low to D0-15 valid (write)		0nS
DS/ high to A1-3, CSN & RW dont care hold time	5nS	
DS/ high to D0-15 High-Z hold time (read)	0nS	25nS
DS/ high to D0-15 dont care hold time (write)	0nS	

Taoe is the personality memory Output Enable Access time.

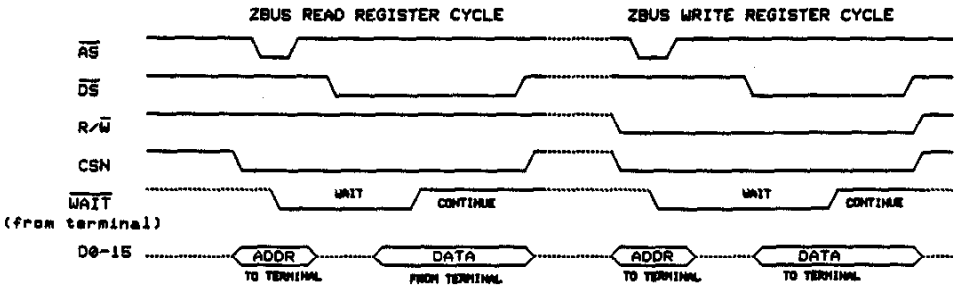
MULTIBUS Configuration



Parameter	Minimum	Maximum
A1-3 & CSN setup before RD/ or WR/ high to low edge	20nS	
RD/ or WR/ low to READY/ low (register access)	100nS	170nS
RD/ or WR/ low to READY/ low (memory access)	319nS	389nS
RD/ low to D0-15 valid (register read)		55nS
RD/ low to D0-15 valid (memory read)		75nS + Taoe
WR/ low to D0-15 valid (write)		0nS
RD/ or WR/ high to A1-3 & CSN dont care hold time	5nS	
RD/ high to D0-15 High-Z hold time (read)	0nS	25nS
WR/ high to D0-15 dont care hold time (write)	0nS	

Taoe is the personality memory Output Enable Access time.

ZBUS Configuration



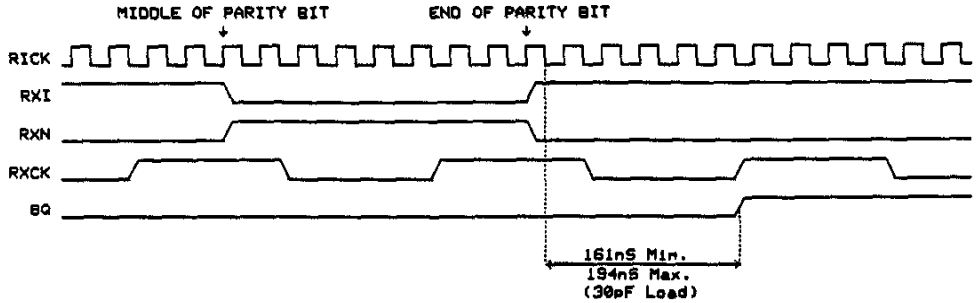
NOTE: ADDRESS BITS A1-3 MUST BE DRIVEN ONTO D1-3 IN THE ADDRESS PHASE OF ZBUS CYCLES.

Parameter	Minimum	Maximum
Address setup time before AS/ low to high edge	12nS	
Address hold time after AS/ low to high edge	5nS	
AS/ (low going) pulse width	20nS	
CSN & RW setup before DS/ high to low edge	20nS	
CSN low to WAIT/ low		50nS
DS/ low to WAIT/ high (register access)	100nS	165nS + Tpu
DS/ low to WAIT/ high (memory access)	319nS	384nS + Tpu
DS/ low to D0-15 valid (register read)		55nS
DS/ low to D0-15 valid (memory read)		75nS + Taoe
DS/ low to D0-15 valid (write)		0nS
DS/ high to CSN & RW dont care hold time	5nS	
DS/ high to D0-15 High-Z hold time (read)	0nS	25nS
DS/ high to D0-15 dont care hold time (write)	0nS	

Tpu is the time taken for the (external)pullup resistor to pull up this signal.
Taoe is the personality memory Output Enable Access time.

8.5 Miscellaneous Signals

RICK	input	32MHz clock. Minimum pulse high or low time = 12.5nS.
PWRSTN	input	Active low power-up/system reset. This signal should be held low for at least 2.5μS to ensure complete initialisation.
CID0-CID3	input	This system channel identifier.
RERFN	output	Active low receive error detected strobe. Pulse width is 500nS nominal.
BQ	output	Bus Quiet detected output (to protocol chip). BQ=0 within 20nS (30pF load) of RXI≠RXN. BQ=1 within 15nS of the next rising edge of RXCK after RXI=RXN. BQ=1 for a two bit period at the end of each word received regardless of the state of RXI and RXN (the diagram below shows the timing of BQ detection at the end of a word).



ADN	output	Active low signal indicates access protocol parameter data is available on RPP data lines (to protocol chip). See personality memory timing diagram for waveform detail.
X	output	Serial link to transmitter chip for XPP loading.
DENN	output	Active low strobe to enable the Terminal Identifier number onto the B200-B207 bus. (The Terminal Identifier number is needed when loading personality data over the ARINC 629 bus. B207-B201 is the 7 bit TID value. B200 is TID parity giving the eight bit field odd parity). TIDENN is a nominally 250nS wide pulse and TID data must be stable on the B200-B207 bus from 30nS before until 0nS after the end of this pulse.
ONRST	input	Strap input to control receive/monitor function on start-up. 0 = Start with receive/monitor function enabled. 1 = Start with receive/monitor function disabled and waiting for enable from sub-system or personality memory load from the ARINC 629 databus.
EHEN	input	Strap input. 0 = Enable 'Word Ends High Error' checking in decoder.
SIMOD1,0	input	Sub-system interface configuration straps: 11 = VME bus mode. 10 = Multibus mode. 00 = Zbus mode.

.0 General Electrical Characteristics

ll timing parameters are specified for the following conditions unless therwise stated:

Ambient temperature range -55°C to 125°C
VDD voltage range 4.5v to 5.5v
Output load Capacitance 50pF
Falling edge measurements are made to Vol=0.8v
Rising edge measurements are made to Voh=2.0v

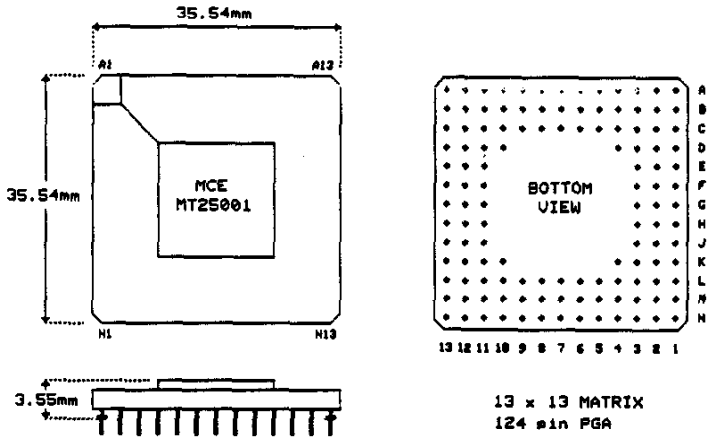
.ll outputs have 4mA drive except NWAIT, NBUSR, RXCK & BQ which have 8mA drive.

ONERRN, NWAIT & NBUSR are open drain output stages.

he following signals have internal high value (50KΩ approx.) pullup resistors:
B200-B207, D0-D15, IVREN, CID0-CID3, WDEHEN, PWRSTN, NDSO, NASO, RWO, NBUSR, SSIMOD0, SSIMOD1, CSN, NWAIT, MONERRN, ENONRST.

he following signals have internal high value (50KΩ approx.) pulldown resistors:
TXHB, TXGO.

9.1 Package Outline



13 x 13 MATRIX
124 pin PGA

9.2 PIN ASSIGNMENTS (124 Pin PGA Package)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	RZ0	C8	B3	G11	IOCK	L7	D1
A2	RDOFFS	C9	B4	G12	NDSO	L8	D0
A3	B207	C10	B5	G13	RWO	L9	VDD (+5V)
A4	B206	C11	B6			L10	CID0
A5	B205	C12	MPPCEN	H1	D10	L11	VSS (0V)
A6	B204	C13	TXE	H2	D9	L12	NWAIT
A7	B203			H3	VSS (0V)	L13	CSN
A8	B202	D1	RICK				
A9	B201	D2	SSIMOD1	H11	VSS (0V)	M1	D14
A10	B200	D3	NBUSA	H12	NBUSAO	M2	D5
A11	PLOADN	D4	not used	H13	NBUSR	M3	A6
A12	BQ					M4	A5
A13	PPOEN	D10	not used	J1	D11	M5	A4
		D11	VSS (0V)	J2	D8	M6	A3
B1	RZ1	D12	TXGO	J3	VDD (+5V)	M7	A2
B2	OPP6	D13	TXHB			M8	A1
B3	B12			J11	ENONRST	M9	PWRSTN
B4	B11	E1	IV5	J12	WDEHEN	M10	CID1
B5	VSS (0V)	E2	IV4	J13	NASO	M11	CID2
B6	B10	E3	IVREN			M12	CID3
B7	VDD (+5V)			K1	D12	M13	A19
B8	VSS (0V)	E11	VDD (+5V)	K2	D7		
B9	B9	E12	SRTX	K3	VSS (0V)	N1	D15
B10	B8	E13	MONERRN	K4	not used	N2	A7
B11	B7					N3	A8
B12	PPWEN	F1	IV6	K10	not used	N4	A9
B13	RPPCEN	F2	IV3	K11	RERFN	N5	A10
		F3	IV0	K12	RIVSN	N6	A11
C1	RZ2			K13	TIDENN	N7	A12
C2	SSIMOD0	F11	RXIIN			N8	A13
C3	VSS (0V)	F12	RXNIN	L1	D13	N9	A14
C4	B0	F13	RXCK	L2	D6	N10	A15
C5	VDD (+5V)			L3	D4	N11	A16
C6	B1	G1	IV7	L4	D3	N12	A17
C7	B2	G2	IV2	L5	VSS (0V)	N13	A18
		G3	IV1	L6	D2		

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Registered in England 1047586

Appendix 1

Loading ARINC 629 Terminal Personality Data from the Databus.

There are applications where it would be advantageous to load transmission schedules, receiver message details and bus parameters into ARINC 629 terminals via the '629 databus. This would allow customisation of units, either at installation where the data would be loaded once into non-volatile memory, or at system initialisation when volatile memory could be used. Since this is a bus-wide process, consideration must be given to compatibility and impact on bus integrity.

Objectives.

These notes will make reference to a master '629 terminal which will control the loading process and supply programme data to a number of slave terminals on a '629 bus. Other configurations are possible, for instance there could be more than one master terminal, or the master terminal could be removed from the bus after initialisation.

1) The loading procedure should provide a high confidence that programming data has been transferred correctly from the master terminal to the right slave terminals.

2) The procedure should provide good protection against abnormal transmissions from a faulty terminal on the bus corrupting program data in another terminal.

3) The procedure should support programming of all the terminal characteristics which could be affected by updates to equipment attached to the bus and software associated with that equipment. The following characteristics should be included:-

   RPP data for each message to be received including labels, string lengths and sub-system destination addresses.

   RPP data for each transmitted message to be monitored including label, maximum string length and maximum number of strings in the message.

   XPP data for each message to be transmitted including label, string length, data source address in sub-system, and scheduling information for sequencing of strings in the message.

   PROTOCOL timing parameters (TI, TG, SG etc.) if these are stored in electrically programmable form.

4) The procedure should be applicable to simple terminals which have no processor in their sub-system or in which the processor is not trusted to handle bus programming data.

5) The procedure should be applicable to read-only terminals which do not have the capability to transmit on the bus.

6) The procedure should be applicable to complex terminals containing sub-system processors which may need to participate in the loading process, e.g., to modify sub-system address or interrupt vector values, or to engage in a dialogue with the master terminal to establish configuration and revision status of equipment.

MCE Loading Scheme

The scheme implemented in the MCE ARINC 629 chipset has these features:-

1) It can completely program simple terminals.

2) It can completely program read-only terminals.

3) It can be used to 'boot-strap' more complex terminals after which the loading process would be completed with the help of software in the sub-system processor.

The programming procedure is very simple:-

1) The master terminal sends a command wordstring directed to a specific slave terminal which disables the slave terminal's normal transmit/receive function and enables its program loading function.

2) The master terminal sends a number of data wordstrings containing programme data for the specific slave terminal.

3) The master terminal sends a command wordstring to the specific slave terminal which disables its program loading function and re-enables its normal transmit/receive function. If any errors were detected whilst receiving program data, the slave remains disabled.

4) The master terminal observes the slave begin normal operation which indicates programming was successful. If this is not the case, the procedure is repeated from step one (and abandoned after a number of re-trys).

The master terminal can determine if programming was successful by observing whether the slave terminal begins transmission after being re-enabled at the end of programming. For read-only terminals, the master terminal must be able to observe some other aspect of the system function which is present when the slave terminal is enabled for normal operation.

A scheme which does not require the slave to transmit was chosen initially for its ability to support read-only terminals. More importantly however is the fact that if a slave terminal is permitted to transmit whilst its normal protocol timing and monitoring functions are disabled or being updated, the bus integrity would be degraded.

A number of features are included to protect against unintentional reprogramming by a faulty terminal and to ensure programming data has been transferred accurately and completely to the correct slave terminal.

1) Each command and data wordstring is sent under the label value FFC (Hex). This label is one which is usually rejected by the terminal receiver and forbidden to the transmitter by the monitor function because the associated RPP area is used to store protocol parameters. This label can be transmitted by the master terminal only with each transmission individually authorized by its sub-system processor.

2) Each slave terminal on the bus is assigned a unique Terminal Identification Number which is 'pin-programmed' and not alterable over the bus. The programming pins include a parity bit to protect against single failures. Each command and data wordstring contains a terminal identification field which must match the value in the slave terminal before it will respond.

3) Each command and data wordstring ends with a CRC check word being the ones complement of the normal CRC checkword as defined in the ARINC 629 standard. This difference further distinguishes a loading wordstring from a normal message. Any command wordstring with invalid CRC word is ignored. Any data wordstring with invalid CRC word sets the programming error flag and prevents the terminal from being re-enabled at the end of programming. The programming error flag is cleared each time the 'enable programming mode' command is received to allow re-trys after a programming failure. A terminal will not respond to a second enable programming command before a disable programming command has been received.

4) A slave terminal will only respond to programming data after is has been enabled for programming by the appropriate command.

5) During programming, the slave terminal maintains a (modulo 32) count of the number of command and data wordstrings it has received. The command to re-enable the slave terminal includes a count field which allows it to check the correct number of wordstrings have been received.

Compatibility.

A few functions need to be standardised to ensure terminals from different suppliers can be used on the same bus.

The only requirement on terminals which do not support programming over the bus is that they must ignore wordstrings received with the label FFC and never transmit wordstrings with label FFC. This is a standard requirement of all ARINC 629 terminals.

Terminals which support programming over the bus should use a consistent format for enable/disable command wordstrings. Data wordstrings (containing program data to be transferred) and other commands should use the same label, terminal identifier, command/data discriminant and CRC fields, but the remainder of the string is not constrained. This is sufficient to ensure programming instructions to one terminal will not affect other terminals.

The adopted Command wordstring format is:-

where:-

cid	Channel Identifier of master terminal, not used.
FFC	Fixed Label value for programming wordstrings.
tid	7 bit Terminal Identifier, uniquely identifies slave.
0	1 bit field, zero indicates this is a command string.
CRC word	16 bit CRC check word, 1's complement of 'normal' CRC word formed from preceding word and label.
com	8 bit field defining the command as follows:-

Enter Programming Mode: 

where Devcode is a 5 bit device type field (see notes below).

Exit Programming Mode: 

where Scount is a 5 bit field containing the (modulo 32) programming wordstring count (see notes below).

Other com field values may be used for device specific commands.

Notes

The Devcode field is provided so that terminals from different suppliers which require different program data formats in their programming wordstrings may be distinguished. A terminal will only enable itself for programming when it receives a compatible Devcode value. This allows a master terminal to program slave terminals without prior knowledge of the terminal type installed in a particular unit (the master would send each programme format in turn until the slave responded).

The Scount field is a modulo 32 count of the number of programming wordstrings directed to the slave terminal starting with the first wordstring after the Enter programming mode command up to and including the Exit programming mode command.

The adopted Data wordstring format is:-

where:-

cid	Channel Identifier of master terminal, not used.
FFC	Fixed Label value for programming wordstrings.
tid	7 bit Terminal Identifier, uniquely identifies slave.
1	1 bit field, one indicates this is a data string.
vwc	8 bit Word Count field, number of words after label.
datawords	A variable number of words containing data to be transferred to the slave terminal. Format and content may be specific to each terminal device type.
CRC word	16 bit CRC check word, 1's complement of 'normal' CRC word formed from all preceding words including label.

Implementation.

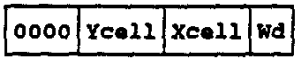
This section describes the device specific programming data used by MCE chips.

1) MCE devices only respond to Enable Programming commands with Devcode value = 01.

2) A Clear Memory command is implemented. A command string with com = 011xxxxx causes the terminal to set all locations in XPP, RPP and MPP to 'all ones', i.e., the unprogrammed state.

3) All programmable characteristics of the MCE chips are stored in RPP, MPP & XPP memory. The variable part of the data wordstring consists of an address word followed by a variable number of data words making the string length up to VWC. The first data word is stored in the byte defined by the address word and the succeeding byte. Following data words are stored in successive bytes. The wordstring length may be up to 255 words plus label (252 program data words). The address word is formatted as follows.

XPP



where:
Ycell is a 5 bit XPP Y cell address.
Xcell is a 5 bit XPP X cell address.
Wd is a 2 bit word address within the cell.

RPP

where:
Rcell is a 12 bit cell address corresponding to one of 4096 label values.
Wd is a 2 bit word address within the cell.

MPP

where:
Maddress is a 15 bit word address within MPP. The first location programmed corresponds to the location loaded via the sub-system bus with the address register bits 1-15 set to Maddress and bit 0 set to zero.

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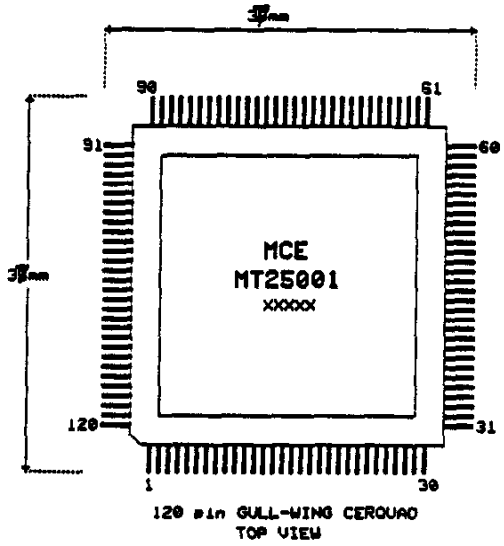
MT25001 ARINC 629 Receiver/Monitor Chip - 120 pin Gull-Wing Package Option.



Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS (0v)	31	VSS (0v)	61	VSS (0v)	91	VSS (0v)
2	D3	32	RERFN	62	B5	92	NBUSA
3	D4	33	A18	63	B6	93	RZ0
4	A6	34	NWAIT	64	B7	94	SSIMOD0
5	A7	35	A19	65	BQ	95	RZ1
6	A8	36	CSN	66	PLOADN	96	RZ2
7	A5	37	RIVSN	67	B8	97	SSIMOD1
8	A9	38	TIDENN	68	B200	98	RICK
9	A4	39	WDEHEN	69	B9	99	IV4
10	A10	40	NASO	70	B201	100	IV5
11	VSS (0v)	41	ENONRST	71	B4	101	IVREN
12	A3	42	NBUSAO	72	VSS (0v)	102	IV3
13	A11	43	NBUSR	73	B202	103	IV6
14	D2	44	VSS (0v)	74	B3	104	IV0
15	A12	45	RWO	75	B203	105	IV7
16	A2	46	NDSO	76	VDD (+5v)	106	IV2
17	D1	47	IOCK	77	B2	107	IV1
18	A13	48	RXCK	78	B204	108	D10
19	A1	49	RXNIN	79	B10	109	D9
20	D0	50	RXIIN	80	B1	110	VSS (0v)
21	A14	51	MONERRN	81	B205	111	D11
22	PWRSTN	52	SRTX	82	VSS (0v)	112	D8
23	A15	53	TXHB	83	B206	113	D12
24	CID1	54	TXGO	84	B11	114	D7
25	A16	55	TXE	85	B207	115	D13
26	A17	56	RPPCEN	86	RDOFFS	116	D14
27	CID2	57	MPPCEN	87	B12	117	D6
28	CID3	58	PPOEN	88	OPP6	118	D15
29	CID0	59	PPWEN	89	B0	119	D5
30	VDD (+5v)	60	VDD (+5v)	90	VDD (+5v)	120	VDD (+5v)