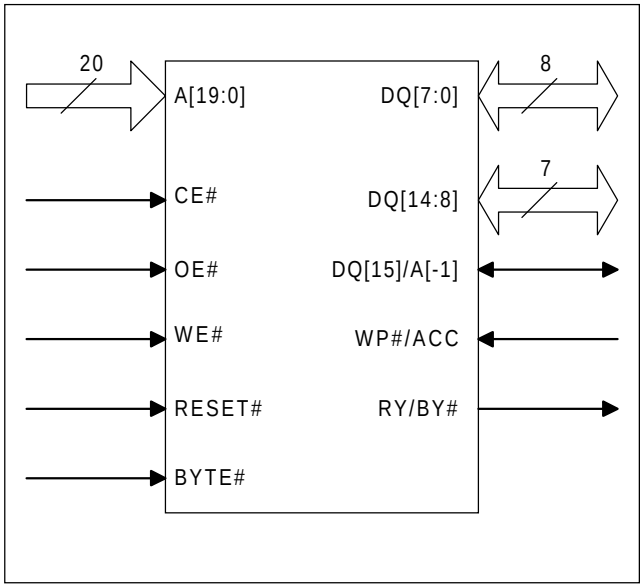
HY29DL162/HY29DL163

16 Megabit (2M x 8/1M x16) Low Voltage, Dual Bank, Simultaneous Read/Write Flash Memory

KEY FEATURES

- **Single Power Supply Operation**
  - Read, program, and erase operations from 2.7 to 3.6 V
  - Ideal for battery-powered applications
- **Simultaneous Read/Write Operations**
  - Host system can program or erase in one bank while simultaneously reading from any sector in the other bank with zero latency between read and write operations
- **High Performance**
  - 70 and 80 ns access time versions with 30pF load
  - 90 and 120 ns access time versions with 100pF load
- **Ultra Low Power Consumption (Typical Values)**
  - Automatic sleep mode current: 200 nA
  - Standby mode current: 200 nA
  - Read current: 10 mA (at 5 MHz)
  - Program/erase current: 15 mA
- **Boot-Block Sector Architecture with 39 Sectors in Two Banks for Fast In-System Code Changes**
- **Secured Sector: An Extra 64 Kbyte Sector that Can Be:**
  - Factory locked and identifiable: 16 bytes available for a secure, random factory-programmed Electronic Serial Number
  - Customer lockable: Can be read, programmed, or erased just like other sectors
- **Flexible Sector Architecture**
  - Sector Protection allows locking of a sector or sectors to prevent program or erase operations within that sector
  - Temporary Sector Unprotect allows changes in locked sectors (requires high voltage on RESET# pin)
- **Automatic Erase Algorithm Erases Any Combination of Sectors or the Entire Chip**
- **Automatic Program Algorithm Writes and Verifies Data at Specified Addresses**
- **Compliant with Common Flash Memory Interface (CFI) Specification**
- **Minimum 100,000 Write Cycles per Sector (1,000,000 cycles Typical)**
- **Compatible with JEDEC Standards**
  - Pinout and software compatible with single-power supply Flash devices
  - Superior inadvertent write protection
- **Data# Polling and Toggle Bits**
  - Provide software confirmation of completion of program or erase operations
- **Ready/Busy# Pin**
  - Provides hardware confirmation of completion of program or erase operations
- **Erase Suspend**
  - Suspends an erase operation to allow programming data to or reading data from a sector in the same bank
  - Erase Resume can then be invoked to complete the suspended erasure
- **Hardware Reset Pin (RESET#) Resets the Device to Reading Array Data**
- **WP#/ACC Input Pin**
  - Write protect (WP#) function allows hardware protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function provides accelerated program times
- **Fast Program and Erase Times**
  - Sector erase time: 0.5 sec typical
  - Byte/Word program time utilizing Acceleration function: 10 µs typical
- **Space Efficient Packaging**
  - 48-pin TSOP and 48-ball FBGA packages

LOGIC DIAGRAM



GENERAL DESCRIPTION

The HY29DL162/HY29DL163 (HY29DL16x) is a 16 Mbit, 3 volt-only CMOS Flash memory organized as 2,097,152 (2M) bytes or 1,048,576 (1M) words. The device is available in 48-pin TSOP and 48-ball FBGA packages. Word-wide data (x16) appears on DQ[15:0] and byte-wide (x8) data appears on DQ[7:0].

The HY29DL16x Flash memory array is organized into 39 sectors in two banks. Bank 1 contains eight 8 Kbyte boot/parameter sectors and 3 or 7 larger sectors of 64 Kbytes each, depending on the version of the device. Bank 2 contains the rest of the memory array, organized as 28 or 24 sectors of 64 Kbytes:

	Bank 1	Bank 2
HY29DL162	8 x 8KB/4KW 3 x 64KB/32KW	28 x 64KB/32KW
HY29DL163	8 x 8KB/4KW 7 x 64KB/32KW	24 x 64KB/32KW

The device features simultaneous read/write operation which allows the host system to invoke a program or erase operation in one bank and immediately and simultaneously read data from the other bank, except if that bank has any sectors marked for erasure, with zero latency. This releases the system from waiting for the completion of program or erase operations, thus improving overall system performance.

The HY29DL16x can be programmed and erased in-system with a single 2.7 - 3.6 volt V_{CC} supply. Internally generated and regulated voltages are provided for program and erase operations, so that the device does not require a higher voltage V_{PP} power supply to perform those functions. The device can also be programmed in standard EPROM programmers. Access times as low as 70 ns are offered for timing compatibility with the zero wait state requirements of high speed microprocessors. To eliminate bus contention, the HY29DL16x has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device is compatible with the JEDEC single-power-supply Flash command set standard. Commands are written to the command register using standard microprocessor write timings, from where they are routed to an internal state-machine that controls the erase and programming circuits. Device programming is performed a byte/word at a time by executing the four-cycle Program Command write sequence. This initiates an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Faster programming times can be achieved by placing the HY29DL16x in the Unlock Bypass mode, which requires only two write cycles to program data instead of four.

The HY29DL16x's sector erase architecture allows any number of array sectors, in one or both banks, to be erased and reprogrammed without affecting the data contents of other sectors. Device erasure is initiated by executing the Erase Command sequence. This initiates an internal algorithm that automatically preprograms the sector before executing the erase operation. As during programming cycles, the device automatically times the erase pulse widths and verifies proper cell margin. Hardware Sector Group Protection optionally disables both program and erase operations in any combination of the sector groups, while Temporary Sector Group Unprotect, which requires a high voltage on one pin, allows in-system erasure and code changes in previously protected sector groups. Erase Suspend enables the user to put erase on hold in a bank for any period of time to read data from or program data to any sector in that bank that is not selected for erasure. True background erase can thus be achieved. Because the HY29DL16x features simultaneous read/write capability, there is no need to suspend to read from a sector located within a bank that does not contain sectors marked for erasure. The device is fully erased when shipped from the factory.

Addresses and data needed for the programming and erase operations are internally latched during write cycles. The host system can detect completion of a program or erase operation by observing the RY/BY# pin or by reading the DQ[7] (Data# Polling) and DQ[6] (Toggle) status bits. Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions.

After a program or erase cycle has been completed, or after assertion of the RESET# pin (which terminates any operation in progress), the device is ready to read data or to accept another com-

mand. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The Secured Sector is an extra 64 Kbyte sector capable of being permanently locked at the factory or by customers. The Secured Indicator Bit (accessed via the Electronic ID mode) is permanently set to a 1 if the part is factory locked, and permanently set to a 0 if customer lockable. This way, customer lockable parts can never be used to replace a factory locked part. Factory locked parts provide several options. The Secured Sector may store a secure, random 16-byte ESN (Electronic Serial Number), customer code programmed at the factory, or both. Customer Lockable parts may utilize the Secured Sector as bonus space, reading and writing like any other Flash sector, or may permanently lock their own code there.

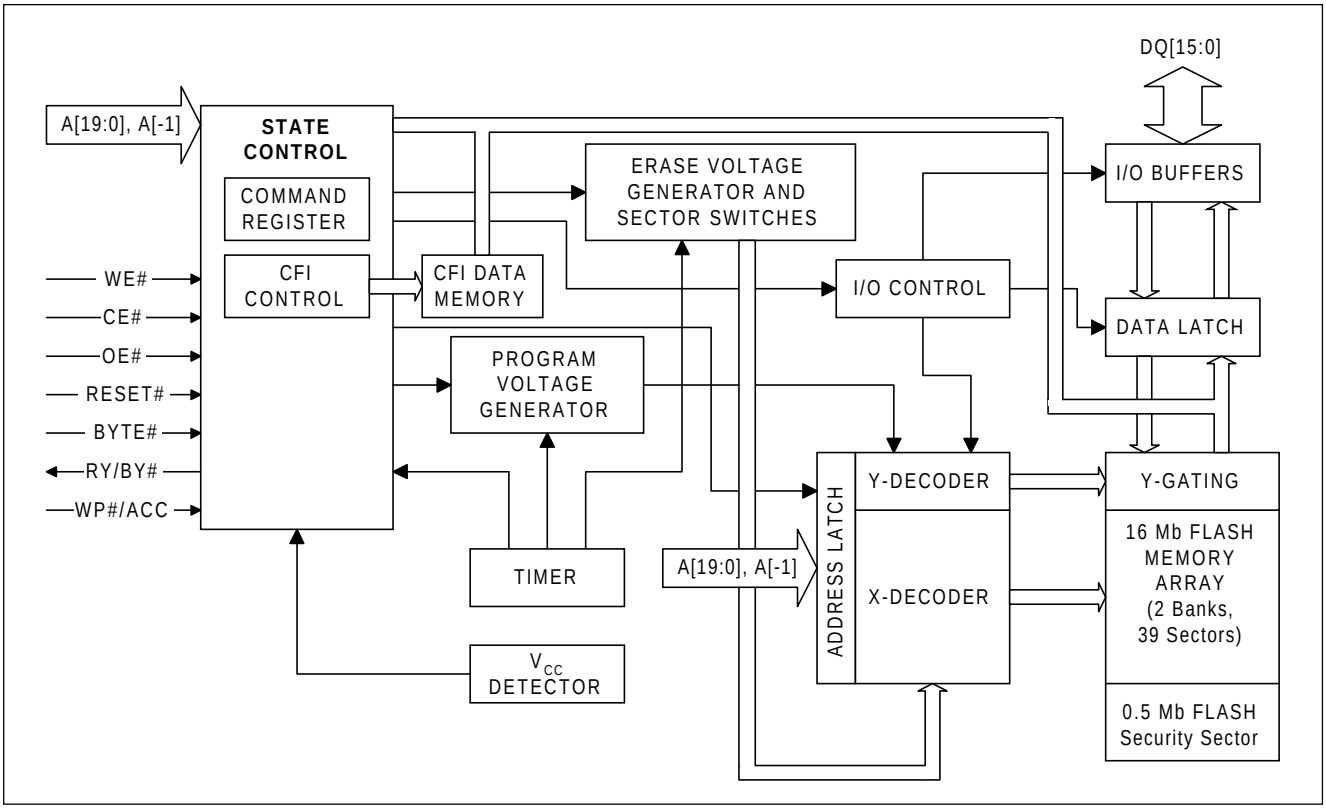
The WP#/ACC pin provides access to two functions. The Write Protect function provides a hardware method of protecting certain boot sectors without using a high voltage. The Accelerate function speeds up programming operations, and is intended primarily to allow faster manufacturing throughput.

Two power-saving features are embodied in the HY29DL16x. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The host can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

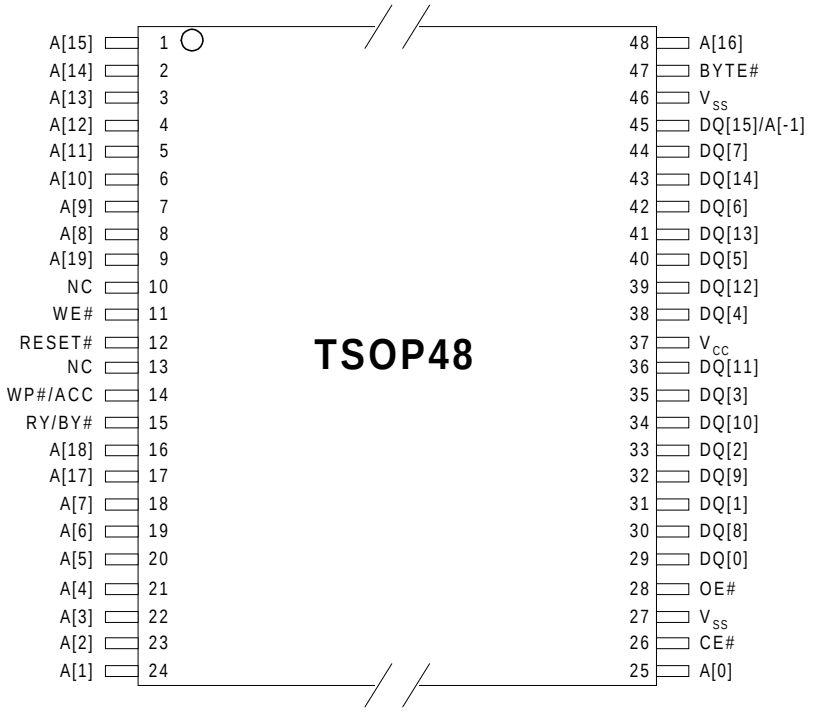
Common Flash Memory Interface (CFI)

To make Flash memories interchangeable and to encourage adoption of new Flash technologies, major Flash memory suppliers developed a flexible method of identifying Flash memory sizes and configurations in which all necessary Flash device parameters are stored directly on the device. Parameters stored include memory size, byte/word configuration, sector configuration, necessary voltages and timing information. This allows one set of software drivers to identify and use a variety of different, current and future Flash products. The standard which details the software interface necessary to access the device to identify it and to determine its characteristics is the Common Flash Memory Interface (CFI) Specification. The HY29DL16x is fully compliant with this specification.

BLOCK DIAGRAM



PIN CONFIGURATIONS



48-Ball FBGA (Top View, Balls Facing Down)

A6 A[13]	B6 A[12]	C6 A[14]	D6 A[15]	E6 A[16]	F6 BYTE#	G6 DQ[15]/A[-1]	H6 V_{SS}
A5 A[9]	B5 A[8]	C5 A[10]	D5 A[11]	E5 DQ[7]	F5 DQ[14]	G5 DQ[13]	H5 DQ[6]
A4 WE#	B4 RESET#	C4 NC	D4 A[19]	E4 DQ[5]	F4 DQ[12]	G4 V_{CC}	H4 DQ[4]
A3 RY/BY#	B3 WP#/ACC	C3 A[18]	D3 NC	E3 DQ[2]	F3 DQ[10]	G3 DQ[11]	H3 DQ[3]
A2 A[7]	B2 A[17]	C2 A[6]	D2 A[5]	E2 DQ[0]	F2 DQ[8]	G2 DQ[9]	H2 DQ[1]
A1 A[3]	B1 A[4]	C1 A[2]	D1 A[1]	E1 A[0]	F1 CE#	G1 OE#	H1 V_{SS}

SIGNAL DESCRIPTIONS

Name	Type	Description
A[19:0]	Inputs	**Address, active High.** In word mode, these 20 inputs select one of 1,048,576 (1M) words within the array for read or write operations. In byte mode, these inputs are combined with the DQ[15]/A[-1] input (LSB) to select one of 2,097,152 (2M) bytes within the array for read or write operations.
DQ[15]/A[-1], DQ[14:0]	Inputs/Outputs Tri-state	**Data Bus, active High**. In word mode, these pins provide a 16-bit data path for read and write operations. In byte mode, DQ[7:0] provide an 8-bit data path and DQ[15]/A[-1] is used as the LSB of the 21-bit byte address input. DQ[14:8] are unused and remain tri-stated in byte mode.
BYTE#	Input	**Byte Mode, active Low.** Controls the Byte/Word configuration of the device. Low selects Byte mode, High selects Word mode.
CE#	Input	**Chip Enable, active Low.** This input must be asserted to read data from or write data to the HY29DL16x. When High, the data bus is tri-stated and the device is placed in the Standby mode.
OE#	Input	**Output Enable, active Low**. This input must be asserted for read operations and negated for write operations. BYTE# determines whether a byte or a word is read during the read operation. When High, data outputs from the device are disabled and the data bus pins are placed in the high impedance state.
WE#	Input	**Write Enable, active Low.** Controls writing of command sequences in order to program data or erase sectors of the memory array. A write operation takes place when WE# is asserted while CE# is Low and OE# is High. BYTE# determines whether a byte or a word is written during the write operation.
RESET#	Input	**Hardware Reset, active Low.** Provides a hardware method of resetting the HY29DL16x to the read array state. When the device is reset, it immediately terminates any operation in progress. The data bus is tri-stated and all read/write commands are ignored while the input is asserted. While RESET# is asserted, the device will be in the Standby mode.
RY/BY#	Output Open Drain	**Ready/Busy Status.** Indicates whether a write or erase command is in progress or has been completed. Valid after the rising edge of the final WE# pulse of a command sequence. It remains Low while the device is actively programming data or erasing, and goes High when it is ready to read array data.
WP#/ACC	Input	**Write Protect, active Low/Accelerate (V_{HH}).** Write Protect Function: Placing this pin at V_{IL} disables program and erase operations in two of the eight 8 Kbyte/4 Kword boot sectors. The affected sectors are S0 and S1 in a bottom-boot device, or S37 and S38 in a top-boot device. If the pin is placed at V_{IH}, the protection state of those two sectors reverts to whether they were last set to be protected or unprotected using the method described in the Sector Group Protection and Unprotection sections. Accelerate Function: If V_{HH} is applied to this input, the device enters the Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would then use the two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the pin returns the device to normal operation. This pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. Leaving the pin unconnected may result in inconsistent device operation.
V_{CC}	--	**3-volt (nominal) power supply.**
V_{SS}	--	**Power and signal ground.**

CONVENTIONS

Unless otherwise noted, a positive logic (active High) convention is assumed throughout this document, whereby the presence at a pin of a higher, more positive voltage (V_{IH}) causes assertion of the signal. A '#' symbol following the signal name, e.g., RESET#, indicates that the signal is asserted in the Low state (V_{IL}). See DC specifications for V_{IH} and V_{IL} values.

Whenever a signal is separated into numbered bits, e.g., DQ[7], DQ[6], ..., DQ[0], the family of bits may also be shown collectively, e.g., as DQ[7:0].

The designation 0xNNNN (N = 0, 1, 2, . . . , 9, A, . . . , E, F) indicates a number expressed in hexadecimal notation. The designation 0bXXXX indicates a number expressed in binary notation (X = 0, 1).

MEMORY ARRAY ORGANIZATION

The 16 Mbit Flash memory array is organized into 39 blocks called *sectors* (S0, S1, . . . , S38). A sector or several contiguous sectors are defined as a *sector group*. A sector is the smallest unit that can be erased and a sector group is the smallest unit that can be protected to prevent accidental or unauthorized erasure. Sectors are also combined into two 'super' groups designated as *banks*.

In the HY29DL16x, eight of the sectors, which comprise the *boot block*, are sized at eight Kbytes (four Kwords), while the remaining 31 sectors are sized at 64 Kbytes (32 Kwords). The boot block can be located at the bottom of the address range (HY29DL16xB) or at the top of the address range (HY29DL16xT).

Tables 1 and 2 define the sector addresses and corresponding array address ranges for the top and bottom boot block versions of the HY29DL16x. Table 3 specifies the bank organizations and corresponding bank addresses. See Tables 7 and 8 for sector group definitions.

Secured Sector Flash Memory Region

The Secured Sector (Sec²) feature provides a 64 Kbyte (32 Kword) Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). An associated 'Sec² Indicator' bit, which is permanently set at the factory and cannot be changed, indicates whether or not the Sec² is locked when shipped from the factory.

The device is offered with the Sec² either factory locked or customer lockable. The *factory-locked* version is always protected when shipped from the factory, and has the Sec² Indicator bit permanently set to a '1'. The *customer-lockable* version is shipped with the Sec² unprotected, allowing customers to utilize the sector in any manner they choose, and has the Sec² Indicator bit permanently set to a '0'. Thus, the Sec² Indicator bit prevents customer-lockable devices from being used to replace devices that are factory locked. The bit prevents cloning of a factory locked part and thus ensures the security of the ESN once the product is shipped to the field.

The system accesses the Sec² through a command sequence (see "Enter/Exit Secured Sector Command Sequence"). After the system has written the Enter Secured Sector command sequence, it may read the Sec² by using the addresses normally occupied by the boot sectors, as specified in Table 4. This mode of operation continues until the system issues the Exit Secured Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to addressing the boot sectors.

Sec² Programmed and Protected At the Factory

In a factory-locked device, the Sec² is protected when the device is shipped from the factory and cannot be modified in any way. The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code
- Both a random, secure ESN and customer code

In devices that have an ESN, it will be located at the bottom of the lowest 8 Kbyte boot sector: starting at byte address 0x000000 and ending at 0x00000F for a Bottom Boot device, and starting at byte address 0x1F0000 and ending at 0x1F000F for a Top Boot device.

Table 1. HY29DL16xT (Top Boot Block) Memory Array Organization

Sector	Size (KB/KW)	Sector Address [1]								Byte Mode Address Range [2]	Word Mode Address Range [3]
		A[19]	A[18]	A[17]	A[16]	A[15]	A[14]	A[13]	A[12]		
S0	64/32	0	0	0	0	0	X	X	X	0x000000 - 0x00FFFF	0x00000 - 0x07FFF
S1	64/32	0	0	0	0	1	X	X	X	0x010000 - 0x01FFFF	0x08000 - 0x0FFFF
S2	64/32	0	0	0	1	0	X	X	X	0x020000 - 0x02FFFF	0x10000 - 0x17FFF
S3	64/32	0	0	0	1	1	X	X	X	0x030000 - 0x03FFFF	0x18000 - 0x1FFFF
S4	64/32	0	0	1	0	0	X	X	X	0x040000 - 0x04FFFF	0x20000 - 0x27FFF
S5	64/32	0	0	1	0	1	X	X	X	0x050000 - 0x05FFFF	0x28000 - 0x2FFFF
S6	64/32	0	0	1	1	0	X	X	X	0x060000 - 0x06FFFF	0x30000 - 0x37FFF
S7	64/32	0	0	1	1	1	X	X	X	0x070000 - 0x07FFFF	0x38000 - 0x3FFFF
S8	64/32	0	1	0	0	0	X	X	X	0x080000 - 0x08FFFF	0x40000 - 0x47FFF
S9	64/32	0	1	0	0	1	X	X	X	0x090000 - 0x09FFFF	0x48000 - 0x4FFFF
S10	64/32	0	1	0	1	0	X	X	X	0x0A0000 - 0x0AFFFF	0x50000 - 0x57FFF
S11	64/32	0	1	0	1	1	X	X	X	0x0B0000 - 0x0BFFFF	0x58000 - 0x5FFFF
S12	64/32	0	1	1	0	0	X	X	X	0x0C0000 - 0x0CFFFF	0x60000 - 0x67FFF
S13	64/32	0	1	1	0	1	X	X	X	0x0D0000 - 0x0DFFFF	0x68000 - 0x6FFFF
S14	64/32	0	1	1	1	0	X	X	X	0x0E0000 - 0x0EFFFF	0x70000 - 0x77FFF
S15	64/32	0	1	1	1	1	X	X	X	0x0F0000 - 0x0FFFFF	0x78000 - 0x7FFFF
S16	64/32	1	0	0	0	0	X	X	X	0x100000 - 0x10FFFF	0x80000 - 0x87FFF
S17	64/32	1	0	0	0	1	X	X	X	0x110000 - 0x11FFFF	0x88000 - 0x8FFFF
S18	64/32	1	0	0	1	0	X	X	X	0x120000 - 0x12FFFF	0x90000 - 0x97FFF
S19	64/32	1	0	0	1	1	X	X	X	0x130000 - 0x13FFFF	0x98000 - 0x9FFFF
S20	64/32	1	0	1	0	0	X	X	X	0x140000 - 0x14FFFF	0xA0000 - 0xA7FFF
S21	64/32	1	0	1	0	1	X	X	X	0x150000 - 0x15FFFF	0xA8000 - 0xAFFFF
S22	64/32	1	0	1	1	0	X	X	X	0x160000 - 0x16FFFF	0xB0000 - 0xB7FFF
S23	64/32	1	0	1	1	1	X	X	X	0x170000 - 0x17FFFF	0xB8000 - 0xBFFFF
S24	64/32	1	1	0	0	0	X	X	X	0x180000 - 0x18FFFF	0xC0000 - 0xC7FFF
S25	64/32	1	1	0	0	1	X	X	X	0x190000 - 0x19FFFF	0xC8000 - 0xCFFFF
S26	64/32	1	1	0	1	0	X	X	X	0x1A0000 - 0x1AFFFF	0xD0000 - 0xD7FFF
S27	64/32	1	1	0	1	1	X	X	X	0x1B0000 - 0x1BFFFF	0xD8000 - 0xDFFFF
S28	64/32	1	1	1	0	0	X	X	X	0x1C0000 - 0x1CFFFF	0xE0000 - 0xE7FFF
S29	64/32	1	1	1	0	1	X	X	X	0x1D0000 - 0x1DFFFF	0xE8000 - 0xEFFFF
S30	64/32	1	1	1	1	0	X	X	X	0x1E0000 - 0x1EFFFF	0xF0000 - 0xF7FFF
S31	8/4	1	1	1	1	1	0	0	0	0x1F0000 - 0x1F1FFF	0xF8000 - 0xF8FFF
S32	8/4	1	1	1	1	1	0	0	1	0x1F2000 - 0x1F3FFF	0xF9000 - 0xF9FFF
S33	8/4	1	1	1	1	1	0	1	0	0x1F4000 - 0x1F5FFF	0XFA000 - 0xFAFFF
S34	8/4	1	1	1	1	1	0	1	1	0x1F6000 - 0x1F7FFF	0xFB000 - 0xFBFFF
S35	8/4	1	1	1	1	1	1	0	0	0x1F8000 - 0x1F9FFF	0xFC000 - 0xFCFFF
S36	8/4	1	1	1	1	1	1	0	1	0x1FA000 - 0x1FBFFF	0xFD000 - 0xFDFFF
S37	8/4	1	1	1	1	1	1	1	0	0x1FC000 - 0x1FDFFF	0XFE000 - 0xFEFFF
S38	8/4	1	1	1	1	1	1	1	1	0x1FE000 - 0x1FFFFF	0xFF000 - 0xFFFFF

Notes:
1. 'X' indicates don't care.
2. '0xN. . . N' indicates an address in hexadecimal notation.
3. The address range in byte mode is A[19:0, -1]. The address range in word mode is A[19:0].

Table 2. HY29DL16xB (Bottom Boot Block) Memory Array Organization

Sector	Size (KB/KW)	Sector Address [1]								Byte Mode Address Range [2]	Word Mode Address Range [3]
		A[19]	A[18]	A[17]	A[16]	A[15]	A[14]	A[13]	A[12]		
S0	8/4	0	0	0	0	0	0	0	0	0x000000 - 0x001FFF	0x00000 - 0x00FFF
S1	8/4	0	0	0	0	0	0	0	1	0x002000 - 0x003FFF	0x01000 - 0x01FFF
S2	8/4	0	0	0	0	0	0	1	0	0x004000 - 0x005FFF	0X02000 - 0x02FFF
S3	8/4	0	0	0	0	0	0	1	1	0x006000 - 0x007FFF	0x03000 - 0x03FFF
S4	8/4	0	0	0	0	0	1	0	0	0x008000 - 0x009FFF	0x04000 - 0x04FFF
S5	8/4	0	0	0	0	0	1	0	1	0x00A000 - 0x00BFFF	0x05000 - 0x05FFF
S6	8/4	0	0	0	0	0	1	1	0	0x00C000 - 0x00DFFF	0X06000 - 0x06FFF
S7	8/4	0	0	0	0	0	1	1	1	0x00E000 - 0x00FFFF	0x07000 - 0x07FFF
S8	64/32	0	0	0	0	1	X	X	X	0x010000 - 0x01FFFF	0x08000 - 0x0FFFF
S9	64/32	0	0	0	1	0	X	X	X	0x020000 - 0x02FFFF	0x10000 - 0x17FFF
S10	64/32	0	0	0	1	1	X	X	X	0x030000 - 0x03FFFF	0x18000 - 0x1FFFF
S11	64/32	0	0	1	0	0	X	X	X	0x040000 - 0x04FFFF	0x20000 - 0x27FFF
S12	64/32	0	0	1	0	1	X	X	X	0x050000 - 0x05FFFF	0x28000 - 0x2FFFF
S13	64/32	0	0	1	1	0	X	X	X	0x060000 - 0x06FFFF	0x30000 - 0x37FFF
S14	64/32	0	0	1	1	1	X	X	X	0x070000 - 0x07FFFF	0x38000 - 0x3FFFF
S15	64/32	0	1	0	0	0	X	X	X	0x080000 - 0x08FFFF	0x40000 - 0x47FFF
S16	64/32	0	1	0	0	1	X	X	X	0x090000 - 0x09FFFF	0x48000 - 0x4FFFF
S17	64/32	0	1	0	1	0	X	X	X	0x0A0000 - 0x0AFFFF	0x50000 - 0x57FFF
S18	64/32	0	1	0	1	1	X	X	X	0x0B0000 - 0x0BFFFF	0x58000 - 0x5FFFF
S19	64/32	0	1	1	0	0	X	X	X	0x0C0000 - 0x0CFFFF	0x60000 - 0x67FFF
S20	64/32	0	1	1	0	1	X	X	X	0x0D0000 - 0x0DFFFF	0x68000 - 0x6FFFF
S21	64/32	0	1	1	1	0	X	X	X	0x0E0000 - 0x0EFFFF	0x70000 - 0x77FFF
S22	64/32	0	1	1	1	1	X	X	X	0x0F0000 - 0x0FFFFF	0x78000 - 0x7FFFF
S23	64/32	1	0	0	0	0	X	X	X	0x100000 - 0x10FFFF	0x80000 - 0x87FFF
S24	64/32	1	0	0	0	1	X	X	X	0x110000 - 0x11FFFF	0x88000 - 0x8FFFF
S25	64/32	1	0	0	1	0	X	X	X	0x120000 - 0x12FFFF	0x90000 - 0x97FFF
S26	64/32	1	0	0	1	1	X	X	X	0x130000 - 0x13FFFF	0x98000 - 0x9FFFF
S27	64/32	1	0	1	0	0	X	X	X	0x140000 - 0x14FFFF	0xA0000 - 0xA7FFF
S28	64/32	1	0	1	0	1	X	X	X	0x150000 - 0x15FFFF	0xA8000 - 0xAFFFF
S29	64/32	1	0	1	1	0	X	X	X	0x160000 - 0x16FFFF	0xB0000 - 0xB7FFF
S30	64/32	1	0	1	1	1	X	X	X	0x170000 - 0x17FFFF	0xB8000 - 0xBFFFF
S31	64/32	1	1	0	0	0	X	X	X	0x180000 - 0x18FFFF	0xC0000 - 0xC7FFF
S32	64/32	1	1	0	0	1	X	X	X	0x190000 - 0x19FFFF	0xC8000 - 0xCFFFF
S33	64/32	1	1	0	1	0	X	X	X	0x1A0000 - 0x1AFFFF	0xD0000 - 0xD7FFF
S34	64/32	1	1	0	1	1	X	X	X	0x1B0000 - 0x1BFFFF	0xD8000 - 0xDFFFF
S35	64/32	1	1	1	0	0	X	X	X	0x1C0000 - 0x1CFFFF	0xE0000 - 0xE7FFF
S36	64/32	1	1	1	0	1	X	X	X	0x1D0000 - 0x1DFFFF	0xE8000 - 0xEFFFF
S37	64/32	1	1	1	1	0	X	X	X	0x1E0000 - 0x1EFFFF	0xF0000 - 0xF7FFF
S38	64/32	1	1	1	1	1	X	X	X	0x1F0000 - 0x1FFFFF	0xF8000 - 0xFFFFF

Notes:
1. 'X' indicates don't care.
2. '0xN. . . N' indicates an address in hexadecimal notation.
3. The address range in byte mode is A[19:0, -1]. The address range in word mode is A[19:0].

Table 3. HY29DL16x Bank Options

		Bank 1			Bank 2		
Device	Reference	Size (Mbit)	Sectors	Bank Address	Size (Mb)	Sectors	Bank Address
HY29DL162T	Table 1	2	S28 - S38	A[19:17] = 111	14	S0 - S27	A[19:17] ≤ 110
HY29DL163T	Table 1	4	S24 - S38	A[19:18] = 11	12	S0 - S23	A[19:18] ≤ 10
HY29DL162B	Table 2	2	S0 - S10	A[19:17] = 000	14	S11 - S38	A[19:17] ≥ 001
HY29DL163B	Table 2	4	S0 - S14	A[19:18] = 00	12	S15 - S38	A[19:18] ≥ 01

Table 4. HY29DL16x Secure Sector Addressing

Device	Sector Size KB/KW	Sector Address A[19:12] [1]	Byte Mode Address Range [2, 3]	Word Mode Address Range [2, 3]
HY29DL162T/163T	64/32	1 1 1 1 1 X X X	0x1F0000 - 0x1FFFFF	0xF8000 - 0xFFFFF
HY29DL162B/163B	64/32	0 0 0 0 0 X X X	0x000000 - 0x00FFFF	0x00000 - 0x07FFF

Notes:
1. 'X' indicates don't care.
2. '0xN. . . N' indicates an address in hexadecimal notation.
3. The address range in byte mode is A[19:0, -1]. The address range in word mode is A[19:0].

Sec² NOT Programmed or Protected at the Factory

If the security feature is not required, the Sec² can be treated as an additional Flash memory space of 64 Kbytes. The Sec² can be read, programmed, and erased as often as required. The Sec² area can be protected using the following procedure:

- Write the three-cycle Enter Secure Sector Region command sequence
- Then follow the sector protect algorithm shown in Figure 1, except that RESET# may be at either V_{IH} or V_{ID}. This allows in-system protection of the Secure Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secure Sector.
- Once the Secure Sector is locked and verified, the system must write the Exit Secure Sector command sequence to return to reading and writing the remainder of the array.

Sec² protection must be used with caution since, once protected, there is no procedure available for unprotecting the Sec² area and none of the bits in the Sec² memory space can be modified in any way.

BUS OPERATIONS

Device bus operations are initiated through the internal command register, which consists of sets of latches that store the commands, along with the address and data information, if any, needed to execute the specific command. The command register itself does not occupy any addressable memory location. The contents of the command register serve as inputs to an internal state machine whose outputs control the operation of the device. Table 5 lists the normal bus operations, the inputs and control levels they require, and the resulting outputs. Certain bus operations require a high voltage on one or more device pins. Those are described in Table 6.

Read Operation

Data is read from the HY29DL16x by using standard microprocessor read cycles while placing the byte or word address on the device's address inputs. The host system must drive the CE# and OE# pins Low and drive WE# High for a valid read operation to take place. The BYTE# pin determines whether the device outputs array data in words (DQ[15:0]) or in bytes (DQ[7:0]).

Table 5. HY29DL16x Normal Bus Operations [1]

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Address [2]	DQ[7:0]	DQ[15:8] [3]	
								BYTE# = H	BYTE# = L
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	High-Z
Write	L	H	L	H	Note 4	A_{IN}	D_{IN}	D_{IN}	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
CE# Normal Standby	H	X	X	H	H	X	High-Z	High-Z	High-Z
CE# Deep Standby	V_{CC} ± 0.3V	X	X	V_{CC} ± 0.3V	H	X	High-Z	High-Z	High-Z
Hardware Reset (Normal Standby)	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Hardware Reset (Deep Standby)	X	X	X	V_{SS} ± 0.3V	L/H	X	High-Z	High-Z	High-Z

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care (L or H), D_{OUT} = Data Out, D_{IN} = Data In. See DC Characteristics for voltage levels.
2. Address is A[19:0, -1] in Byte Mode and A[19:0] in Word Mode.
3. DQ[15] is the A[-1] input in Byte Mode (BYTE# = L).
4. If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the protection state of the two outermost boot sectors depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP#/ACC = V_{HH}, all sectors will be unprotected.

Table 6. HY29DL16x Bus Operations Requiring High Voltage [1, 2]

Operation [3]		CE#	OE#	WE#	RESET#	A[19:12]	A[9]	A[6]	A[1]	A[0]	DQ[7:0]	DQ[15:8]	
												BYTE# = H	BYTE# = L [5]
Sector Group Protect		L	H	L	V_{ID}	SGA [4]	X	L	H	L	D_{IN}	X	X
Sector Unprotect		L	H	L	V_{ID}	X	X	H	H	L	D_{IN}	X	X
Temporary Sector Unprotect [6, 7]		--	--	--	V_{ID}	--	--	--	--	--	--	--	--
Manufacturer Code		L	L	H	H	X	V_{ID}	L	L	L	0xAD	X	High-Z
Device Code	HY29DL162B	L	L	H	H	X	V_{ID}	L	L	H	0x2E	0x22	High-Z
	HY29DL162T										0x2D		
	HY29DL163B										0x2B		
	HY29DL163T										0x28		
Sector Protect State	Unprotected	L	L	H	H	SA [4]	V_{ID}	L	H	L	0x00	X	High-Z
	Protected										0x01		
Secure Sector Indicator Bit	Factory Locked	L	L	H	H	X	V_{ID}	L	H	H	0x80	X	High-Z
	Not Factory Locked										0x00		

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care (L OR H), V_{ID} = 10V nominal. See DC Characteristics for voltage levels.
2. Address bits not specified are Don't Care.
3. See text and Appendix for additional information.
4. SA = Sector Address, SGA = Sector Group Address. See Tables 1, 2, 7, and 8.
5. DQ[15] is the A[-1] input in Byte Mode (BYTE# = L).
6. Normal read, write and output disable operations are used in this mode. See Table 5.
7. If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected.

The HY29DL16x is automatically set for reading array data after device power-up and after a hardware reset to ensure that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data, and both banks of the device remain enabled for read accesses until the command register contents are altered.

This device features the capability of reading data from one bank of the memory while a program or erase operation is in progress in the other bank. If the host reads from an address within an erasing or erase-suspended sector, or from a bank where a programming operation is taking place, the device outputs status data instead of array data (see Write Operation Status section). After completing an Automatic Program or Automatic Erase algorithm within a bank, that bank automatically returns to the read array data mode.

When the host issues an Erase Suspend command, the bank specified in the command enters the Erase- Suspended Read mode. While in that mode, the host can read data from, or program data into, any sector in that bank except the sector(s) being erased. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception noted above.

The host must issue a hardware reset or the software reset command to return a sector to the read array data mode if DQ[5] goes high during a program or erase cycle, or to return the device to the read array data mode while it is in the Electronic ID mode.

Write Operation

Certain operations, including programming data and erasing sectors of memory, require the host to write a command or command sequence to the HY29DL16x. Writes to the device are performed by placing the byte or word address on the device's address inputs while the data to be written is input on DQ[15:0] (BYTE# = High) or DQ[7:0] (BYTE# = Low). The host system must drive the CE# and WE# pins Low and drive OE# High for a valid write operation to take place. All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first.

The "Device Commands" section of this data sheet provides details on the specific device commands implemented in the HY29DL16x.

Accelerated Program Operation

This device offers improved performance for programming operations through the 'Accelerate (ACC)' function. This is one of two functions provided by the WP#/ACC pin and is intended primarily to allow faster manufacturing throughput at the factory.

If V_{HH} is applied to this input, the device enters the Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The host system would then use the two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the pin returns the device to normal operation.

This pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. Leaving the pin floating or unconnected may result in inconsistent device operation.

Write Protect Function

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This is the second function provided by the WP#/ACC pin.

Placing this pin at V_{IL} disables program and erase operations in two of the eight 8 Kbyte (4 Kword) boot sectors. The affected sectors are sectors S0 and S1 in a bottom-boot device, or S37 and S38 in a top-boot device. If the pin is placed at V_{IH}, the protection state of those two sectors reverts to whether they were last set to be protected or unprotected using the method described in the Sector Group Protection and Unprotection sections.

Standby Operation

When the system is not reading or writing to the device, it can place the device in the Standby mode. In this mode, current consumption is greatly reduced, and the data bus outputs are placed in the high impedance state, independent of the OE# input. The Standby mode can invoked using two methods.

The device enters the *CE# controlled Deep Standby* mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3V. Note that this is a more restricted voltage range than V_{IH}. If both CE# and RESET# are held at V_{IH} , but not within V_{CC} ± 0.3V, the device will be in the *Normal Standby* mode, but the standby current will be greater.

The device enters the *RESET# controlled Deep Standby* mode when the RESET# pin is held at V_{SS} ± 0.3V. If RESET# is held at V_{IL} but not within V_{SS} ± 0.3V, the standby current will be greater. See RESET# section for additional information on the reset operation.

The device requires standard access time (t_{CE}) for read access when the device is in any of the standby modes, before it is ready to read data. If the device is deselected during erasure or programming, it continues to draw active current until the operation is completed.

Sleep Mode

The Sleep mode automatically minimizes device power consumption. This mode is automatically entered when addresses remain stable for t_{ACC} + 30 ns (typical) and is independent of the state of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in Sleep mode, output data is latched and always available to the system.

> **NOTE:** Sleep mode is entered only when the device is in Read mode. It is not entered if the device is executing an automatic algorithm, if it is in erase suspend mode, or during receipt of a command sequence.

Output Disable Operation

When the OE# input is at V_{IH}, output data from the device is disabled and the data bus pins are placed in the high impedance state.

Reset Operation

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for the minimum specified period, the device immediately terminates any operation in progress, tri-states the data bus pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. If an operation was interrupted by the assertion of RESET#, it should be reinitiated once the device is ready to accept another command sequence to ensure data integrity.

Current is reduced for the duration of the RESET# pulse as described in the Standby Operation section above.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains Low (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Automatic Algorithms). The system can thus monitor RY/BY# to determine when the reset operation completes, and can perform a read or write operation t_{RB} after RY/BY# goes High. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is High), the reset operation is completed within a time of t_{RP}. In this case, the host can perform a read or write operation t_{RH} after the RESET# pin returns High .

The RESET# pin may be tied to the system reset signal. Thus, a system reset would also reset the device, enabling the system to read the boot-up firmware from the Flash memory.

Sector Group Protect Operation

The hardware sector group protection feature disables both program and erase operations in any combination of sector groups. A sector group consists of a single sector or a group of adjacent sectors, as specified in Tables 7 and 8. This function can be implemented either in-system or by using programming equipment. It requires a high voltage (V_{ID}) on the RESET# pin and uses standard microprocessor bus cycle timing to implement sector protection. The flow chart in Figure 1 illustrates the algorithm.

The HY29DS16x is shipped with all sector groups unprotected. It is possible to determine whether a sector is protected or unprotected. See the Electronic ID Mode section for details.

Sector Unprotect Operation

The hardware sector unprotection feature re-enables both program and erase operations in previously protected sector groups. This function can be implemented either in-system or by using programming equipment. Note that to unprotect any sector, all unprotected sector groups must first be protected prior to the first sector unprotect write

Table 7. Sector Groups - Top Boot Versions

Group	Sectors (Table 1)	Group Address A[19:12]	Block Size KB/KW
SG0	S0	0 0 0 0 0 X X X	64/32
SG1	S1 - S3	0 0 0 0 1 X X X	192/96
		0 0 0 1 0 X X X	
		0 0 0 1 1 X X X	
SG2	S4 - S7	0 0 1 X X X X X	256/128
SG3	S8 -S11	0 1 0 X X X X X	256/128
SG4	S12 - S15	0 1 1 X X X X X	256/128
SG5	S16 - S19	1 0 0 X X X X X	256/128
SG6	S20 - S23	1 0 1 X X X X X	256/128
SG7	S24 - S27	1 1 0 X X X X X	256/128
SG8	S28 - S30	1 1 1 0 0 X X X	192/96
		1 1 1 0 1 X X X	
		1 1 1 1 0 X X X	
SG9	S31	1 1 1 1 1 0 0 0	8/4
SG10	S32	1 1 1 1 1 0 0 1	8/4
SG11	S33	1 1 1 1 1 0 1 0	8/4
SG12	S34	1 1 1 1 1 0 1 1	8/4
SG13	S35	1 1 1 1 1 1 0 0	8/4
SG14	S36	1 1 1 1 1 1 0 1	8/4
SG15	S37	1 1 1 1 1 1 1 0	8/4
SG16	S38	1 1 1 1 1 1 1 1	8/4

Table 8. Sector Groups - Bottom Boot Versions

Group	Sectors (Table 2)	Group Address A[19:12]	Block Size KB/KW
SG0	S0	0 0 0 0 0 0 0 0	8/4
SG1	S1	0 0 0 0 0 0 0 1	8/4
SG2	S2	0 0 0 0 0 0 1 0	8/4
SG3	S3	0 0 0 0 0 0 1 1	8/4
SG4	S4	0 0 0 0 0 1 0 0	8/4
SG5	S5	0 0 0 0 0 1 0 1	8/4
SG6	S6	0 0 0 0 0 1 1 0	8/4
SG7	S7	0 0 0 0 0 1 1 1	8/4
SG8	S8 - S10	0 0 0 0 1 X X X	192/96
		0 0 0 1 0 X X X	
		0 0 0 1 1 X X X	
SG9	S11 - S14	0 0 1 X X X X X	256/128
SG10	S15 - S18	0 1 0 X X X X X	256/128
SG11	S19 - S22	0 1 1 X X X X X	256/128
SG12	S23 - S26	1 0 0 X X X X X	256/128
SG13	S27 - S30	1 0 1 X X X X X	256/128
SG14	S31 - S34	1 1 0 X X X X X	256/128
SG15	S35 - S37	1 1 1 0 0 X X X	192/96
		1 1 1 0 1 X X X	
		1 1 1 1 0 X X X	
SG16	S38	1 1 1 1 1 X X X	64/32

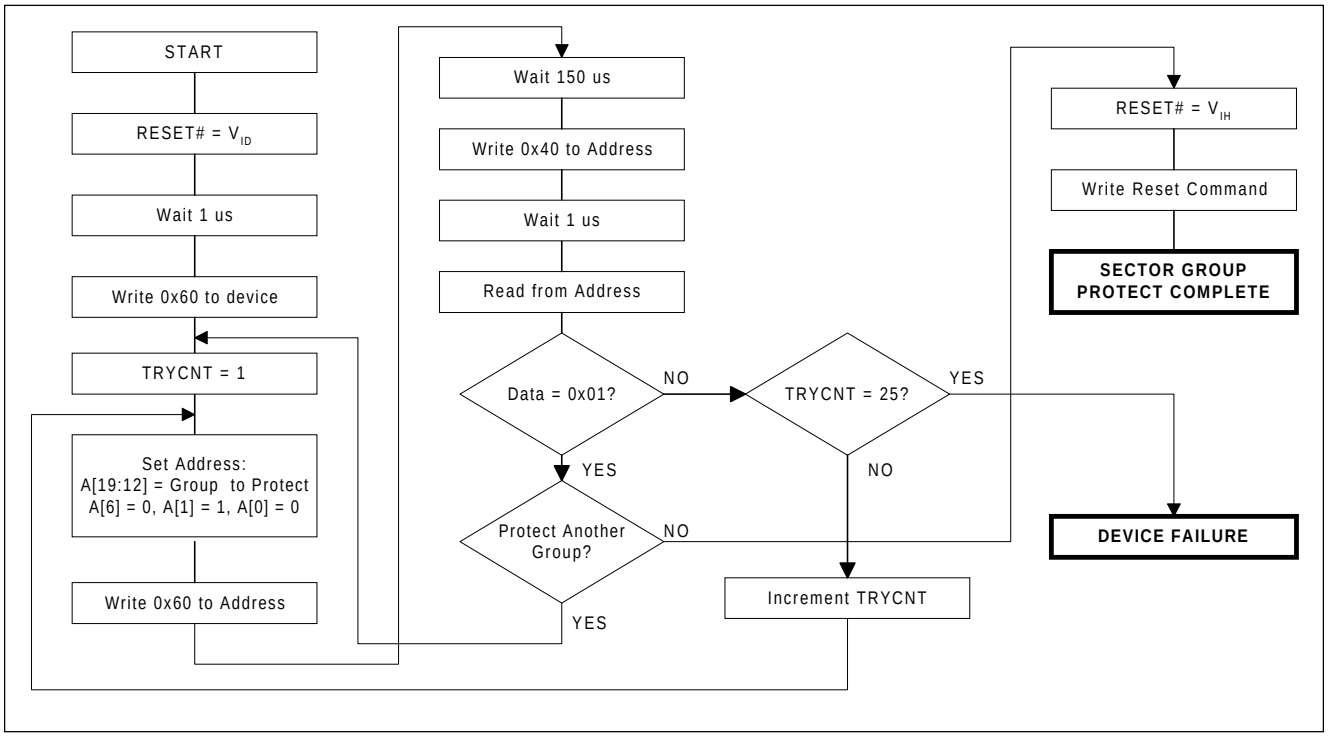


Figure 1. Sector Group Protect Algorithm

cycle. *Also, the unprotect procedure will cause all sectors to become unprotected, thus, sector groups that require protection must be protected again after the unprotect procedure is run.*

This procedure requires V_{ID} on the RESET# pin and uses standard microprocessor bus cycle timing to implement sector unprotection. The flow chart in Figure 2 illustrates the algorithm.

Temporary Sector Unprotect Operation

This feature allows temporary unprotection of protected sectors to allow changing the data in-system. Temporary Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. While in this mode, formerly protected sectors can be programmed or erased by invoking the appropriate commands (see Device Commands section). Once V_{ID} is removed from RESET#, all the previously protected sector groups are protected again. Figure 3 illustrates the algorithm.

NOTE: If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected.

Electronic ID Operation (High Voltage Method)

The Electronic ID mode provides manufacturer and device identification, sector protection verification and Sec[2] region protection status through identifier codes output on DQ[7:0]. This mode is intended primarily for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm.

Two methods are provided for accessing the Electronic ID data. The first requires V_{ID} on address pin A[9], with additional requirements for obtaining specific data items listed in Table 6. The Electronic ID data can also be obtained by the host through specific commands issued via the command register, as described later in the 'Device Commands' section of this data sheet.

While in the high-voltage Electronic ID mode, the system may read at specific addresses to obtain certain device identification and status information:

- A read cycle at address 0xXXX00 retrieves the manufacturer code.
- A read cycle at address 0xXXX01 in word mode or 0xXXX02 in byte mode returns the device code.

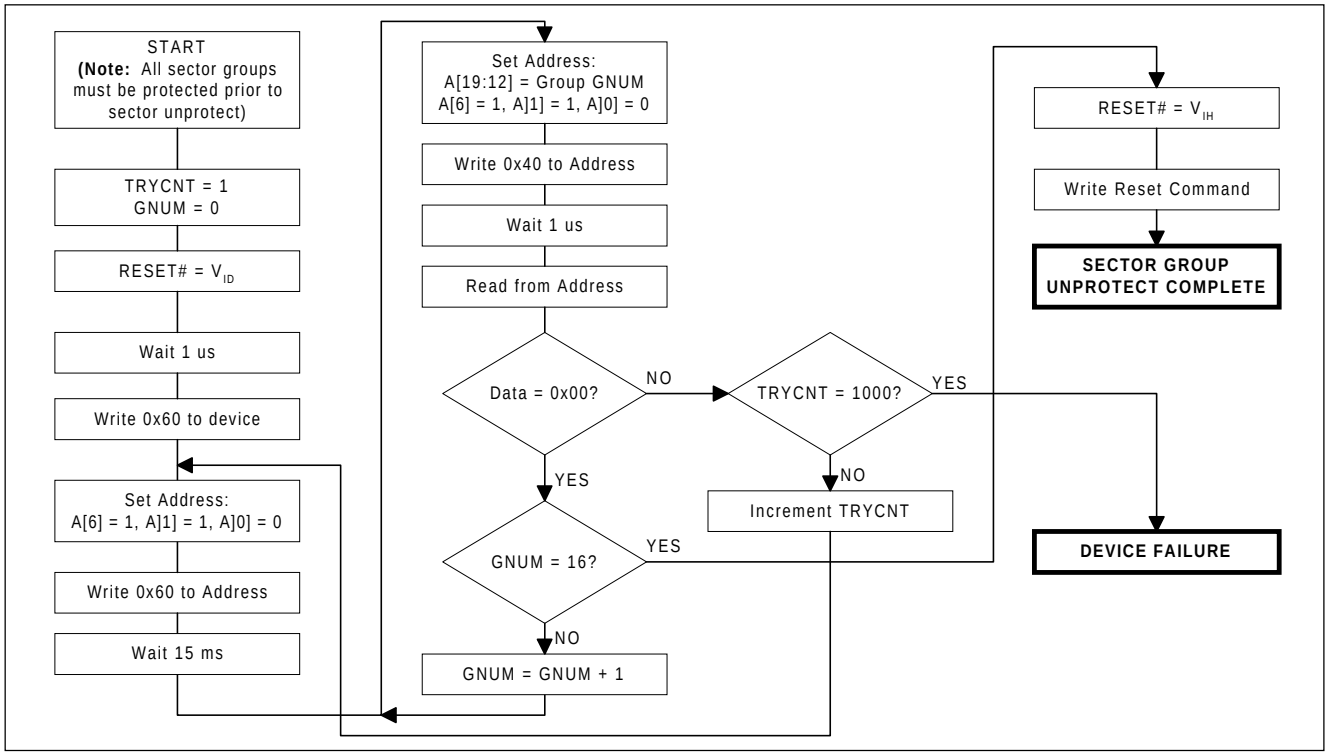


Figure 2. Sector Unprotect Algorithm

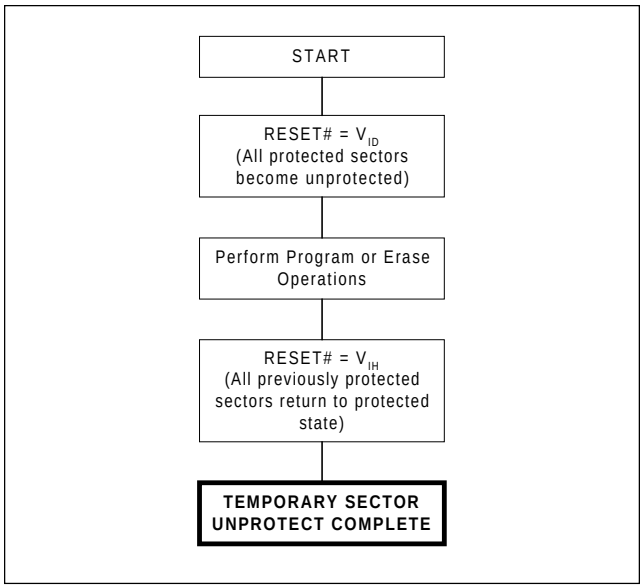


Figure 3. Temporary Sector Unprotect Algorithm

- A read cycle containing a sector address (SA) within the designated bank in A[19:12] and the address 0x04 in A[6:0, A-1] in byte mode, or 0x02 in A[7:0] in word mode, returns 0x01 if that sector is protected, or 0x00 if it is unprotected.
- A read cycle at address 0xXXX03 in word mode or 0xXXX06 in byte mode returns 0x80 if the Sec[2] region is protected and locked at the factory and 0x00 if it is not.

DEVICE COMMANDS

Device operations are initiated by writing designated address and data *command sequences* into the device. Addresses are latched on the falling edge of WE# or CE#, whichever happens later. Data is latched on the rising edge of WE# or CE#, whichever happens first.

A command sequence is composed of one, two or three of the following sub-segments: an *unlock cycle*, a *command cycle* and a *data cycle*. Table 9 summarizes the composition of the valid command sequences implemented in the HY29DL16x, and these sequences are fully described in Table 10 and in the sections that follow.

Writing incorrect address and data values or writing them in the improper sequence resets the HY29DL16x to the Read mode.

Reading Data

The device automatically enters the Read mode after device power-up, after the RESET# input is asserted and upon the completion of certain commands. Commands are not required to retrieve data in this mode. See Read Operation section for additional information.

Reset Command

Writing the Reset command resets the sectors to the Read or Erase-Suspend mode. Address bits are don't cares for this command.

Table 9. Composition of Command Sequences

Command Sequence	Number of Bus Cycles		
	Unlock	Command	Data
Read	0	0	Note 1
Reset	0	1	0
Enter Sec[2] Region	2	1	0
Exit Sec[2] Region	2	1	1
Byte/Word Program	2	1	1
Unlock Bypass	2	1	0
Unlock Bypass Reset	0	1	1
Unlock Bypass Byte/Word Program	0	1	1
Chip Erase	4	1	1
Sector Erase	4	1	1 (Note 2)
Erase Suspend	0	1	0
Erase Resume	0	1	0
Electronic ID	2	1	Note 3
CFI Query	0	1	Note 4

Notes:
1. Any number of Flash array read cycles are permitted.
2. Additional data cycles may follow. See text.
3. Any number of Electronic ID read cycles are permitted.
4. Any number of CFI data read cycles are permitted.

Table 10. HY29DL16x Command Sequences

Command Sequence		Write Cycles	Bus Cycles [1, 2, 3] First Add	First Data	Second Add	Second Data	Third Add	Third Data	Fourth Add	Fourth Data	Fifth Add	Fifth Data	Sixth Add	Sixth Data
Read		0	RA	RD										
Reset [7]		1	XXX	F0										
Enter Sec[2] Region	Word	3	555	AA	2AA	55	555	88						
	Byte	3	AAA		555		AAA							
Exit Sec[2] Region	Word	4	555	AA	2AA	55	555	90	XXX	00				
	Byte	4	AAA		555		AAA		XXX					
Normal Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte		AAA		555		AAA							
Unlock Bypass	Word	3	555	AA	2AA	55	555	20						
	Byte		AAA		555		AAA							
Unlock Bypass Reset		2	XXX	90	XXX	00								
Unlock Bypass Program [9]		2	XXX	A0	PA	PD								
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte		AAA		555		AAA		AAA		555			
Erase Suspend [4]		1	BA	B0										
Erase Resume [5]		1	BA	30										
Electronic ID [6] Manufacturer Code	Word	3	555	AA	2AA	55	(BA)555	90	(BA)X00	AD				
	Byte		AAA		555		(BA)AAA							
Device Code	Word	3	555	AA	2AA	55	(BA)555	90	(BA)X01	2D = '162T, 2E = '162B 28 = '163T, 2B = '163B				
	Byte		AAA		555		(BA)AAA		(BA)X02					
Sector Protect Verify	Word	3	555	AA	2AA	55	(BA)555	90	(SA)X02	00 = Unprotected Sector 01 = Protected Sector				
	Byte		AAA		555		(BA)AAA		(SA)X04					
Sec[2] Region Indicator Bit	Word	3	555	AA	2AA	55	(BA)555	90	(BA)X03	00 = NOT protected and locked at factory 80 = Protected and locked at factory				
	Byte		AAA		555		(BA)AAA		(BA)X06					
Common Flash Interface (CFI) Query [8]	Word	1	(BA)X55	98										
	Byte		(BA)XAA											

See next page for legend and notes.

Legend and notes for Table 10:

Legend:
X = Don't Care
RA/RD = Memory address/data for the read operation
PA/PD = Memory address/data for the program operation
SA = A[19:12], sector address of the sector to be erased or verified (see Note 3 and Tables 1 and 2).
BA = A[19:18] or A[19:17], depending on the device version, bank address, see Note 3 and Table 3.

Notes:
1. All values are in hexadecimal. DQ[15:8] are don't care for unlock and command cycles.
2. All bus cycles are write operations unless otherwise noted.
3. Address is A[10:0] in Word mode and A[10:0, -1] in Byte mode. A[19:11] are don't care except as follows:
   - For RA and PA, A[19:11] are the upper address bits of the byte to be read or programmed.
   - Where 'SA' is indicated, A[19:12] are the sector address.
   - Where 'BA' is indicated, A[19:18] or A[19:17], depending on the device version, are the bank address.
4. The Erase Suspend command is valid only during a sector erase operation. The system may read and program in non-erasing sectors, or enter the Electronic ID mode, while in the Erase Suspend mode.
5. The Erase Resume command is valid only during the Erase Suspend mode.
6. The fourth bus cycle is a read cycle.
7. The command is required only to return to the Read mode when the device is in the Electronic ID command mode or in the CFI Query mode. It must also be issued to return to read mode if DQ[5] goes High during a program or erase operation. It is not required for normal read operations.
8 This command is valid only when the device is in Read mode or in Electronic ID mode.
9. The Unlock Bypass command is required prior to the Unlock Bypass Program command.

As described above, a Reset command is not normally required to begin reading array data. However, a Reset command must be issued in order to read array data in the following cases:

- If the device is in the Electronic ID mode, a Reset command must be written to return to the Read mode. If the device was in the Erase Suspend mode when the device entered the Electronic ID mode, writing the Reset command returns the device to the Erase Suspend mode.

  Note: When in the Electronic ID bus operation mode, the device returns to the Read mode when V_{ID} is removed from the A[9] pin. The Reset command is not required in this case.

- If the device is in the CFI Query mode, a Reset command must be written to return to the array Read mode.

- If DQ[5] (Exceeded Time Limit) goes High during a program or erase operation, a Reset command must be invoked to return the sectors to the Read mode (or to the Erase Suspend mode if the device was in Erase Suspend when the Program command was issued).

The Reset command may also be used to abort certain command sequences:

- In a Sector Erase or Chip Erase command sequence, the Reset command may be written at any time before erasing actually begins, including, for the Sector Erase command, between the cycles that specify the sectors to be erased (see Sector Erase command description). This aborts the command and resets the device to the Read mode. Once erasure begins, however, the device ignores the Reset command until the operation is complete.

- In a Program command sequence, the Reset command may be written between the sequence cycles before programming actually begins. This aborts the command and resets the device to the Read mode, or to the Erase Suspend mode if the Program command sequence is written while the device is in the Erase Suspend mode. Once programming begins, however, the device ignores the Reset command until the operation is complete.

- The Reset command may be written between the cycles in an Electronic ID command sequence to abort that command. As described above, once in the Electronic ID mode, the Reset command *must* be written to return to the array Read mode.

Enter /Exit Sec^2 Command Sequence

The system can access the Sec^2 region of the device by issuing the Enter Sec^2 Region command sequence. The device continues to access the Sec^2 region until the system issues the Exit Sec^2 Region command sequence, which returns the device to normal operation.

Note: A hardware reset will reset the device to the read array mode.

Program Command

The system programs the device a word or byte at a time by issuing the appropriate four-cycle Program command sequence, as shown in Table 10. The sequence begins by writing two unlock cycles, followed by the program setup command and, lastly, the program address and data. This initiates the Automatic Program algorithm that automatically provides internally generated program pulses and verifies the programmed cell margin. The host is not required to provide further controls or timings during this operation. When the Automatic Program algorithm is complete, that bank returns to the Read mode. Several methods are provided to allow the host to determine the status of the programming operation, as described in the Write Operation Status section. While the Automatic Program algorithm is in progress in one bank, the host may read data from the non-programming bank.

Commands written to the device during execution of the Automatic Program algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. To ensure data integrity, the aborted program command sequence should be reinitiated once the reset operation is complete.

Programming is allowed in any sequence. Only erase operations can convert a stored ‘0’ to a ‘1’. Thus, a bit cannot be programmed from a ‘0’ back to a ‘1’. Attempting to do so may cause that bank to halt the operation and set DQ[5] to ‘1’, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still ‘0’.

Unlock Bypass/Bypass Program/Bypass Reset Commands

Unlock Bypass provides a faster method than the normal Program command for the host system to program bytes or words to a bank. As shown in Table 10, the Unlock Bypass command sequence consists of two unlock write cycles followed by a third write cycle containing the Unlock Bypass command, 0x20. That bank then enters the Unlock Bypass mode. In this mode, a two-cycle Unlock Bypass Program command sequence is used instead of the standard four-cycle program sequence to invoke a programming operation. The first cycle in this sequence contains the Unlock Bypass Program command, 0xA0, and the second cycle specifies the program address and data, thus eliminating the initial two unlock cycles required in the standard Program command sequence. Additional data is programmed in the same manner.

During the Unlock Bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the Unlock Bypass mode, the host must issue the two-cycle Unlock Bypass Reset command sequence shown in Table 10. The bank specified in the first cycle of that command then returns to the Read array data mode.

Figure 4 illustrates the procedures for the normal and unlock bypass program operations.

Note: The device automatically enters the Unlock Bypass mode when it is placed in Accelerate mode via the WP#/ACC pin.

Chip Erase Command

The Chip Erase command sequence consists of two unlock cycles, followed by a set-up command, two additional unlock cycles and then the Chip Erase command. This sequence invokes the Automatic Erase algorithm that automatically preprograms (if necessary) and verifies the entire memory for an all zero data pattern prior to electrical erase. The host system is not required to provide any controls or timings during these operations.

If all sectors in the device are protected, the device returns to reading array data after approximately 100 µs. If at least one sector is unprotected, the erase operation erases the unprotected sectors, and ignores the command for the sectors that are protected. However, even if every sector in one of the banks is protected, reads from that bank are not permitted until the completion of the Automatic Erase algorithm for the unprotected sectors in the other bank.

Commands written to the device during execution of the Automatic Erase algorithm are ignored. Note that a hardware reset immediately terminates the chip erase operation. To ensure data integrity, the aborted Chip Erase command sequence should be reissued once the reset operation is complete.

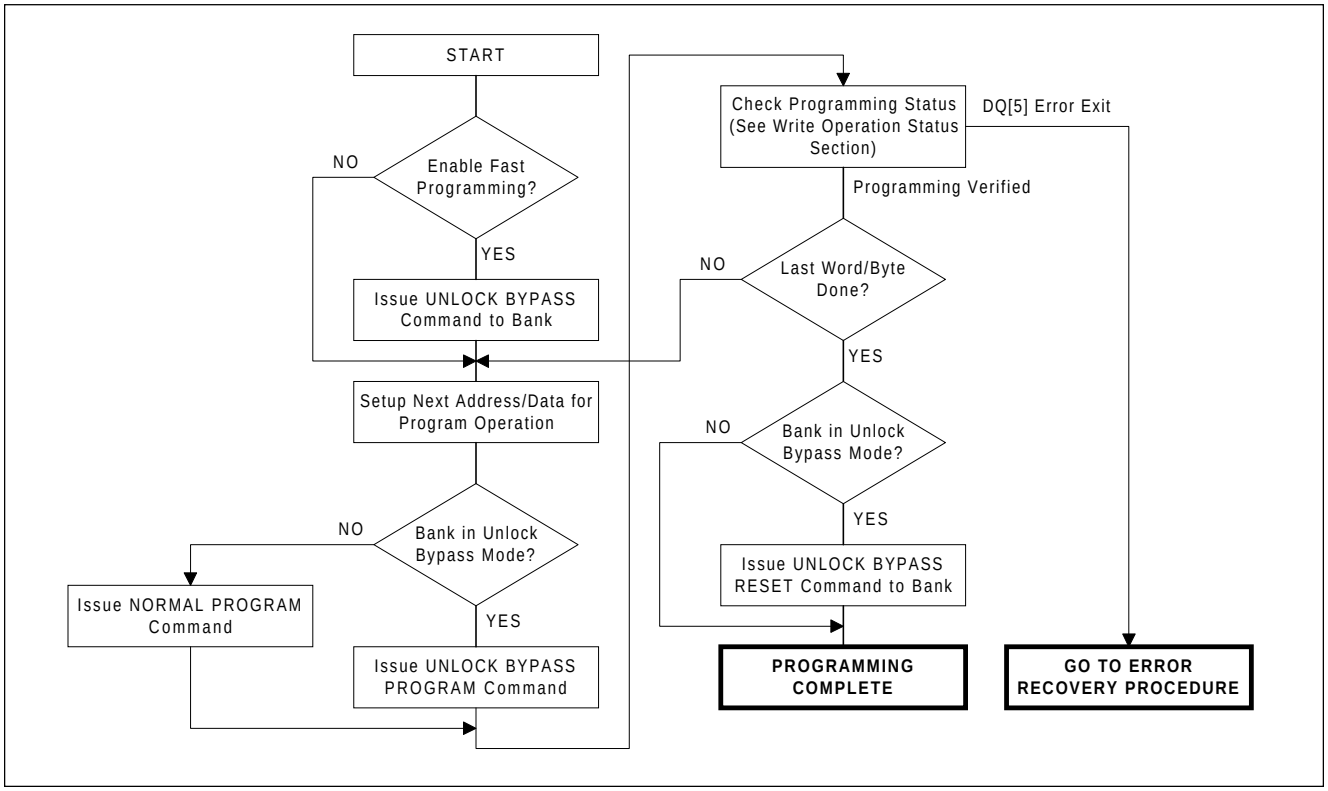


Figure 4. Normal and Unlock Bypass Programming Procedures

When the Automatic Erase algorithm is complete, the device returns to the reading array data mode. Several methods are provided to allow the host to determine the status of the erase operation, as described in the Write Operation Status section.

Figure 5 illustrates the chip erase procedure.

Sector Erase Command

The Sector Erase command sequence consists of two unlock cycles, followed by a set-up command, two additional unlock cycles and then the Sector Erase command, which specifies which sector is to be erased. This sequence invokes the Automatic Erase algorithm that automatically preprograms (if necessary) and verifies the specified sector for an all zero data pattern prior to electrical erase. The host system is not required to provide any controls or timings during these operations.

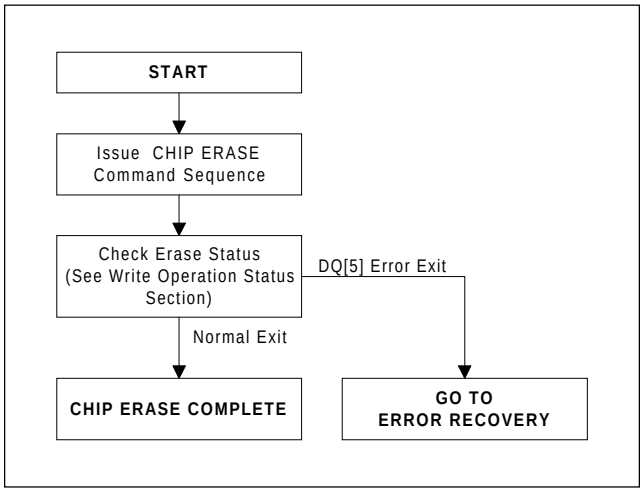


Figure 5. Chip Erase Procedure

After the sector erase data cycle (the sixth cycle) of the command sequence is issued, a sector erase time-out of 50 µs (min) begins, measured from the rising edge of the final WE# pulse in the command sequence. During this time, an additional sector address and sector erase data cycle may be written into an internal sector erase buffer. This buffer may be loaded in any sequence, and the number of sectors designated for erasure may be from one sector to all sectors. The only restriction is that the time between these additional cycles must be less than 50 µs, otherwise erasure may begin before the last address and command are accepted. To ensure that all commands are accepted, it is recommended that host processor interrupts be disabled during the time that

the additional sector erase commands are being issued and then be re-enabled afterwards.

The system can monitor DQ[3] to determine if the 50 µs sector erase time-out has expired, as described in the Write Operation Status section. If the time between additional sector erase commands can be assured to be less than the time-out, the system need not monitor DQ[3].

Any command other than Sector Erase or Erase Suspend during the time-out period resets the bank(s) to reading array data. The system must then rewrite the command sequence, including any additional sector addresses. Once the sector erase operation itself has begun, only the Erase Suspend command is valid. All other commands are ignored.

As for the Chip Erase command, note that a hardware reset immediately terminates the erase operation. To ensure data integrity, the aborted Sector Erase command sequence should be reissued once the reset operation is complete.

If all sectors designated for erasing are protected, the device returns to reading array data after approximately 100 µs. If at least one designated sector is unprotected, the erase operation erases the unprotected sectors, and ignores the command for the sectors that are protected. If sectors in a bank are designated for erasure, read array operations from that bank cannot take place until the Automatic Erase algorithm terminates, even if all of those sectors are protected. However, the HY29DL16x's simultaneous read feature allows data to be read from a bank that does not contain any sectors that are designated for erasure while the erase algorithm is in progress in the other bank.

When the Automatic Erase algorithm is complete, the device returns the erased sector(s) to the Read array data mode. Several methods are provided to allow the host to determine the status of the erase operation, as described in the Write Operation Status section.

Figure 6 illustrates the sector erase procedure.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation to program data into, or to read data from, any sector not designated for erasure. (The HY29DL16x's simultaneous read feature allows data to be read from a bank that does not contain any sectors marked for erasure even while the erase operation is not suspended). The command, which requires the

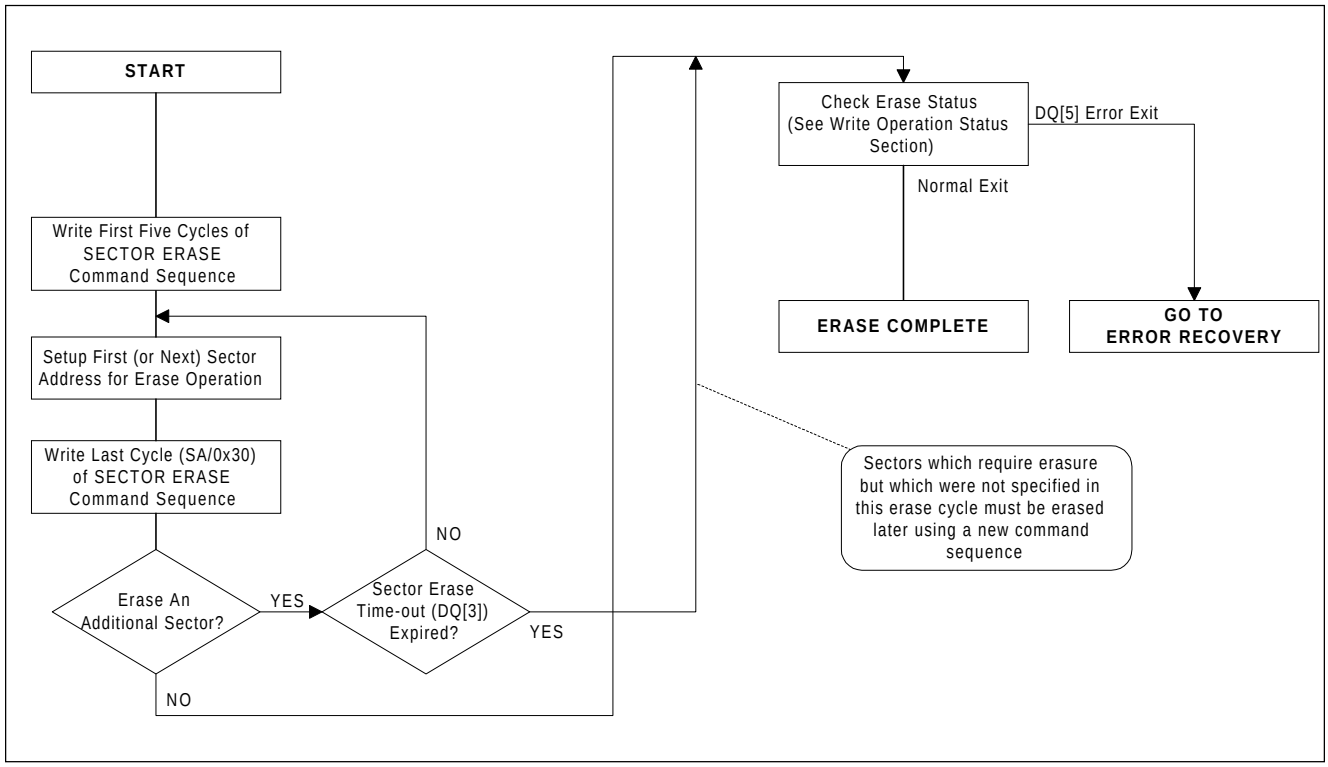


Figure 6. Sector Erase Procedure

bank address, causes the erase operation to be suspended in all sectors designated for erasure in the specified bank. This command is valid only during the sector erase operation, including during the 50 µs time-out period at the end of the command sequence, and is ignored if it is issued during chip erase or programming operations.

The HY29DL16x requires a maximum of 20 µs to suspend the erase operation if the erase suspend command is issued during active sector erasure. However, if the command is written during the sector erase time-out, the time-out is terminated and the erase operation is suspended immediately. Once the erase operation has been suspended in the bank, the system can read array data from or program data into any sector in that bank that is not designated for erasure. Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ[7:0]. The host can use DQ[7], or DQ[6] and DQ[2] together, to determine if a sector is actively erasing or is erase-suspended. See 'Write Operation Status' for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspended read state and the host can initiate another programming operation (or read operation) within non-suspended sectors. The host can determine the status of a program operation during the erase-suspended state just as in the standard programming operation.

The host may also write the Electronic ID command sequence when the bank is in the Erase Suspend mode. The device allows reading Electronic ID codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the Electronic ID mode, the bank reverts to the Erase Suspend mode, and is ready for another valid operation. See the Electronic ID Command section for more information.

The system must write the Erase Resume command to the erase-suspended bank to exit the Erase Suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Table 11 summarizes the erase operations in the HY29DL16x.

Electronic ID Command

The Electronic ID mode provides manufacturer and device identification and sector protection verification through identifier codes output on DQ[7:0]. This mode is intended primarily for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm.

Table 11. HY29DL16x Erase Operations Summary [7]

	Erase Suspend Allowed?		Programming Allowed? [1]		Output from Read Operation [3]			
					ES Sector [4]		Non-ES Sector [5]	
Operation in Progress	**Bank 1**	**Bank 2**	**Bank 1**	**Bank 2**	**Bank 1**	**Bank 2**	**Bank 1**	**Bank 2**
No erase	n/a	n/a	Yes	Yes	n/a	n/a	Data	Data
Chip Erase	No	No	No	No	n/a	n/a	Status	Status
Sector Erase in Bank 1 Only	Yes	No	Yes [2]	Yes [6]	Status	n/a	Data	Data
Sector Erase in Bank 2 Only	No	Yes	Yes [6]	Yes [2]	n/a	Status	Data	Data
Sector Erase in Banks 1 and 2	Yes	Yes	Yes [2]	Yes [2]	Status	Status	Data	Data

Notes:
1. Only one simultaneous programming operation is permitted.
2. Allowed only when the bank is in erase suspend state and only into a sector that is not designated for erasure.
3. Output may differ if program operation is in progress. See Write Operation Status section for additional information.
4. Read from a sector that is designated for erasure while the bank is in erase suspend state.
5. Read from a sector that is not designated for erasure while the bank is in erase suspend state, or read from any sector in a bank where an erase operation has not been commanded, or any read for the Chip Erase operation.
6. Erase operation in the other bank must be suspended.
7. n/a = not applicable. Condition cannot exist.
   Data = array data from addressed location.
   Status = write operation status (see Write Operation Status section for additional information).

Two methods are provided for accessing the Electronic ID data. The first requires V_{ID} on address pin A[9], as described previously in the Device Operations section.

The Electronic ID data can also be obtained by the host through specific commands issued via the command register, as shown in Table 10. This method does not require V_{ID}. The Electronic ID command sequence may be written to an address within a bank that is in the read mode or in the Erase Suspend mode. The command may not be written while the device is actively programming or erasing in the other bank.

The Electronic ID command sequence is initiated by writing two unlock cycles, followed by a third write cycle that contains the bank address and the Electronic ID command. The addressed bank then enters the Electronic ID mode, and the system may read at any address in that bank any number of times, without initiating another command sequence.

- A read cycle at address 0x(BA)X00, where BA is the Bank Address, retrieves the manufacturer code.
- A read cycle at address 0x(BA)X01 in word mode or 0x(BA)X02 in byte mode returns the device code.
- A read cycle containing a sector address (SA) within the designated bank in A[19:12] and the address 0x04 in A[6:0, A-1] in byte mode, or 0x02 in A[7:0] in word mode, returns 0x01 if that sector is protected, or 0x00 if it is unprotected.
- A read cycle at address 0x(BA)X03 in word mode or 0x(BA)X06 in byte mode returns 0x80 if the Sec[2] region is protected and locked at the factory and 0x00 if it is not.

Array data may be read from the other bank while the designated bank is in the Electronic ID mode. The system must write the Reset command to exit the Electronic ID mode and return the bank to the normal Read mode, or to the Erase-Suspended read mode if the bank was in that mode when the Electronic ID command was invoked. In the latter case, an Erase Resume command to that bank will continue the suspended erase operation.

Query Command and Common Flash Interface (CFI) Mode

The HY29DL16x is capable of operating in the Common Flash Interface (CFI) mode. This mode allows the host system to determine the manufacturer of the device, its operating parameters, its configuration and any special command codes that the device may accept. With this knowledge, the system can optimize its use of the chip by using appropriate timeout values, optimal voltages and commands necessary to use the chip to its full advantage.

Two commands are employed in association with CFI mode. The first places the device in CFI mode (Query command) and the second takes it out of CFI mode (Reset command). These are described in Table 10.

The single cycle Query command is valid only when the device is in the Read mode, including during Erase Suspend and Standby states and while in Electronic ID command mode, but is ignored otherwise. The command is not valid while the HY29DL16x is in the Electronic ID bus operation mode. The command places the Bank designated in the ‘Bank Address’ field of the command in the CFI Query mode. Array data may be read from the other bank while the designated bank is in the CFI Query mode. Read cycles at appropriate addresses within the designated bank while in the Query mode provide CFI data as described later in this section. Write cycles are ignored, except for the Reset command.

The Reset command returns the device from the CFI mode to the array Read mode, or to the Erase Suspend mode if the device was in that mode prior to entering CFI mode, or to the Electronic ID mode if the device was in that mode prior to entering CFI mode. The command is valid only when the device is in the CFI mode and as otherwise described for the normal Reset command.

Tables 12 - 15 specify the data provided by the HY29DL16x during CFI mode. Data at unspecified addresses reads out as 0x00. Note that a value of 0x00 for a data item normally indicates that the function is not supported. All values in these tables are in hexadecimal.

Table 12. CFI Mode: Identification Data Values

	Word Mode		Byte Mode	
Description	**Address**	**Data**	**Address**	**Data**
Query-unique ASCII string "QRY"	10 11 12	0051 0052 0059	20 22 24	51 52 59
Primary vendor command set and control interface ID code	13 14	0002 0000	26 28	02 00
Address for primary algorithm extended query table	15 16	0040 0000	2A 2C	40 00
Alternate vendor command set and control interface ID code (none)	17 18	0000 0000	2E 30	00 00
Address for secondary algorithm extended query table (none)	19 1A	0000 0000	32 34	00 00

Table 13. CFI Mode: System Interface Data Values

	Word Mode		Byte Mode	
Description	**Address**	**Data**	**Address**	**Data**
V_{CC} supply, minimum (2.7V)	1B	0027	36	27
V_{CC} supply, maximum (3.6V)	1C	0036	38	36
V_{PP} supply, minimum (none)	1D	0000	3A	00
V_{PP} supply, maximum (none)	1E	0000	3C	00
Typical timeout for single word/byte write (2^N µs)	1F	0004	3E	04
Typical timeout for maximum size buffer write (2^N µs)	20	0000	40	00
Typical timeout for individual block erase (2^N ms)	21	000A	42	0A
Typical timeout for full chip erase (2^N ms)	22	000F	44	0F
Maximum timeout for single word/byte write (2^N x Typ)	23	0005	46	05
Maximum timeout for maximum size buffer write (2^N x Typ)	24	0000	48	00
Maximum timeout for individual block erase (2^N x Typ)	25	0004	4A	04
Maximum timeout for full chip erase (not supported)	26	0000	4C	00

Table 14. CFI Mode: Device Geometry Data Values

Description	Word Mode		Byte Mode	
	Address	Data	Address	Data
Device size (2^N bytes)	27	0015	4E	15
Flash device interface code (02 = asynchronous x8/x16)	28 29	0002 0000	50 52	02 00
Maximum number of bytes in multi-byte write (not supported)	2A 2B	0000 0000	54 56	00 00
Number of erase block regions	2C	0002	58	02
Erase block region 1 information [2E, 2D] = # of blocks in region - 1 [30, 2F] = size in multiples of 256-bytes	2D 2E 2F 30	0007 0000 0020 0000	5A 5C 5E 60	07 00 20 00
Erase block region 2 information	31 32 33 34	001E 0000 0000 0001	62 64 66 68	1E 00 00 01

Table 15. CFI Mode: Vendor-Specific Extended Query Data Values

Description	Word Mode		Byte Mode	
	Address	Data	Address	Data
Query-unique ASCII string "PRI"	40 41 42	0050 0052 0049	80 82 84	50 52 49
Major version number, ASCII	43	0031	86	31
Minor version number, ASCII	44	0030	88	30
Address sensitive unlock (0 = required, 1 = not required)	45	0000	8A	00
Erase suspend (2 = to read and write)	46	0002	8C	02
Sector protect (N = # of sectors/group)	47	0001	8E	01
Temporary sector unprotect (1 = supported)	48	0001	90	01
Sector protect/unprotect scheme (4 = Am29LV800A method)	49	0004	92	04
Simultaneous R/W operation (xx = number of sectors in Bank 2: HY29DL162 = 1C, HY29DL163 = 18)	4A	001C or 0018	94	1C or 18
Burst mode type (0 = not supported)	4B	0000	96	00
Page mode type (0 = not supported)	4C	0000	98	00
ACC Supply minimum (8.5V)	4D	0085	9A	85
ACC Supply maximum (9.5V)	4E	0095	9C	95
Top/bottom boot version (BB = Bottom Boot, TB = Top Boot)	4F	0002 (BB) 0003 (TB)	9E	02 (BB) 03 (TB)

WRITE OPERATION STATUS

The HY29DL16x provides a number of facilities to determine the status of a program or erase operation. These are the RY/BY# (Ready/Busy#) pin and certain bits of a status word which can be read from the device during the programming and erase operations. Table 16 summarizes the status indications and further detail is provided in the subsections which follow.

RY/BY# - Ready/Busy#

RY/BY# is an open-drain output pin that indicates whether a programming or erase Automatic Algorithm is in progress or has completed. A pull-up resistor to V_{CC} is required for proper operation. RY/BY# is valid after the rising edge of the final WE# pulse in the corresponding command sequence, including during the sector erase time-out.

If the output is Low (busy), the device is actively erasing or programming, including programming while in the Erase Suspend mode. If the output is High (ready), the device has completed the operation and is ready to read array data, is in the standby mode, or at least one bank is in the erase-suspend read mode.

DQ[7] - Data# Polling

The Data# Polling bit, DQ[7], indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether a bank is in Erase Suspend mode. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

While a programming operation is in progress, the device outputs the complement of the value programmed to DQ[7]. When the programming operation is complete, the device outputs the value programmed to DQ[7]. If a program operation is attempted within a protected sector, Data# Polling on DQ[7] is active for approximately 1 µs, then the device returns to reading array data. *The host system must do a read at the program address to obtain valid programming status information on this bit.*

During an erase operation, Data# Polling produces a “0” on DQ[7]. When the erase operation is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ[7]. *The host must read at an address within any of the non-protected sectors designated for erasure to*

Table 16. Write and Erase Operation Status Summary

Mode	Operation	DQ[7] [1]	DQ[6]	DQ[5]	DQ[3]	DQ[2] [1]	RY/BY#
Normal	Programming in progress	DQ[7]#	Toggle	0/1 [2]	N/A	N/A	0
	Programming completed	Data	Data [4]	Data	Data	Data	1
	Erase in progress	0	Toggle	0/1 [2]	1 [3]	Toggle	0
	Erase completed [5]	Data	Data [4]	Data	Data	Data [4]	1
Erase Suspend	Read within erase suspended sector	1	No toggle	0	N/A	Toggle	1
	Read within non-erase suspended sector	Data	Data	Data	Data	Data	1
	Programming in progress [6]	DQ[7]#	Toggle	0/1 [2]	N/A	N/A	0
	Programming completed [6]	Data	Data [4]	Data	Data	Data	1

Notes:
1. A valid address within the bank where an Automatic algorithm is in progress is required when reading status information except RY/BY#. For a programming operation, the address used for the read cycle should be the program address. For an erase operation, the address used for the read cycle should be any address within a non-protected sector marked for erasure (any address for the chip erase operation).
2. DQ[5] status switches to a ‘1’ when a program or erase operation exceeds the maximum timing limit.
3. A ‘1’ during sector erase indicates that the 50 µs time-out has expired and active erasure is in progress. DQ[3] is not applicable to the chip erase operation.
4. Equivalent to ‘No Toggle’ because data is obtained in this state.
5. Data (DQ[7:0]) = 0xFF immediately after erasure.
6. Programming can be done only in a non-suspended sector (a sector not specified for erasure).

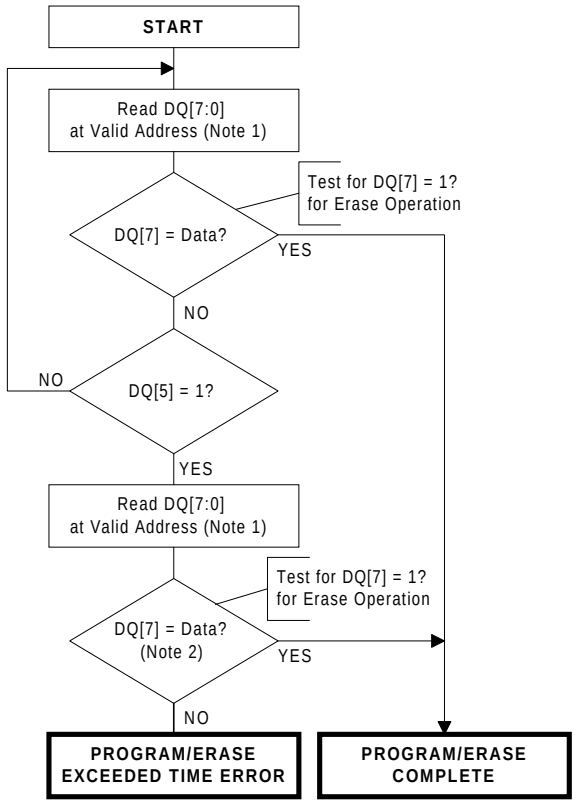
obtain valid erase status information on DQ[7]. If all sectors designated for erasing are protected, Data# Polling on DQ[7] is active for approximately 100 µs, then the bank returns to reading array data.

When the system detects that DQ[7] has changed from the complement to true data (or "0" to "1" for erase), it should do an additional read cycle to ensure that valid data is read on DQ[7:0] or DQ[15:0]. This is because DQ[7] may change asynchronously with respect to the other data bits while Output Enable (OE#) is asserted low.

Figure 7 shows the Data# Polling test algorithm.

DQ[6] - Toggle Bit I

Toggle Bit I on DQ[6] indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address within the programming or erasing bank and is valid after the rising edge of the final WE# pulse in the Program or Erase command sequence, including during the sector erase time-out. The system may use either OE# or CE# to control the read cycles.



Notes:
1. During *programming* , the program address. During *sector erase* , an address within any non-protected sector specified for erasure. During *chip erase* , an address within any non-protected sector.
2. Recheck DQ[7] since it may change asynchronously to DQ[5].

Figure 7. Data# Polling Test Algorithm

During an Automatic Program algorithm operation (including programming while in Erase Suspend mode), successive read cycles at any address in the bank where the program operation is taking place cause DQ[6] to toggle. DQ[6] stops toggling when the operation is complete. If a program address falls within a protected sector, DQ[6] toggles for approximately 1 µs after the Program command sequence is written, then returns to reading array data.

While erasing, successive read cycles within any sector designated for erasure (or any sector for the chip erase operation) cause DQ[6] to toggle. DQ[6] stops toggling when the erase operation is complete or when the device is placed in the Erase Suspend mode. The host may use DQ[2] to determine which sectors are erasing or erase-suspended (see below).

After an Erase command sequence is written, if all the sectors designated for erasure are protected, DQ[6] toggles for approximately 100 µs, and the device then returns to reading array data.

DQ[2] - Toggle Bit II

Toggle Bit II, DQ[2], when used with DQ[6], indicates whether a particular sector is actively erasing or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. The device toggles DQ[2] with each OE# or CE# read cycle.

DQ[2] toggles when the host reads at addresses within sectors that have been designated for erasure, but cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ[6], by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are designated for erasure. Thus, both status bits are required for sector and mode information.

Figure 8 illustrates the operation of Toggle Bits I and II.

DQ[5] - Exceeded Timing Limits

DQ[5] is set to a '1' when the program or erase time has exceeded a specified internal pulse count limit. This is a failure condition that indicates that the program or erase cycle was not successfully completed. DQ[5] status is valid only while DQ[7] or DQ[6] indicate that the Automatic Algorithm is in progress.

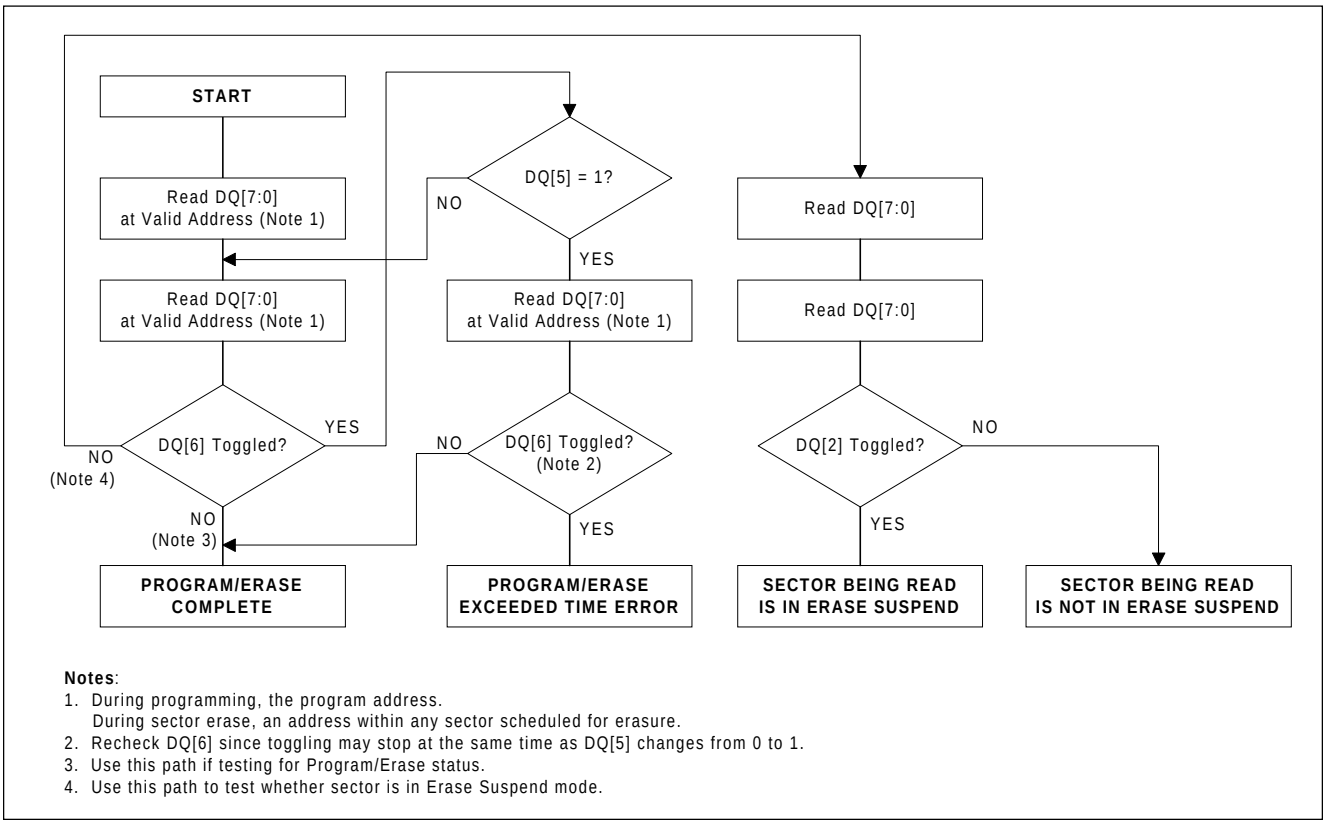
The DQ[5] failure condition will also be signaled if the host tries to program a '1' to a location that is previously programmed to '0', since only an erase operation can change a '0' to a '1'.

For both of these conditions, the host must issue a Reset command to return the device to the Read mode.

DQ[3] - Sector Erase Timer

After writing a Sector Erase command sequence, the host may read DQ[3] to determine whether or not an erase operation has begun. When the sector erase time-out expires and the sector erase operation commences, DQ[3] switches from a '0' to a '1'. Refer to the "Sector Erase Command" section for additional information. Note that the sector erase timer does not apply to the Chip Erase command.

After the initial Sector Erase command sequence is issued, the system should read the status on DQ[7] (Data# Polling) or DQ[6] (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ[3]. If DQ[3] is a '1', the internally controlled erase cycle has begun and all further sector erase data cycles or commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ[3] is a '0', the device will accept a sector erase data cycle to mark an additional sector for erasure. To ensure that the data cycles have been accepted, the system software should check the status of DQ[3] prior to and following each subsequent sector erase data cycle. If DQ[3] is high on the second status check, the last data cycle might not have been accepted.



Notes:
1. During programming, the program address.
   During sector erase, an address within any sector scheduled for erasure.
2. Recheck DQ[6] since toggling may stop at the same time as DQ[5] changes from 0 to 1.
3. Use this path if testing for Program/Erase status.
4. Use this path to test whether sector is in Erase Suspend mode.

Figure 8. Toggle Bit I and II Test Algorithm

HARDWARE DATA PROTECTION

The HY29DL16x provides several methods of protection to prevent accidental erasure or programming which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise. These methods are described in the sections that follow.

Command Sequences

Commands that may alter array data require a sequence of cycles as described in Table 10. This provides data protection against inadvertent writes.

Low V_{cc} Write Inhibit

To protect data during V_{CC} power-up and power-down, the device does not accept write cycles when V_{CC} is less than V_{LKO} (typically 2.4 volts). The command register and all internal program/erase circuits are disabled, and the device resets to the Read mode. Writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by asserting any one of the following conditions: OE# = V_{IL} , CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the Read mode on power-up.

Sector Protection

Additional data protection is provided by the HY29DL16x’s sector protect features, described previously, which can be used to protect sensitive areas of the Flash array from accidental or unauthorized attempts to alter the data.

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	ºC
T_{BIAS}	Ambient Temperature with Power Applied	-55 to +125	ºC
V_{IN2}	Voltage on Pin with Respect to V_{SS}: V_{CC} [2] WP#/ACC [3] A[9], OE#, RESET# [3] All Other Pins [2]	 -0.5 to +4.0 -0.5 to +9.5 -0.5 to +12.5 -0.5 to (V_{CC} + 0.5)	 V V V V
I_{OS}	Output Short Circuit Current [4]	200	mA

Notes:
1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0V for periods of up to 20 ns. See Figure 9. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 10.
3. Minimum DC input voltage on pins WP#/ACC, A[9], OE#, and RESET# is -0.5 V. During voltage transitions, A[9], OE# and RESET# may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pins A[9], OE#, and RESET#] is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns. Maximum DC input voltage on pin WP#/ACC is +9.5 V which may overshoot to 12.0 V for periods up to 20 ns.
4. No more than one output at a time may be shorted to V_{SS}. Duration of the short circuit should be less than one second.

RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: Commercial Temperature Devices Industrial Temperature Devices	 0 to +70 -40 to +85	 ºC ºC
V_{CC}	Operating Supply Voltage	+2.7 to +3.6	V

Notes:
1. Recommended Operating Conditions define those limits between which the functionality of the device is guaranteed.

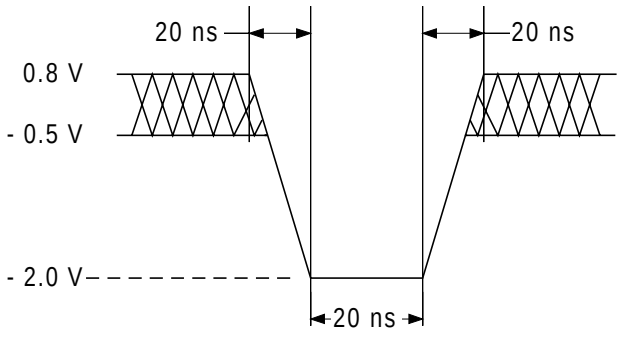


Figure 9. Maximum Undershoot Waveform

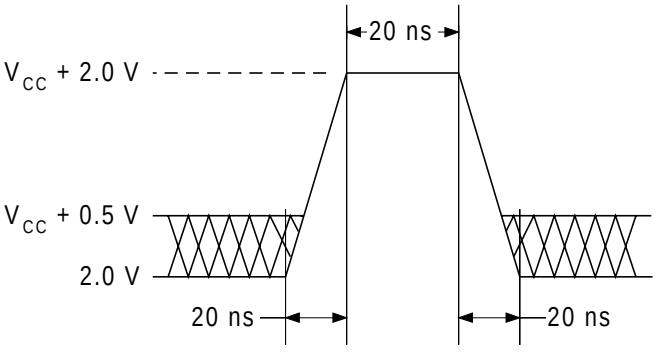


Figure 10. Maximum Overshoot Waveform

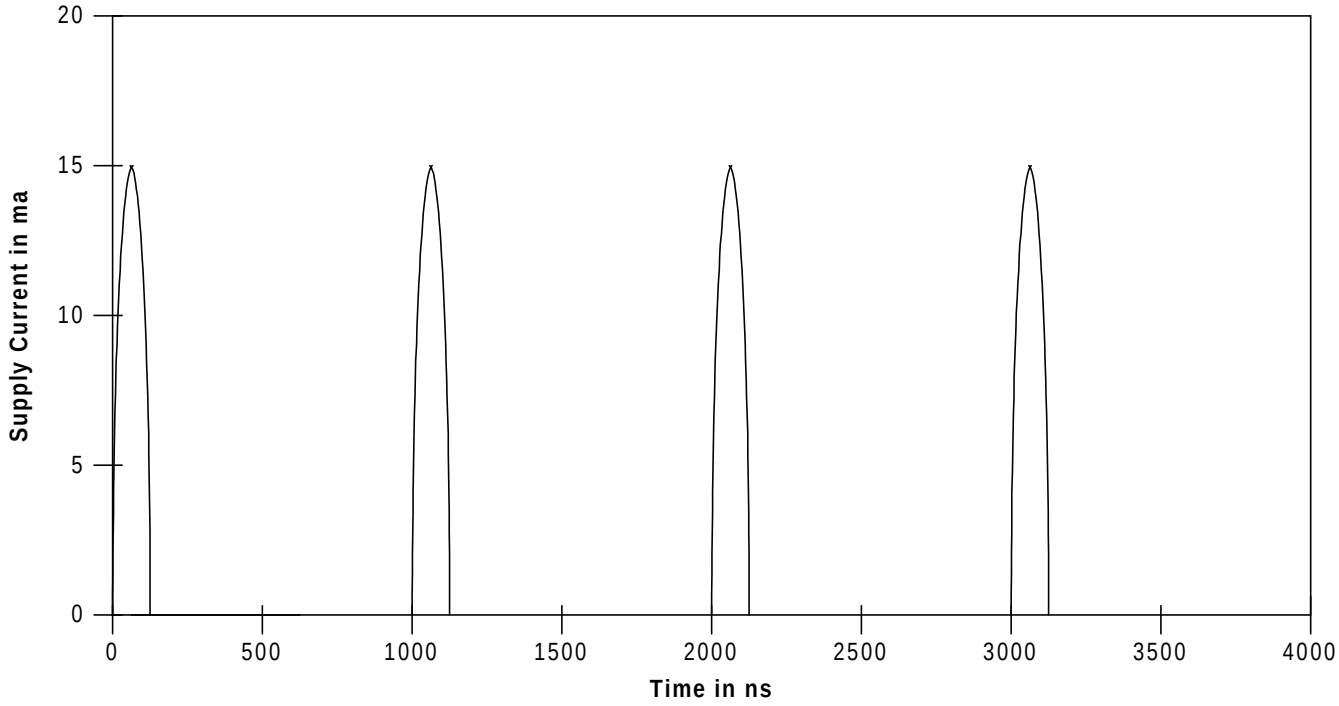
DC CHARACTERISTICS

Parameter	Description	Test Setup [2]		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}				±1.0	µA
I_{LIT}	A[9] Input Load Current	A[9] = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}				±1.0	µA
I_{CC1}	V_{CC} Active Read Current [1]	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		10	16	mA
			1 MHz		2	4	mA
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		10	16	mA
			1 MHz		2	4	mA
I_{CC2}	V_{CC} Active Read While Write (Program or Erase) Current [1]	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		21	45	mA
			1 MHz		16	34	mA
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		21	45	mA
			1 MHz		16	34	mA
I_{CC3}	V_{CC} Active Write Current [3, 4]	CE# = V_{IL}, OE# = V_{IH}			15	35	mA
I_{CC4}	V_{CC} CE# Controlled Deep Standby Current	CE# = V_{CC} ± 0.3 V, RESET# = V_{CC} ± 0.3 V			0.2	5	µA
I_{CC5}	V_{CC} RESET# Controlled Deep Standby Current	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC6}	Automatic Sleep Mode Current [5]	$V_{IH} = V_{CC}$ ± 0.3 V, $V_{IL} = V_{SS}$ ± 0.3 V			0.2	5	µA
I_{CC7}	V_{CC} CE# Controlled Normal Standby Current	CE# = RESET# = V_{IH}			50	300	µA
I_{CC8}	V_{CC} RESET# Controlled Normal Standby Current [2]	RESET# = V_{IL}			50	300	µA
I_{ACC}	Accelerated Program Current, Byte or Word Mode	CE# = V_{IL}, OE# = V_{IH}	V_{HH}		5	10	mA
			V_{CC}		15	30	mA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Electronic ID and Temporary Sector Unprotect	V_{CC} = 3.0V ± 10%		8.5		12.5	V
V_{HH}	Voltage for Program Acceleration	V_{CC} = 3.0V ± 10%		8.5		9.5	V
V_{OL1}	Output Low Voltage	$V_{CC} = V_{CC}$ Min, I_{OL} = 4.0 mA				0.45	V
V_{OH1}	Output High Voltage	$V_{CC} = V_{CC}$ Min, I_{OH} = -2.0 mA		0.85 x V_{CC}			V
V_{OH2}		$V_{CC} = V_{CC}$ Min, I_{OH} = -100 µA		V_{CC} - 0.4			V
V_{LKO}	Low V_{CC} Lockout Voltage [4]			2.3		2.5	V

Notes:
1. The I_{CC} current is listed is typically less than 2 mA/MHz with OE# at V_{IH}. Typical V_{CC} is 3.0 V.
2. All parameters are tested with $V_{CC} = V_{CC}$ Max unless otherwise noted.
3. I_{CC} active while the Automatic Erase or Automatic Program algorithm is in progress.
4. Not 100% tested.
5. Automatic sleep mode is enabled when addresses remain stable for t_{ACC} + 30 ns (typical).

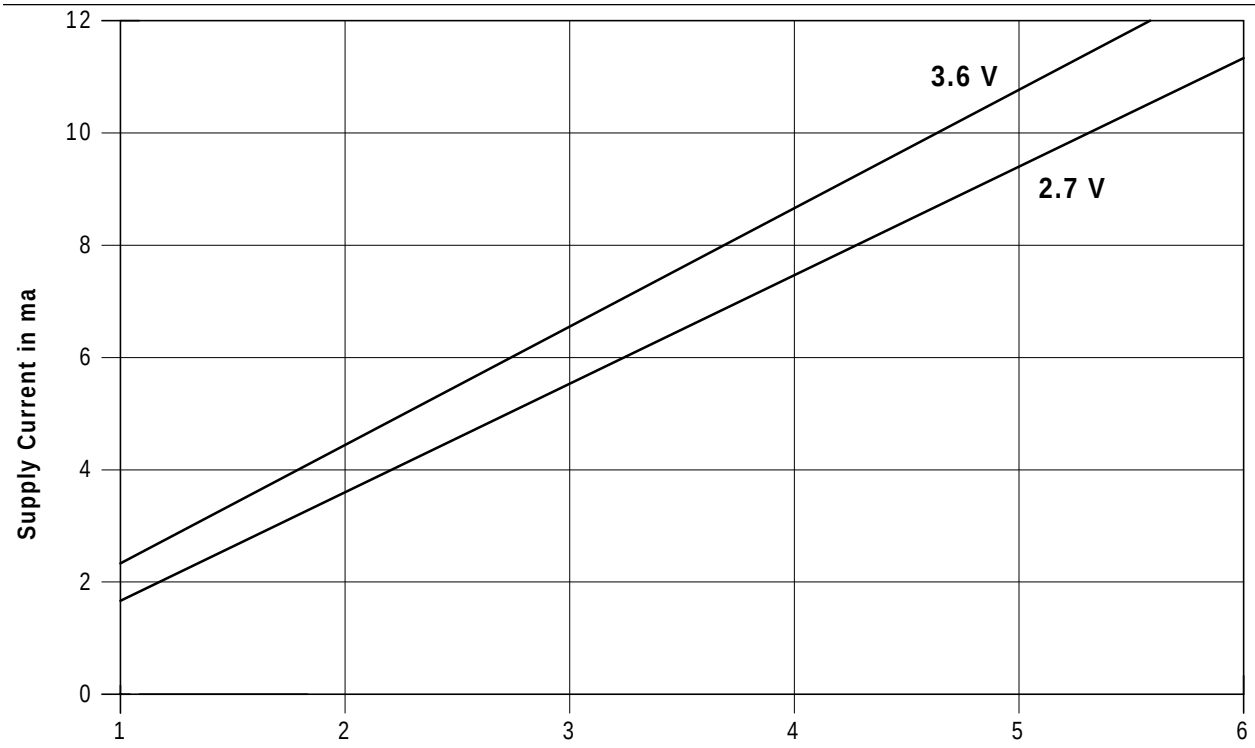
DC CHARACTERISTICS

Zero Power Flash



Note: Addresses are switching at 1 MHz.

Figure 11. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: T = 25 °C.

Figure 12. Typical I_{CC1} Current vs. Frequency

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Centerline is High Impedance State (High Z)

TEST CONDITIONS

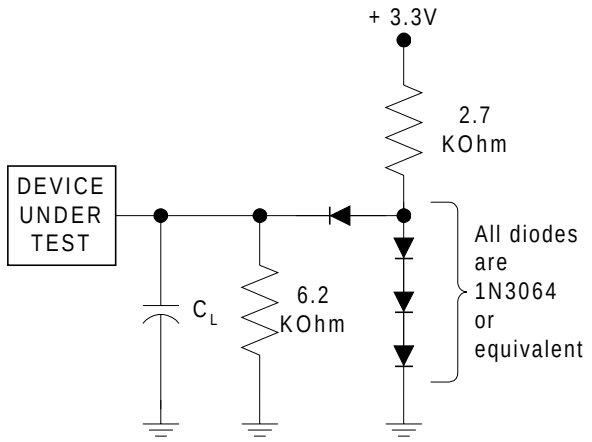


Figure 13. Test Setup

Table 17. Test Specifications

Test Condition	- 70 - 80	- 90 - 12	Unit
Output Load	Figure 13		
Output Load Capacitance (C_L)	30	100	pF
Input Rise and Fall Times	5		ns
Input Signal Low Level	0.0		V
Input Signal High Level	3.0		V
Input Timing Measurement Signal Level	1.5		V
Output Timing Measurement Signal Level	1.5		V

Note: Timing measurements are made at the reference levels specified above regardless of where the illustrations in the timing diagrams appear to indicate the measurement is made

Figure 14. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Option				Unit
JEDEC	Std					- 70	- 80	- 90	- 12	
t_{AVAV}	t_{RC}	Read Cycle Time [1]			Min	70	80	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	80	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	80	90	120	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z [1]			Max	30	30	40	50	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		CE# = V_{IL}	Max	25	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z [1]			Max	25	25	30	30	ns
	t_{OEH}	Output Enable Hold Time [1]	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First [1]			Min	0				ns

Notes:
1. Not 100% tested.

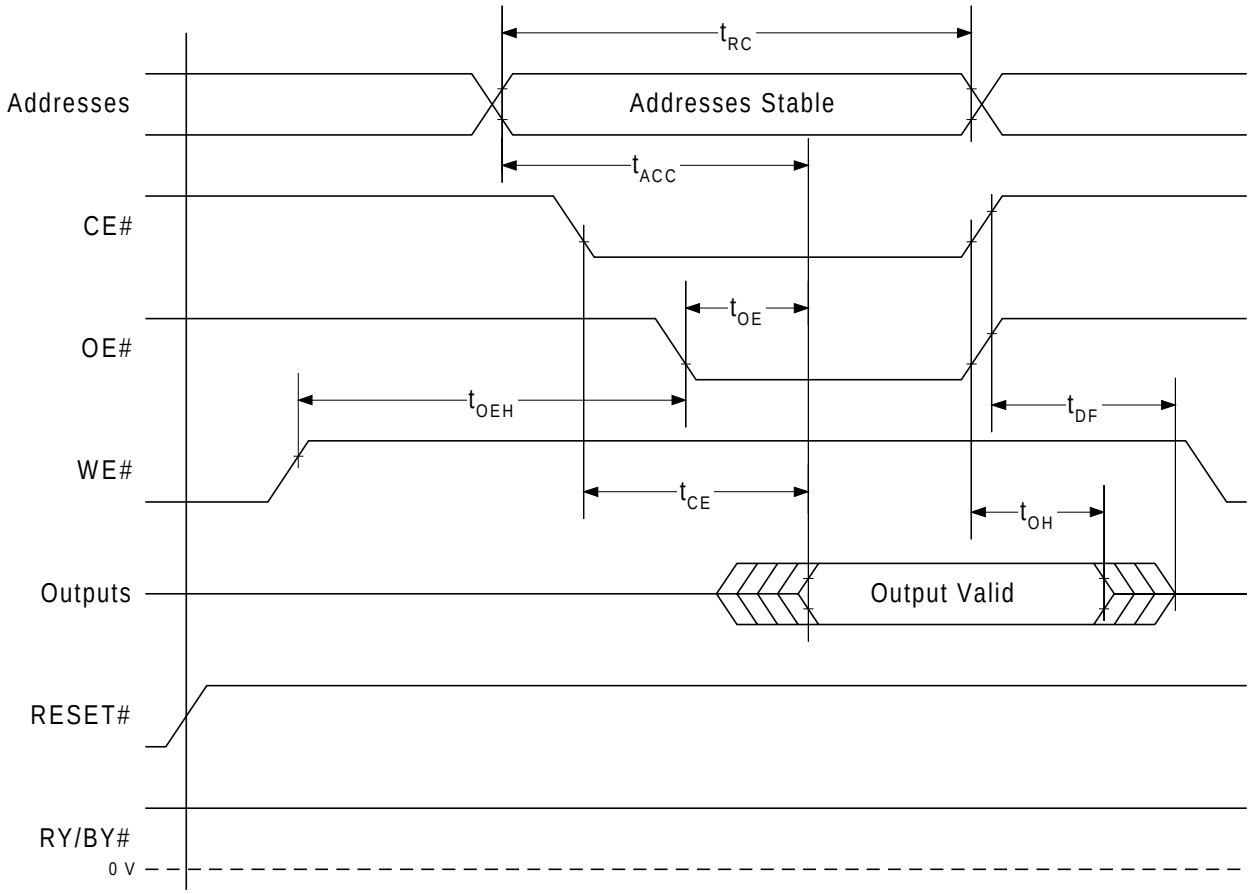


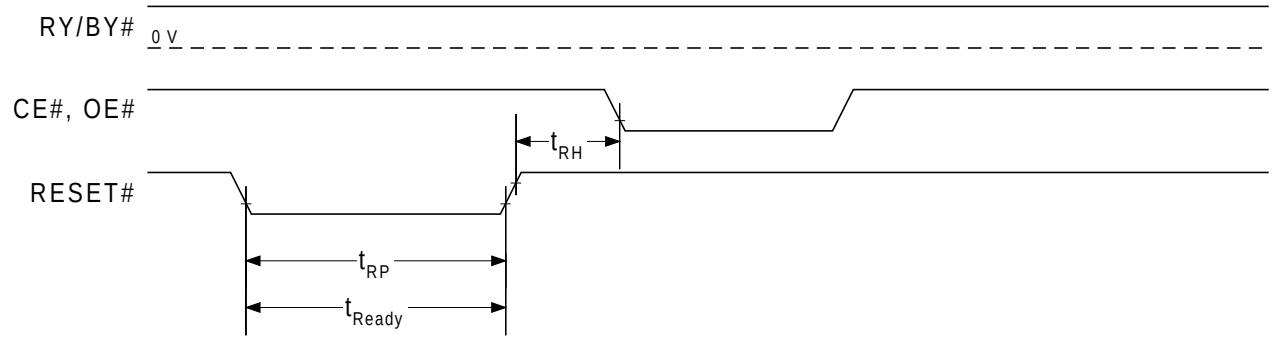
Figure 15. Read Operation Timings

AC CHARACTERISTICS

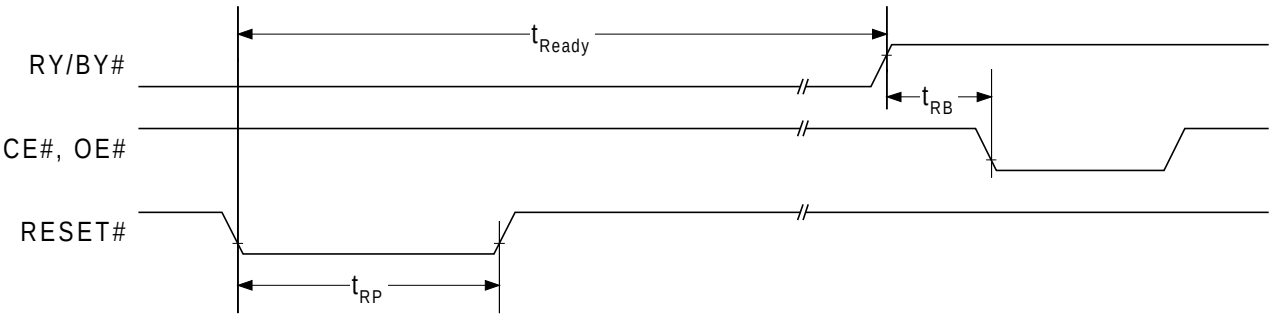
Hardware Reset (RESET#)

Parameter		Description	Test Setup		Speed Option				Unit
JEDEC	Std				- 70	- 80	- 90	- 12	
	t_{READY}	RESET# Pin Low (During Automatic Algorithms) to Read or Write [1]		Max	20				µs
	t_{READY}	RESET# Pin Low (NOT During Automatic Algorithms) to Read or Write[1]		Max	500				ns
	t_{RP}	RESET# Pulse Width		Min	500				ns
	t_{RH}	RESET# High Time Before Read [1]		Min	50				ns
	t_{RPD}	RESET# Low to Standby Mode		Max	20				µs
	t_{RB}	RY/BY# Recovery Time		Min	0				ns

Notes:
1. Not 100% tested.



Reset Timings NOT During Automatic Algorithms



Reset Timings During Automatic Algorithms

Figure 16. RESET# Timings

AC CHARACTERISTICS

Word/Byte Configuration (BYTE#)

Parameter		Description		Speed Option				Unit
JEDEC	Std			- 70	- 80	- 90	- 12	
	t_{ELFL}	CE# to BYTE# Switching Low	Max	5				ns
	t_{ELFH}	CE# to BYTE# Switching High	Max	5				ns
	t_{FLQZ}	BYTE# Switching Low to Output High-Z	Max	25	25	30	30	ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	70	80	90	120	ns

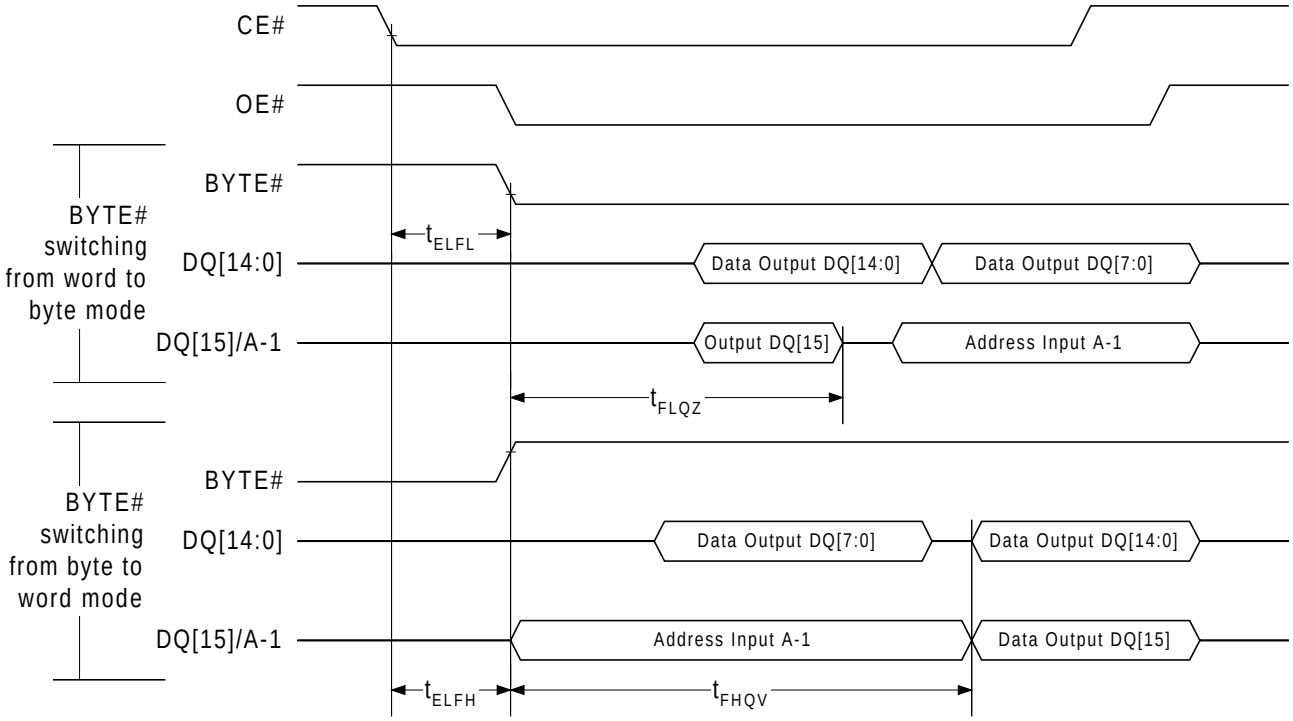
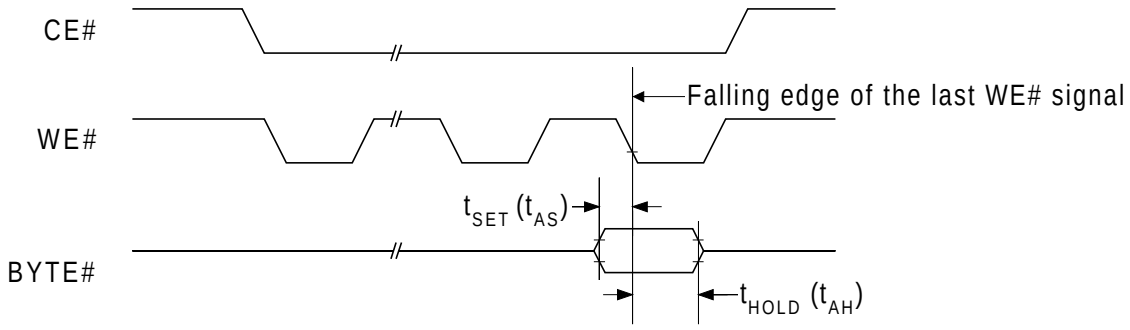


Figure 17. BYTE# Timings for Read Operations



Note: Refer to the Program/Erase Operations table for t_{AS} and t_{AH} specifications.

Figure 18. BYTE# Timings for Write Operations

AC CHARACTERISTICS

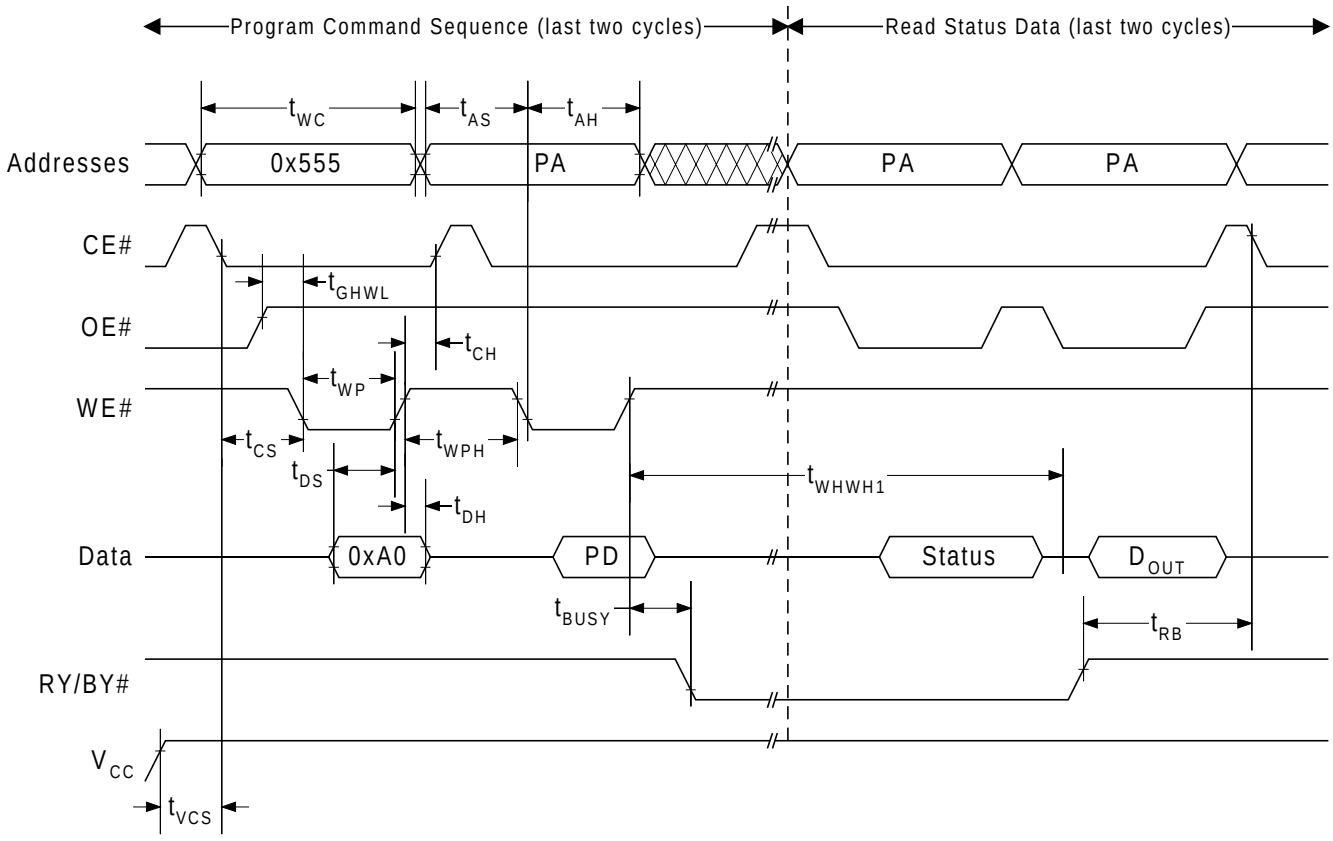
Program and Erase Operations

Parameter		Description			Speed Option				Unit
JEDEC	Std				- 70	- 80	- 90	- 12	
t_{AVAV}	t_{WC}	Write Cycle Time [1]		Min	70	80	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
	t_{AST}	Address Setup Time for Toggle Bit Test		Min	15				ns
	t_{AHT}	Address Hold Time for Toggle Bit Test		Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
	t_{OEPH}	OE# High Time for Toggle Bit Test		Min	20				ns
	t_{CEPH}	CE# High Time for Toggle Bit Test		Min	20				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30	30	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30				ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation [1, 2, 3]	Byte Mode	Typ	10				µs
				Max	150				µs
			Word Mode	Typ	15				µs
				Max	210				µs
		Accelerated Programming Operation [1, 2, 3] (WP#/ACC = V_{HH})	Byte or Word Mode	Typ	10				µs
				Max	150				µs
		Chip Programming Operation [1, 2, 3, 5]	Byte Mode	Typ	20				sec
				Max	60				sec
			Word Mode	Typ	16				sec
				Max	48				sec
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation [1, 2, 4]		Typ	0.5				sec
				Max	7.5				sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation [1, 2, 4]		Typ	16				sec
		Erase and Program Cycle Endurance [1]		Typ	1,000,000				cycles
				Min	100,000				cycles
	t_{VCS}	V_{CC} Setup Time [1]		Min	50				µs
	t_{RB}	Recovery Time from RY/BY#		Min	0				ns
	t_{BUSY}	WE# High to RY/BY# Delay		Min	90				ns

Notes:

1. Not 100% tested.
2. Typical program and erase times assume the following conditions: 25 °C, V_{CC} = 2.0 volts, 100,000 cycles. In addition, programming typicals assume a checkerboard pattern. Maximum program and erase times are under worst case conditions of 90 °C, V_{CC} = 1.8 volts, 100,000 cycles.
3. Excludes system-level overhead, which is the time required to execute the four-bus-cycle sequence for the Program command. See Table 10 for further information on command sequences.
4. Excludes 0x00 programming prior to erasure. In the preprogramming step of the Automatic Erase algorithm, all bytes are programmed to 0x00 before erasure.
5. The typical chip programming time is considerably less than the maximum chip programming time listed since most bytes/words program faster than the maximum programming times specified. The device sets DQ[5] = 1 only If the maximum byte/word program time specified is exceeded. See Write Operation Status section for additional information.

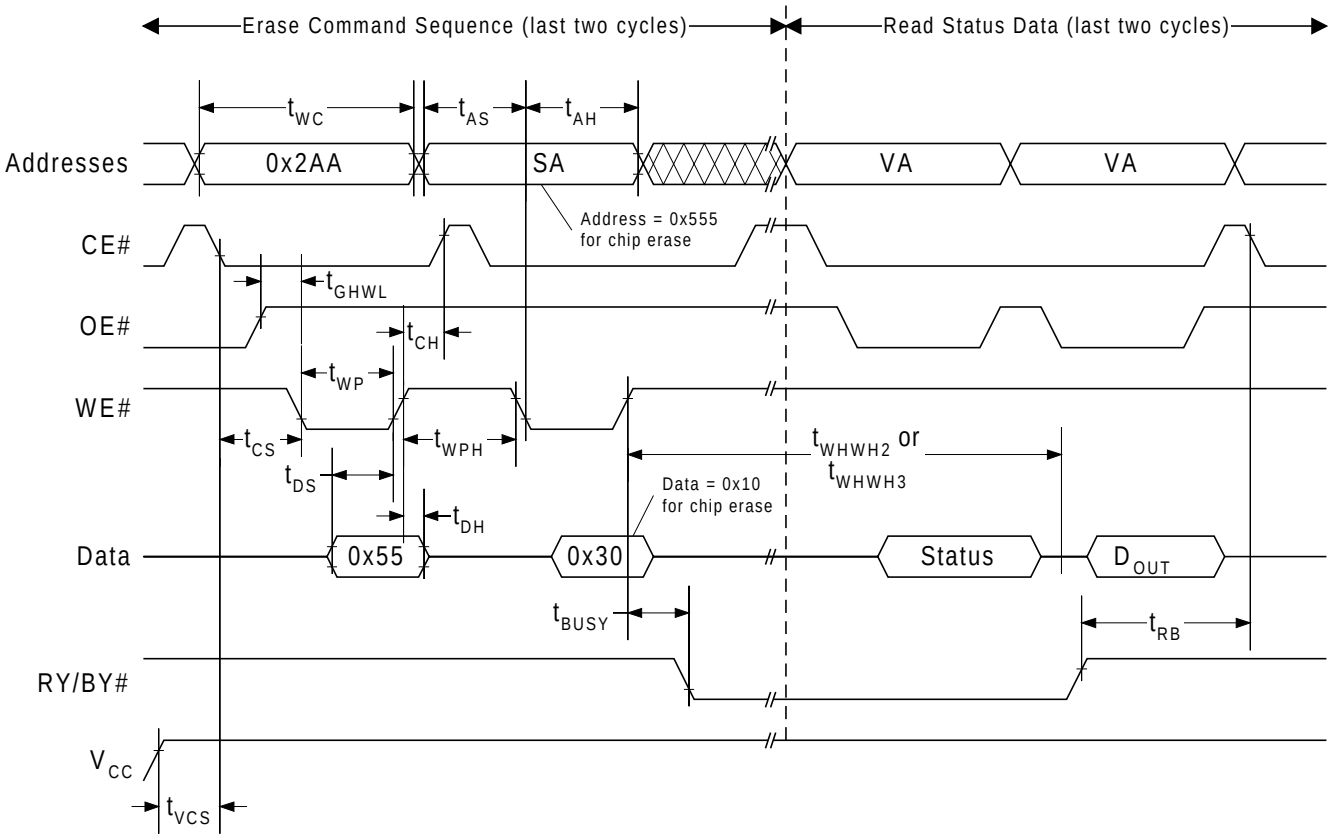
AC CHARACTERISTICS



Notes:
1. PA = Program Address, PD = Program Data, D_{OUT} is the true data at the program address.
2. Commands shown are for Word mode operation.
3. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 19. Program Operation Timings

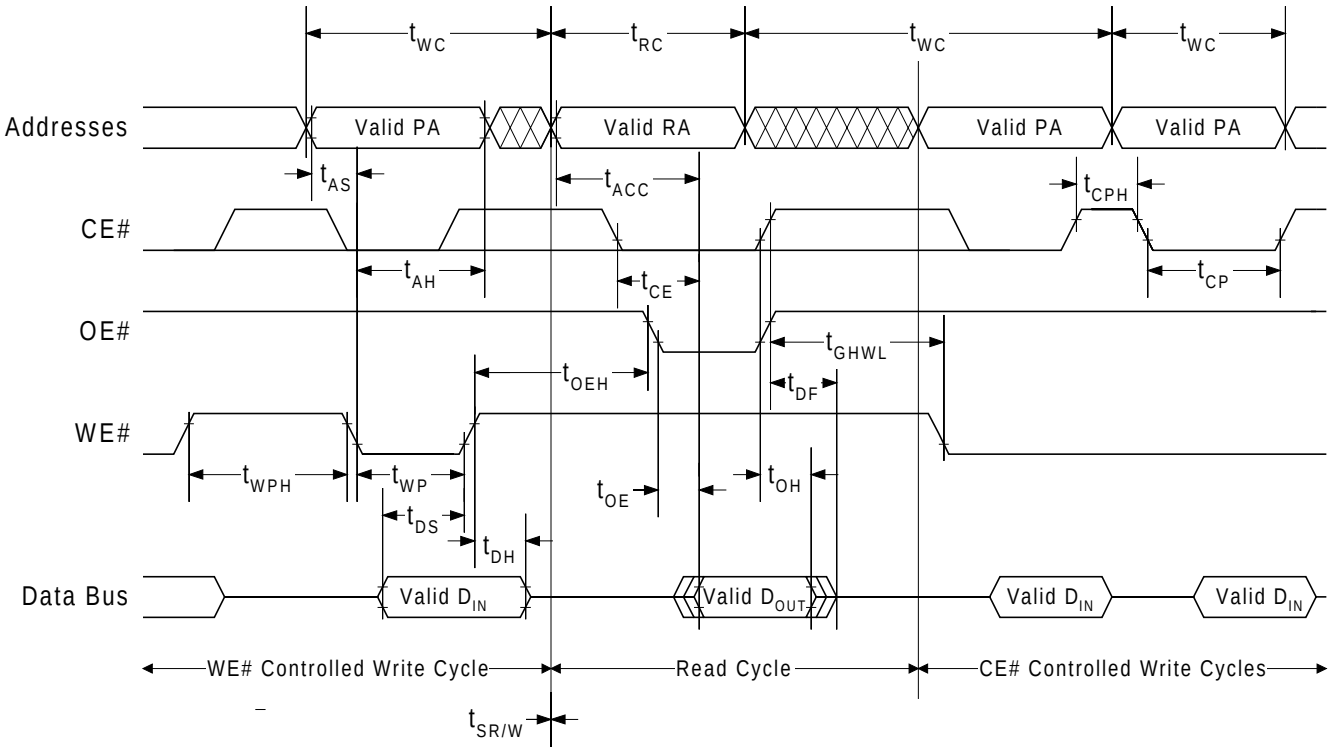
AC CHARACTERISTICS



Notes:
1. SA =Sector Address (for sector erase), VA = Valid Address for reading status data (see Write Operation Status section), D_{OUT} is the true data at the read address. (0xFF after an erase operation).
2. Commands shown are for Word mode operation.
3. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 20. Sector/Chip Erase Operation Timings

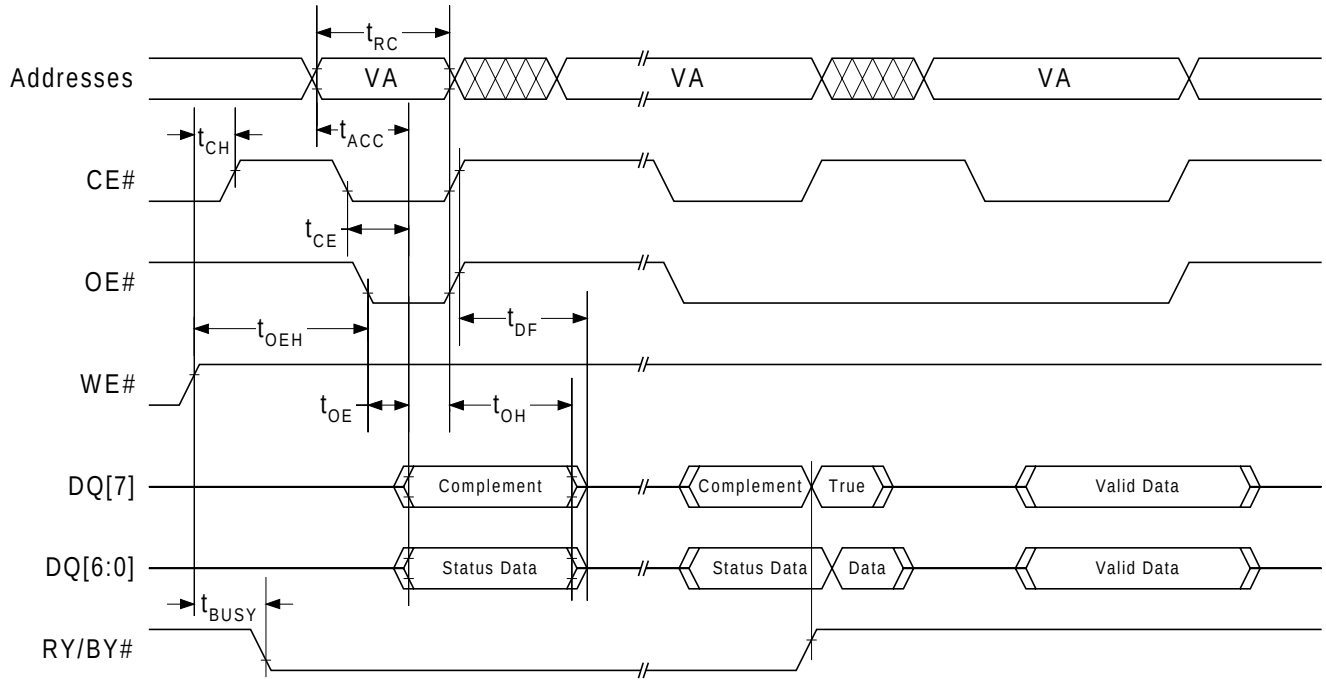
AC CHARACTERISTICS



Notes:
1. PA = Program Address, RA = Read Address, D_{OUT} is the data at the read address.

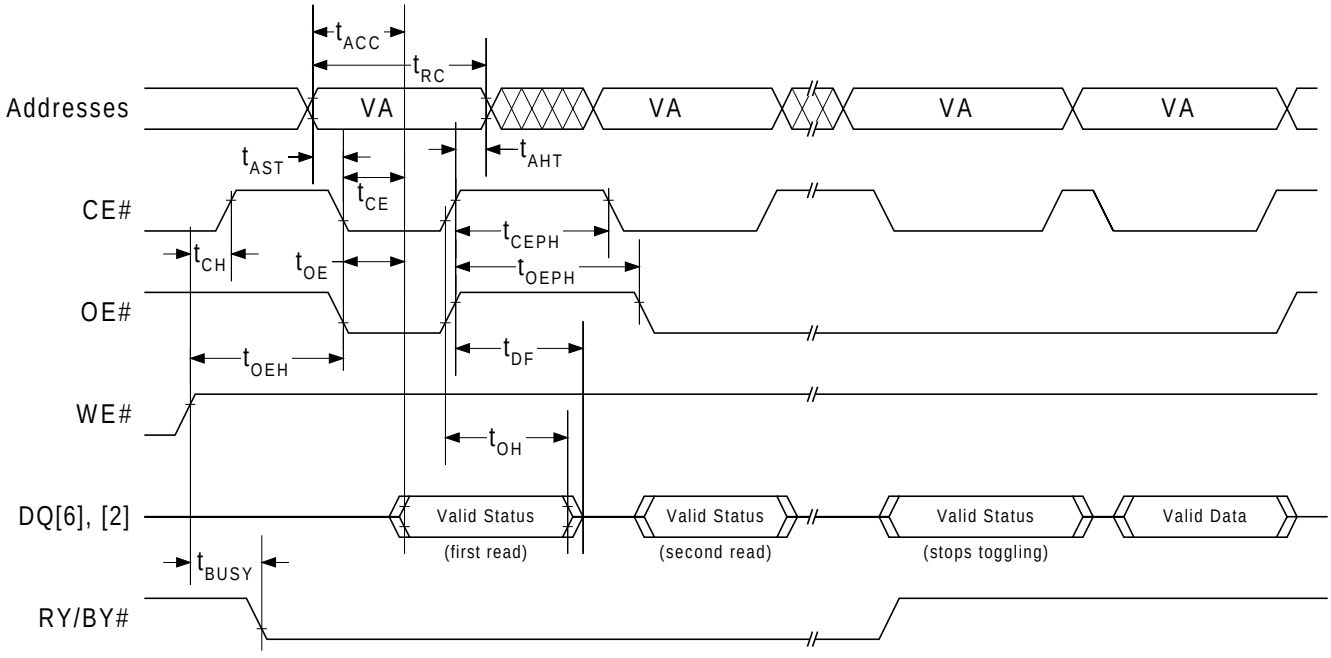
Figure 21. Back-to-Back Read/Write Operation Timings

AC CHARACTERISTICS



Notes:
1. VA = Valid Address for reading Data# Polling status data (see Write Operation Status section).
2. Illustration shows first status cycle after command sequence, last status read cycle and array data read cycle.

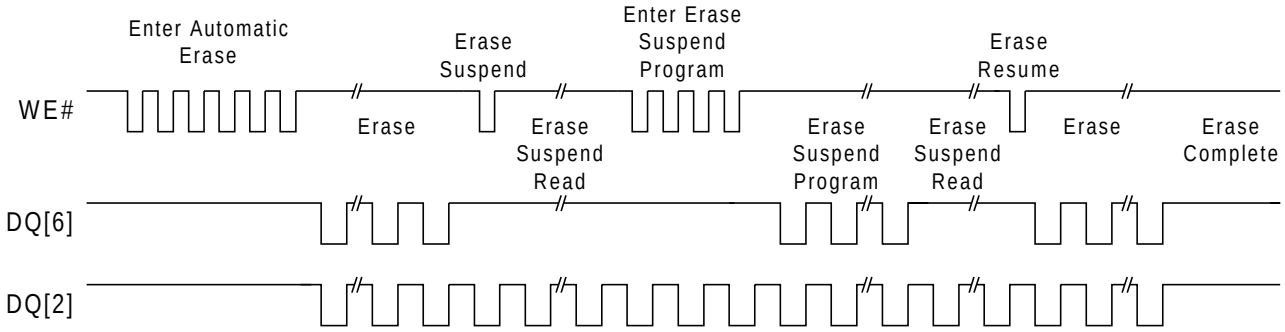
Figure 22. Data# Polling Timings (During Automatic Algorithms)



Notes:
1. VA = Valid Address for reading Toggle Bits (DQ[2], DQ[6]) status data (see Write Operation Status section).
2. Illustration shows first two status read cycles after command sequence, last status read cycle and array data read cycle.

Figure 23. Toggle Polling Timings (During Automatic Algorithms)

AC CHARACTERISTICS



Notes:
1. The system may use CE# or OE# to toggle DQ[2] and DQ[6]. DQ[2] toggles only when read at an address within an erase-suspended sector.

Figure 24. DQ[2] and DQ[6] Operation

Sector Group Protect/Unprotect, Temporary Sector Unprotect, Accelerated Program

Parameter		Description		Speed Option				Unit
JEDEC	Std			- 70	- 80	- 90	- 12	
	t_{VIDR}	V_{ID} Transition Time for Temporary Sector Unprotect [1]	Min	500				ns
	t_{VHH}	V_{HH} Transition Time for Accelerated Programming [1]	Min	250				ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4				µs
	t_{RRB}	RESET# Hold Time for Temporary Sector Unprotect	Min	4				µs
	t_{VRST}	RESET# Setup Time for Sector Group Protect and Unprotect	Min	1				µs
	t_{PROT}	Sector Group Protect Time	Max	150				µs
	t_{UNPR}	Sector Unprotect Time	Max	15				ms
	t_{VERW}	Protect/Unprotect Verify Wait Time	Min	1				µs

Notes:
1. Not 100% tested.

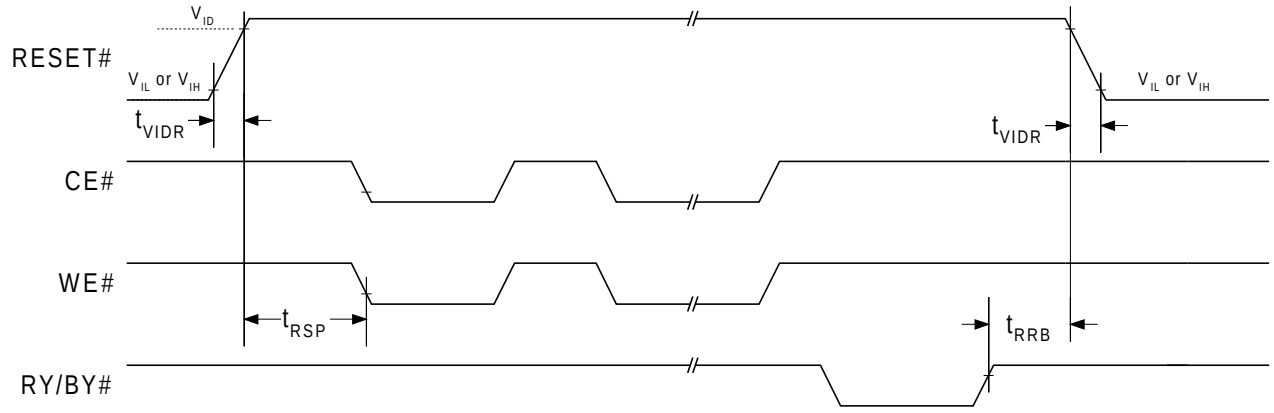


Figure 25. Temporary Sector Unprotect Timings

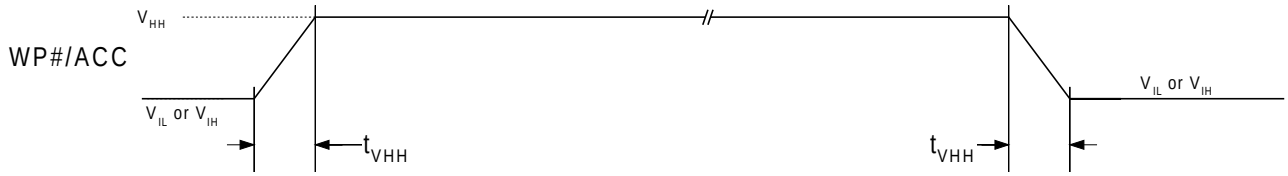
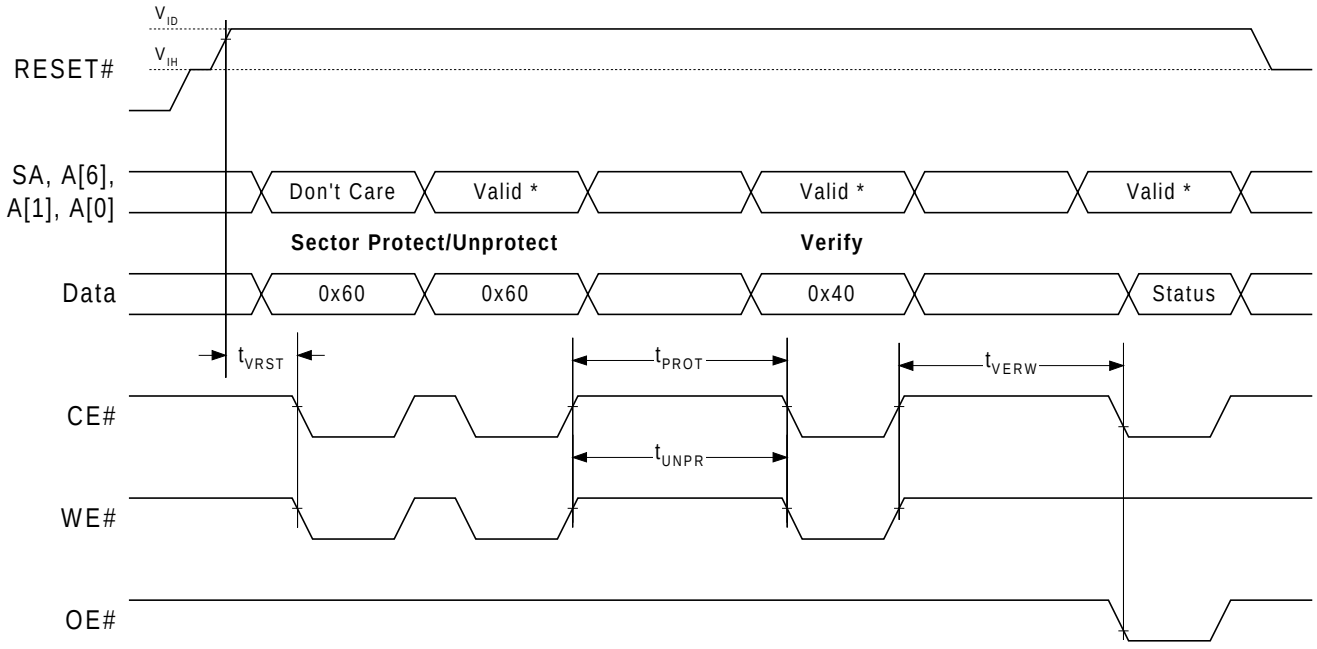


Figure 26. Accelerated Programming Timings



Note: For Sector Group Protect, A[6] = 0, A[1] = 1, A[0] = 0. For Sector Unprotect, A[6] = 1, A[1] = 1, A[0] = 0.

Figure 27. Sector Group Protect and Unprotect Timings

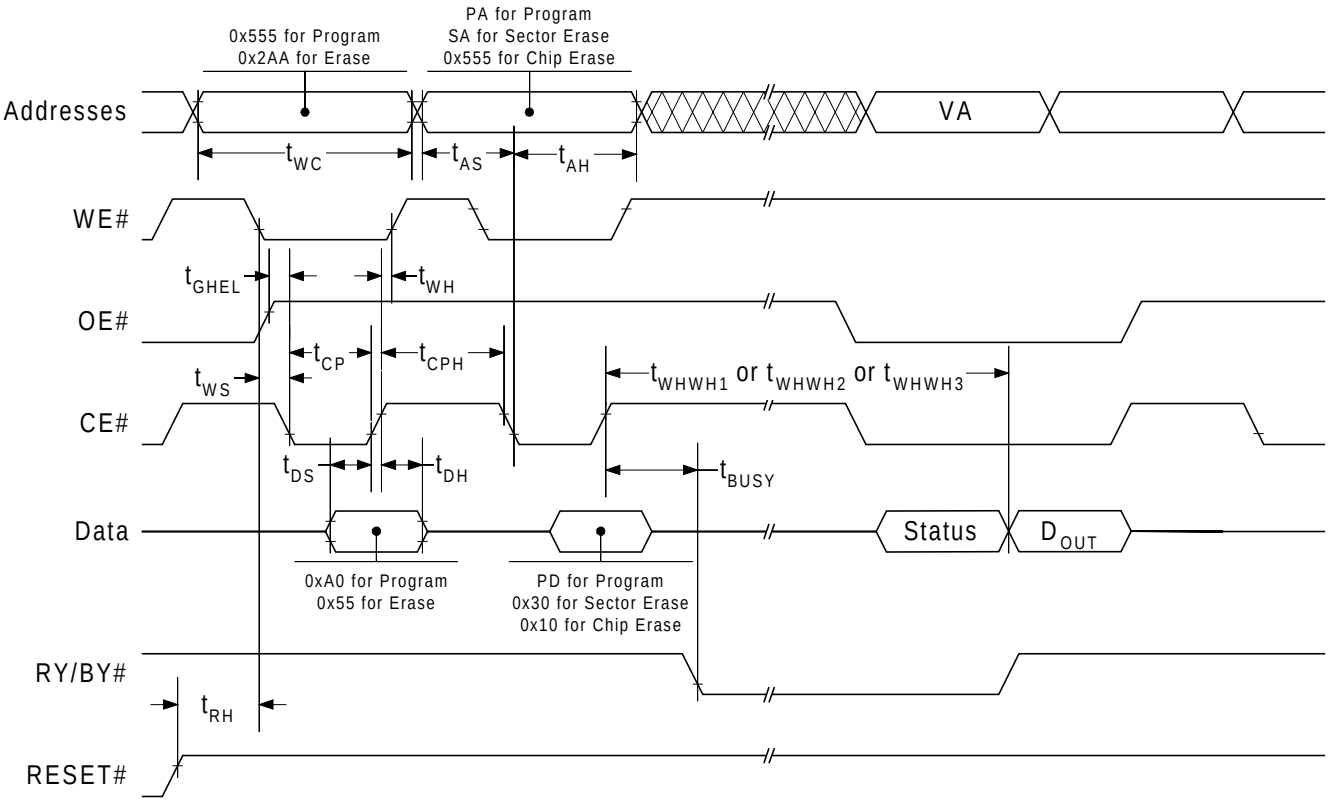
AC CHARACTERISTICS

Alternate CE# Controlled Erase/Program Operations

Parameter		Description			Speed Option				Unit
JEDEC	Std				- 70	- 80	- 90	- 12	
t_{AVAV}	t_{WC}	Write Cycle Time [1]		Min	70	80	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	30	30	45	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation [1, 2, 3]	Byte Mode	Typ	10				µs
				Max	150				µs
			Word Mode	Typ	15				µs
				Max	210				µs
		Accelerated Programming Operation [1, 2, 3] (WP#/ACC = V_{HH})	Byte or Word Mode	Typ	10				µs
				Max	150				µs
		Chip Programming Operation [1, 2, 3, 5]	Byte Mode	Typ	20				sec
				Max	60				sec
			Word Mode	Typ	16				sec
				Max	48				sec
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation [1, 2, 4]		Typ	0.5				sec
				Max	7.5				sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation [1, 2, 4]		Typ	16				sec
		Erase and Program Cycle Endurance [1]		Typ	1,000,000				cycles
				Min	100,000				cycles
	t_{BUSY}	CE# to RY/BY# Delay		Min	90				ns

Notes:
1. Not 100% tested.
2. Typical program and erase times assume the following conditions: 25 °C, V_{CC} = 3.0 volts, 100,000 cycles. In addition, programming typicals assume a checkerboard pattern. Maximum program and erase times are under worst case conditions of 90 °C, V_{CC} = 2.7 volts, 100,000 cycles.
3. Excludes system-level overhead, which is the time required to execute the four-bus-cycle sequence for the Program command. See Table 10 for further information on command sequences.
4. Excludes 0x00 programming prior to erasure. In the preprogramming step of the Automatic Erase algorithm, all bytes are programmed to 0x00 before erasure.
5. The typical chip programming time is considerably less than the maximum chip programming time listed since most bytes program faster than the maximum programming times specified. The device sets DQ[5] = 1 only If the maximum byte program time specified is exceeded. See Write Operation Status section for additional information.

AC CHARACTERISTICS



Notes:

1. PA = program address, PD = program data, VA = Valid Address for reading program or erase status (see Write Operation Status section), D_{OUT} = array data read at VA.
2. Illustration shows the last two cycles of the program or erase command sequence and the last status read cycle.
3. Word mode addressing shown.
4. RESET# shown only to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

Figure 28. Alternate CE# Controlled Write Operation Timings

Latchup Characteristics

Description	Minimum	Maximum	Unit
Input voltage with respect to V_{SS} on all pins except I/O pins (including A[9], OE# and RESET#)	- 1.0	12.5	V
Input voltage with respect to V_{SS} on all I/O pins	- 1.0	V_{CC} + 1.0	V
V_{CC} Current	- 100	100	mA

Notes:
1. Includes all pins except V_{CC}. Test conditions: V_{CC} = 1.8 V, one pin at a time.

TSOP Pin Capacitance

Symbol	Parameter	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions: T_A = 25 ºC, f = 1.0 MHz.

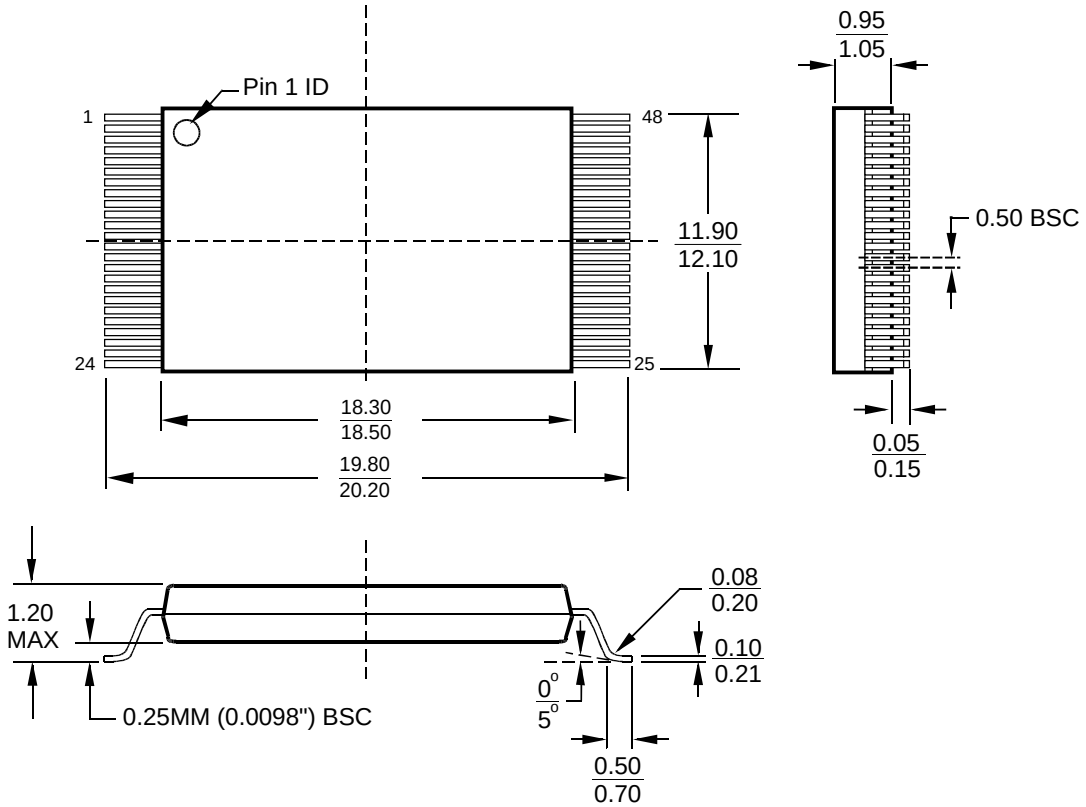
Data Retention

Parameter	Test Conditions	Minimum	Unit
Minimum Pattern Data Retention Time	150 ºC	10	Years
	125 ºC	20	Years

PACKAGE DRAWINGS

Physical Dimensions

TSOP48 - 48-pin Thin Small Outline Package (measurements in millimeters)

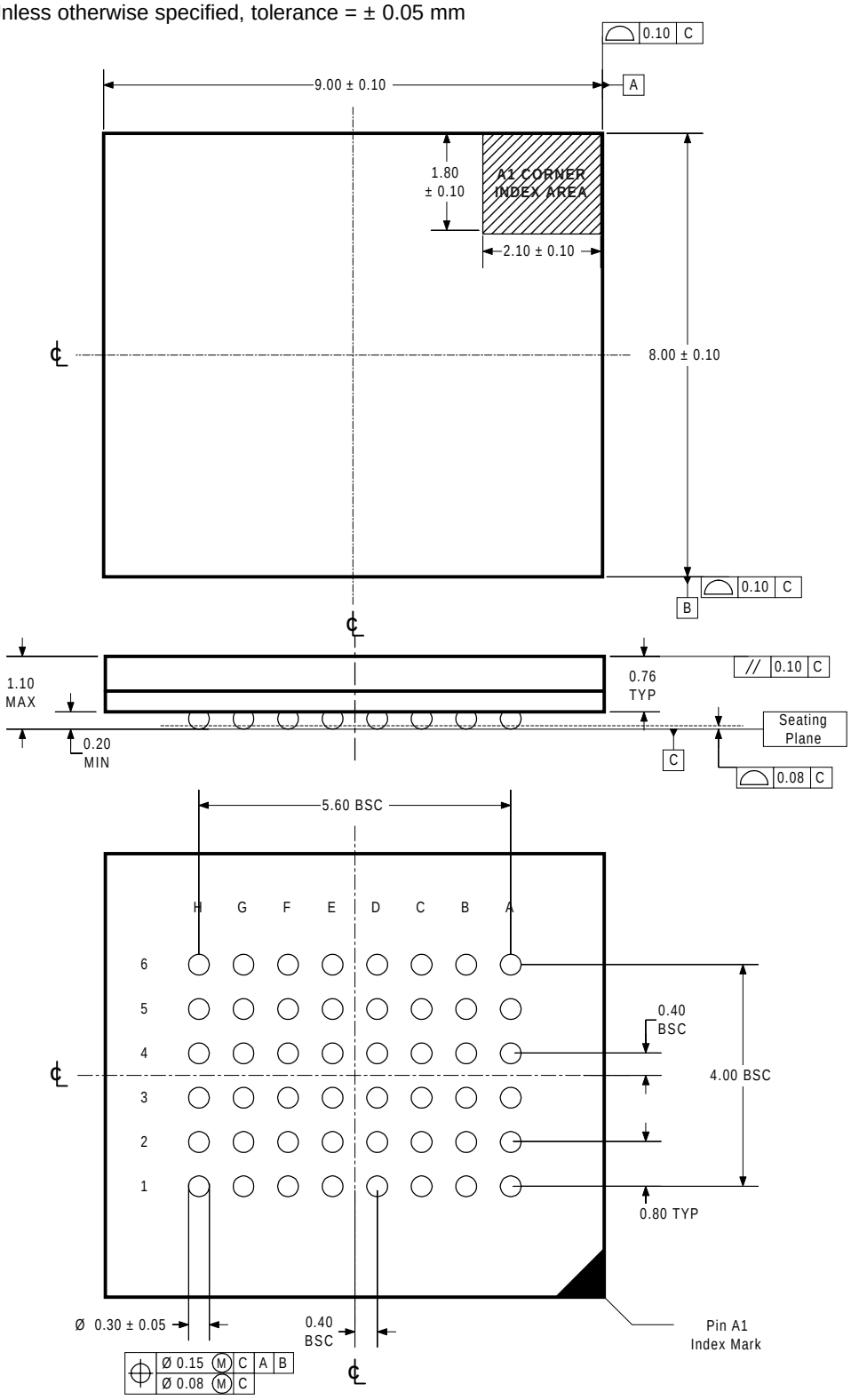


PACKAGE DRAWINGS

Physical Dimensions

FBGA48 - 48-Ball Fine-Pitch Ball Grid Array, 8 x 9 mm (measurements in millimeters)

Note: Unless otherwise specified, tolerance = ± 0.05 mm



ORDERING INFORMATION

Hynix products are available in several speeds, packages and operating temperature ranges. The ordering part number is formed by combining a number of fields, as indicated below. Refer to the 'Valid Combinations' table, which lists the configurations that are planned to be supported in volume. Please contact your local Hynix representative or distributor to confirm current availability of specific configurations and to determine if additional configurations have been released.

HY29DL16x X X - X X X

SPECIAL INSTRUCTIONS

TEMPERATURE RANGE

Blank = Commercial (0 to +70 °C)
I = Industrial (-40 to +85 °C)

SPEED OPTION

70 = 70 ns
80 = 80 ns
90 = 90 ns
12 = 120 ns

PACKAGE TYPE

T = 48-Pin Thin Small Outline Package (TSOP)
F = 48-Ball Fine-Pitch Ball Grid Array (FBGA), 8 x 9 mm

BOOT BLOCK LOCATION

T = Top Boot Block Option
B = Bottom Boot Block Option

DEVICE NUMBER

HY29DL162 = 16 Megabit (2M x 8/1M x 16) CMOS 3 Volt-Only Sector Erase Flash Memory with 2Mb/14Mb Bank Split
HY29DL163 = 16 Megabit (2M x 8/1M x 16) CMOS 3 Volt-Only Sector Erase Flash Memory with 4Mb/12Mb Bank Split

VALID COMBINATIONS

	Package and Speed							
	FBGA				TSOP			
Temperature	**70 ns**	**80 ns**	**90 ns**	**120ns**	**70 ns**	**80 ns**	**90 ns**	**120ns**
Commercial	F-70	F-80	F-90	F-12	T-70	T-80	T-90	T-12
Industrial	F-70I	F-80I	F-90I	F-12I	T-70I	T-80I	T-90I	T-12I

Note:
1. The complete part number is formed by appending the suffix shown in the table to the Device Number. For example, the part number for a 120 ns, Industrial temperature range, 2Mb/14Mb bank-split device in the TSOP package with the top boot block option is *HY29DL162TT-12I*.
2. Please contact your local Hyundai representative or distributor for current product availability.

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Revision Record

Rev.	Date	Details
1.0	5/00	Original issue.
1.1	7/00	Corrected description of CFI Query and Reset commands in CFI mode description section. Minor typographical corrections.
1.2	4/01	Change to Hynix format. Removed 'BA' as requirement for several operations in Table 6 and corrected description of Electronic ID Operation (High Voltage Method). Added Bank Address to CFI Query command and changed operational description in CFI section. Removed high voltage sector group protect/unprotect method and all references to such.
1.3	6/01	Changed program and erase parameter values. Corrected error in CFI Table 13.

Memory Sales and Marketing Division
Hynix Semiconductor Inc.
10 Fl., Hynix Youngdong Building
89, Daechi-dong
Kangnam-gu
Seoul, Korea

Telephone: +82-2-580-5000
Fax: +82-2-3459-3990

http://www.hynix.com

Flash Memory Business Unit
Hynix Semiconductor America Inc.
3101 North First Street
San Jose, CA 95134
USA

Telephone: (408) 232-8800
Fax: (408) 232-8805

http://www.us.hynix.com