DRAM MODULE

MT9LD(T)872(F)X, MT18LD(T)1672(F)(D)X,
MT36LD(T)3272(C)(F)X

For the latest data sheet, please refer to the Micron Web site:
www.micronsemi.com/datasheets/datasheet.html

FEATURES

- JEDEC-standard ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 64MB (8 Meg x 72), 128MB (16 Meg x 72), and 256MB (32 Meg x 72)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs, and clocks are LVTTL-compatible
- All inputs are buffered except RAS#
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- Extended Data-Out (EDO) PAGE MODE access cycle

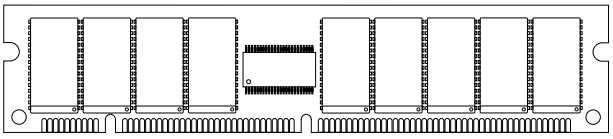
OPTIONS — MARKING

- Components
  - SOJ — D
  - TSOP — DT
- Package
  - 168-pin DIMM (gold) — G
- Refresh Addressing
  - 4,096 (4K) rows — Blank
  - 8,192 (8K) rows — F
- Module Height
  - Low profile, 1.65" (256MB only) — C
  - Low profile, 1.25" (128MB only) — D
- Timing
  - 50ns access — -5
  - 60ns access — -6
- Access Cycle
  - EDO PAGE MODE — X

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-5	84ns	50ns	20ns	30ns	18ns	8ns
-6	104ns	60ns	25ns	35ns	20ns	10ns

Front View (128MB) 168-PIN DIMM



PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	OE2#	86	DQ36	128	RFU
3	DQ1	45	RAS2#	87	DQ37	129	NC/RAS3#*
4	DQ2	46	CAS4#	88	DQ38	130	NC/CAS5#*
5	DQ3	47	RFU	89	DQ39	131	RFU
6	VDD	48	WE2#	90	VDD	132	PDE#
7	DQ4	49	VDD	91	DQ40	133	VDD
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	VDD	101	DQ49	143	VDD
18	VDD	60	DQ24	102	VDD	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	VSS	65	DQ25	107	VSS	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	VDD	68	VSS	110	VDD	152	VSS
27	WE0#	69	DQ28	111	RFU	153	DQ64
28	CAS0#	70	DQ29	112	NC/CAS1#*	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	RAS0#	72	DQ31	114	NC/RAS1#*	156	DQ67
31	OE0#	73	VDD	115	RFU	157	VDD
32	VSS	74	DQ32	116	VSS	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	A12	81	PD5	123	NC (A13)	165	PD6
40	VDD	82	PD7	124	VDD	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	VDD	126	B0	168	VDD

*256MB version only

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

PART NUMBER	CONFIGURATION	REFRESH ADDRESSING
MT9LD872G-x X	8 Meg x 72 ECC	4K
MT9LDT872G-x X	8 Meg x 72 ECC	4K
MT9LD872FG-x X	8 Meg x 72 ECC	8K
MT9LDT872FG-x X	8 Meg x 72 ECC	8K
MT18LD1672G-x X	16 Meg x 72 ECC	4K
MT18LDT1672G-x X	16 Meg x 72 ECC	4K
MT18LD1672FG-x X	16 Meg x 72 ECC	8K
MT18LDT1672FG-x X	16 Meg x 72 ECC	8K
MT18LDT1672FDG-x X	16 Meg x 72 ECC	8K
MT36LD3272G-x X	32 Meg x 72 ECC	4K
MT36LDT3272G-x X	32 Meg x 72 ECC	4K
MT36LD3272FG-x X	32 Meg x 72 ECC	8K
MT36LDT3272FG-x X	32 Meg x 72 ECC	8K
MT36LD3272CG-x X	32 Meg x 72 ECC	4K
MT36LD3272CFG-x X	32 Meg x 72 ECC	8K

x = speed

GENERAL DESCRIPTION

The Micron® MT9LD(T)872(F)X, MT18LD(T)1672(F)X, and MT36LD(T)3272(F)X are randomly accessed 64MB, 128MB, and 256MB memories organized in a x72 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the address bits. First, the row address is latched by the RAS# signal, then the column address by CAS#. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. EARLY WRITE occurs when WE# goes LOW prior to CAS# going LOW, and the output pins remain open (High-Z) until the next CAS# cycle.

EDO PAGE MODE

EDO PAGE MODE is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

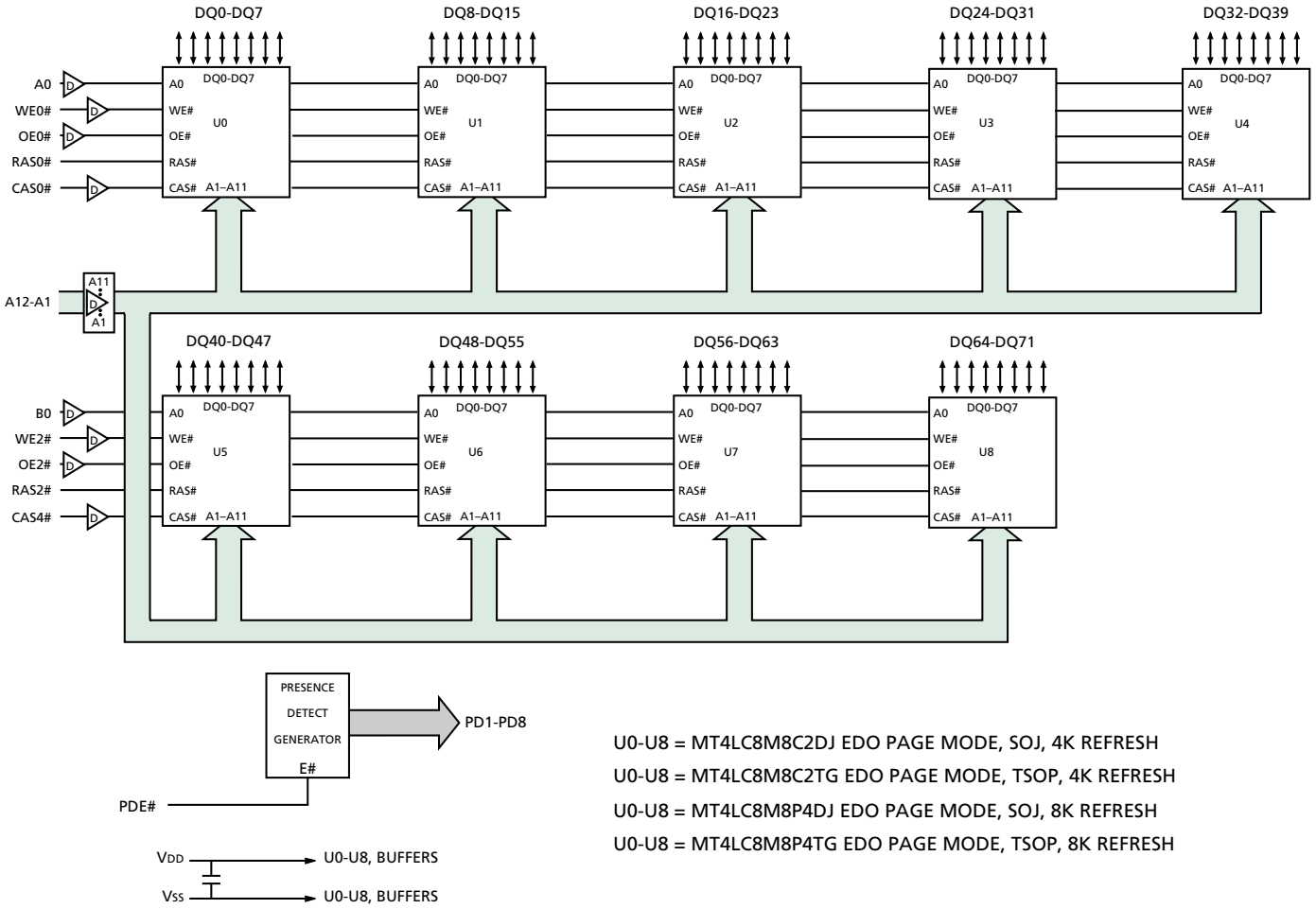
FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also tristate the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the MT4LC16M4H9 DRAM data sheet for additional information on EDO functionality.)

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all 4,096 combinations of RAS# addresses (A0-A11) are executed at least every 64ms, regardless of sequence. However, with the RAS#-ONLY REFRESH method some compatibility issues may become apparent (128MB and 256MB versions only). For example, both 4K and 8K refresh options require 4,096 CBR REFRESH cycles, yet require a different number of RAS#-ONLY REFRESH cycles (4K = 4,096 and 8K = 8,192). JEDEC strongly recommends the use of CBR REFRESH for these devices. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

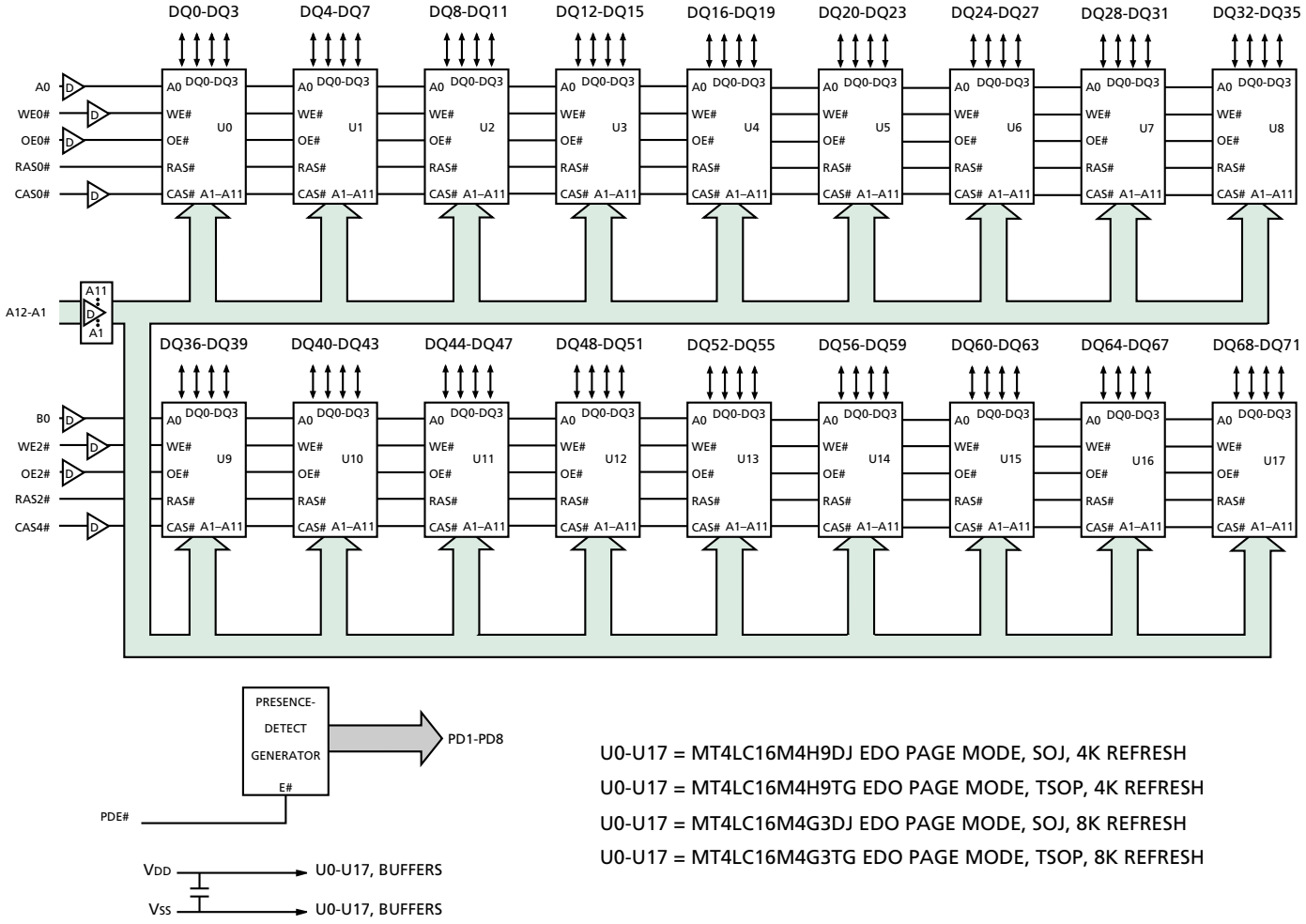
FUNCTIONAL BLOCK DIAGRAM
MT9LD(T)872(F)X (64MB)



U0-U8 = MT4LC8M8C2DJ EDO PAGE MODE, SOJ, 4K REFRESH
U0-U8 = MT4LC8M8C2TG EDO PAGE MODE, TSOP, 4K REFRESH
U0-U8 = MT4LC8M8P4DJ EDO PAGE MODE, SOJ, 8K REFRESH
U0-U8 = MT4LC8M8P4TG EDO PAGE MODE, TSOP, 8K REFRESH

NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.
3. Reference designators in this diagram do not necessarily match the actual module.

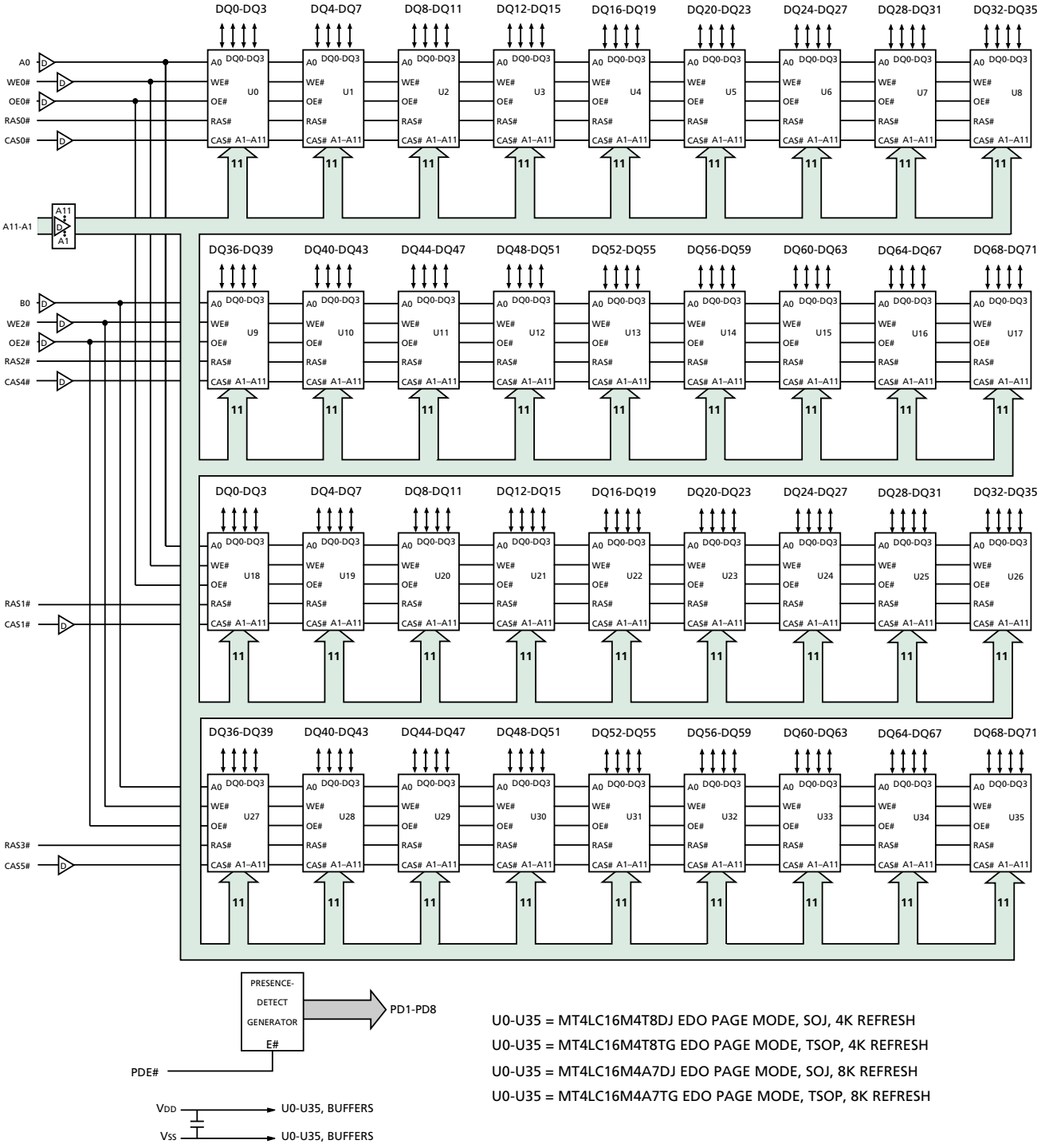
FUNCTIONAL BLOCK DIAGRAM
MT18LD(T)1672(F)X (128MB)



U0-U17 = MT4LC16M4H9DJ EDO PAGE MODE, SOJ, 4K REFRESH
U0-U17 = MT4LC16M4H9TG EDO PAGE MODE, TSOP, 4K REFRESH
U0-U17 = MT4LC16M4G3DJ EDO PAGE MODE, SOJ, 8K REFRESH
U0-U17 = MT4LC16M4G3TG EDO PAGE MODE, TSOP, 8K REFRESH

NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.
3. Reference designators in this diagram do not necessarily match the actual module.

FUNCTIONAL BLOCK DIAGRAM
MT36LD(T)3272(C)(F)X (256MB)



U0-U35 = MT4LC16M4T8DJ EDO PAGE MODE, SOJ, 4K REFRESH
U0-U35 = MT4LC16M4T8TG EDO PAGE MODE, TSOP, 4K REFRESH
U0-U35 = MT4LC16M4A7DJ EDO PAGE MODE, SOJ, 8K REFRESH
U0-U35 = MT4LC16M4A7TG EDO PAGE MODE, TSOP, 8K REFRESH

NOTE: 1. All inputs with the exception of RAS# are redriven.
2. D = line buffers.
3. Reference designators in this diagram do not necessarily match the actual module.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45, 114, 129	RAS0#-RAS3#	Input	Row-Address Strobe: RAS# is used to clock in the row-address bits. Two RAS# inputs allow for one x72 bank or two x36 banks.
28, 46, 112, 130	CAS0#, CAS1#, CAS4#, CAS5#	Buffered Input	Column-Address Strobe: CAS# is used to clock in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	WE0#, WE2#	Buffered Input	Write Enable: WE# is the READ/WRITE control for the DQ pins. WE0# controls DQ0-DQ35. WE2# controls DQ36-DQ71. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0#, OE2#	Buffered Input	Output Enable: OE# is the input/output control for the DQ pins. OE0# controls DQ0-DQ35. OE2# controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-39, 117-122, 126	A0-A12, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71.
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/ Output	Data I/Os: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either no connect (1), or they will be driven to V_{OL} (0).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	–	Reserved for Future Use: These pins should be left unconnected.
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	V_{SS}	Supply	Ground.
83, 167	ID0, ID1	Output	ID Bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (V_{SS}).
132	PDE#	Input	Presence Detect-Enable: PDE# is the READ control for the buffered presence-detect pins.

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	**Module Organization**	**Row/Column Addresses**	**ID0**	**ID1**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0MB	No module installed	X			1	1	1	1				
8MB 8MB	1 Meg x 64/72 1 Meg x 64/72	10/9 10/10			1 0	1 0	0 1	0 0				
16MB 16MB	2 Meg x 64/72 2 Meg x 64/72	10/10 11/10			1 1	0 0	1 0	0 1				
32MB 32MB	4 Meg x 64/72 4 Meg x 64/72	11/10 12*/11*			0 1	1 1	0 0	1 1				
• 64MB	8 Meg x 64/72	12/11			1	0	1	1				
128MB • 128MB	16 Meg x 64/72 16 Meg x 64/72	12/11 12/13/11/12			0 1	1 1	1 1	1 1				
• 256MB	32 Meg x 64/72	12/13/11/12			1	0	0	0				
Operating Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: V_{SS} = Ground; V_{OL} = 0; NC = 1.
* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Pin Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 18W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	SIZE	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	ALL	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	ALL	2	V_{DD} + 0.3	V	2
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	ALL	-0.5	0.8	V	2
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V (All other pins not under test = 0V)	CAS0#, CAS1#, CAS4#, CAS5#, A0-A12, B0, WE0#, WE2#, OE0#, OE2#, PDE#	I_{I1}	ALL	-2	2	µA	
	RAS0#-RAS3#	I_{I2}	64MB 128MB 256MB	-9 -18 -18	9 18 18	µA	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V_{OUT} ≤ V_{DD} + 0.3V	DQ0-DQ71	I_{OZ}	64MB 128MB 256MB	-5 -5 -10	5 5 10	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -2mA)		V_{OH}	ALL	2.4	–	V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}	ALL	–	0.4	V	

NOTE: 1. All voltages referenced to V_{SS}.
2. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.

IDD OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1-3) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	REFRESH	SIZE	MAX -5	MAX -6	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{DD1}	All	64MB 128MB 256MB	66 75 99	66 75 99	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = V_{DD} - 0.2V)	I_{DD2}	All	64MB 128MB 256MB	4.5 9 18	4.5 9 18	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{DD3}	4K	64MB 128MB 256MB	1,575 3,060 3,135	1,485 2,880 2,955	mA	4, 5
		8K	64MB 128MB 256MB	1,215 2,340 2,415	1,125 2,160 2,235		
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{DD4}	All	64MB 128MB 256MB	1,395 2,700 2,775	1,125 2,160 2,235	mA	4, 5
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{DD5}	4K	64MB 128MB 256MB	1,575 3,060 3,135	1,485 2,880 2,955	mA	4, 6
		8K	64MB 128MB 256MB	1,215 2,340 2,415	1,125 2,160 2,235		
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{DD6}	4K	64MB 128MB 256MB	1,485 2,880 2,955	1,395 2,700 2,778	mA	4, 7
		8K	64MB 128MB 256MB	1,485 2,880 2,955	1,395 2,700 2,778		

NOTE:
1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
3. An initial pause of 100µs is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Column address changed once each cycle.
6. RAS#-ONLY REFRESH requires that all rows be refreshed at least once every 64ms (4,096 rows for the 4K version and 8,192 rows for the 8K version). CBR REFRESH requires that at least 4,096 cycles be completed every 64ms.
7. Enables on-chip refresh and address counters.

CAPACITANCE

		MAX			
PARAMETER	SYMBOL	64MB	128MB	256MB	UNITS
Input Capacitance: A0-A12, B0, WE0#, WE2#, OE0#, OE2#	C_{I1}	9	9	9	pF
Input Capacitance: CAS0#, CAS1#, CAS4#, CAS5#, PDE#	C_{I2}	9	9	9	pF
Input Capacitance: RAS0#-RAS3#	C_{I3}	39	67	67	pF
Input/Output Capacitance: DQ0-DQ71	C_{IO}	12	12	22	pF
Output Capacitance: PD1-PD8	C_O	10	10	10	pF

NOTE: This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 31; notes appear on next page and page 13) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		30		35	ns	10
Column-address setup to CAS# going HIGH during WRITE	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	36		43		ns	11
Column-address setup time	^tASC	2		2		ns	12
Row-address setup time	^tASR	5		5		ns	10
Column address to WE# delay time	^tAWD	44		51		ns	12, 13
Access time from CAS#	^tCAC		18		20	ns	10, 14
Column-address hold time	^tCAH	13		15		ns	10
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# hold time (CBR Refresh)	^tCHR	6		8		ns	11, 16
CAS# to output in Low-Z	^tCLZ	2		2		ns	12, 18
Data output hold after CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	15
Access time from CAS# precharge	^tCPA		33		40	ns	10
CAS# to RAS# precharge time	^tCRP	10		10		ns	10
CAS# hold time	^tCSH	36		43		ns	11
CAS# setup time (CBR Refresh)	^tCSR	7		7		ns	12, 16
CAS# to WE# delay time	^tCWD	30		37		ns	12, 13
WRITE command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	13		15		ns	10, 17
Data-in setup time	^tDS	-2		-2		ns	11, 17
Output disable	^tOD	0	12	0	15	ns	18
Output enable	^tOE		12		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	6		8		ns	11
OE# HIGH hold time from CAS# HIGH	^tOEHC	5		10		ns	
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	2	17	2	20	ns	19, 20
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	20		25		ns	
PDE# to valid presence-detect data	^tPD		10		10	ns	21
PDE# inactive to presence-detects inactive	^tPDOFF	2		2		ns	21
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	49		58		ns	12
Access time from RAS#	^tRAC		50		60	ns	22
RAS# to column-address delay time	^tRAD	7		10		ns	23, 24
Row-address hold time	^tRAH	7		8		ns	11
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	84		104		ns	
RAS# to CAS# delay time	^tRCD	9		12		ns	24, 25

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 1-8; notes appear below and on next page) (V_{DD} = +3.3V ±0.3V)

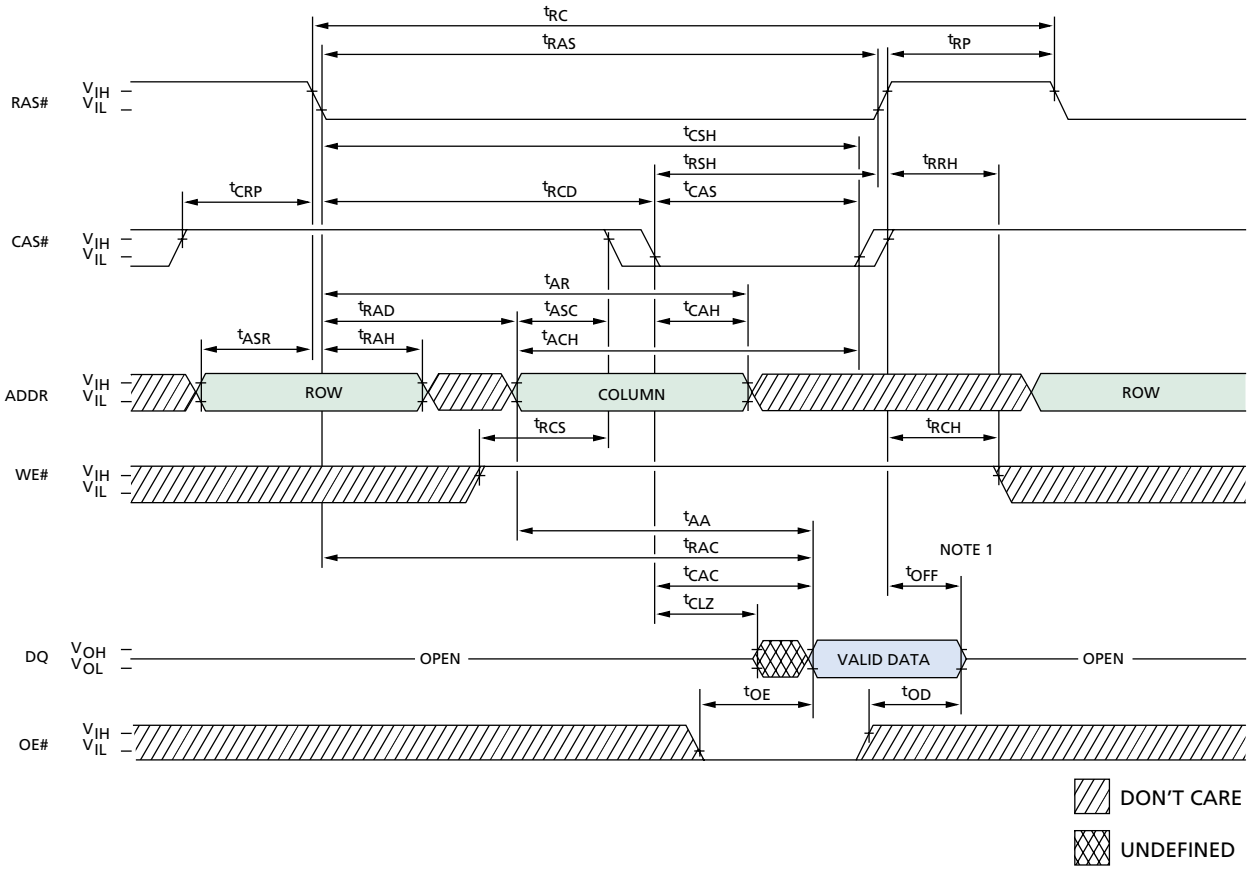
AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
READ command hold time (referenced to CAS#)	^tRCH	2		2		ns	27
READ command setup time	^tRCS	2		2		ns	
Refresh period	^tREF		64		64	ms	28
RAS# precharge time	^tRP	30		40		ns	
RAS# to CAS# precharge time	^tRPC	5		5		ns	
READ command hold time (referenced to RAS#)	^tRRH	0		0		ns	27
RAS# hold time	^tRSH	18		20		ns	10
READ-WRITE cycle time	^tRWC	121		145		ns	10
RAS# to WE# delay time	^tRWD	69		81		ns	26
WRITE command to RAS# lead time	^tRWL	18		20		ns	10
Transition time (rise or fall)	^tT	2	50	2	50	ns	
WRITE command hold time	^tWCH	13		15		ns	10
WRITE command hold time (referenced to RAS#)	^tWCR	36		43		ns	11
WE# command setup time	^tWCS	2		2		ns	16
WE# to outputs in High-Z	^tWHZ		17		20	ns	10
WRITE command pulse width	^tWP	5		5		ns	
WE# pulse width to disable outputs	^tWPZ	10		10		ns	
WE# hold time (CBR Refresh)	^tWRH	6		8		ns	10
WE# setup time (CBR Refresh)	^tWRP	10		12		ns	12

NOTE:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
2. An initial pause of 100µs is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
3. AC characteristics assume ^tT = 2ns for -5 and 2.5ns for -6.
4. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
5. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
6. If CAS# and RAS# = V_{IH}, data output is High-Z.
7. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
8. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
9. If OE# is tied permanently LOW, LATE WRITE, or READ-MODIFY-WRITE operations are not possible.
10. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
11. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
12. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
13. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. If $^tWCS > ^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. ^tRWD, ^tAWD and ^tCWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
14. Requires that ^tAA and ^tRAC are not violated.
15. If CAS# is LOW at the falling edge of RAS#, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^tCP.
16. Enables on-chip refresh and address counters.
17. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
18. The 3ns minimum is a parameter guaranteed by design.

NOTES: (continued)

19. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
20. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
21. ^{t}PDOFF (MAX) is determined by the pullup resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
22. Requires that ^{t}AA and ^{t}CAC are not violated.
23. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
24. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
25. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
26. Column address changed once each cycle.
27. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
28. RAS#-ONLY REFRESH requires that all rows be refreshed at least once every 64ms (4,096 rows for the 4K version and 8,192 rows for the 8K version). CBR REFRESH requires that at least 4,096 cycles be completed every 64ms.

READ CYCLE



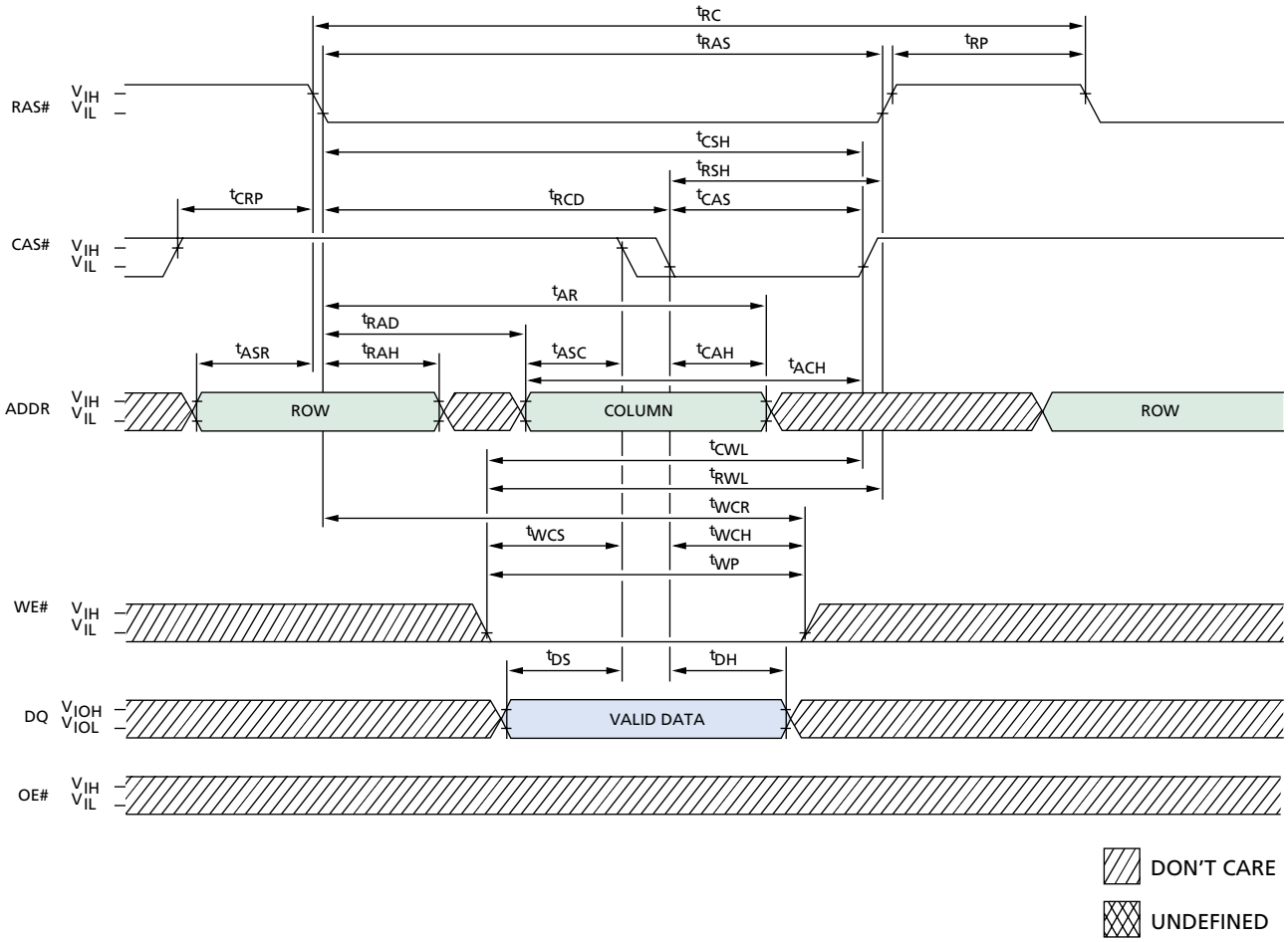
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		30		35	ns
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	2		2		ns
tCRP	10		10		ns
tCSH	36		43		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	2	17	2	20	ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	9		12		ns
tRCH	2		2		ns
tRCS	2		2		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	18		20		ns

NOTE: 1. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE

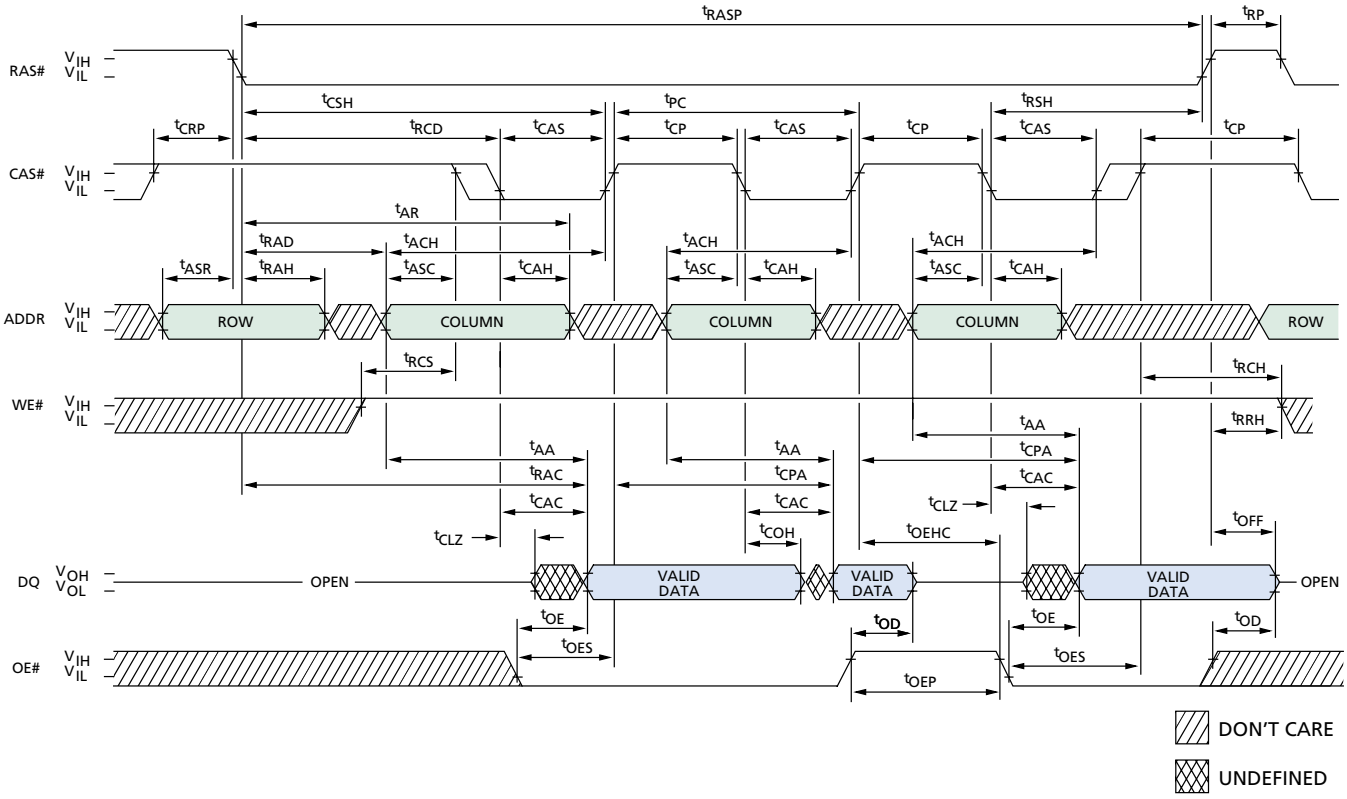


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCRP	10		10		ns
tCSH	36		43		ns
tCWL	8		10		ns
tDH	13		15		ns
tDS	-2		-2		ns
tRAD	7		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	9		12		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWL	18		20		ns
tWCH	13		15		ns
tWCR	36		43		ns
tWCS	2		2		ns
tWP	5		5		ns

EDO-PAGE-MODE READ CYCLE

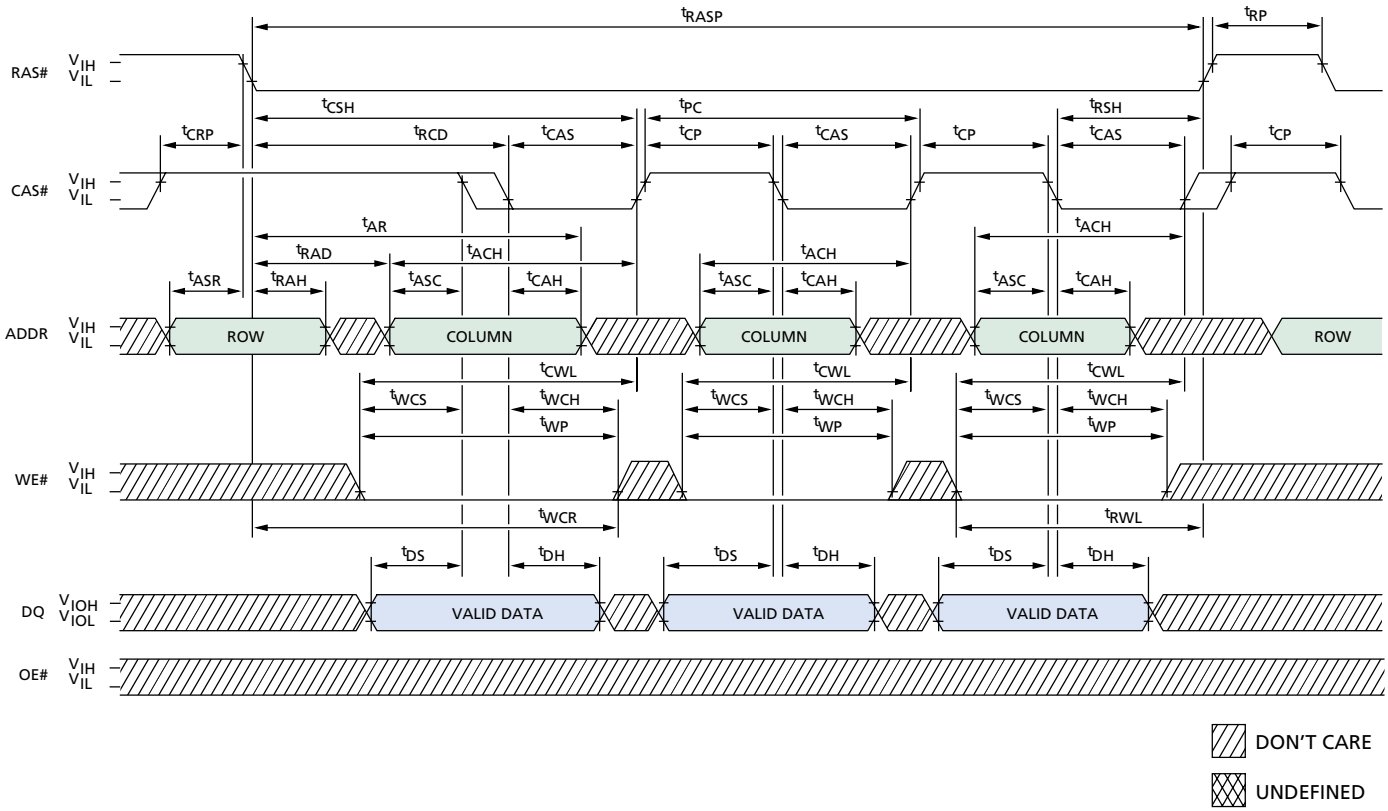


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		30		35	ns
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	2		2		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		33		40	ns
tCRP	10		10		ns
tCSH	36		43		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	2	17	2	20	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD	9		12		ns
tRCH	2		2		ns
tRCS	2		2		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	18		20		ns

EDO-PAGE-MODE EARLY WRITE CYCLE

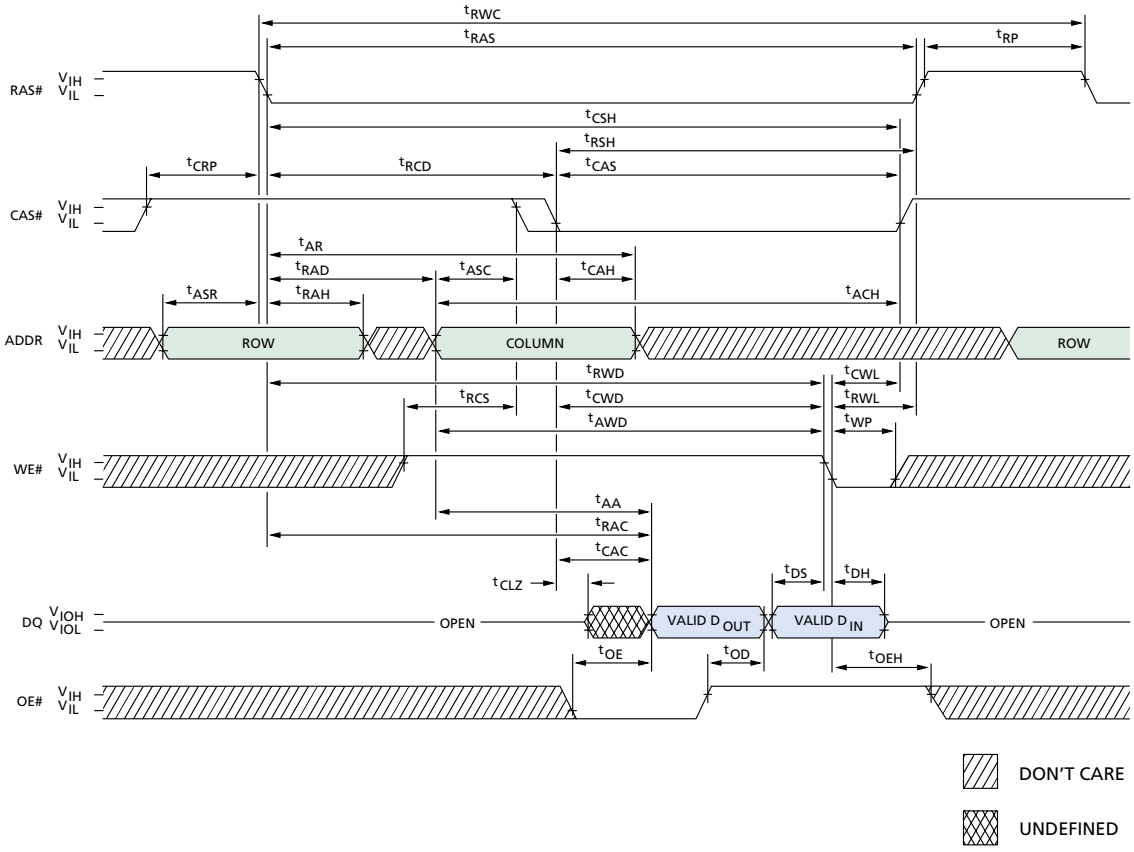


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCP	8		10		ns
tCRP	10		10		ns
tCSH	36		43		ns
tCWL	8		10		ns
tDH	13		15		ns
tDS	-2		-2		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tPC	20		25		ns
tRAD	7		10		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD	9		12		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWL	18		20		ns
tWCH	13		15		ns
tWCR	36		43		ns
tWCS	2		2		ns
tWP	5		5		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

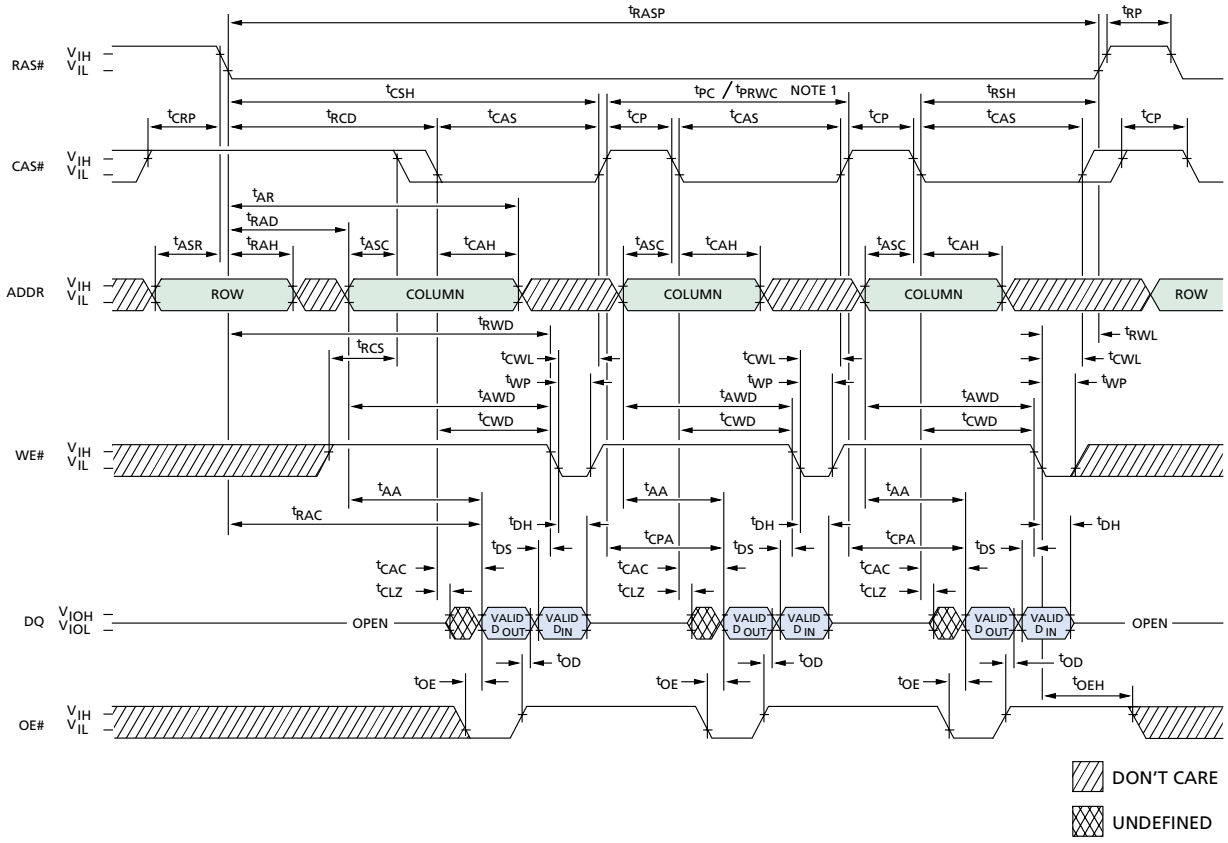


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		30		35	ns
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tAWD	44		51		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	2		2		ns
tCRP	10		10		ns
tCSH	36		43		ns
tCWD	30		37		ns
tCWL	8		10		ns
tDH	13		15		ns
tDS	-2		-2		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	6		8		ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRCD	9		12		ns
tRCS	2		2		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWC	121		145		ns
tRWD	69		81		ns
tRWL	18		20		ns
tWP	5		5		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



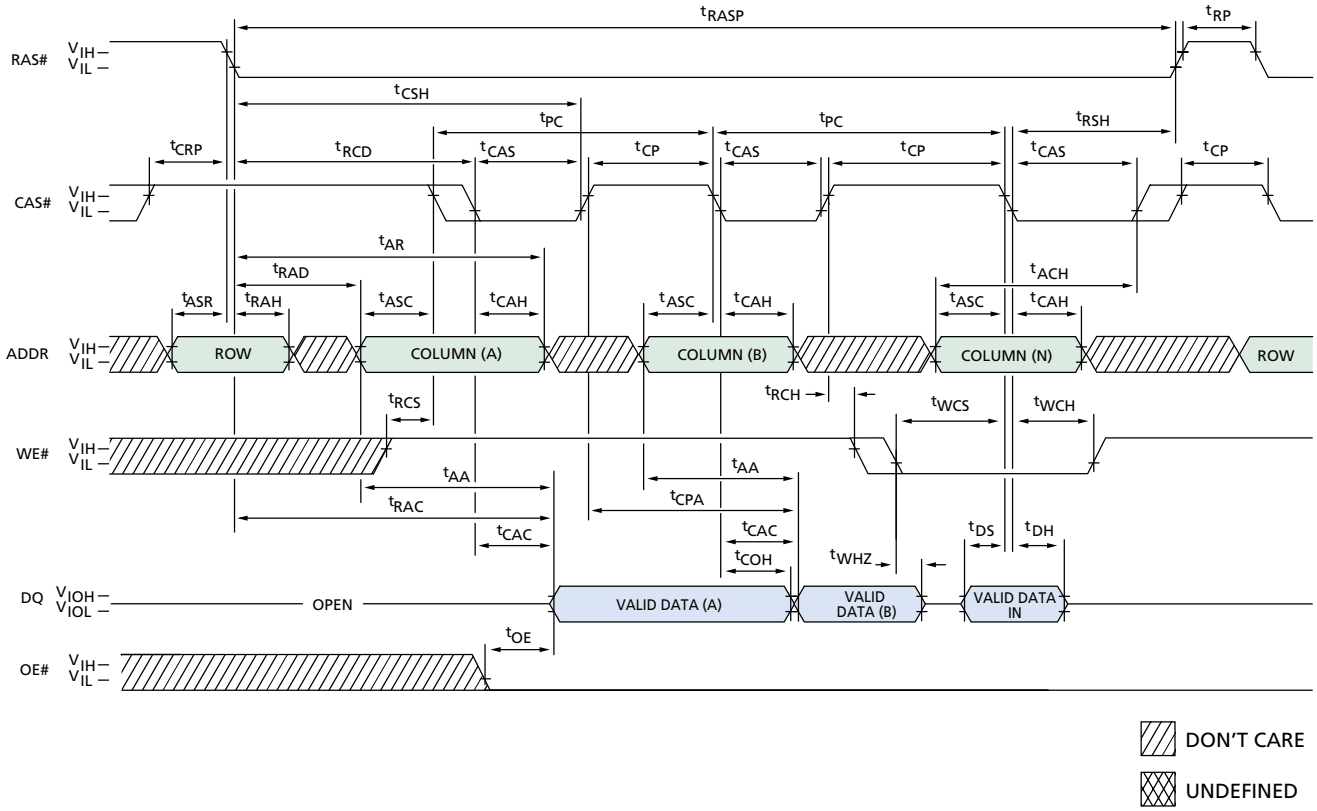
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		30		35	ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tAWD	44		51		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	2		2		ns
tCP	8		10		ns
tCPA		33		40	ns
tCRP	10		10		ns
tCSH	36		43		ns
tCWD	30		37		ns
tCWL	8		10		ns
tDH	13		15		ns
tDS	-2		-2		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	6		8		ns
tPC	20		25		ns
tPRWC	49		58		ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD	9		12		ns
tRCS	2		2		ns
tRP	30		40		ns
tRSH	18		20		ns
tRWD	69		81		ns
tRWL	18		20		ns
tWP	5		5		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

EDO-PAGE-MODE READ EARLY WRITE CYCLE (Pseudo READ-MODIFY-WRITE)

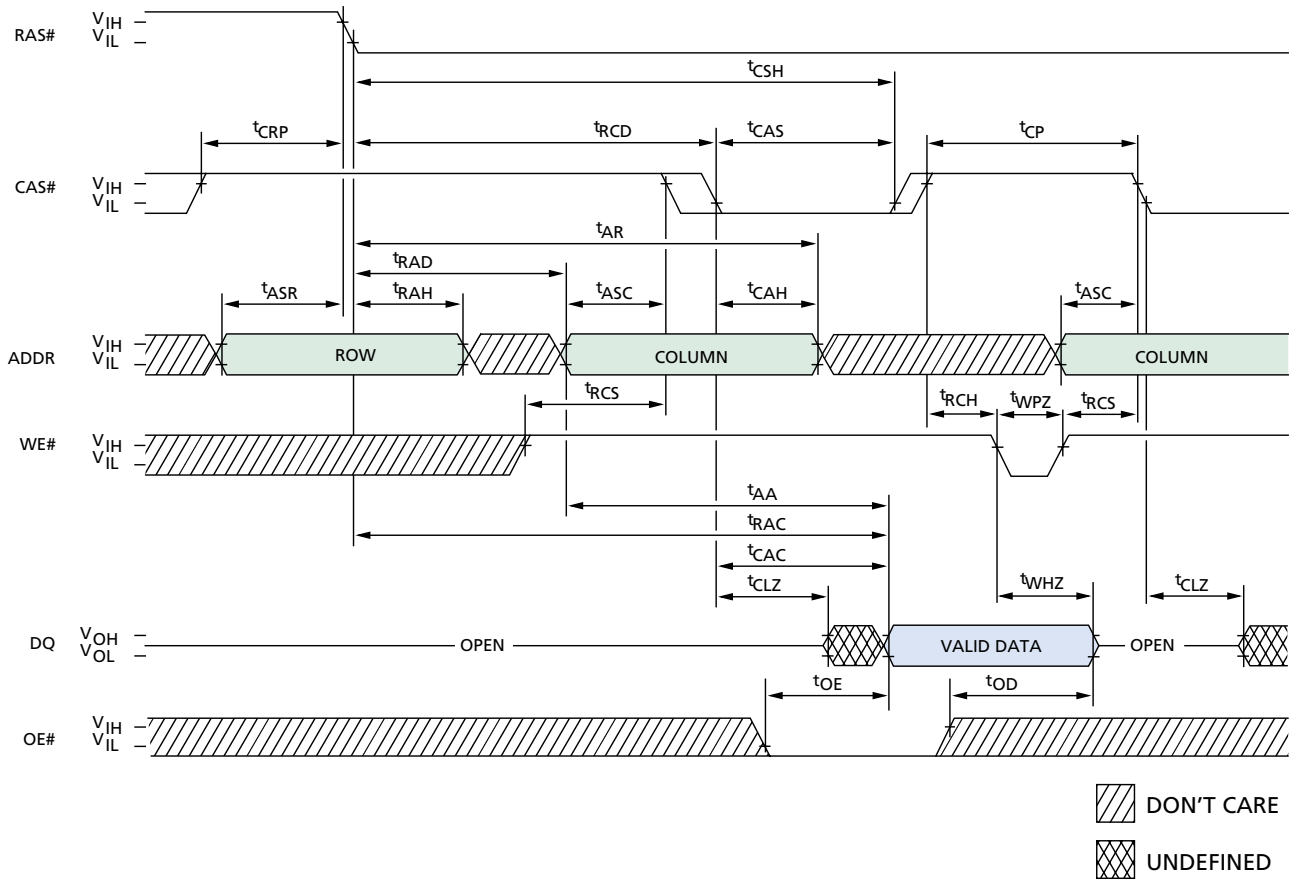


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		30		35	ns
tACH	12		15		ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		33		40	ns
tCRP	10		10		ns
tCSH	36		43		ns
tDH	13		15		ns
tDS	-2		-2		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRASP	50	125,000	60	125,000	ns
tRCD	9		12		ns
tRCH	2		2		ns
tRCS	2		2		ns
tRP	30		40		ns
tRSH	18		20		ns
tWCH	13		15		ns
tWCS	2		2		ns
tWHZ		17		20	ns

EDO READ CYCLE
(with WE#-controlled disable)

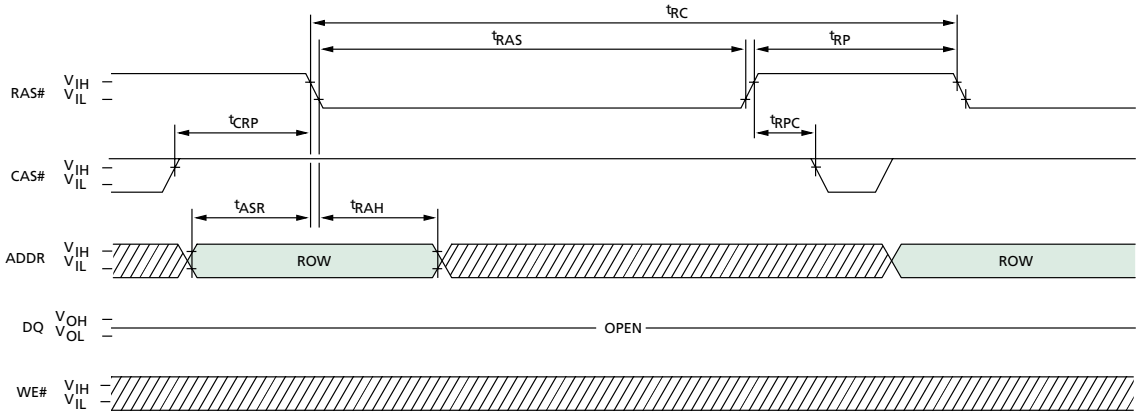


TIMING PARAMETERS

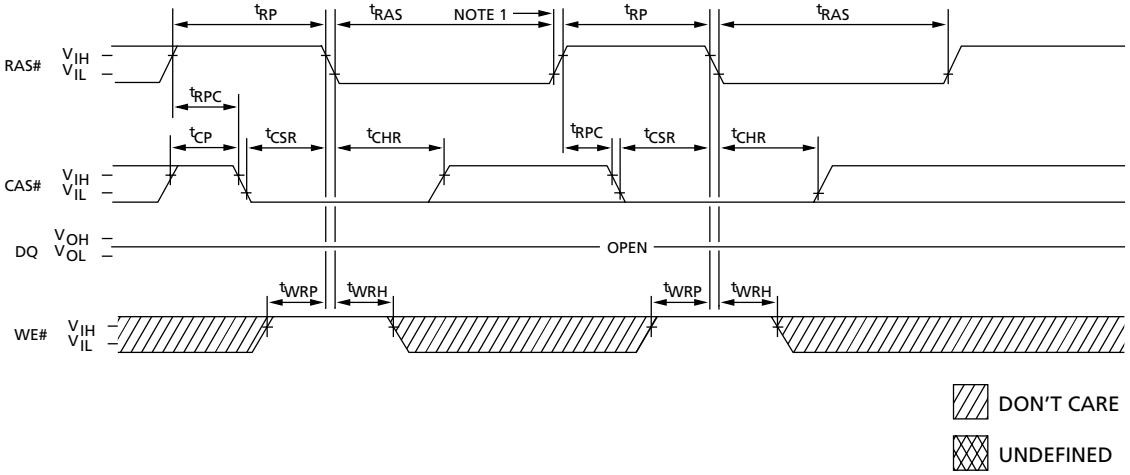
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		30		35	ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	2		2		ns
tCP	8		10		ns
tCRP	10		10		ns
tCSH	36		43		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRCD	9		12		ns
tRCH	2		2		ns
tRCS	2		2		ns
tWHZ		17		20	ns
tWPZ	10		10		ns

RAS#-ONLY REFRESH CYCLE



CBR REFRESH CYCLE
(Addresses, OE# = DON'T CARE)

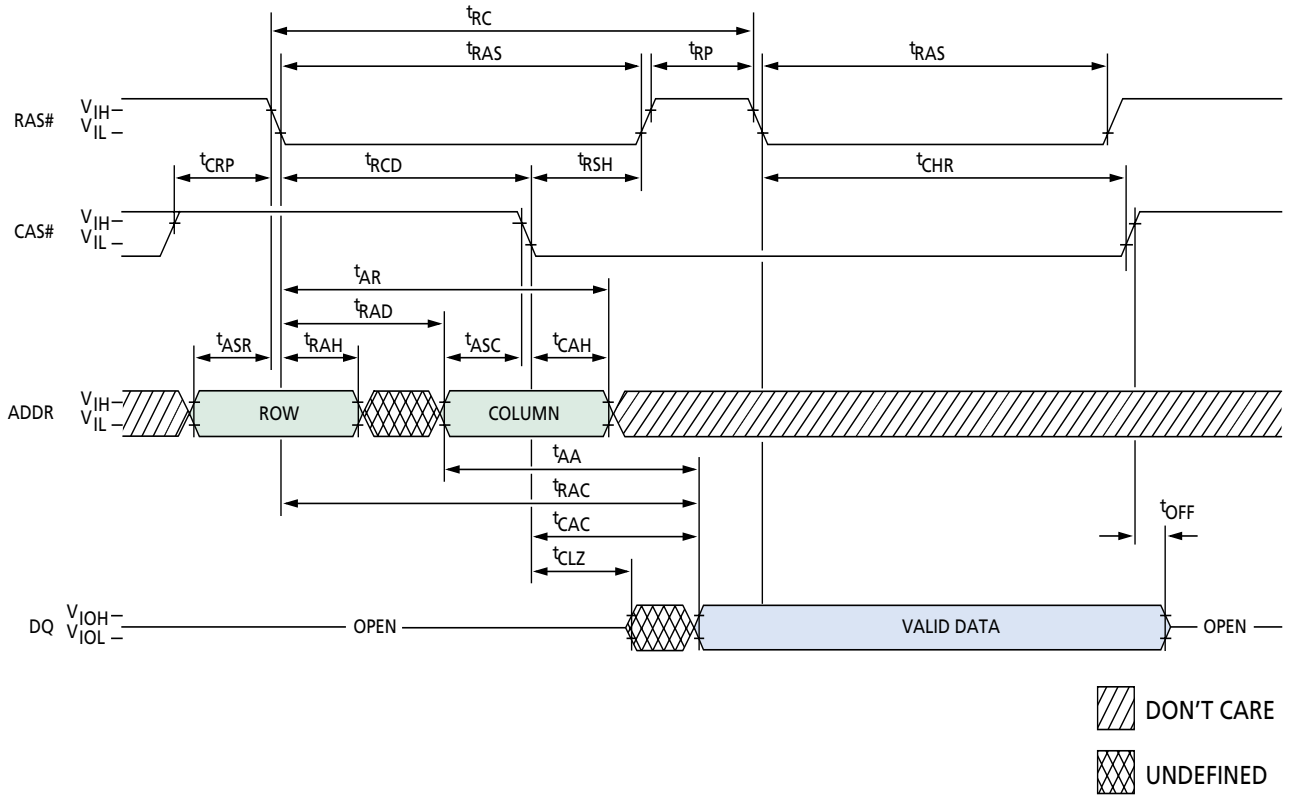


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	5		5		ns
tCHR	6		8		ns
tCP	8		10		ns
tCRP	10		10		ns
tCSR	7		7		ns
tRAH	7		8		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	6		8		ns
tWRP	10		12		ns

HIDDEN REFRESH CYCLE
(WE# = HIGH; OE# = LOW)



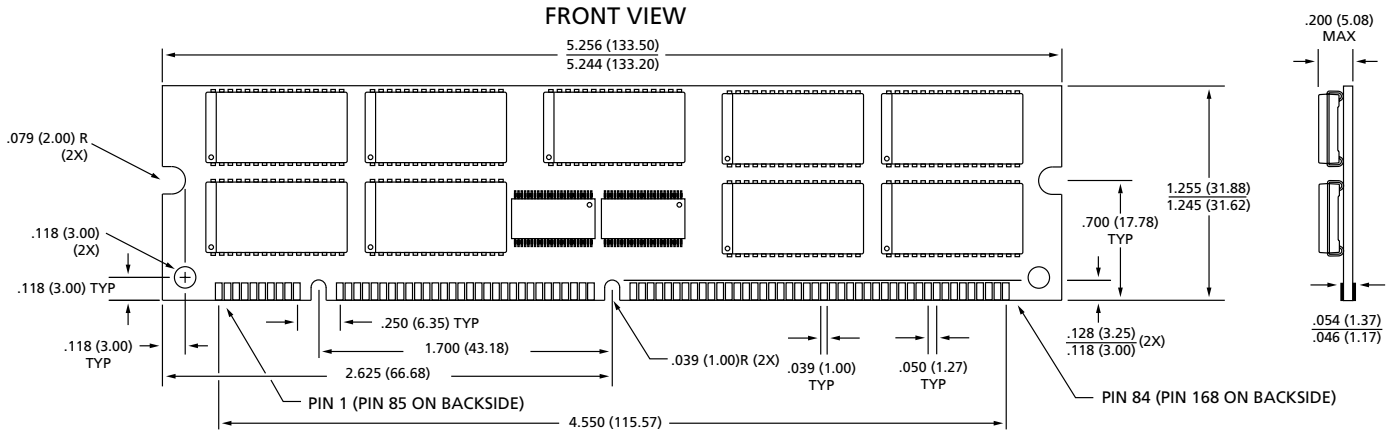
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		30		35	ns
tAR	36		43		ns
tASC	2		2		ns
tASR	5		5		ns
tCAC		18		20	ns
tCAH	13		15		ns
tCHR	6		8		ns
tCLZ	2		2		ns
tCRP	10		10		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

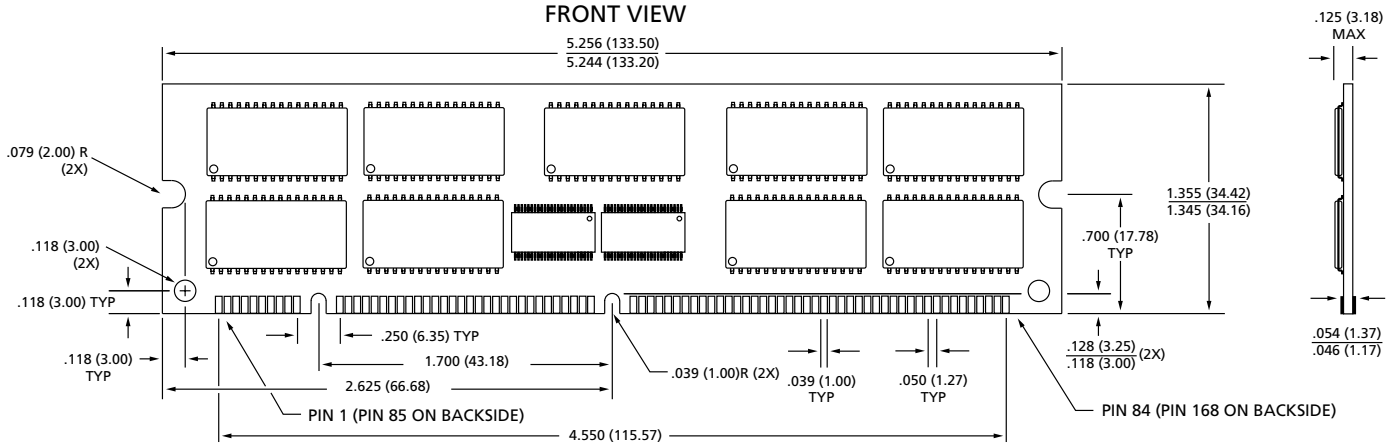
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	2	17	2	20	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD	7		10		ns
tRAH	7		8		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	9		12		ns
tRP	30		40		ns
tRSH	18		20		ns

NOTE: A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.

168-PIN DIMM
(64MB SOJ)

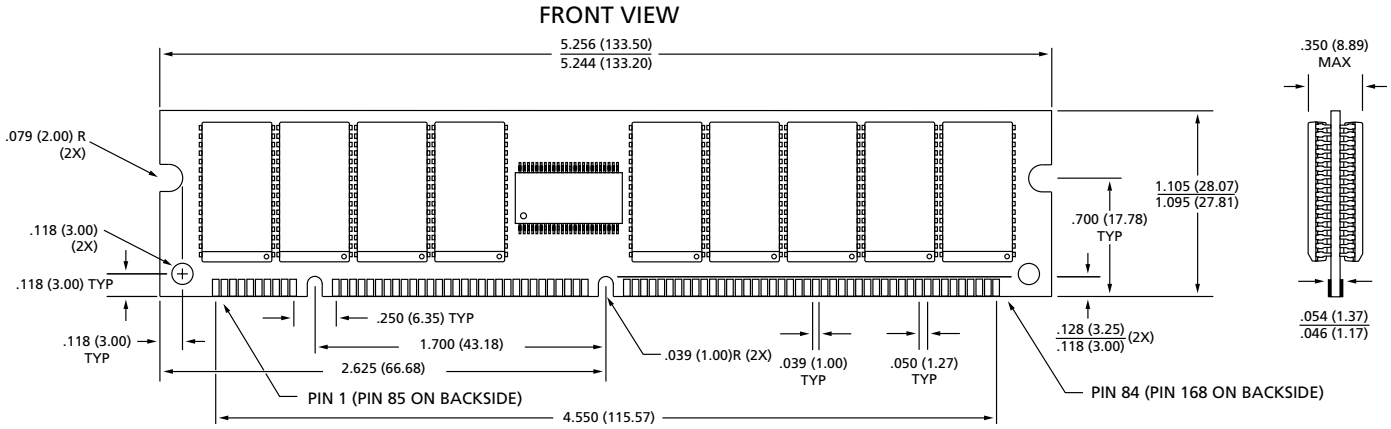


168-PIN DIMM
64MB TSOP

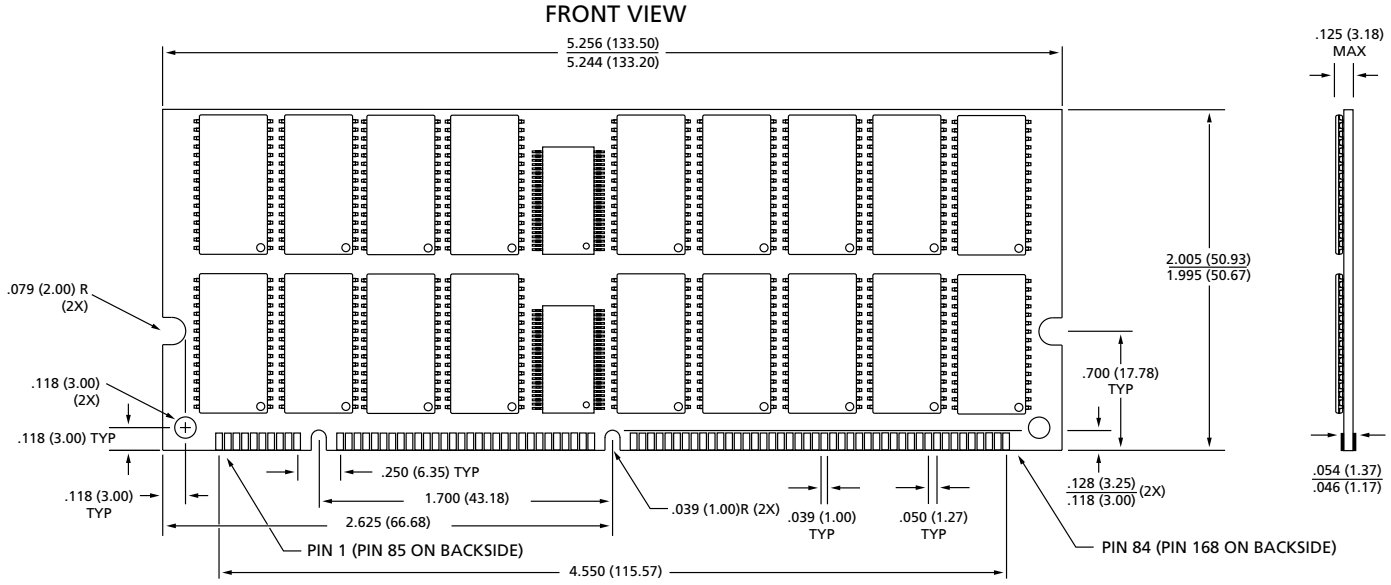


NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM
(128MB SOJ)

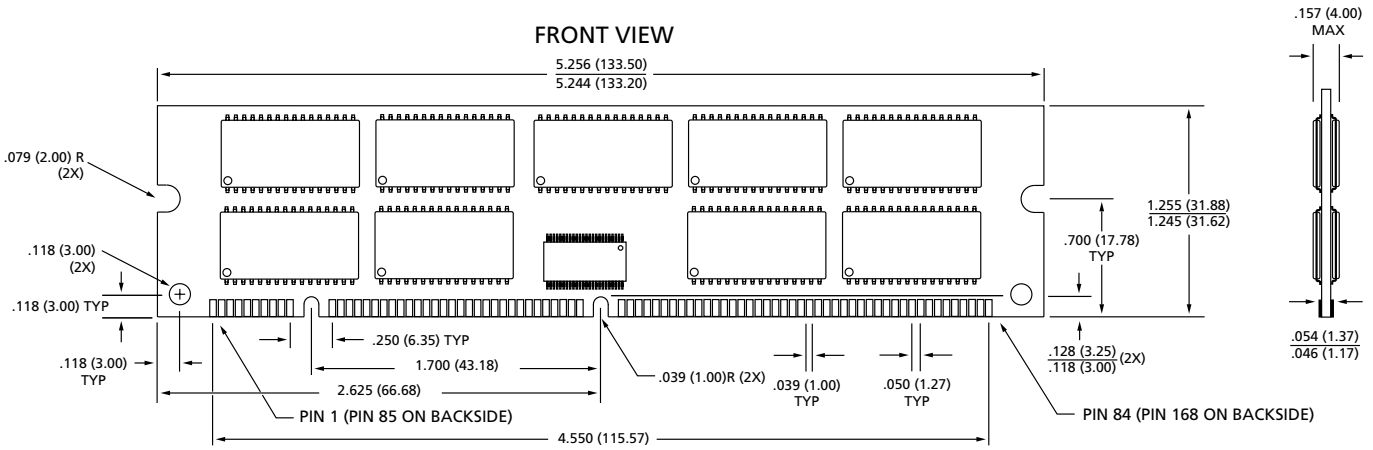


168-PIN DIMM
(128MB TSOP)



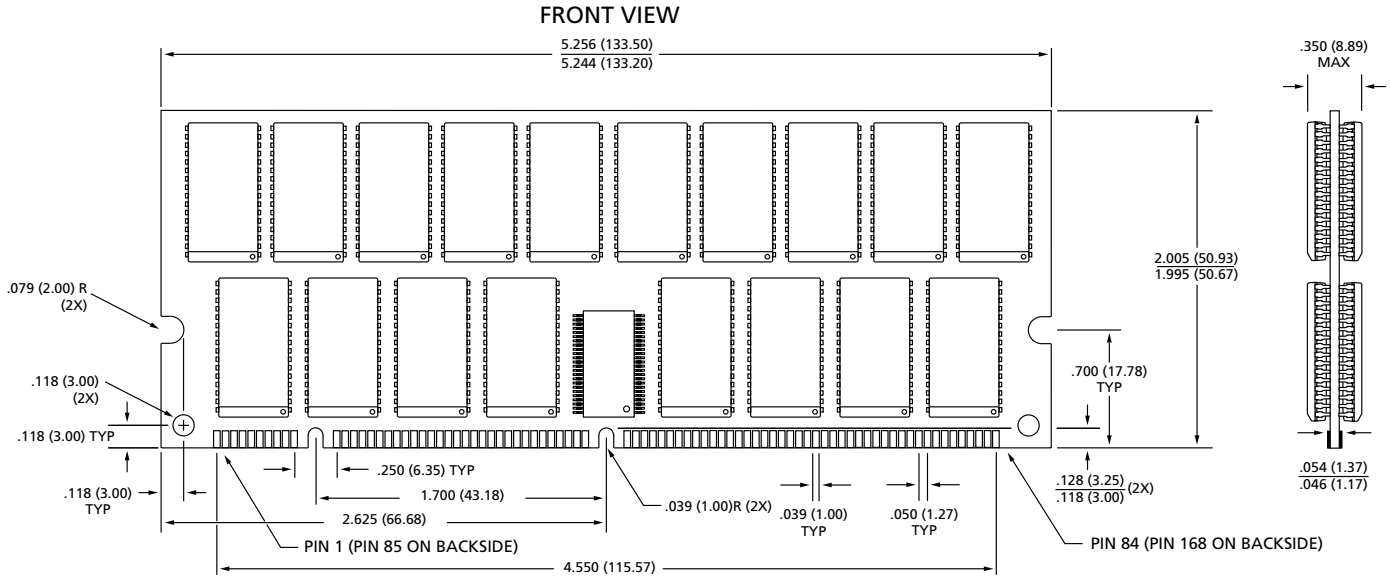
NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM
(128MB TSOP)

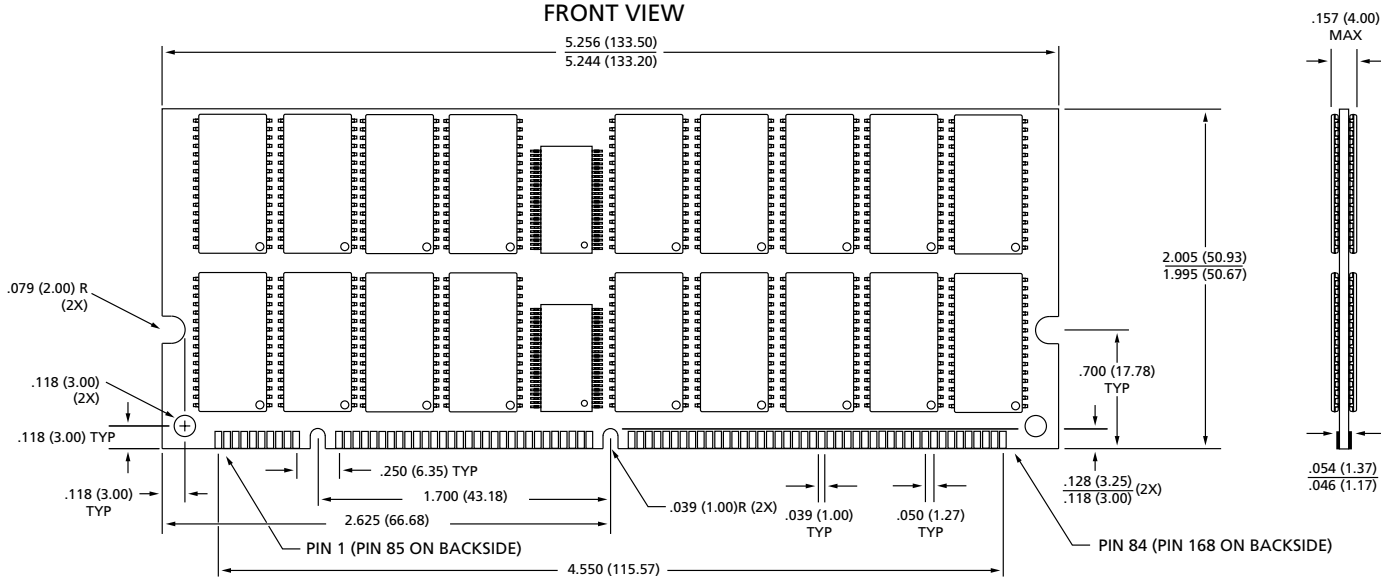


NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM
(256MB SOJ)

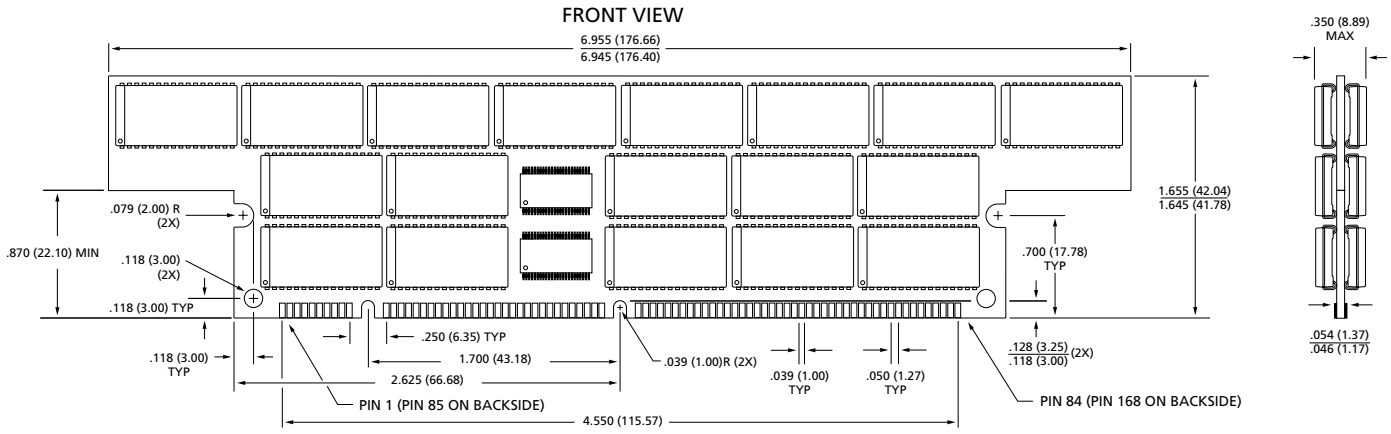


168-PIN DIMM
(256MB TSOP)



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM
(256MB SOJ)



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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