



DRAM MODULE

MT9D436 X MT18D836 X

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/datasheets

FEATURES

- Four-CAS#, ECC-optimized configuration in a 72-pin, single in-line memory module (SIMM)
- 16MB (4 Meg x 36) and 32MB (8 Meg x 36)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Extended Data-Out (EDO) PAGE MODE access

OPTIONS

- Timing
 - 50ns access
 - 60ns access
- Package
 - 72-pin SIMM

MARKING

- 5
- 6
- M

KEY TIMING PARAMETERS

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{CAS}
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

PART NUMBERS

PART NUMBER	CONFIGURATION	FEATURES	MODE
MT9D436M-x X	4 Meg x 36	4 CAS#, ECC	EDO
MT18D836M-x X	8 Meg x 36	4 CAS#, ECC	EDO

x = speed

GENERAL DESCRIPTION

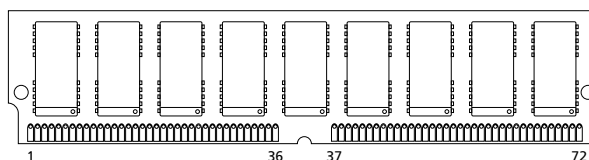
The MT9D436 X and MT18D836 X are randomly accessed, 16MB and 32MB solid-state memories organized in a x36 configuration. These modules are designed for systems that utilize ECC and do not conduct single-byte accesses. These modules do not support parity functionality.

During READ or WRITE cycles, each bit is uniquely addressed through 20 address bits that are entered 10 bits (A0-A9) at a time. RAS# is used to latch the first 10 bits and CAS# the latter 10 bits. READ or WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched

PIN ASSIGNMENT (Front View)

72-Pin SIMM

4 Meg x 36 (shown)
8 Meg x 36



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V _{SS}	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	V _{SS}	57	DQ14
4	DQ2	22	DQ6	40	CAS0#	58	DQ32
5	DQ20	23	DQ24	41	CAS2#	59	V _{BD}
6	DQ3	24	DQ7	42	CAS3#	60	DQ33
7	DQ21	25	DQ25	43	CAS1#	61	DQ15
8	DQ4	26	DQ8	44	RAS0#	62	DQ34
9	DQ22	27	DQ26	45	NC/RAS1#*	63	DQ16
10	V _{DD}	28	A7	46	NC	64	DQ35
11	NC	29	NC (A11)	47	WE#	65	DQ17
12	A0	30	V _{DD}	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC/RAS3#*	51	DQ11	69	PRD3
16	A4	34	RAS2#	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	V _{SS}

*32MB version only

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

by the falling edge of WE# or CAS#, whichever occurs last. EARLY WRITE occurs when WE# goes LOW prior to CAS# going LOW, and the output pin(s) remain open (High-Z) until the next CAS# cycle.

EDO PAGE MODE

EDO PAGE MODE is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (t_{CP}) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.



EDO PAGE MODE (continued)

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates like FAST-PAGE-MODE READs, except data will be held valid or become valid after CAS# goes HIGH, as long as RAS# is held LOW. (Refer to the MT4C4M4E8 DRAM data sheet for additional information on EDO functionality.)

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS# ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS# addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS# addressing.

**JEDEC-DEFINED
PRESENCE-DETECT – MT9D436 (16MB)**

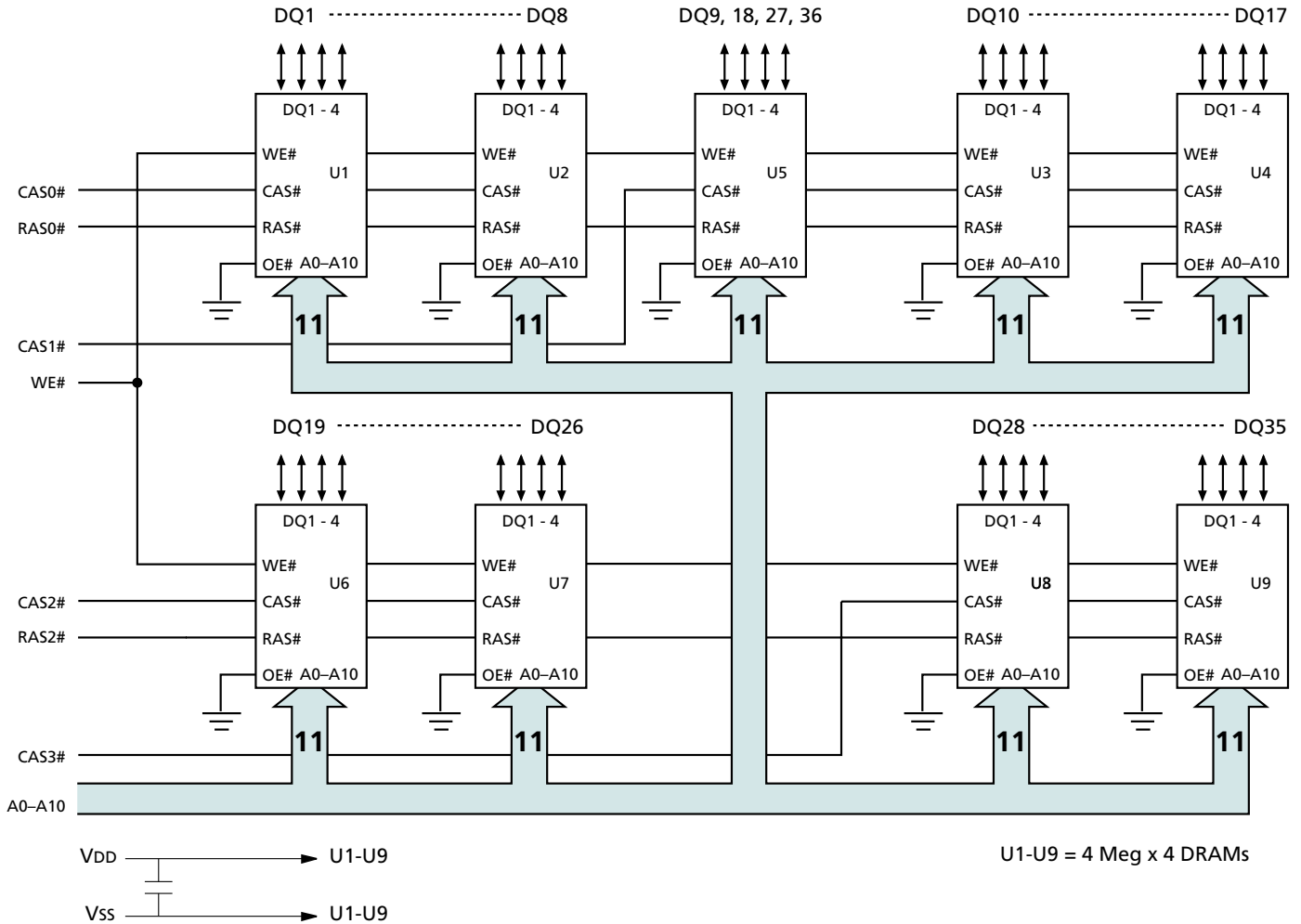
SYMBOL	PIN	-5	-6
PRD1	67	V _{ss}	V _{ss}
PRD2	68	NC	NC
PRD3	69	V _{ss}	NC
PRD4	70	V _{ss}	NC

**JEDEC-DEFINED
PRESENCE-DETECT – MT18D836 (32MB)**

SYMBOL	PIN	-5	-6
PRD1	67	NC	NC
PRD2	68	V _{ss}	V _{ss}
PRD3	69	V _{ss}	NC
PRD4	70	V _{ss}	NC

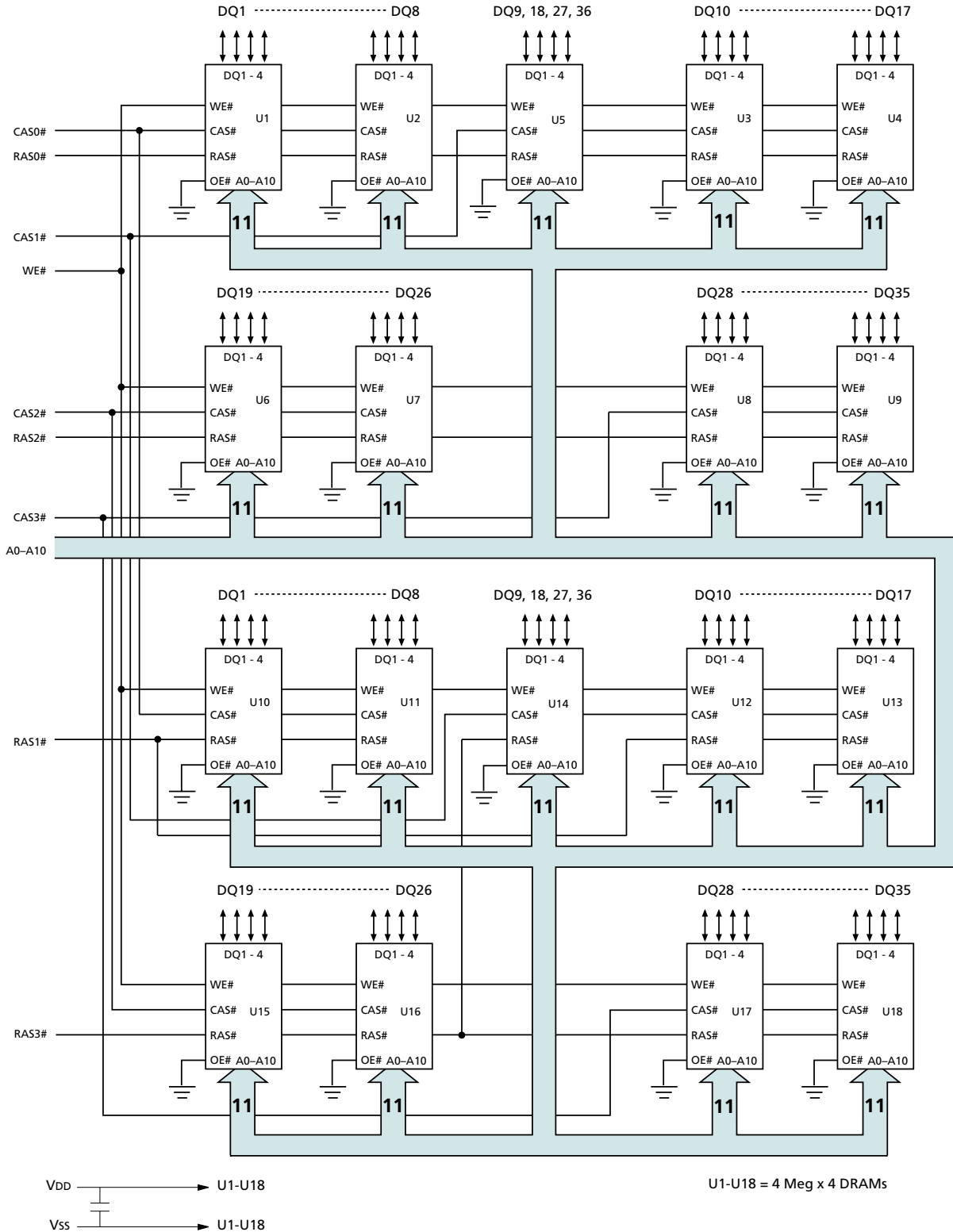


FUNCTIONAL BLOCK DIAGRAM
MT9D436 (16MB)





FUNCTIONAL BLOCK DIAGRAM
MT18D836 (32MB)



NOT RECOMMENDED FOR NEW DESIGNS



4, 8 MEG x 36 ECC-OPTIMIZED DRAM SIMMs

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} -1V to +7V
 Operating Temperature, T_A (ambient) ... 0°C to +70°C
 Storage Temperature (plastic) -55°C to +125°C
 Power Dissipation 9W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) ($V_{DD} = +5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
SUPPLY VOLTAGE	V_{DD}	4.5	5.5	V		
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	2.4	$V_{DD} + 1$	V		
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1.0	0.8	V		
INPUT LEAKAGE CURRENT: Any input $0V \leq V_{IN} \leq 5.5V$ (All other pins not under test = 0V)	CAS0#-CAS3#	I_{I1}	-12	12	μA	22
	A0-A10, WE#	I_{I2}	-36	36	μA	22
	RAS0#-RAS3#	I_{I3}	-10	10	μA	
OUTPUT LEAKAGE CURRENT: (DQ is disabled; $0V \leq V_{OUT} \leq 5.5V$)	DQ1-DQ36	I_{OZ}	-10	10	μA	22
OUTPUT LEVELS: Output High Voltage ($I_{OUT} = -5mA$) Output Low Voltage ($I_{OUT} = 4.2mA$)	V_{OH}	2.4	-	V		
	V_{OL}	-	0.4	V		

I_{CC} SPECIFICATIONS AND CONDITIONS

(Notes: 1, 5, 6) ($V_{DD} = +5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-5	-6		
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	16MB 32MB	9 18	9 18	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = Other Inputs = $V_{DD} - 0.2V$)	I_{CC2}	16MB 32MB	5 9	5 9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: $t^*_{RC} = t^*_{RC}$ [MIN])	I_{CC3}	16MB 32MB	1,260 1,269	1,170 1,179	mA	3, 21
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL} , CAS#, address cycling: $t^*_{PC} = t^*_{PC}$ [MIN])	I_{CC4}	16MB 32MB	990 999	900 909	mA	3, 21
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH} : $t^*_{RC} = t^*_{RC}$ [MIN])	I_{CC5}	16MB 32MB	1,260 1,269	1,170 1,179	mA	3, 21
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling; $t^*_{RC} = t^*_{RC}$ [MIN])	I_{CC6}	16MB 32MB	1,260 1,269	1,170 1,179	mA	3, 4

NOT RECOMMENDED FOR NEW DESIGNS



4, 8 MEG x 36 ECC-OPTIMIZED DRAM SIMMs

CAPACITANCE

PARAMETER	SYMBOL	MAX		UNITS	NOTES
		16MB	32MB		
Input Capacitance: A0-A10	C11	52	105	pF	2
Input Capacitance: WE#	C12	70	140	pF	2
Input Capacitance: RAS0#-RAS3#	C13	42	42	pF	2
Input Capacitance: CAS0#-CAS3#	C14	25	50	pF	2
Input/Output Capacitance: DQ1-DQ36	C10	10	18	pF	2

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{DD} = +5V \pm 10\%$)

AC CHARACTERISTICS		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Access time from column address	t_{AA}		25		30	ns	
Column-address setup to CAS# precharge during WRITE	t_{ACH}	12		15		ns	
Column-address hold time (referenced to RAS#)	t_{AR}	38		45		ns	
Column-address setup time	t_{ASC}	0		0		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Access time from CAS#	t_{CAC}		13		15	ns	
Column-address hold time	t_{CAH}	8		10		ns	
CAS# pulse width	t_{CAS}	8	10,000	10	10,000	ns	
CAS# hold time (CBR Refresh)	t_{CHR}	8		10		ns	4
CAS# to output in Low-Z	t_{CLZ}	0		0		ns	
Data output hold after next CAS# LOW	t_{COH}	3		3		ns	
CAS# precharge time	t_{CP}	8		10		ns	13
Access time from CAS# precharge	t_{CPA}		28		35	ns	
CAS# to RAS# precharge time	t_{CRP}	5		5		ns	
CAS# hold time	t_{CSH}	38		45		ns	
CAS# setup time (CBR Refresh)	t_{CSR}	5		5		ns	4
WRITE command to CAS# lead time	t_{CWL}	8		10		ns	
Data-in hold time	t_{DH}	8		10		ns	18
Data-in setup time	t_{DS}	0		0		ns	18
Output buffer turn-off delay	t_{OFF}	0	12	0	15	ns	17
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		ns	
Access time from RAS#	t_{RAC}		50		60	ns	
RAS# to column-address delay time	t_{RAD}	9		12		ns	15
Row-address hold time	t_{RAH}	9		10		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	84		104		ns	
RAS# to CAS# delay time	t_{RCD}	11		14		ns	14
READ command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	16
READ command setup time	t_{RCS}	0		0		ns	
Refresh period (2,048 cycles)	t_{REF}		32		32	ms	

NOT RECOMMENDED FOR NEW DESIGNS**4, 8 MEG x 36
ECC-OPTIMIZED DRAM SIMMs****AC ELECTRICAL CHARACTERISTICS**(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{DD} = +5V \pm 10\%$)

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	16
RAS# hold time	t_{RSH}	13		15		ns	
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	8		10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	38		45		ns	
WE# command setup time	t_{WCS}	0		0		ns	
Output disable delay from WE# (CAS# HIGH)	t_{WHZ}	0	12	0	15	ns	
WRITE command pulse width	t_{WP}	5		5		ns	
WE# pulse width for output disable when CAS# HIGH	t_{WPZ}	10		10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	8		10		ns	
WE# setup time (CBR Refresh)	t_{WRP}	8		10		ns	

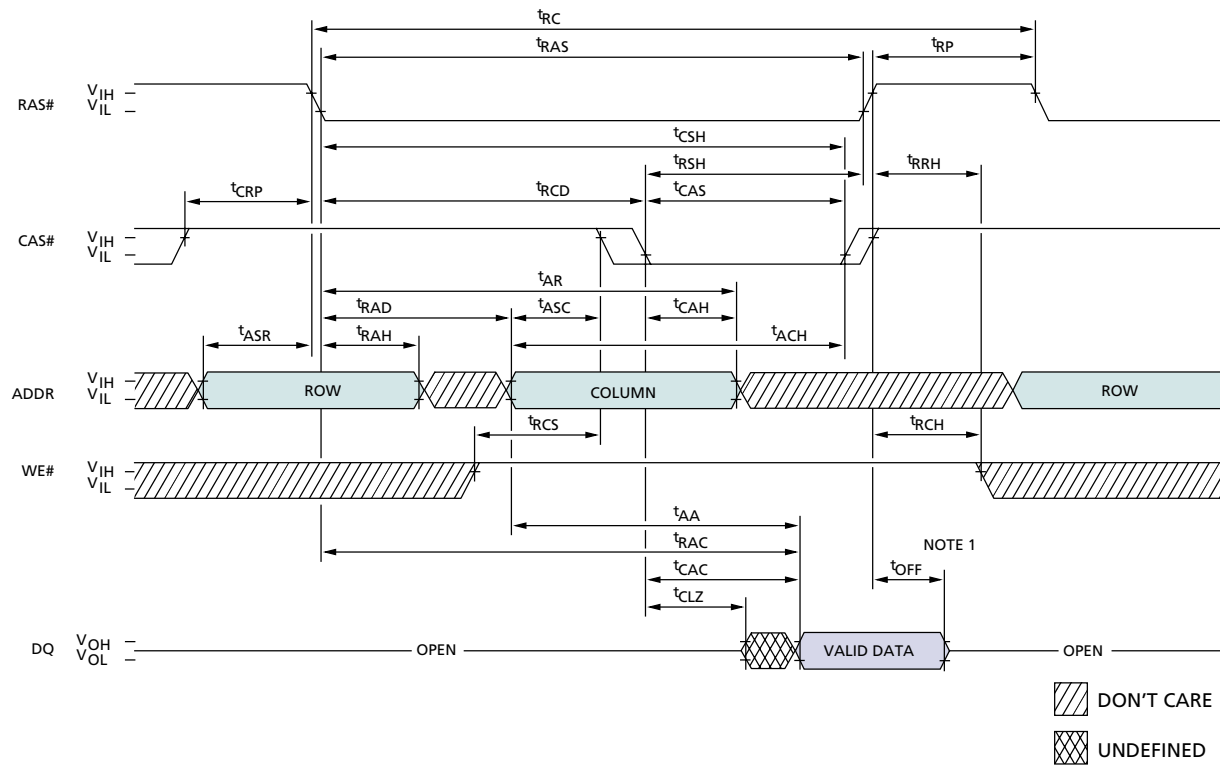


NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, $V_{DD} = 4.5V$, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100 μ s is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 2.5ns$.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF, and $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
14. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} (MAX) limit, t_{AA} and t_{CAC} must always be met.
15. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} and t_{CAC} must always be met.
16. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
17. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
19. OE# is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. Column address changed once each cycle.
22. 16MB module values will be half of those shown.



READ CYCLE



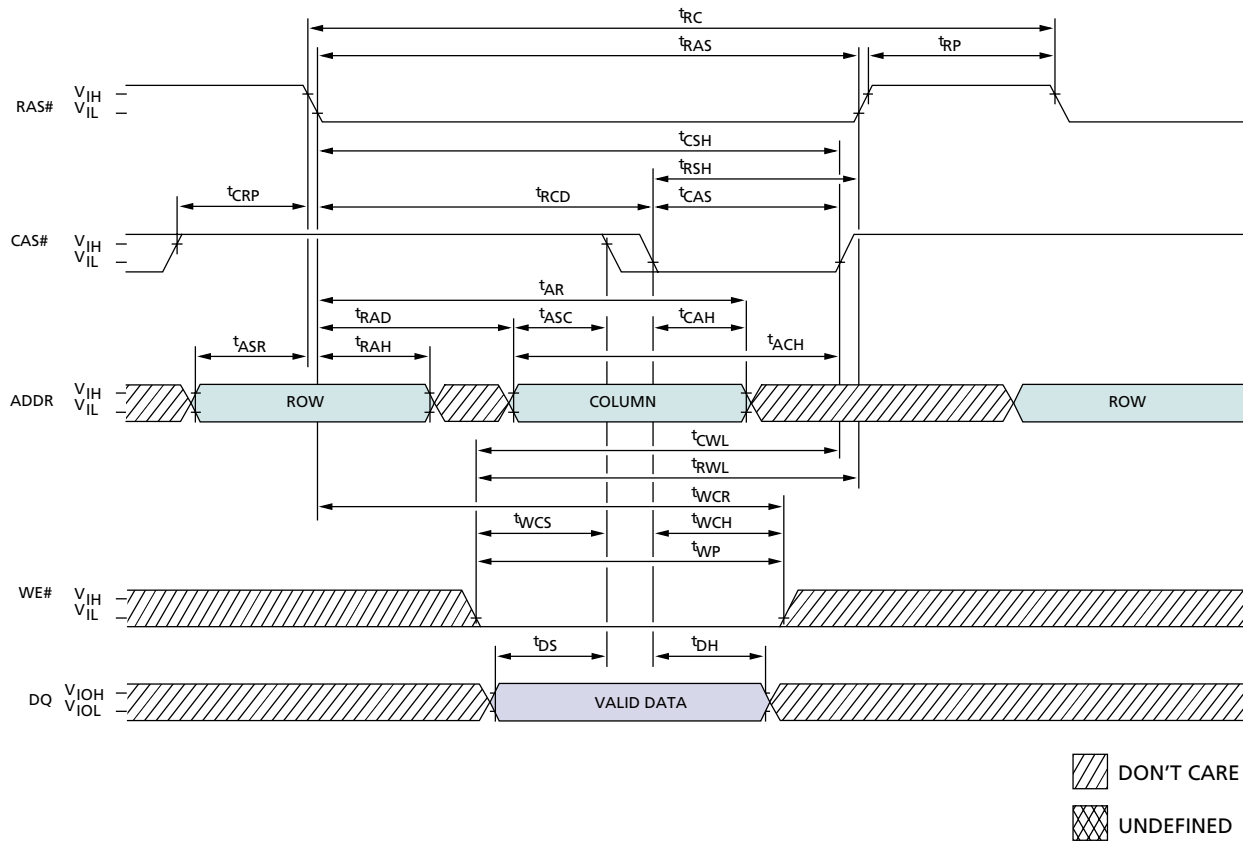
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{OFF}	0	12	0	15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	84		104		ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

NOTE: 1. t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE



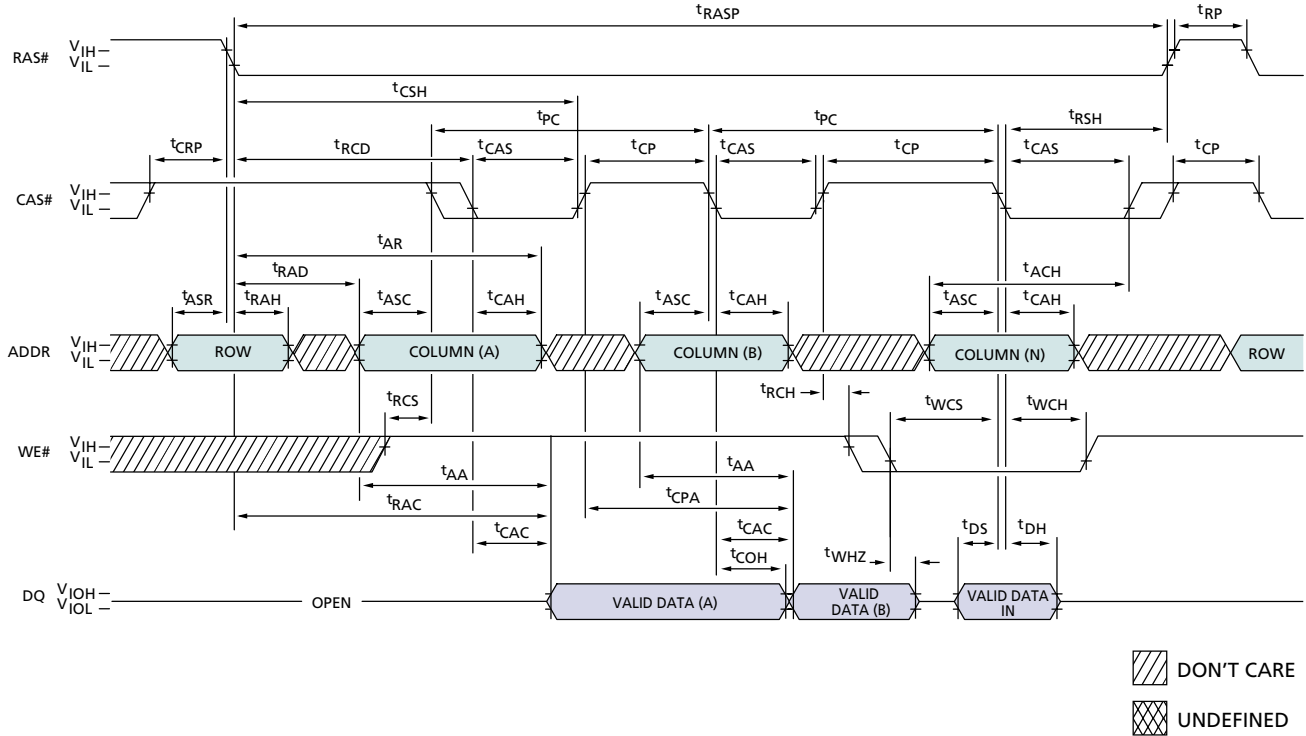
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns
t_{RAD}	9		12		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	84		104		ns
t_{RCD}	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR}	38		45		ns
t_{WCS}	0		0		ns
t_{WP}	5		5		ns



EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



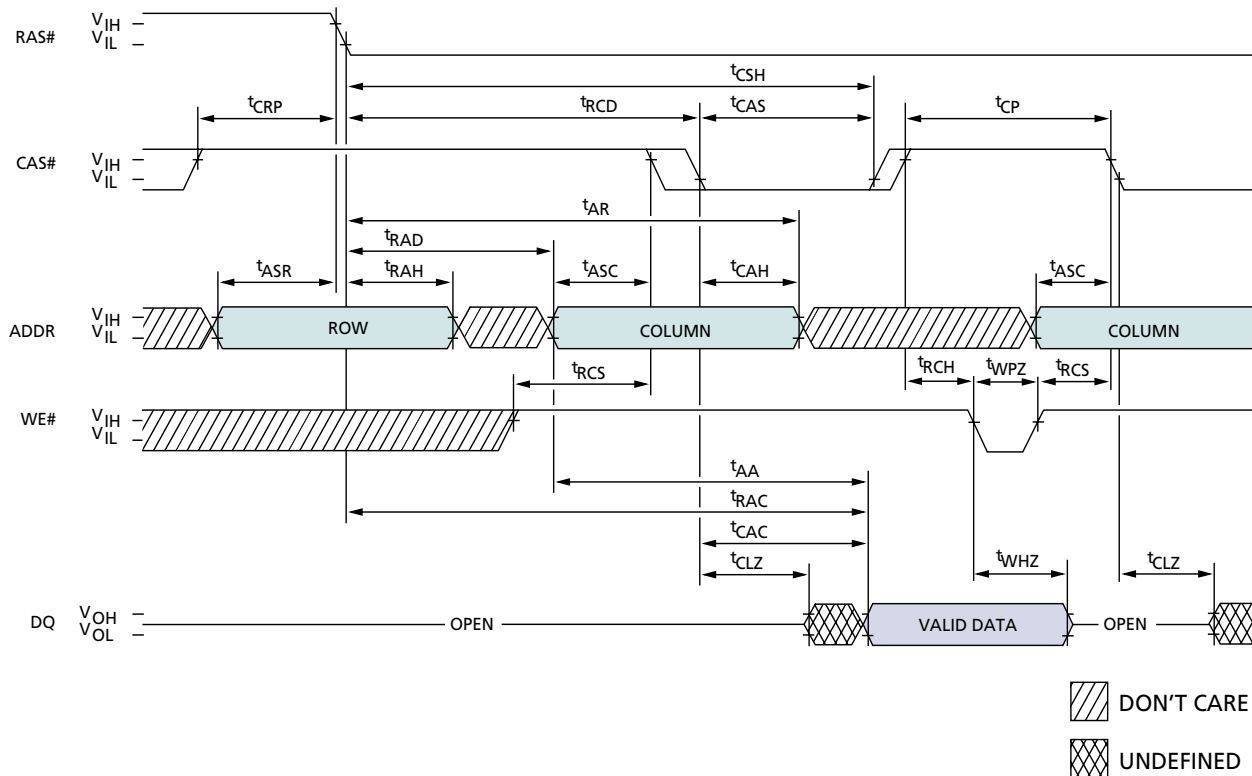
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tDS	0		0		ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns



EDO READ CYCLE
(with WE#-controlled disable)



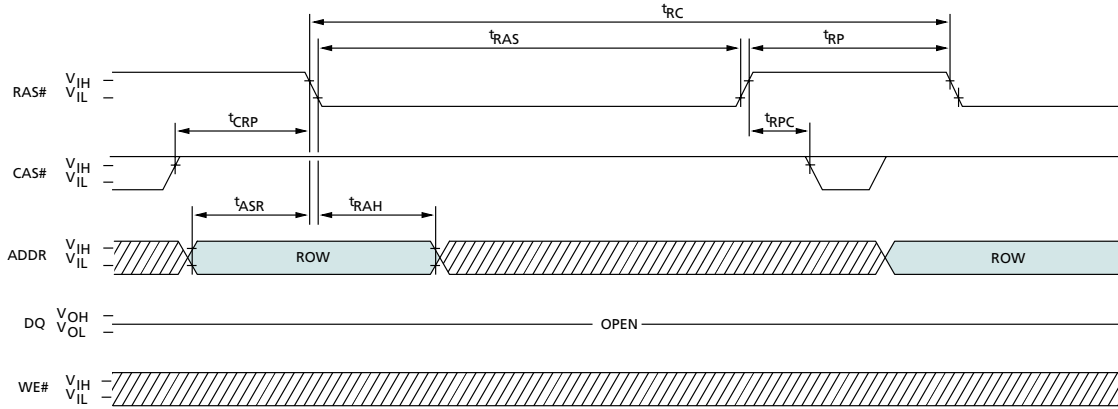
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CP}	8		10		ns
t_{CRP}	5		5		ns

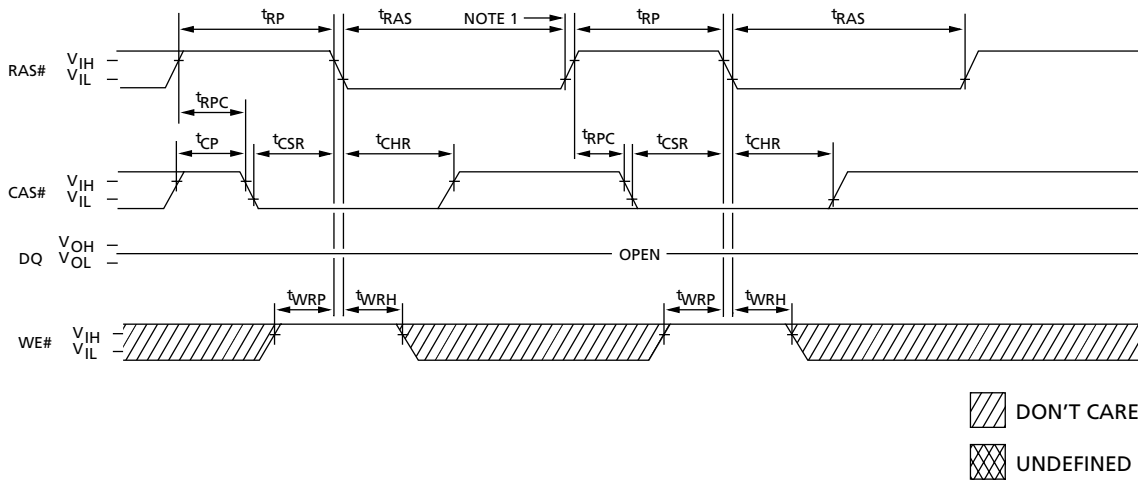
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{CSH}	38		45		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{WHZ}	0	12	0	15	ns
t_{WPZ}	10		10		ns



RAS#-ONLY REFRESH CYCLE



CBR REFRESH CYCLE
(Addresses = DON'T CARE)



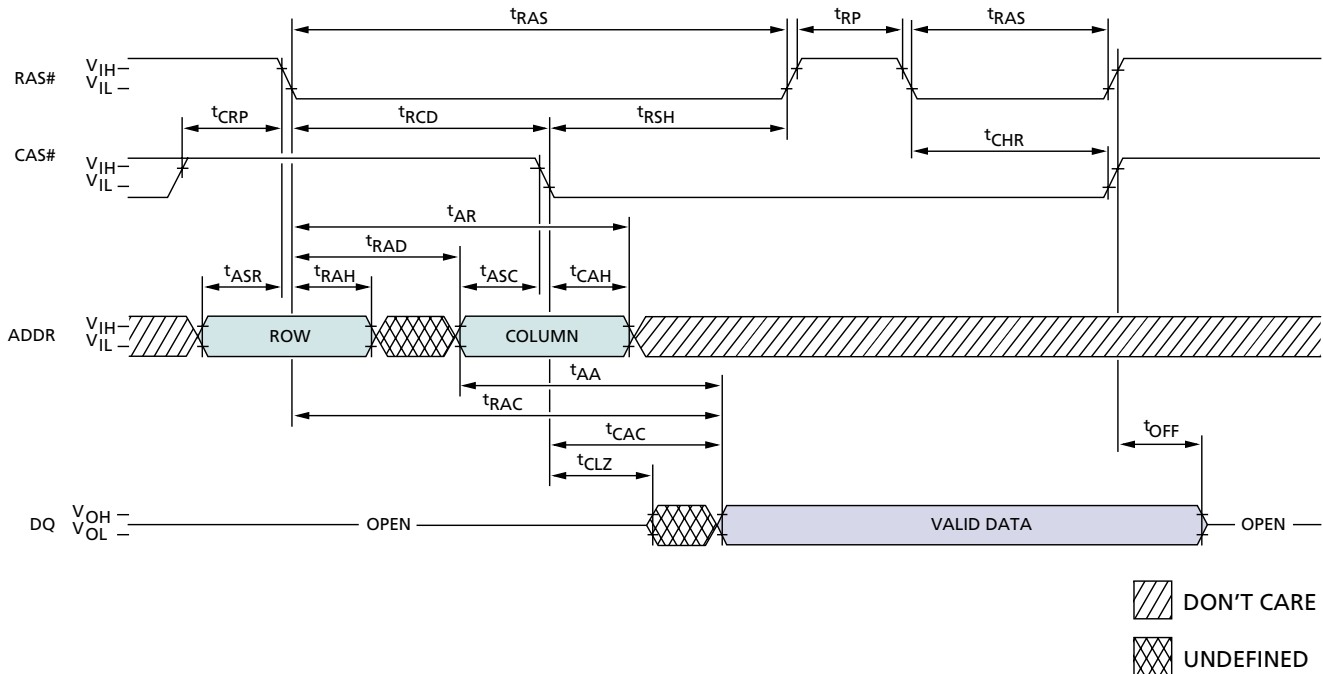
DON'T CARE
 UNDEFINED

TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	0		0		ns
t _{CHR}	8		10		ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSR}	5		5		ns
t _{RAH}	9		10		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RAS}	50	10,000	60	10,000	ns
t _{RC}	84		104		ns
t _{RP}	30		40		ns
t _{RPC}	5		5		ns
t _{WRH}	8		10		ns
t _{WRP}	8		10		ns

HIDDEN REFRESH CYCLE ²⁰
(WE# = HIGH)



TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		13		15	ns
t _{CAH}	8		10		ns
t _{CHR}	8		10		ns
t _{CLZ}	0		0		ns
t _{CRP}	5		5		ns

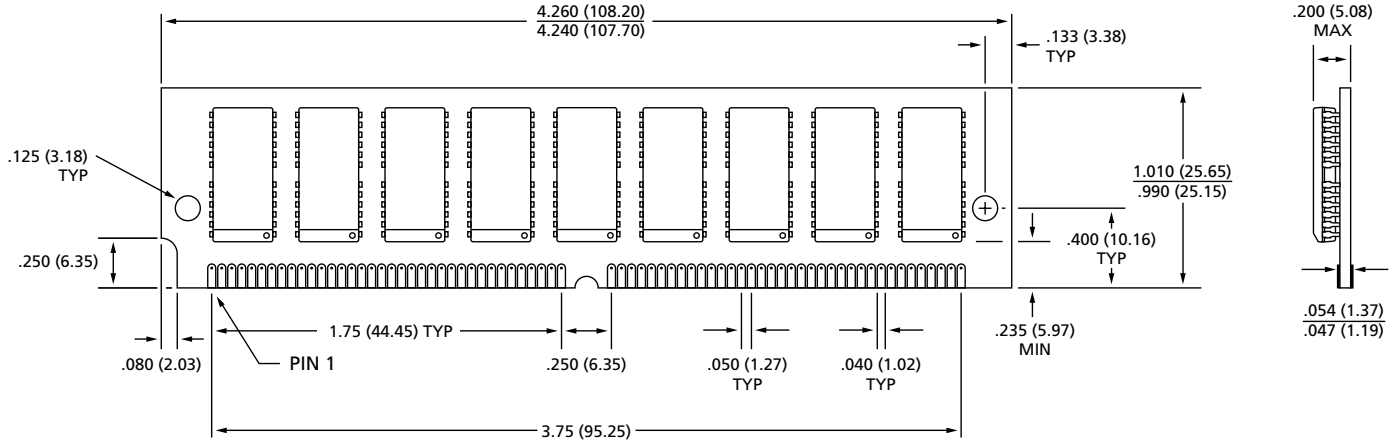
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OFF}	0	12	0	15	ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RCD}	11		14		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns

NOT RECOMMENDED FOR NEW DESIGNS

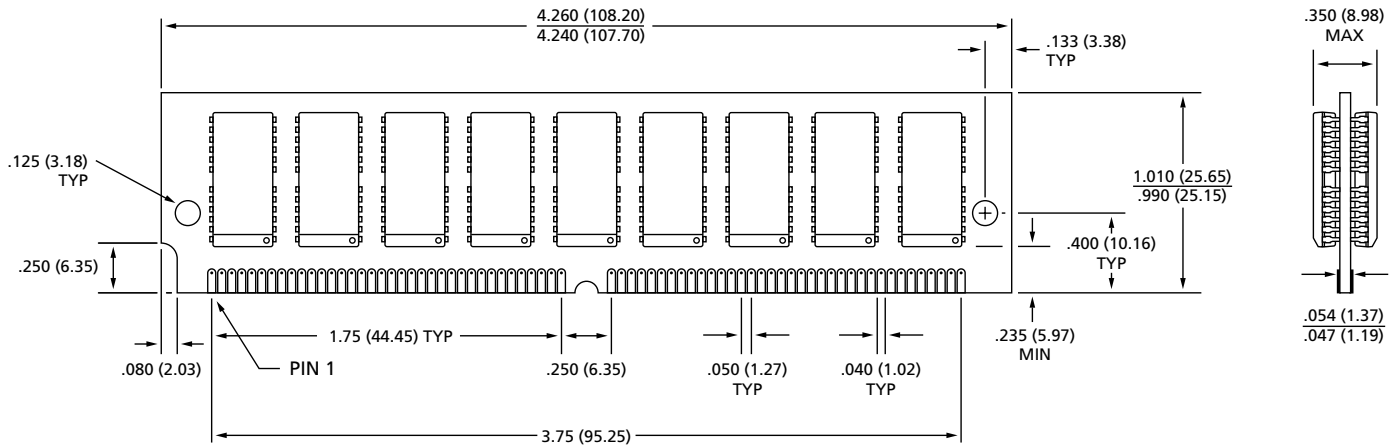


4, 8 MEG x 36
ECC-OPTIMIZED DRAM SIMMs

72-Pin SIMM (16MB)



72-Pin SIMM (32MB)



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