MT1020A

Bluetooth™ Baseband Controller

Product Brief

PB5630 ISSUE 2.0 September 2001

Ordering Information

MT1020A/IG/BP1N 121-pin SSBGA

Features

- *Bluetooth* v1.1 compliant Link Controller
- Programmable Radio Interface including BlueRF
- Full *Bluetooth* Protocol Stack up to HCI
- Full Duplex Audio CODEC including filtering
- Linear PCM to log PCM and CVSD conversion
- Advanced Block Power Management
- Embedded ARM7TDMI™ Microcontroller Core
- Configurable I/O supply 1.8 to 3.6V
- 1.8V internal supply option for Low Power
- IP Hardware and Software available for embedded applications
- Single CPU *Bluetooth* system capability

Applications

- Wireless Headsets
- Wireless Accessories
- Cellular Phones
- Automotive
- PDA, Laptop Computers
- Digital Cameras

Description

The MT1020A is a complete *Bluetooth* baseband processor It combines an advanced ARM7TDMI based microcontroller with on-chip memory, a full duplex voice CODEC and a dedicated *Bluetooth* Baseband Peripheral (BBP) block.

The BBP implements all the time-critical elements of *Bluetooth* communication in hardware, with minimal involvement by the microcontroller. Relieving the on-chip processor of these repetitive tasks makes it possible for the MT1020A to run entire applications without an external host processor. A UART Interface is provided for use when operation with an an external host processor is required.

Comprehensive power management maximises battery life for portable applications making the MT1020A particularly suitable for low power applications, especially those involving voice traffic.

Absolute Maximum Ratings

Supply voltage (VDD)	-0.5V to +5V
Input voltage	-0.5V to OpV_{DD} +0.5V
Output voltage	-0.5V to OpV_{DD} +0.5V
Static discharge (HBM)*	2kV
Storage temperature, TSTG	-55°C to +150°C

* Human Body Model

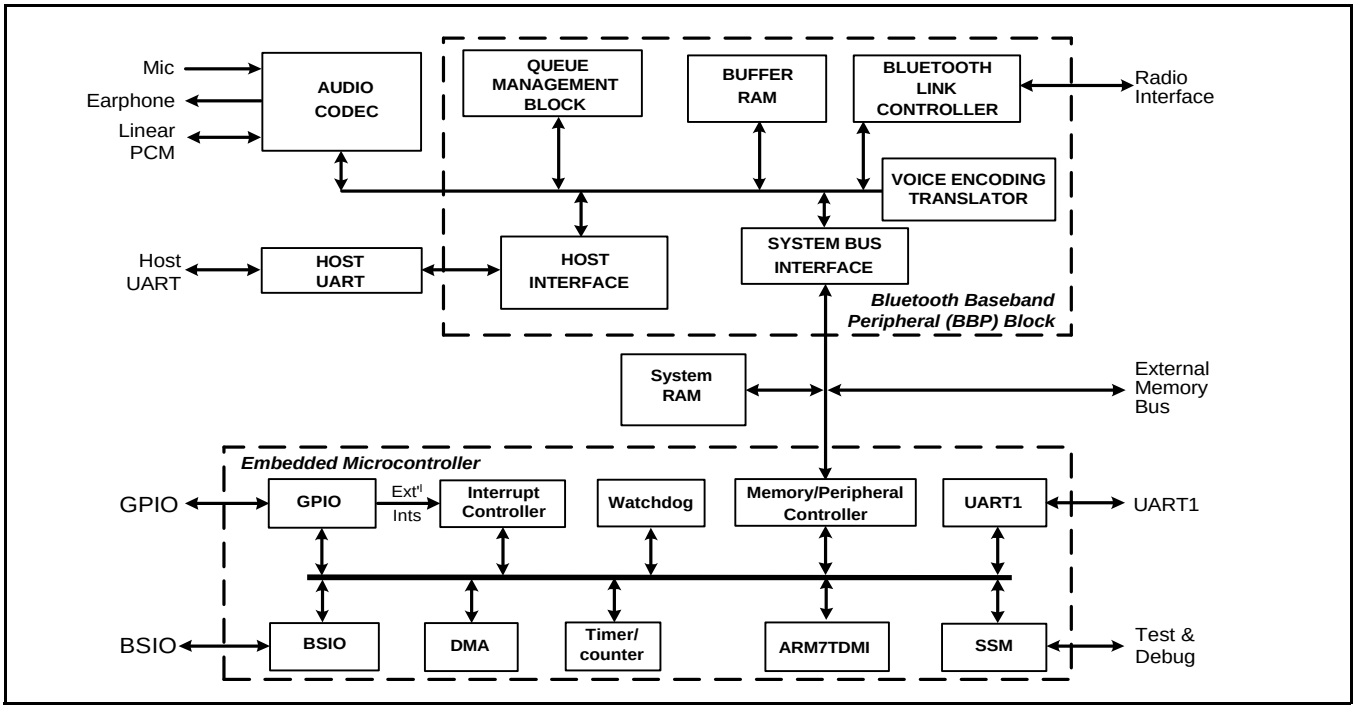


Figure 1 - MT1020A Block Diagram

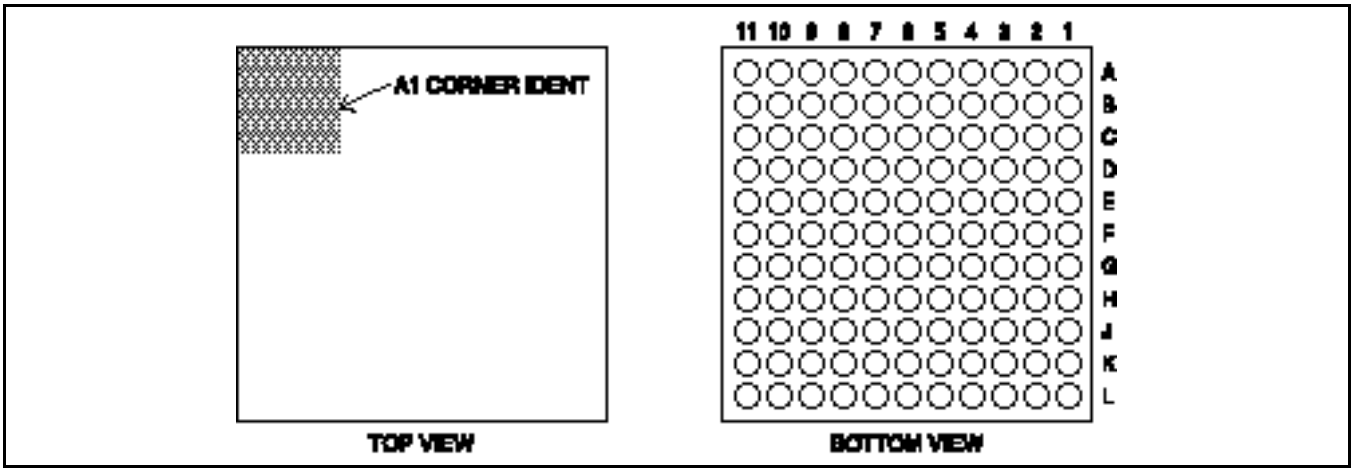


Figure 2 - Pin Connections

Signal Name	Pin (see notes)	I/O Type	Qty	Description
Memory/Peripheral Interface				
SADD[18:0]	A8: A9: C8: D3: E4: G10: G8: G9: H10: H4: H9: J1: J2: J4: K1: K2: K4: L3: L4	O(hd)	19	System Address
SDATA[15:0]	C9: F7: B9: C6: B1: C7: D4: D7: F9: D8: B8: E7: D6: C3: C2: B7	I/O(hd)	16	System Data Bus
NSCS[1:0]	B6: E6	O(hd)	2	Active low System Chip Select 1 and 0
NSCS[3]	A1	O(hd)	1	Active low System Chip Select 3
NSWE[1:0]	K3: L2	O(hd)	2	Active low System Write Enable 1 and 0
NSOE	B5	O(hd)	1	Active low System output enable
NSUB	D2	O	1	Active low System Upper Byte (for 16-bit RAM)(SADD[0] = lower byte)
SWAIT	F10	I(pd)	1	System Wait. Extended MPC access
UART1				
U1RXD	F3	I(hd)	1	UART1 Receive Data
U1TXD	E3	O	1	UART1 Transmit Data
U1RTS	F4	O	1	UART1 Ready to Send (active low[1])
U1CTS	E2	I(hd)	1	UART1 Clear to Send (active low[1])
Host Interfaces				
HST_UART_RXD	C5	I(hd)	1	Serial Host Interface Receive Data

Table 1 - Pin Descriptions

Signal Name	Pin (see notes)	I/O Type	Qty	Description
HST_UART_TXD	D5	O	1	Serial Host Interface Transmit Data
HST_UART_RTS	C4	O	1	Serial Host Interface Ready to Send
HST_UART_CTS	A3	I/O(hd)	1	Serial Host Interface Clear to Send
Reserved	A2	I/O	1	**Tie to OPVDD**
Reserved	B3	I/O	1	**Tie to GND**
Serial I/O				
BSIO_SS	C10	O	1	Serial I/O Block Slave Select
BSIO_DATA_O	B11	O	1	Serial I/O Block Data Output
BSIO_DATA_I	B10	I(hd)	1	Serial I/O Block Data Input
BSIO_CLK	A11	O	1	Serial I/O Block Clock Output
General Purpose IO				
GPIO[7] EXTINT[2]	F8	I/O(hd)	1	General purpose I/O plus External interrupt 2 input
GPIO[6] EXTINT[1]	F6	I/O(hd)	1	General purpose I/O plus External interrupt 1 input
GPIO[5]	E10	I/O(hd)	1	General purpose I/O plus
GPIO[4]	E9	I/O(hd)	1	General purpose I/O plus
GPIO[3]	E8	I/O(hd)	1	General purpose I/O plus
GPIO[2] INTNSCS0	D10	I/O(hd)	1	General purpose I/O During reset input selects int/ext NSCS0
GPIO[1] BBPWAKE	D9	I/O(hd)	1	General purpose I/O plus Optional external BBP wake up input
GPIO[0]	C11	I/O(hd)	1	General purpose I/O
Mode Control				
NICE	J9	I(pu)	1	Diagnostic or ICE mode ('0' = ICE mode)
NTRST	J3	I(pu)	1	Xpins/diag. Mode or ICE reset
TEST	H8	I(pd)	1	Test enable **DO NOT CONNECT**
NSRESET	H11	I	1	System reset
Diagnostics				
TCK BDIAG[0]	G5	I/O	1	ICE Test clock input or Xdiag[0] output
TDI BDIAG[1]	H2	I/O	1	ICE Test data input or Xdiag[1] output
TDO BDIAG[2]	G4	O	1	ICE Test data output or Xdiag[2] output
TMS BDIAG[3]	H3	I/O	1	ICE Scan test mode input or Xdiag[3] output

Table 1 - Pin Descriptions (continued)

Signal Name	Pin (see notes)	I/O Type	Qty	Description
Radio Interface				
RI_SYS_CLK	L7	I	1	System Clock Input
RI_CTR3	J7	I/O	1	Bi-directional Radio Interface Control Signal 3
RI_TXDRXD	G6	I/O(hd)	1	Radio Transmit Data Output. (Receive Data input in Bi-Di pin mode)
RI_RXD	L5	I	1	Radio Receive Data Input (Uni-directional pin mode)
RI_NRESET	K8	I/O(pu)	1	Radio Reset
RI_CTR2	G7	I/O	1	Bi-directional radio interface control signal 2
RI_NSEN	H7	O	1	Active low radio serial interface enable
RI_SBBO	L6	I/O	1	Radio Serial Transfer Data Output
RI_SBBI	J6	I	1	Radio Serial Transfer Data Input
RI_SCLK	H6	O	1	Radio Serial Transfer Clock
RI_CTR1	H5	I/O(pd)	1	Bi-directional Radio Interface Control Signal 1
RI_CTR0	J5	O	1	Bi-directional Radio Interface Control Signal 0
Linear PCM Interface				
LIN_PCM_IN	F2	I(hd)	1	16bit Linear PCM Input stream
LIN_PCM_OUT	F5	O	1	16bit Linear PCM Output stream
LIN_PCM_FRM	G3	I/O(hd)	1	16bit Linear PCM Frame Sync Master / Slave
LIN_PCM_CLK	G2	I/O(hd)	1	16bit Linear PCM Clock Master / Slave
CODEC Interface				
EAR_PLUS	J11	AO	1	Earpiece audio positive differential output
EAR_MINUS	J10	AO	1	Earpiece audio negative differential output
MIC_MINUS	L9	AI	1	Microphone audio negative differential input
MIC_PLUS	K9	AI	1	Microphone audio positive differential input
VREF	K10	AO	1	Audio CODEC Vref decoupling capacitor pin; 100nF to AGND
PLL Analogue Test				
PLL_AT1	E5		1	Phase Lock Loop 1 Analogue Test Pin **DO NOT CONNECT**
Power Supplies				
GNDP	L11		1	CODEC Output amplifier ground
VDDP	K11		1	CODEC Output amplifier VDD
GND	A6: B2: D1: D11: F1: G11: K6		7	Common Ground
VDDA	L8		1	CODEC Analog VDD

Table 1 - Pin Descriptions (continued)

Signal Name	Pin (see notes)	I/O Type	Qty	Description
SUBGND	A4: A10: J8: L1: L10		5	Analog Ground
OPVDD	A7: C1: F11: H1		4	System I/O VDD
RIVDD	K5		1	Radio Interface VDD
LAVDD	A5: E1: E11: G1: K7		5	Core VDD
PLL_VDD	B4		1	Phase Lock Loop VDD

Table 1 - Pin Descriptions (continued)

Note:

The UART CTS and RTS signals(U1RTS, U1CTS, HST_UART_RTS & HST_UART_CTS) are all active low at the chip, but become active high after passing through a RS232 line driver IC.

Key to Signal Types:

I input
O Output
I/O Bidirectional
pu Internal Pull-up
pd Internal Pull-down
hd Internal Peripheral HOLD cell: holds the previous voltage level of an input, until the weak drive of the hold cell is overdriven by normal drive output. This can be either as part of a MT1020A bi-directional peripheral cell or an external device.

Electrical Characteristics

These characteristics are guaranteed by either production test or design.
They apply within the specified ambient temperature and supply voltage ranges, unless otherwise stated.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
DC Characteristics					
Logic supply voltage	1.8		3.6	V	T_{AMB}= -40°C to +85°C
CODEC supply voltage	2.7		3.6	V	
Supply current		40		µA	
Dynamic Power Consumption					
SCO connection HV3 packets utilising 1s interval sniff. Internal CODEC.		18		mW	VDDA, VDDP, RIVDD & OPVDD =3.0V LAVDD =2.0V Temperature 25°C System clock and BBP clock frequency = 5 MHz.
SCO connection HV1 packets utilising 1s interval sniff. Internal CODEC.		19		mW	
ACL connection utilising 1s interval sniff, no data transfer.		12		mW	

Normal Operating Conditions

Characteristic	Value		Units
	Min.	Max.	
Core supply voltage, LAVDD	1.8	3.6	V
I/O supply voltage, OPVDD	1.8	3.6	V
Radio Interface supply voltage, RIVDD	1.8	3.6	V
CODEC supply voltages, VDDP & VDDA	2.7	3.6	V
Input voltage	0.0	OpV_{DD}	V
Output voltage	0.0	OpV_{DD}	V
DC current per bond pad	-	30	mA
Ambient temperature	-40	+85	°C

Circuit Description

General

The MT1020A is a complete *Bluetooth* Baseband processor. When used with the Zarlink-supplied firmware and an appropriate radio transceiver it forms a complete low power *Bluetooth* solution.

The MT1020A features :

- ARM7TDMI Embedded Microcontroller
- Dedicated *Bluetooth* Baseband Peripheral block
- Full Duplex Audio CODEC
- 20KB System RAM

Low Power Architecture

The architecture is designed for ultra low power applications. This is achieved by:

- Minimising the processor overhead, allowing internal system clock speeds to be reduced to as low as 5MHz
- Having a dedicated *Bluetooth* bus for data packet DMA transfers
- A system partition that decodes *Bluetooth* packets in hardware
- Operating internal core with a 2V supply
- Low-power CODEC for voice applications

Bluetooth Baseband Peripheral

The *Bluetooth* Baseband Peripheral (BBP) sub system performs all time critical *Bluetooth* operations, with minimal processor overhead. It works as a slave peripheral device connected to the on-board Microprocessor.

The block includes the Link Controller hardware required to communicate with other *Bluetooth* devices via a radio IC, a queue manager system with RAM to store packets of data, a host interface and a CODEC. Once configured, the *Bluetooth* Baseband Peripheral block can automatically transport packets between a host interface and the *Bluetooth* radio, without interaction with the processor

Bluetooth Link Controller

The *Bluetooth* Link Controller controls the *Bluetooth* radio. The Link controller has a programmable Radio interface enabling it to work with a number of different *Bluetooth* Radio Transceivers. Within the Link Controller payload data is assembled into data packets for transmission and extracted from received data. Packets are assembled/decoded with preamble, sync words, headers and CRCs. Data whitening is performed; encryption is optional.

Queue Manager Block

This block performs intelligent DMA transfers between a dedicated *Bluetooth* data buffer RAM and the *Bluetooth* link controller, the host interface and the voice interface. It understands and translates between different *Bluetooth* packet formats, and performs payload data queue management. The MT1020A has 12KB of Data Buffer RAM.

Host Interface

The host interface manages the communication between the MT1020A and an external host processor. It handles the assembly and decoding of Host Controller Interface (HCI) packets. The MT1020A supports communication with the external host using a high speed host UART.

Audio CODEC

The full duplex CODEC includes a microphone amplifier and earpiece driver, together with filtering to ITU-T G712.

Embedded Microcontroller Core

The Embedded Microcontroller, in addition to configuring and controlling the *Bluetooth* Baseband Peripheral block, has the capability to run complete applications, including the *Bluetooth* Protocol Stacks. This capability eliminates the need for an external host processor, making the MT1020A particularly suitable for stand-alone applications, where an external processor is not available.

The Microcontroller consists of an ARM7TDMI CPU and the following general purpose peripheral blocks :

- Peripheral Controller
- Serial I/O
- Interrupt Controller
- 2 Counter/Timers
- DMA Controller
- UART

ARM7TDMI Processor

The ARM7TDMI RISC processor contains the ARM7 32-bit core and with the Thumb® instruction decompressor supporting 16-bit instructions, debug extensions, fast multiplier and the ICEBreaker™ extension.

Memory/Peripheral Controller

The Memory/Peripheral Controller (MPC) is the main gateway between the internal and external bus systems. It allows dynamic bus sizing and generates all control signals to access peripheral components.

The MPC also supports fly-by DMA between all combinations of internal and external modes.

Serial I/0

The Serial (BSIO) I/0 block supports the serial interface to a variety of external devices, such as serial EEPROM, NVRAM and Flash. It is compatible with two common interfaces:

- MICROWIRE™ for use with memory and peripheral devices supporting the MICROWIRE standard
- SPI microcontroller serial interface

The block operates in either Interrupt or Polled modes also supports Fly-by DMA transfers.

Interrupt Controller (INTC)

The ARM7TDMI core accepts two types of interrupt: Normal (IRQ) and Fast (FIQ). All Interrupts can be switched between types, depending upon the relative priorities required. The INTC is the central control logic that decodes the priority level and handles interrupt request signals from a total of 8 fixed predefined sources within the microcontroller core and two external sources, Gpio<7:6>. External interrupts can be set for edge or level sensitivity with a polarity option. To minimize interrupt latency, there is a hard-wired priority scheme for each channel for both FIQ and IRQ; alternatively this can be ignored and the priority assessment handled in software.

Timers

Two dual independent 32-bit timer/counters, with an 8-bit prescaler capability for each counter, are provided (Timers 1A, 1B, 2A and 2B). These are synchronous to the system clock and may be polled, or set up to generate interrupts on over-run, with auto-reload.

DMA Controller

Two DMA engines are available in the controller. These may be configured as a pair to provide a memory-to-memory DMA capability between any two locations in the ARM7TDMI memory space. Alternatively, they may be used independently for fly by transfers between off-core requesters and either on-core or off-core locations. Single or multiple byte transfers (Demand or Burst Mode) are supported and may be word, half-word or byte wide.

Universal Asynchronous Receiver Transmitter (UART1)

The full duplex asynchronous channel provides an RS232 type interface, which supports both hardware handshaking and XON/XOFF software protocols. The Receive and Transmit channels are double buffered. UART1 may be polled, or may use an interrupt scheme for module bus transfers. An internal baud rate generator can provide selectable data rates, derived from on-chip sources for an Rx/Tx pair. Directly triggered DMA transfers with the UART are also possible without the need for CPU intervention.

System Debug Options

The microcontroller core allows for two sophisticated methods of hardware and software debug. The designer should choose which methods are required. The options are:

- ARM7TDMI™ Debug Interface, via the ARM MultiICE™ module, or equivalent
- Logic Analyser coupled with an Inverse Assembler and Zarlink's Diagnostic Broadcast feature

Baseband Protocol Stack

The MT1020A is supplied with the Zarlink baseband protocol stack software. This stack, when used in conjunction with the *Bluetooth* Baseband Peripheral block, implements the *Bluetooth* Specification v1·1 up to the HCI layer. Features of the Stack include :

Link Controller

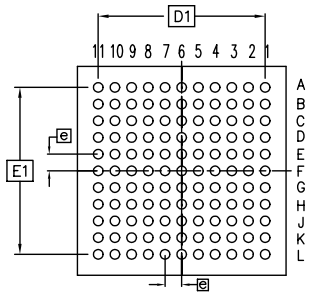
The Link Controller includes multi-point capability, support for multi-slot packets, and Authentication and Encryption.

Link Manager

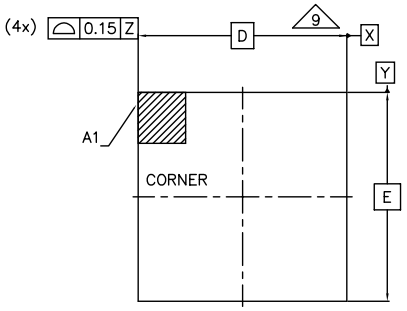
Supports Park, Hold and Sniff modes for reduced power consumption.

Host Controller Interface

Operates a UART interface, supporting ACL (asynchronous) and SCO (synchronous) data types.

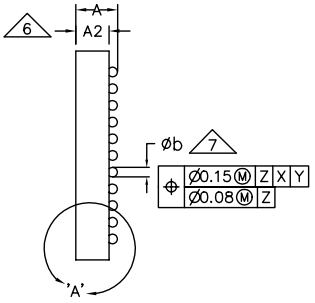


BOTTOM VIEW

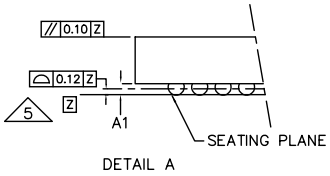


TOP VIEW

DIMENSION	MIN	NOM	MAX
A	1.22	1.36	1.50
A1	0.31	0.36	0.41
A2	0.91	1.00	1.09
D		10.00 BSC	
D1		8.00 BSC	
E		10.00 BSC	
E1		8.00 BSC	
b	0.41	0.46	0.51
e		0.80 BSC	
N		121	
		2 LAYERS	
Conforms to JEDEC MO-205 BC iss. D			



SIDE VIEW



DETAIL A

NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. Not To Scale.
4. CONTACT BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
5. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS DIMENSION INCLUDES STAND–OFF HEIGHT "A1", PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL HEAT SINK OR CHIP CAPACITORS. AN INTEGRAL HEAT SLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
7. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -Z-.
8. A1 CORNER MUST BE IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE, AND METALLIZED MARKINGS ON BOTTOM PACKAGE
9. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
10. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.

						ORIGINATING SITE: Swindon
ISSUE	1	2				Title: Outline for 121 SSBGA(10 x 10)mm (BP)
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DATE	5APR00	11JUL00				Drawing Number GPD00723
APPRD.						

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