

Surface Mount P-Channel Enhancement Mode MOSFET

(Pb) Lead(Pb)-Free

Features:

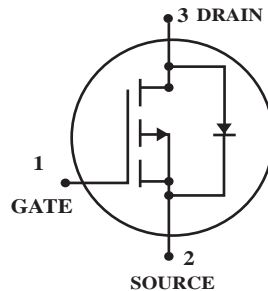
*Super high dense cell design for low $R_{DS(ON)}$

$R_{DS(ON)} < 75 \text{ m}\Omega @ V_{GS} = -10\text{V}$

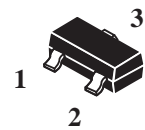
$R_{DS(ON)} < 100 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$

*Rugged and Reliable

*SOT-23 Package



DRAIN CURRENT
- 3 AMPERES
DRAIN SOURCE VOLTAGE
- 30 VOLTAGE



SOT-23

Maximum Ratings (TA=25°C Unless Otherwise Specified)

Rating	Symbol	Value	Unite
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 125^\circ\text{C}$) ⁽¹⁾	I_D	-3	A
Pulsed Drain Current ⁽²⁾	I_{DM}	-10	A
Drain-Source Diode Forward Current (1)	I_S	-1.25	A
Power Dissipation (1)	P_D	1.25	W
Maximax Junction-to-Ambient	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Device Marking

WT3401=T01

Electrical Characteristics ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Static (2)

Drain-Source Breakdown Voltage $V_{GS}=0V, I_D=-250\ \mu\text{A}$	$V_{(BR)DSS}$	-30	-	-	V
Gate-Source Threshold Voltage $V_{DS}=V_{GS}, I_D=-250\ \mu\text{A}$	$V_{GS(th)}$	-1	-1.5	-2.5	V
Gate-Source Leakage Current $V_{DS}=0V, V_{GS}=\pm 20V$	I_{GSS}	-	-	± 100	nA
Zero Gate Voltage Drain Current $V_{DS}=-24V, V_{GS}=0V$	I_{DSS}	-	-	-1	μA
Drain-Source On-Resistance $V_{GS}=-10V, I_D=-3.0\text{A}$ $V_{GS}=-4.5V, I_D=-2.0\text{A}$	$r_{DS(on)}$	- -	- -	75 100	$\text{m}\Omega$
On-State Drain Current $V_{DS}=-5V, V_{GS}=-10\text{A}$	$I_{D(on)}$	6	-	-	A
Forward Transconductance $V_{DS}=-5V, I_D=-3\text{A}$	g_{fs}	5	-	-	S

Dynamic (3)

Input Capacitance $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	C_{iss}	-	653	-	PF
Output Capacitance $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	C_{oss}	-	130	-	
Reverse Transfer Capacitance $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	C_{rss}	-	97	-	

Switching (3)

Turn-On Delay Time $V_{GS}=-10V, V_{DD}=-15V, I_D=-1\text{A}, R_L=15\ \Omega, R_{GEN}=6\ \Omega$	$t_{d(on)}$	-	13	-	nS
Rise Time $V_{GS}=-10V, V_{DD}=-15V, I_D=-1\text{A}, R_L=15\ \Omega, R_{GEN}=6\ \Omega$	t_r	-	7	-	nS
Turn-Off Delay Time $V_{GS}=-10V, V_{DD}=-15V, I_D=-1\text{A}, R_L=15\ \Omega, R_{GEN}=6\ \Omega$	$t_{d(off)}$	-	58	-	nS
Fall Time $V_{GS}=-10V, V_{DD}=-15V, I_D=-1\text{A}, R_L=15\ \Omega, R_{GEN}=6\ \Omega$	t_f	-	26	-	nS
Total Gate Charge $V_{DS}=-15V, I_D=-3\text{A}, V_{GS}=-10V$	Q_g	-	13.5	-	nc
Total Gate Charge $V_{DS}=-15V, I_D=-3\text{A}, V_{GS}=-4.5V$	Q_g	-	7	-	nc
Gate-Source Charge $V_{DS}=-15V, I_D=-3\text{A}, V_{GS}=-10V$	Q_{gs}	-	2.3	-	nc
Gate-Drain Charge $V_{DS}=-15V, I_D=-3\text{A}, V_{GS}=-10V$	Q_{gd}	-	2.8	-	nc
Drain-Source Diode Forward Voltage $V_{GS}=0V, I_S=-1.25\text{A}$	V_{SD}	-	-0.8	-1.2	V

- Note: 1. Surface Mounted on FR4 Board $t \leq 10\text{sec}$.
 2. Pulse Test : $PW \leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
 3. Guaranteed by Design, not Subject to Production Testing.

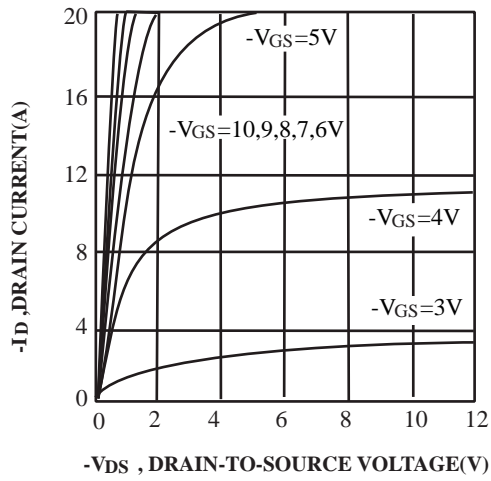


FIG.1. Output Characteristics

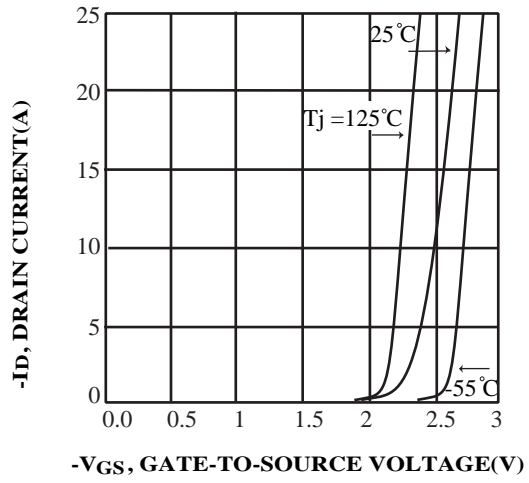


FIG.2 Transfer Characteristics

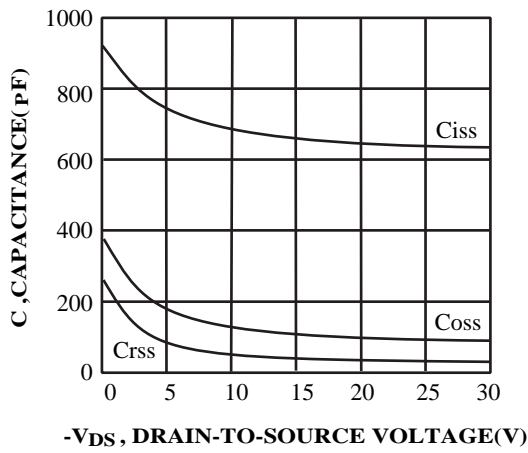


FIG.3 Capacitance

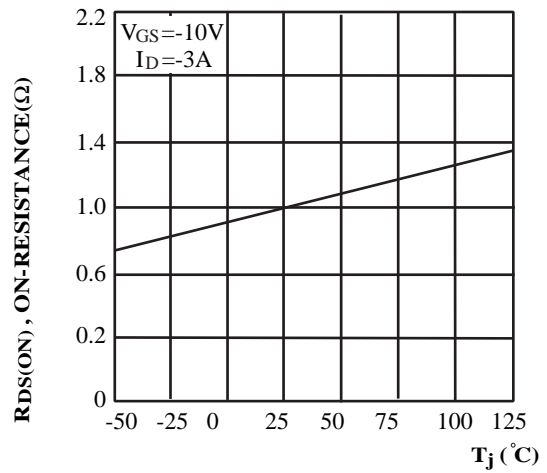


FIG.4 On-Resistance Variation with Temperature

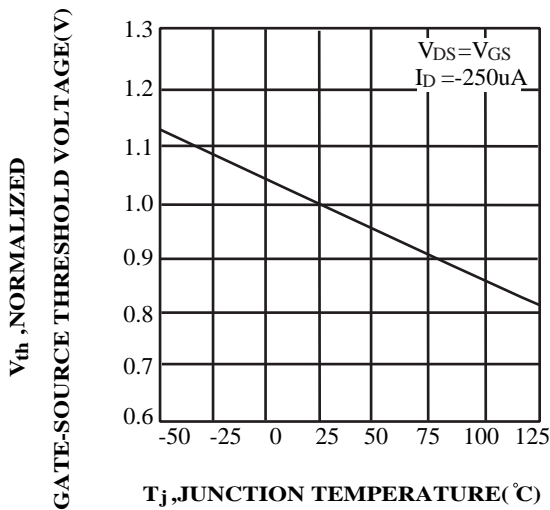


FIG.5 Gate Threshold Variation with Temperature

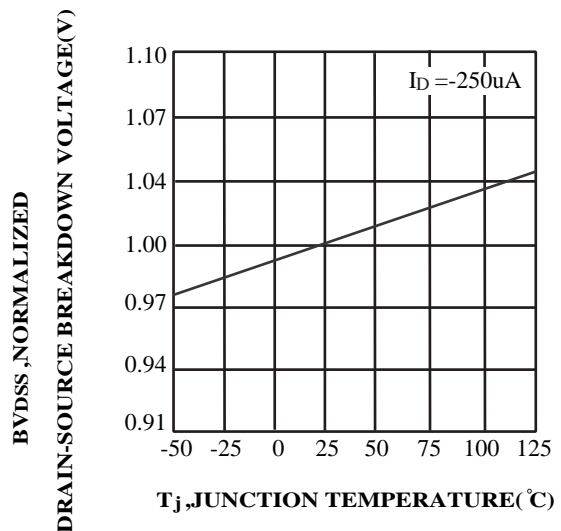
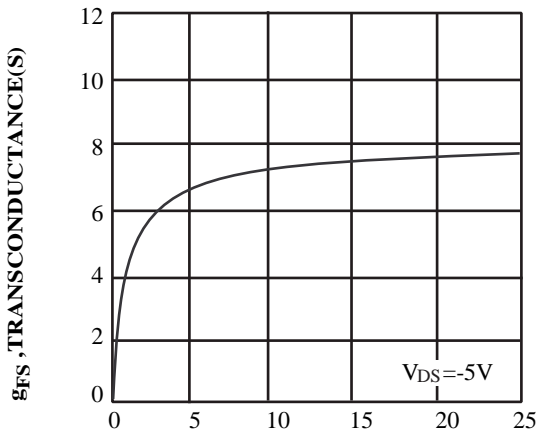
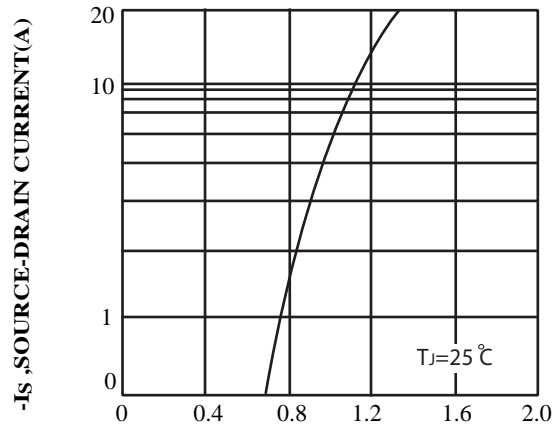


FIG.6 Breakdown Voltage Variation with Temperature



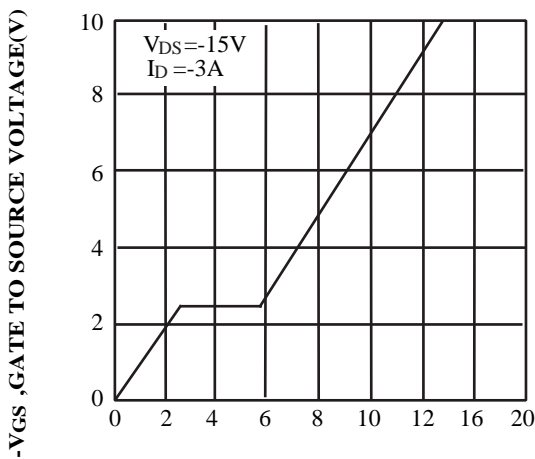
-IDS ,DRAIN-SOURCE CURRENT(A)

FIG.7 Transconductance Variation with Drain Current



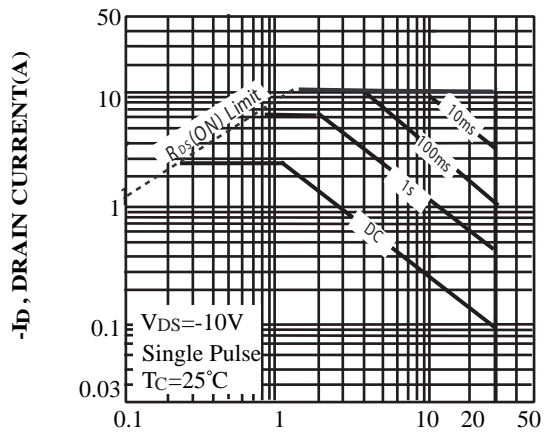
-VSD ,BODY DIODE FORWARD VOLTAGE(V)

FIG.8 Body Diode Forward Voltage Variation with Source Current



Qg ,TOTAL GATE CHARGE(nC)

FIG.9 Gate Charge



-VDS ,DRAIN-SOURCE VOLTAGE(V)

FIG.10 Maximum Safe Operating Area

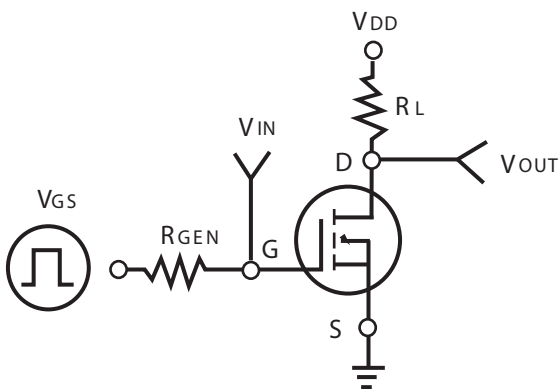


FIG.11 Switching Test Circuit

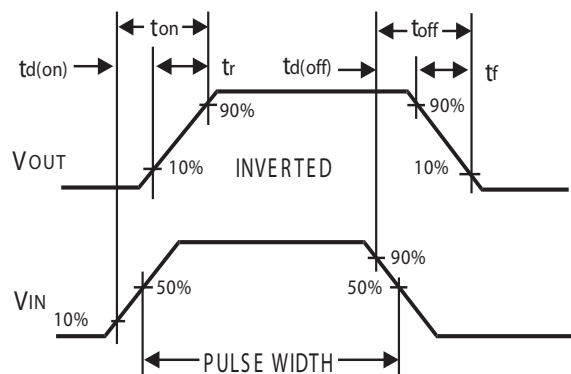


FIG.12 Switching Waveforms

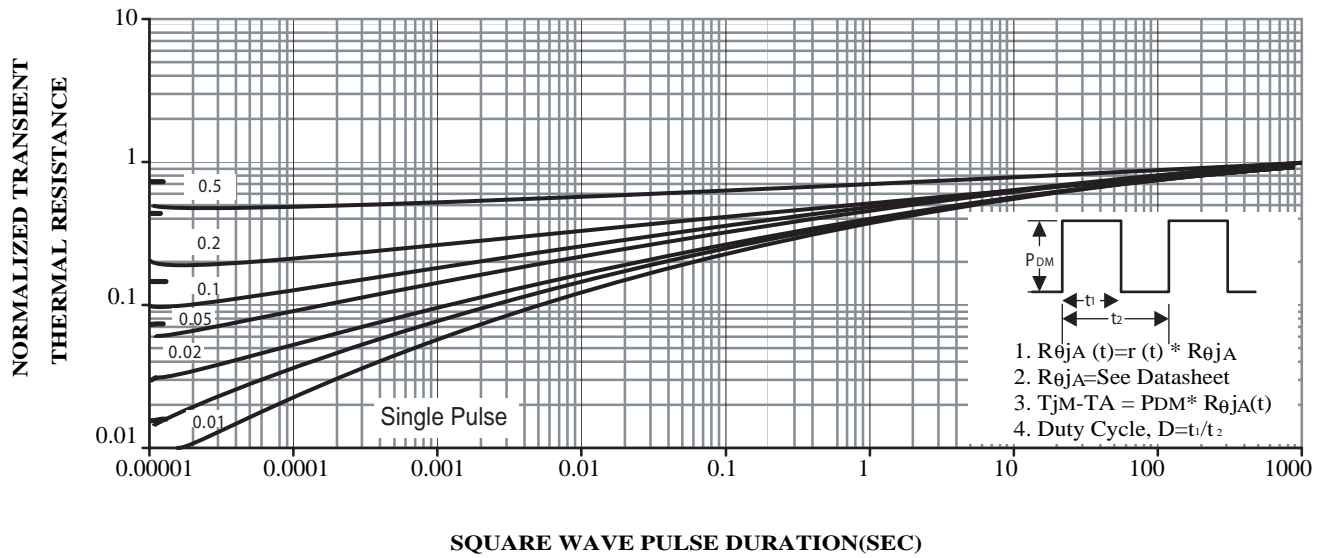
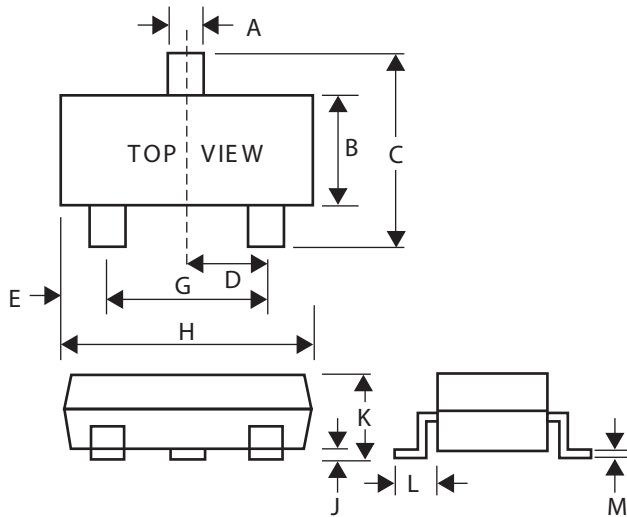


FIG.13 NORMALIZED THERMAL TRANSIENT IMPEDANCE CUREVE

SOT-23 Package Outline Dimensions

Unit:mm



Dim	Min	Max
A	0.35	0.51
B	1.19	1.40
C	2.10	3.00
D	0.85	1.05
E	0.46	1.00
G	1.70	2.10
H	2.70	3.10
J	0.01	0.13
K	0.89	1.10
L	0.30	0.61
M	0.076	0.25