

AT91RM9200 Development Kit

User Guide

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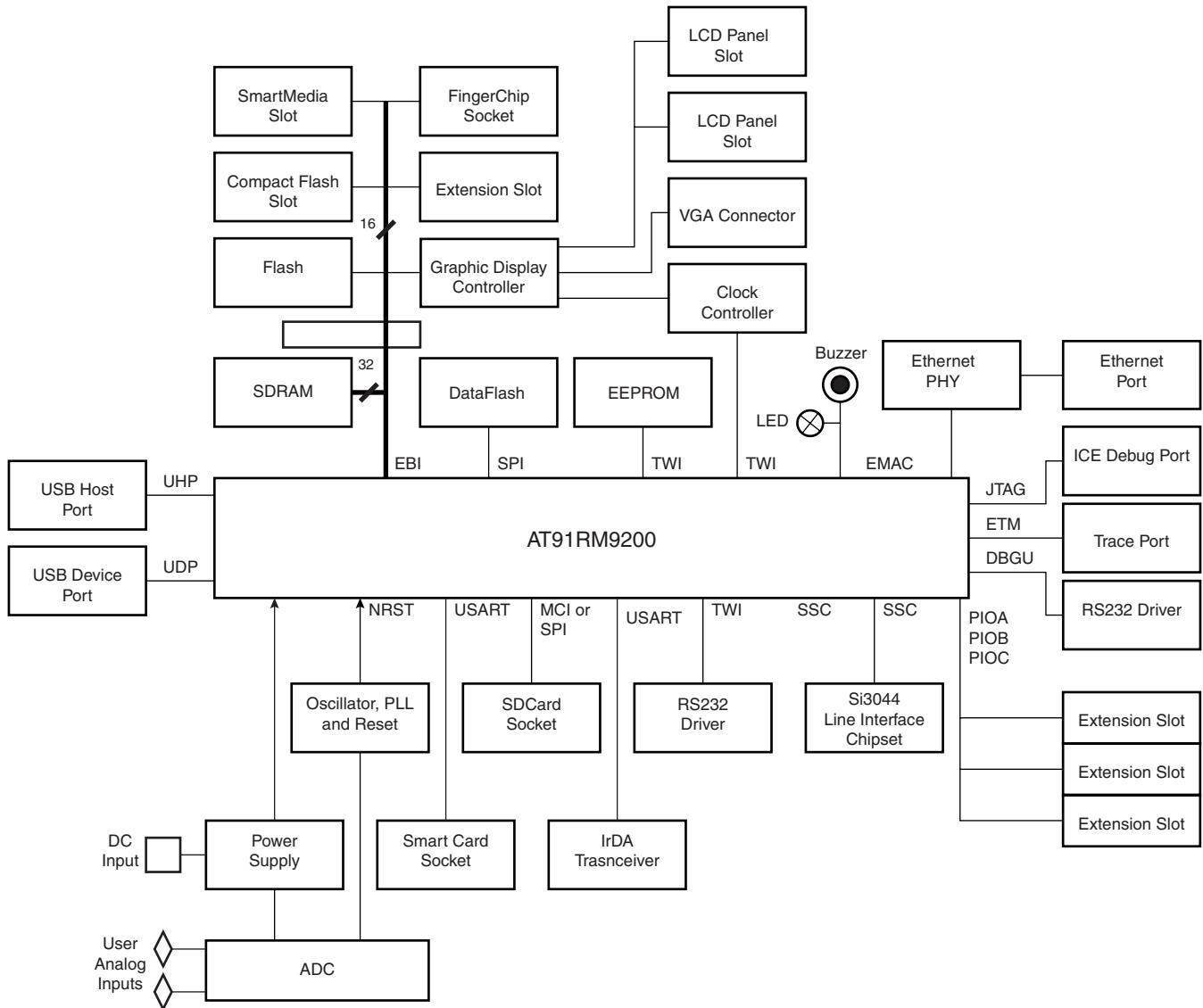
Section 1

Overview

| | | |
|------------|---|--|
| 1.1 | Scope | <p>The AT91RM9200 Development Board enables real-time code development and evaluation. It supports the AT91RM9200 ARM9-based 32-bit RISC microcontroller.</p> <p>This guide focuses on the AT91RM9200 Development Board as an evaluation and demonstration platform:</p> <ul style="list-style-type: none"> ■ Section 1 is this overview. ■ Section 2 gives information on setting up the installation. ■ Section 3 contains a description of the development board. ■ Section 4 details the configuration straps. ■ Section 5 shows board schematics. |
| 1.2 | Deliverables | <p>The development kit is delivered with:</p> <ul style="list-style-type: none"> ■ One AC adapter 100 - 240V ~ 1.0A, 50 - 60 Hz ■ One modem RS232 cable ■ One RJ45 Ethernet crossed cable ■ One A/B-type USB cable ■ Two power supply cables, one US format, one French format ■ One CD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly. |
| 1.3 | The AT91RM9200 Development Board | <p>The board consists of an AT91RM9200 together with the following:</p> <ul style="list-style-type: none"> ■ 2M bytes of parallel Flash memory ■ Four banks of 2M x 32-bit SDRAM ■ 128K bytes of EEPROM with two-wire interface access |

Overview

- 8M bytes of serial DataFlash®
- Five communication ports (USB host and device, Ethernet, serial and IrDA)
- Graphic controller with output to a standard VGA monitor
- JTAG/ICE, ETM and debug interface
- Expansion connector

Figure 1-1. AT91RM9200 Development Board Block Diagram



Section 2

Setting Up the AT91RM9200 Development Board

2.1

Electrostatic Warning

The AT91RM9200 development board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2

Requirements

In order to connect the AT91RM9200 development board, the following elements are required:

- The AT91RM9200 development board itself
- Power supply cable capable of supplying 7V to 12V at 1A (not supplied)

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2.3

Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (J1). The polarity of the power supply is not critical. The minimum voltage required is 7V.

The board has a voltage regulator providing +3.3V. The regulator allows the input voltage range to be from 7V to 12V.

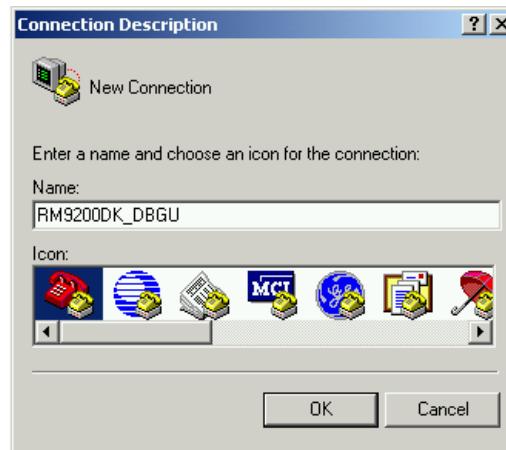
Setting Up the AT91RM9200 Development Board

2.4 Connecting the Board

- Using the RS232 cable supplied in the AT91RM9200-DK kit, connect the board to your PC via the Serial Debug Port (J23).

- Start the HyperTerminal application:  HyperTerminal

- In the window *Connection Description*, enter a name for the connection, e.g., "RM9200K_DBGU".



- Click on *OK*.

- In the window *Connect To*, click on the drop-down list arrow at *Connect using:*. Select the COM port used.



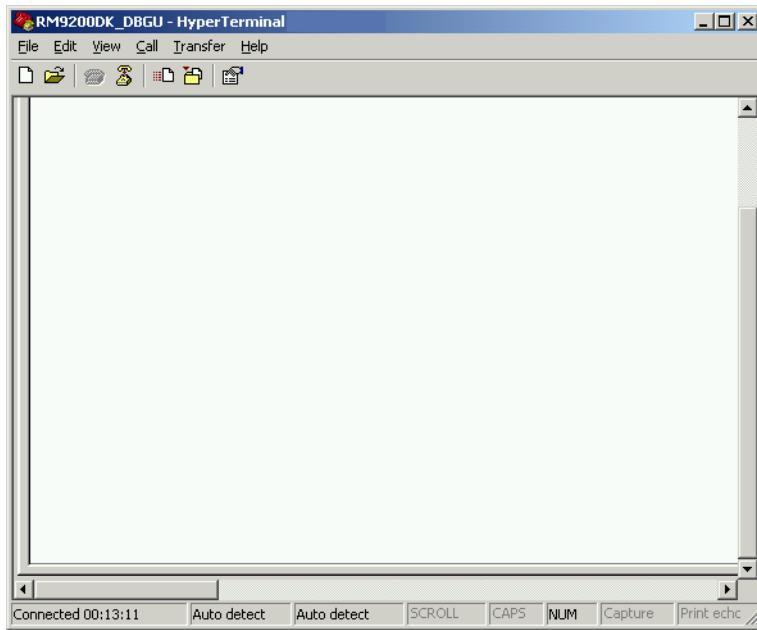
- Click on *OK*.

- Set the serial parameters of the COM port as follows:

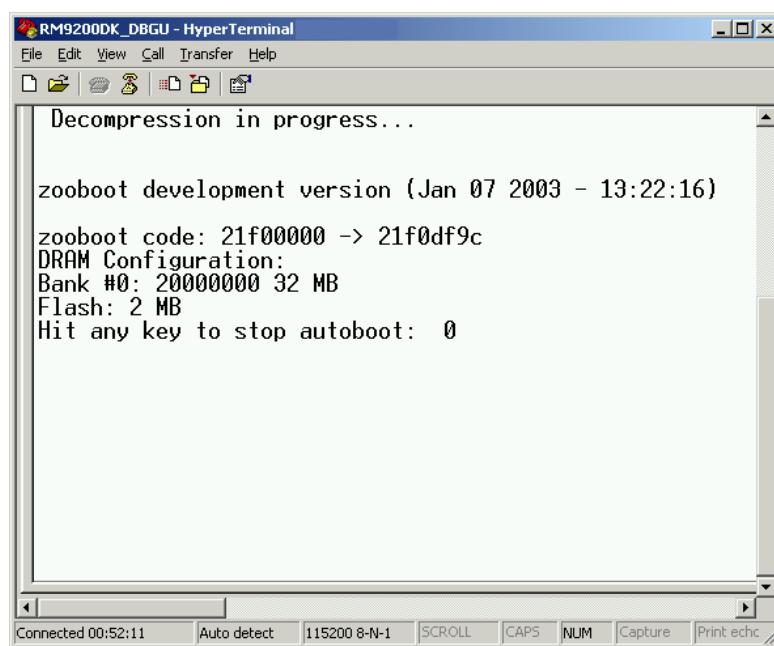
- Bit rate: 115 kbps
- Data bit: 8
- Parity: NONE
- Stop bit: 1
- Flux control: NONE

- Click on *OK*.

- The AT91RM9200-DK and your PC are connected, as indicated in the lower left-hand corner of the console and by the title bar.



- Press the RESET button on the board.
- A message is sent from the board to the HyperTerminal console. Note that this message can vary depending on the version of Zooboot.



2.5

Getting Started with the AT91RM9200

The AT91RM9200 Development Kit is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development toolchains. Please refer to this CD-ROM, or to the AT91 web site, <http://www.atmel.com/products/AT91/>, for the most up-to-date information on getting started with the AT91RM9200.

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Section 3

Board Description

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| 3.1 | AT91RM9200 Processor <ul style="list-style-type: none"> ■ Incorporates the ARM920T™ ARM® Thumb® Processor <ul style="list-style-type: none"> – 200 MIPS at 180 MHz – 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer – Memory Management Unit – In-circuit Emulator including Debug Communication Channel – Mid-level Implementation Embedded Trace Macrocell ■ Additional Embedded Memories <ul style="list-style-type: none"> – 16K Bytes of SRAM and 128K Bytes of ROM ■ External Bus Interface (EBI) <ul style="list-style-type: none"> – Supports SDRAM, Static Memory, Burst Flash, Glueless Connection to CompactFlash®, SmartMedia™ and NAND Flash ■ System Peripherals: <ul style="list-style-type: none"> – Enhanced Clock Generator and Power Management Controller – Two On-chip Oscillators with Two PLLs – Very Slow Clock Operating Mode and Software Power Optimization Capabilities – Four Programmable External Clock Signals – System Timer Including Periodic Interrupt, Watchdog and Second Counter – Real-time Clock with Alarm Interrupt – Debug Unit, Two-wire UART and Support for Debug Communication Channel – Advanced Interrupt Controller with 8-level Priority, Individually Maskable Vectored Interrupt Sources, Spurious Interrupt Protected – Seven External Interrupt Sources and One Fast Interrupt Source – Four 32-bit PIO Controllers with Up to 122 Programmable I/O Lines, Input Change Interrupt and Open-drain Capability on Each Line – 20-channel Peripheral Data Controller (DMA) ■ Ethernet MAC 10/100 Base-T ■ USB 2.0 Full Speed (12 M-bits per second) Host Double Port and Device Port |
|-----|--|

Board Description

- Multimedia Card Interface (MCI)
- Three Synchronous Serial Controllers (SSC)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
- Master/Slave Serial Peripheral Interface (SPI)
- Two 3-channel, 16-bit Timer/Counters (TC)
- Two-wire Interface (TWI)
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins

3.2**Memory**

- 2-Mbyte parallel Flash memory
- Four banks of 2M x 32-bit SDRAM
- 128-Kbyte EEPROM with 2-wire interface
- 8-Mbyte serial DataFlash

3.3**Memory Card**

- SD Card/MMC
 - Supports MultiMedia and SD Card
 - Analog switches provide support for DataFlash Card
- Smart Media® Socket
- CompactFlash® Socket
- Smart Card Interface

3.4**Clock Circuitry and Analog Functions**

- 32.768 kHz standard crystal for the AT91RM9200
- 18.432 MHz standard crystal for the AT91RM9200
- 50 MHz CMOS oscillator for the Display Controller
- Temperature sensor
- Analog-to-digital converter
- FingerChip (Socket only)

3.5**Reset Circuitry**

- Reset Controller

3.6**Power Supply Circuitry**

- 3.3V DC/DC converter
- 1.8V DC/DC converter



| | | |
|------|-----------------------------|--|
| 3.7 | Remote Communication | <ul style="list-style-type: none"> ■ Fast Ethernet Physical Layer Single Chip Transceiver ■ IrDA Transceiver ■ Host Interface via RS-232 DB9 male socket ■ Line interface ■ Debug Port via RS-232 DB9 connector ■ Host and Device USB socket |
| 3.8 | User Interface | <ul style="list-style-type: none"> ■ Graphic Display Controller ■ TFT/SNT panel socket ■ 15-pin standard socket for an external VGA monitor ■ On-board buzzer and one LED managed via general PIO lines |
| 3.9 | Expansion Slots | <ul style="list-style-type: none"> ■ Three expansion slots give access to all the microcontroller's signals |
| 3.10 | Debug Interface | <ul style="list-style-type: none"> ■ 38-pin trace Port socket ■ 20-pin JTAG interface connector ■ Serial Debug Unit |

Board Description

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Section 4

Configuration Straps

4.1

Configuration Straps and Jumper Settings

Table 4-1 gives details on configuration straps and jumper settings on the AT91RM9200 development board and their default settings.

Table 4-1. Configuration Straps and Jumper Settings

| Designation | Default Setting | Feature |
|-------------|-----------------|--|
| S1 | Closed | The earth plane and the GDN potential are connected. |
| S3 | Closed | The ETM reset (NSRST) and the System Reset (NRST) are connected. |
| S4 | Closed | The PD6/DTXD PIO line is connected to the READY/NBUSY output signal of the SPI DataFlash (MN13). |
| S5 | Opened | The Write Protect feature of the SPI DataFlash (MN13) is disabled. |
| S6 | Closed | The PA26/ TWCK /IRQ1 signal is connected to three remote devices (MN14, MN33, MN34). |
| S7 | Closed | The PA25/ TWD /IRQ2 signal is connected to three remote devices (MN14, MN33, MN34). |
| S8 | Opened | The PA3/ NPCS0 /IRQ5 output signal is not connected to the NCS of the serial DataFlash (MN13). |
| S9 | Closed | The PA5/ NPCS2 /TXD3 signal is connected to the 10-bit SPI ADC (MN15). |
| S10 | Closed | The PC15 I/O line is connected to the 10-bit ADC to read the End Of Conversion event (MN15). |
| S11 | Closed | Not Used: The PS2 Controller is not installed. |
| S12 | Closed | Not Used: The PS2 Controller is not installed. |
| S13 | Closed | The PB12/ TF2 /ETX2 signal is connected to the NRGDT/FSD output signal of the Line Interface (MN23). |
| S14 | Closed | The PB16/ RK2 /ERX2 signal is connected to the NOFHK input signal of the Line Interface (MN23). |
| S15 | Closed | The PB17/ RF2 /ERXDV signal is connected to the NFSYN input signal of the Line Interface (MN23). |

Configuration Straps**Table 4-1.** Configuration Straps and Jumper Settings

| Designation | Default Setting | Feature |
|--------------------|------------------------|--|
| S16 | Closed | The PB13/ TK2 /ETX3 signal is connected to the SCLK output signal of the Line Interface (MN23). |
| S17 | Closed | The PB15/ RD2 /ERX2 signal is connected to the SDO output signal of the Line Interface (MN23). |
| S18 | Closed | Not Used: The Front End AC97 is not installed. |
| S19 | Closed | The PA30/ DRXD /CTS2 signal is connected to the receive buffer output of the DBGU transceiver (MN26). |
| S20 | Closed | The AT91RM9200's PC14 PIO line is connected to the NREADY output signal of the Smart Card Interface (MN29). |
| S21 | Closed | The PA17/TXD0/TIOA0 is connected to the DATA input/output signal of the Smart Card Interface (MN29). |
| S22 | Closed | The PA22/ RXD2 /TIOB2 is connected to the RX output signal of the IrDA Transceiver (MN30). |
| S23 | Closed | Enables all output signals (DCD1, DSR1, RXD1, CTS1, RI1) of the Transceiver (MN28) used for the RS232 Port COM. |
| S24 | Closed | The PD4 /ETXEN input line is connected to the USB device socket (J28) to detect a host connection. |
| S25 | Closed | The System Reset signal (NRST) is connected to the ICE/JTAG socket (J8, pin 15). |
| S26 | Closed | The NCS2 output signal is connected to the display controller (MN32). |
| S27 | Closed | The NCS0 output signal is connected to the parallel Flash memory (MN21). |
| S28 | Closed | Enables the OE signal from the Atmel FingerChip (MN31). Only the socket is installed. |
| S29 | Closed | The SMCS /NCS3 output signal is connected to the bidirectional buffer used by the Smart Media Connector (MN20B). |
| S30 | Closed | The PA15/ EMDC /TCLK2 output signal is connected to the MDC input signal of the Ethernet Transceiver (MN22). |
| S31 | Closed | The PA16/ EMDIO /IRQ6 input/output signal is connected to the MDIO input/output signal of the Ethernet Transceiver (MN22). |
| S32 | Closed | Disables the power-down mode of the Ethernet Transceiver (MN22). |
| S33 | Closed | Not Used: The Front End AC97 is not installed. |
| S34 | Closed | Not Used: The Front End AC97 is not installed. |
| S35 | Closed | Not Used: The Front End AC97 is not installed. |
| S36 | Closed | Connects the system ground to the Ethernet ground. |
| S37 | Closed | Not Used: The Front End AC97 is not installed. |

Table 4-1. Configuration Straps and Jumper Settings

| Designation | Default Setting | Feature |
|-------------|-----------------|---|
| S38 | Opened | The AT91RM9200 boots up from the parallel Flash Memory. |
| S39 | Closed | Enables the use of the User LED (DS5). |
| S40 | Closed | Not Used: The Buzzer is not installed. |

Note: Shaded cells indicate configuration straps/jumpers with open connections.

Note: Signal names in bold indicate that the function is shared between several signals.

Configuration Straps

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Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

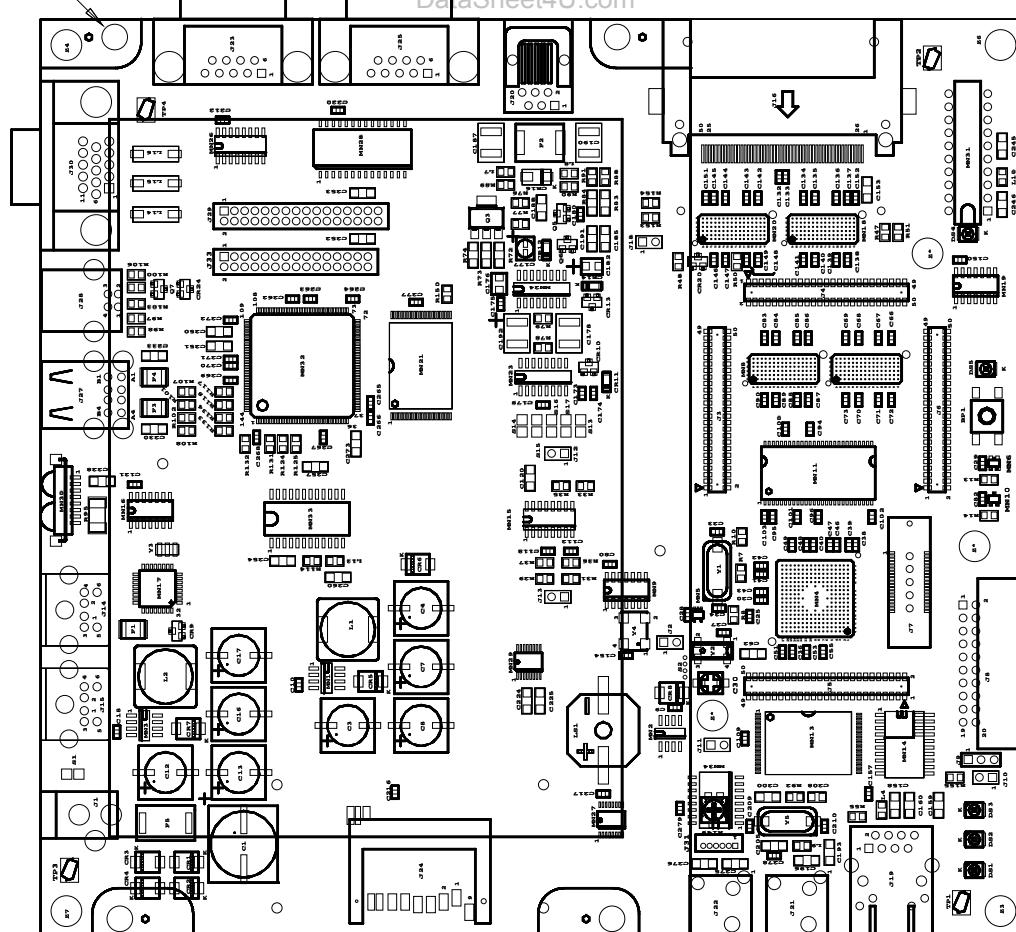
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- AT91RM9200 Board Layout - Bottom View
- Power Supply
- AT91RM9200 Chip
- Buffers
- SDRAM and Flash
- Serial Devices DataSheet4U.com
- PS2 COM Ports
- 3V3 Memory Card
- Ethernet
- DAA
- AC97 Analog Front End
- Serial Interfaces
- Fingerchip
- VGA TFT/CRT Display

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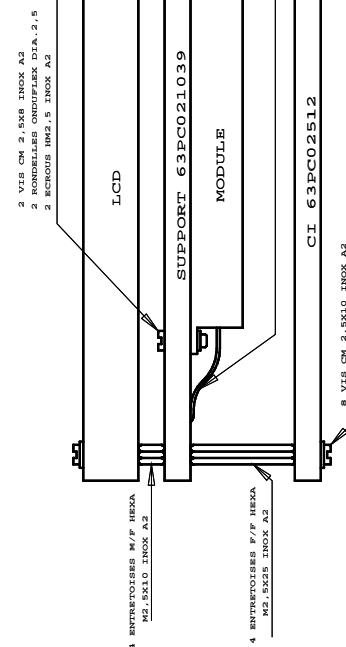
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SUR SUPPORT 63PC021039 VOIR DETAIL



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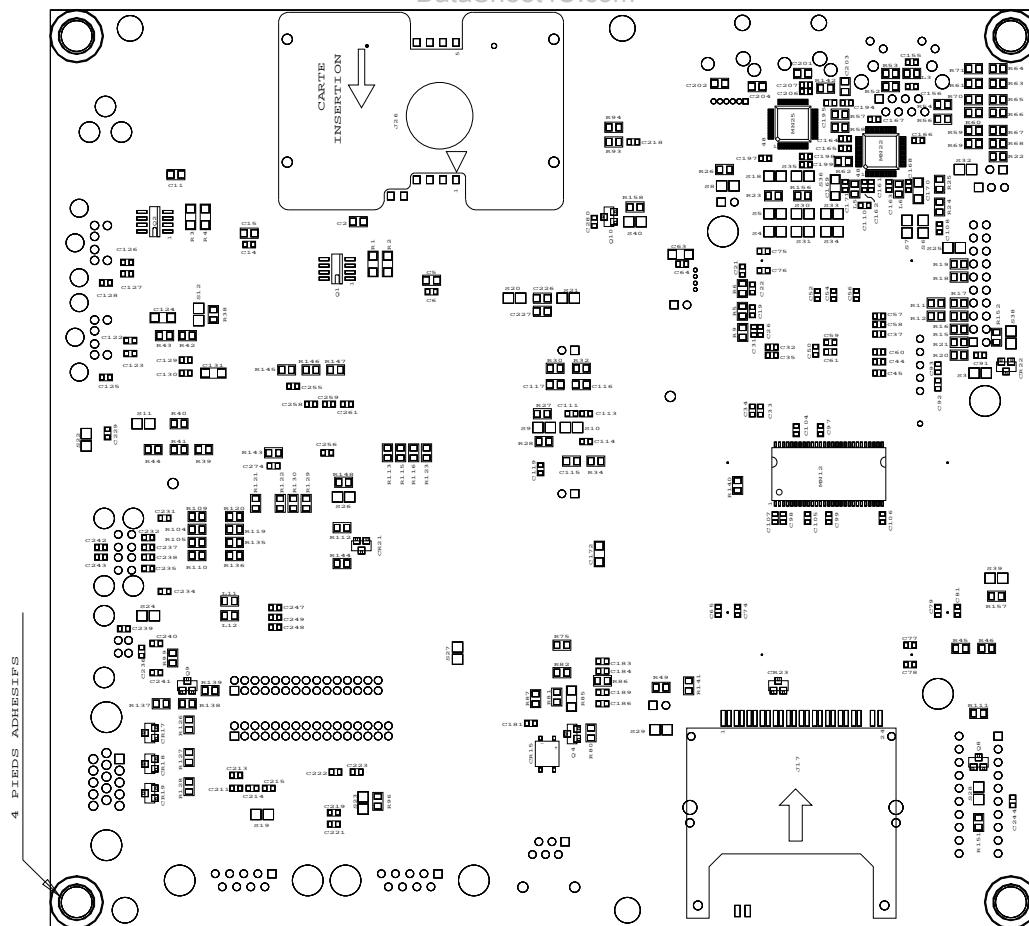
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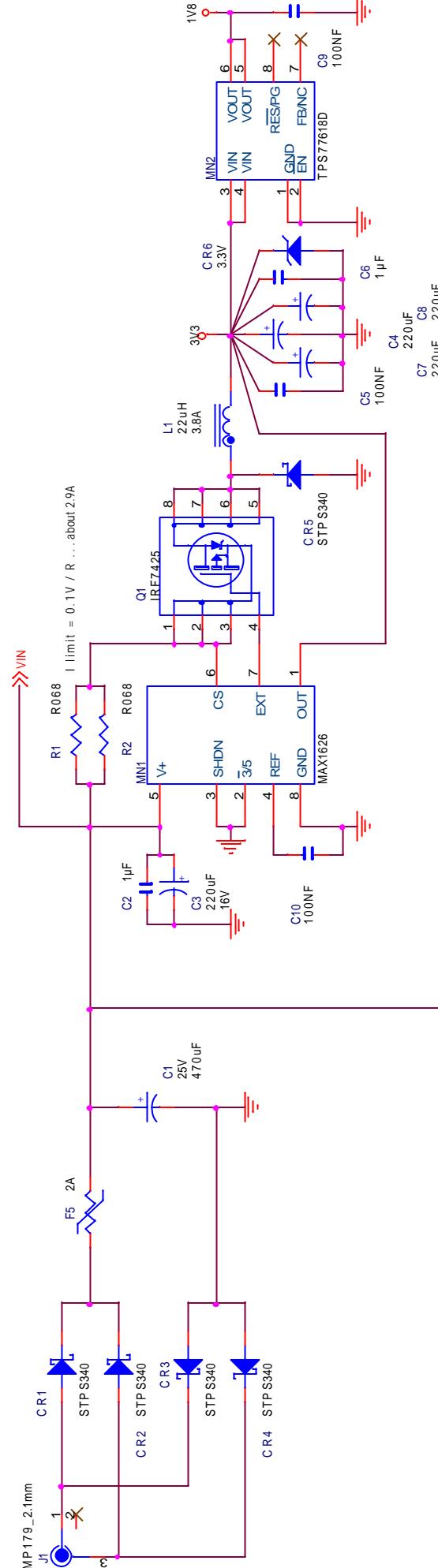
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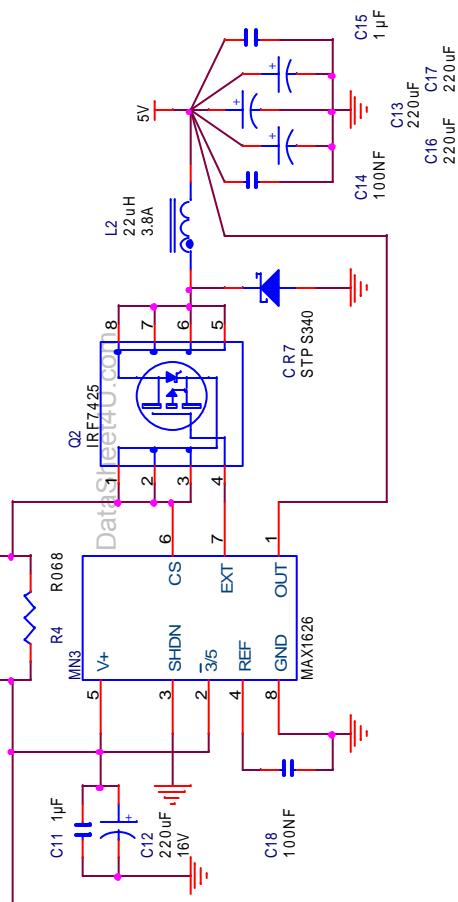
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12V TO 14V DC INPUT

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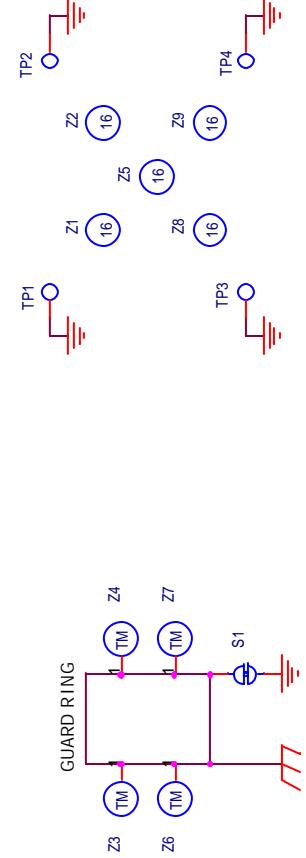


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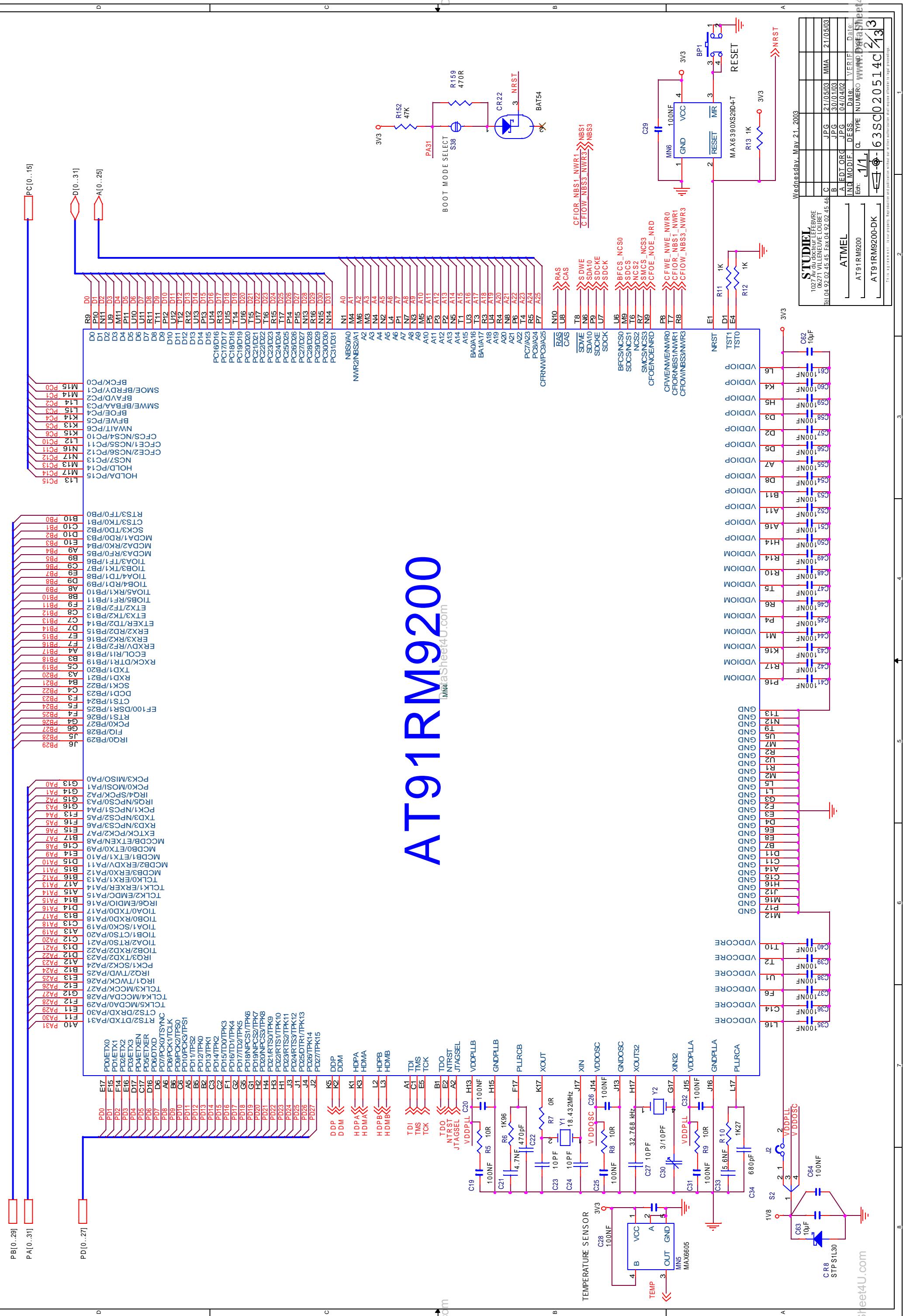


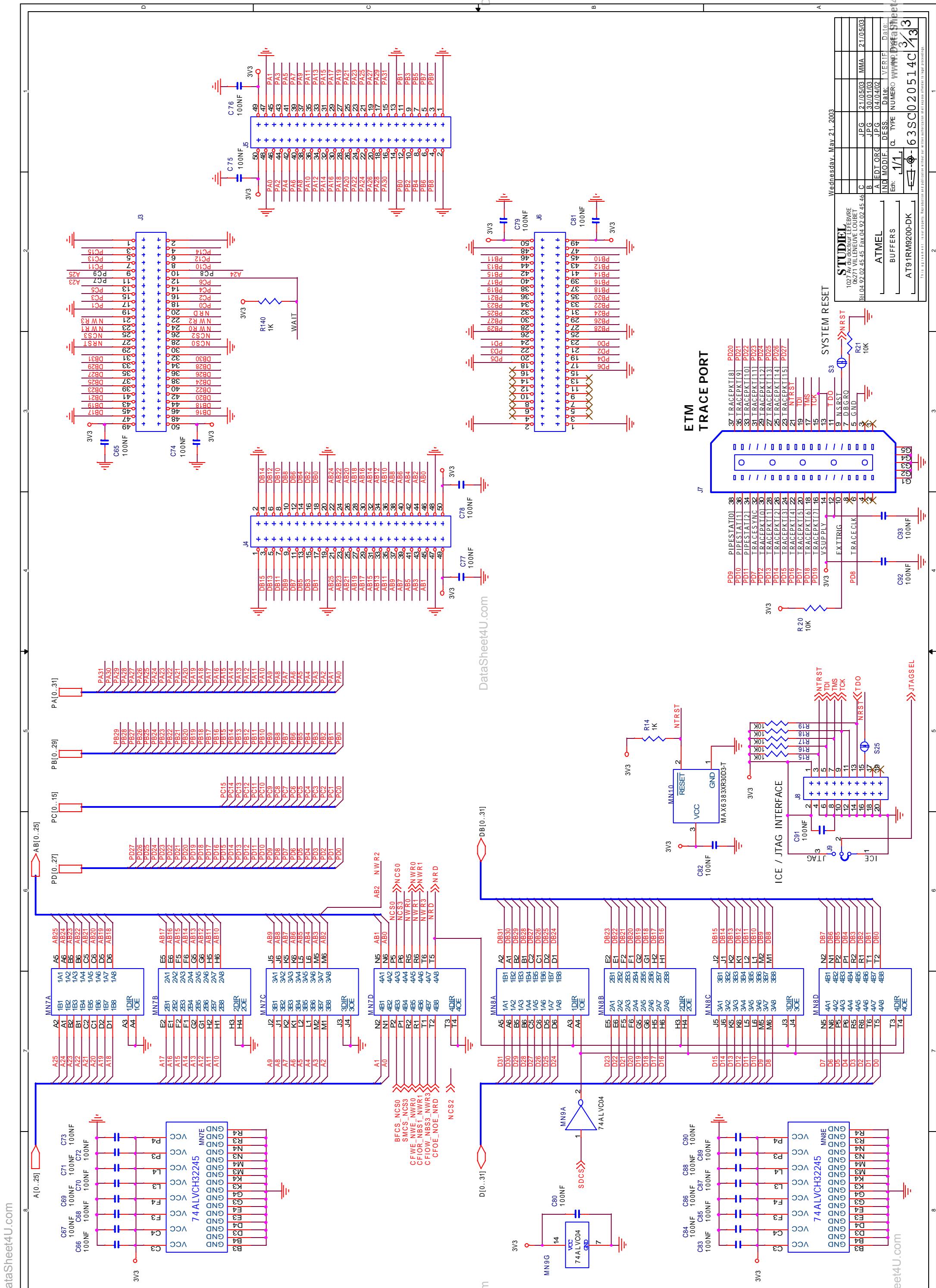
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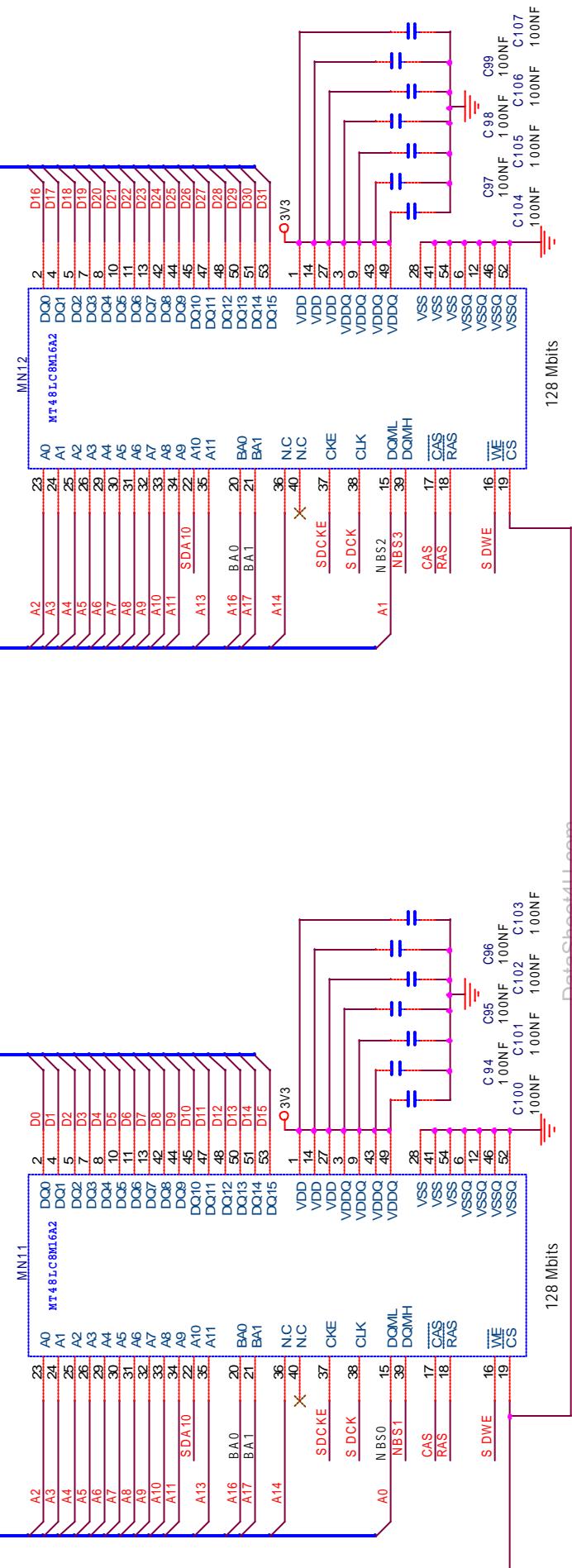
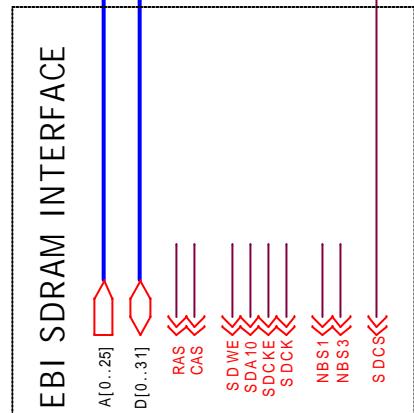
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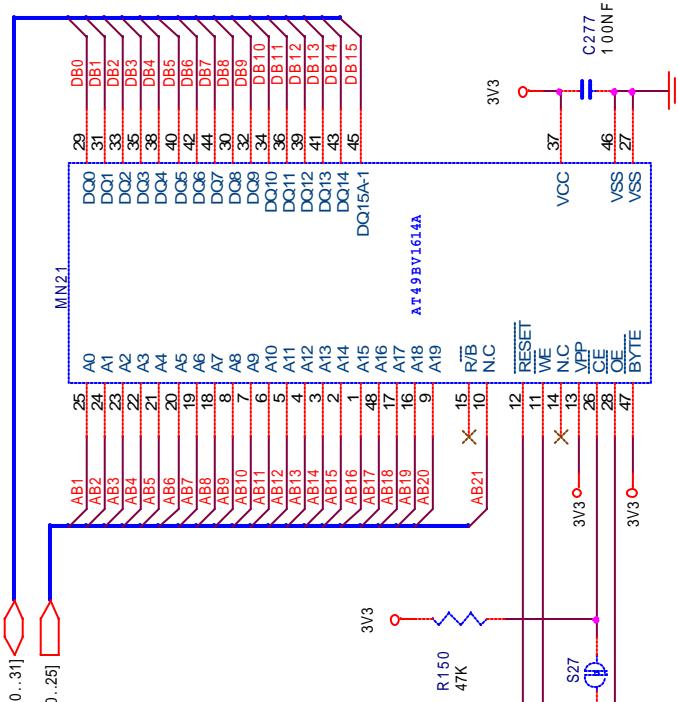
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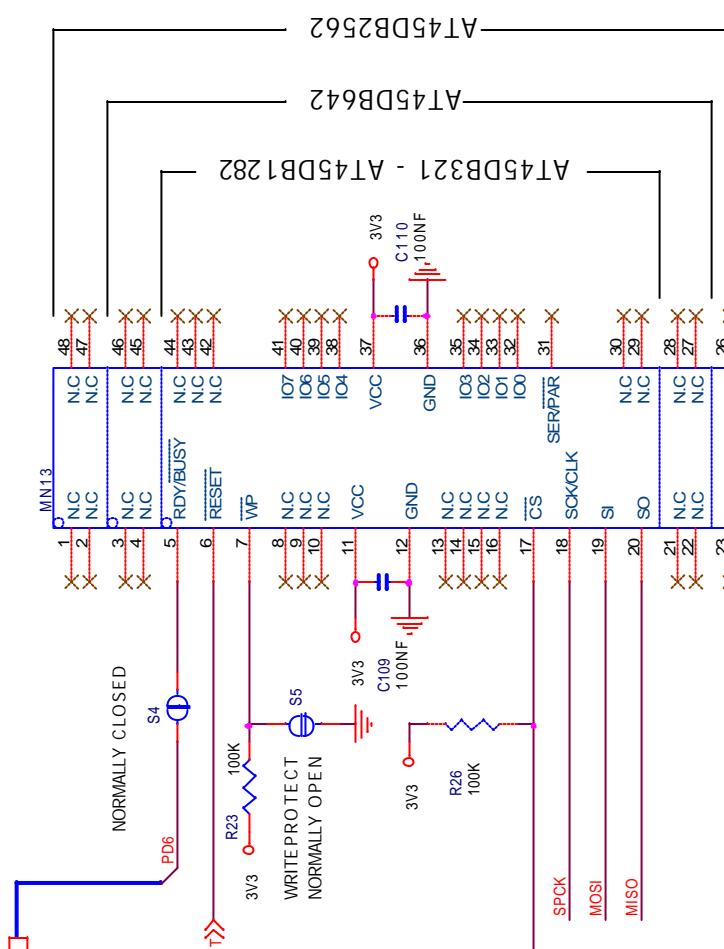


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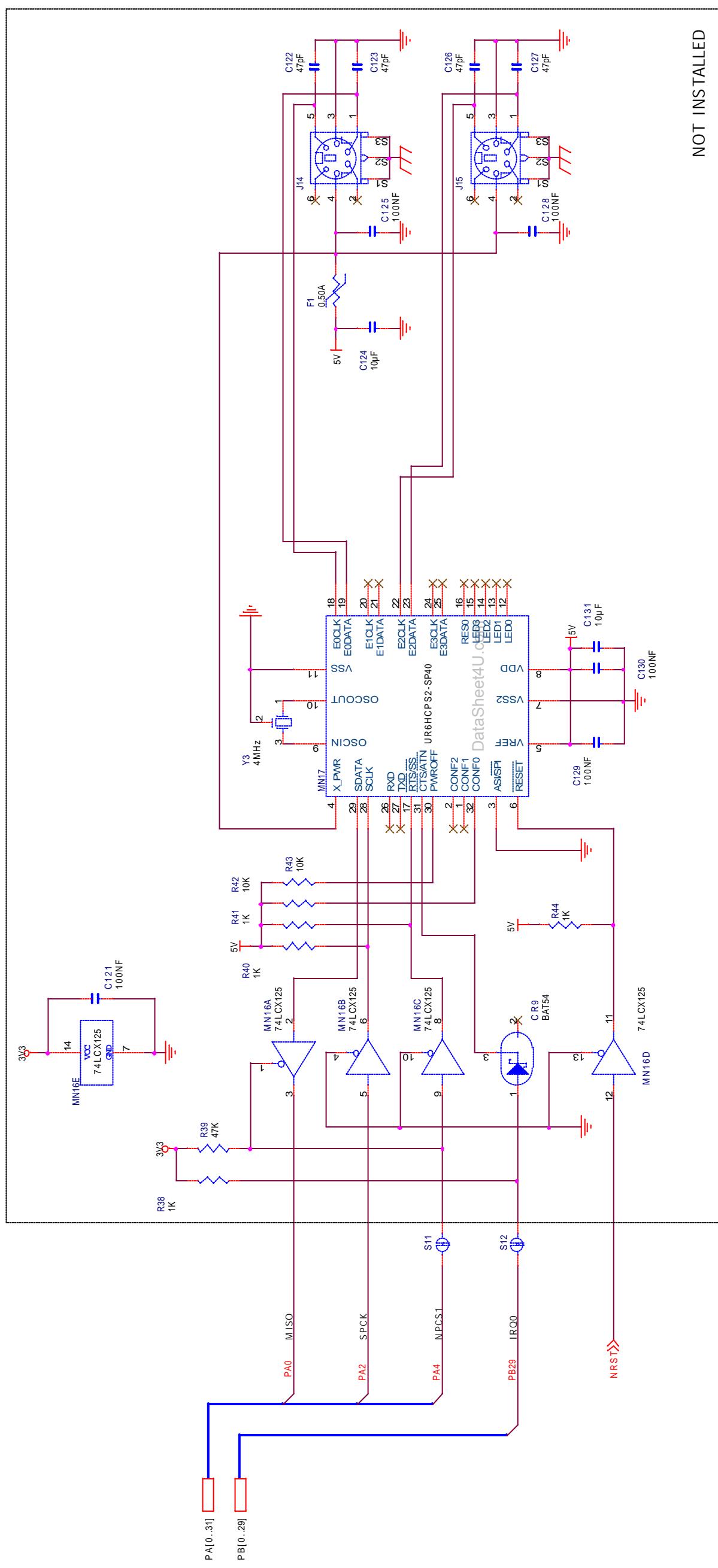
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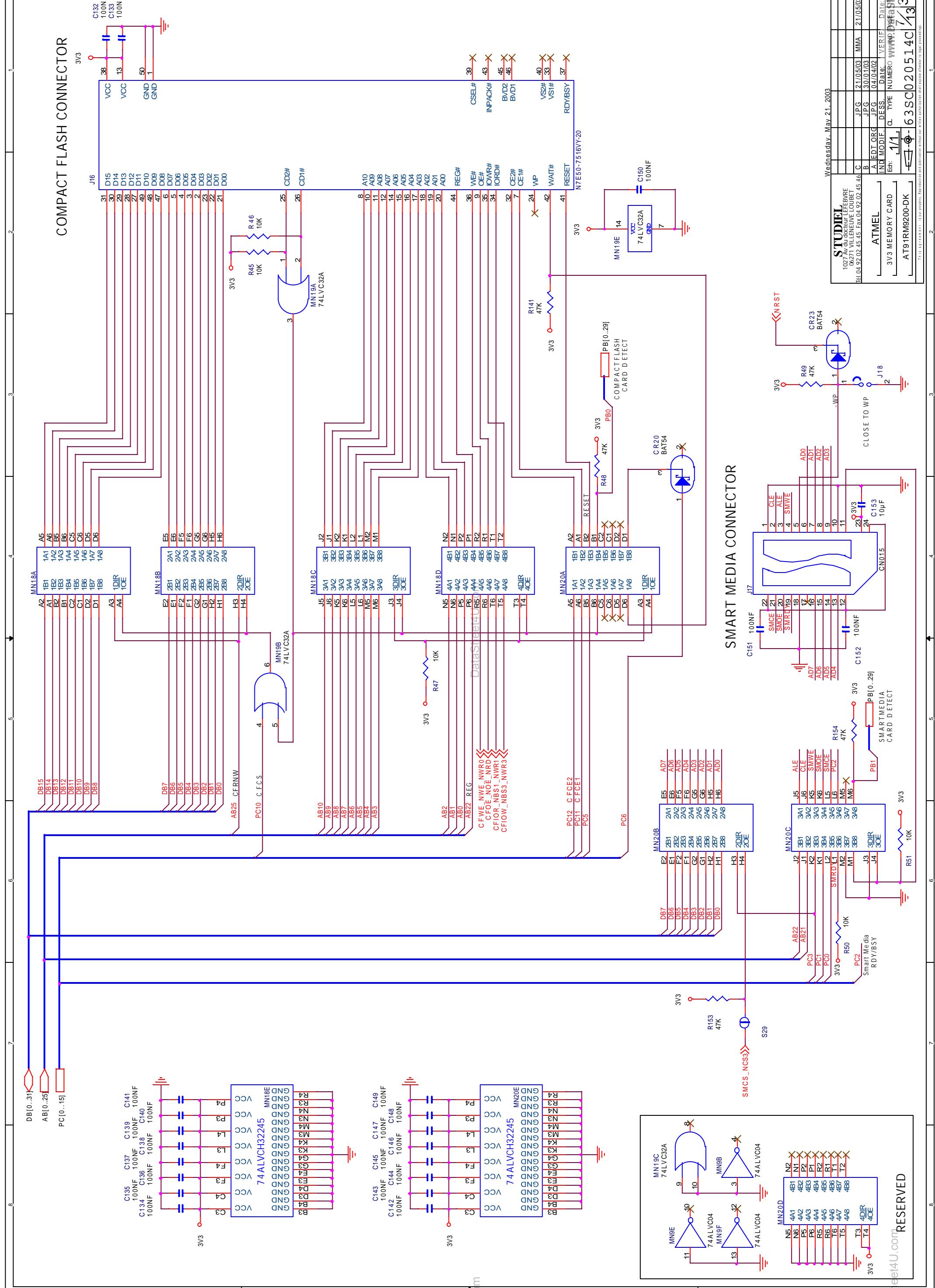
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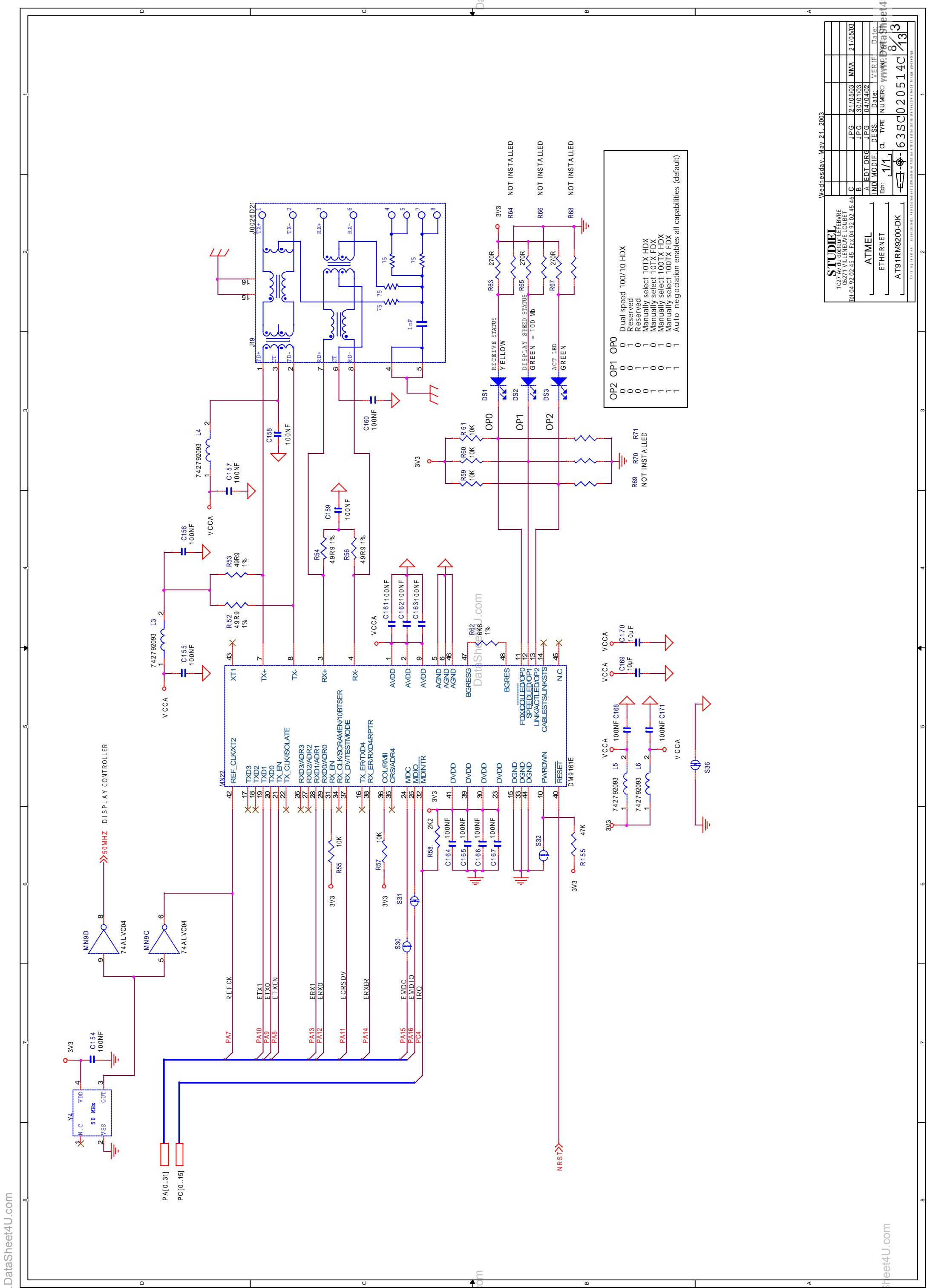
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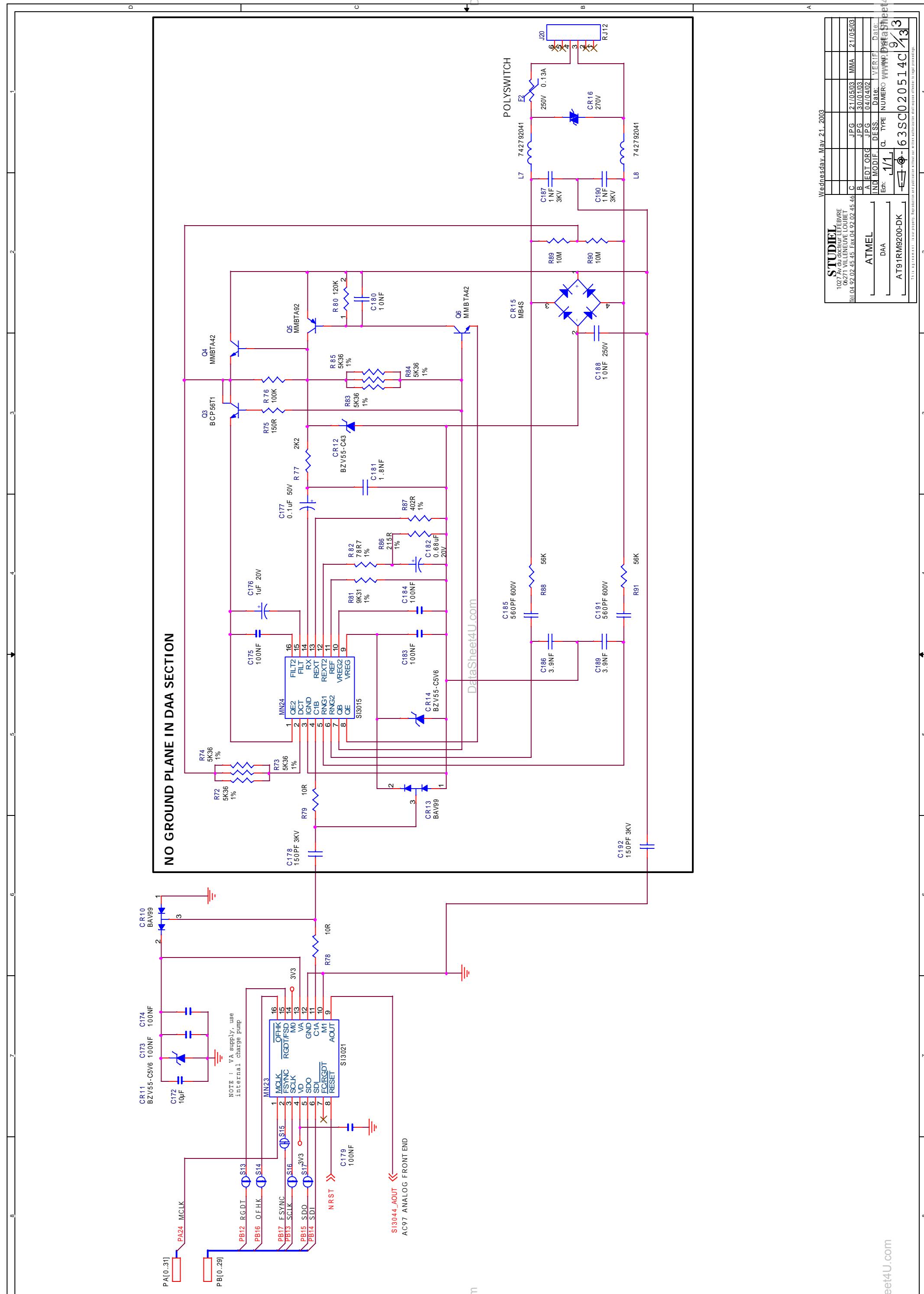
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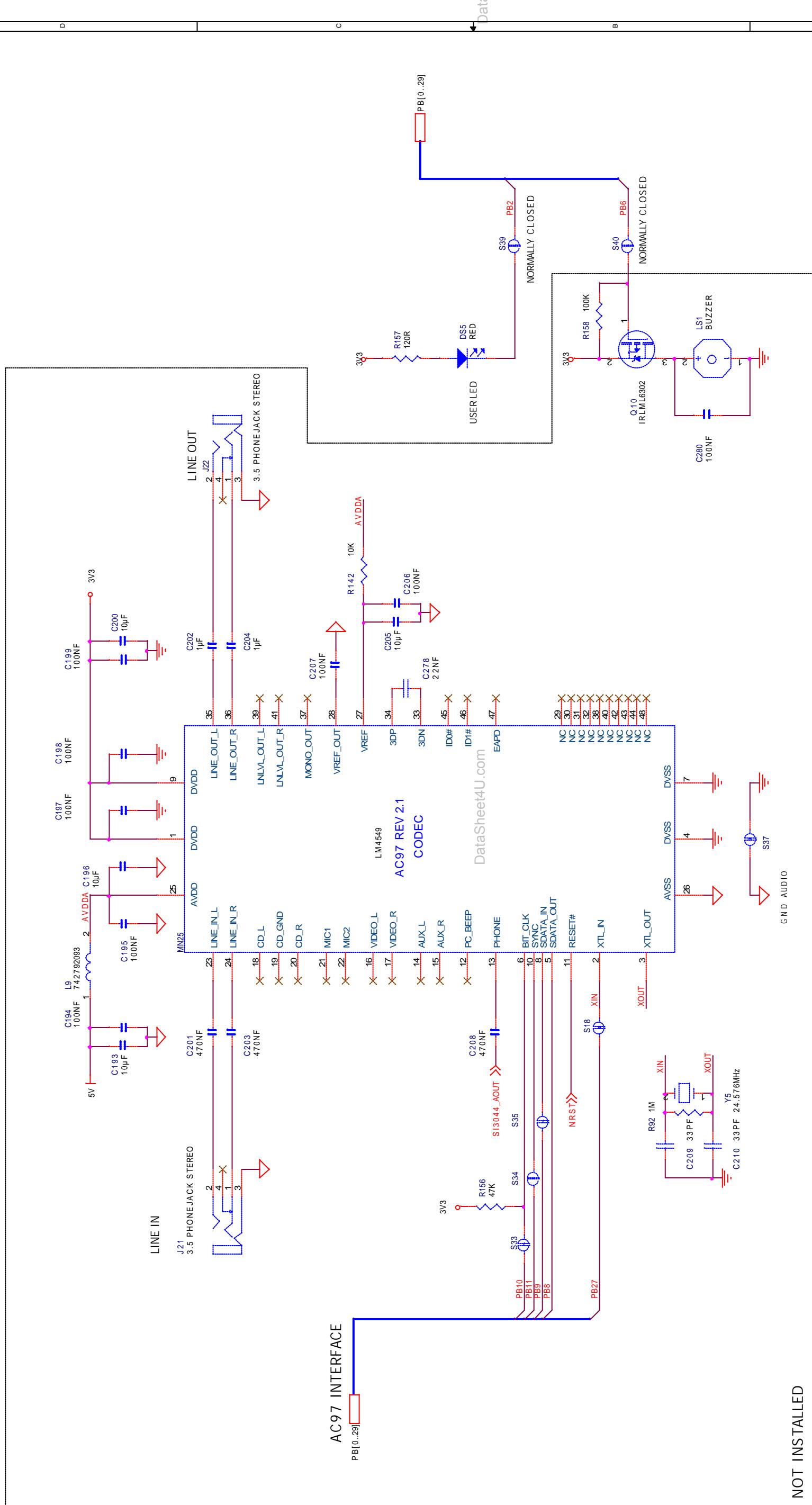






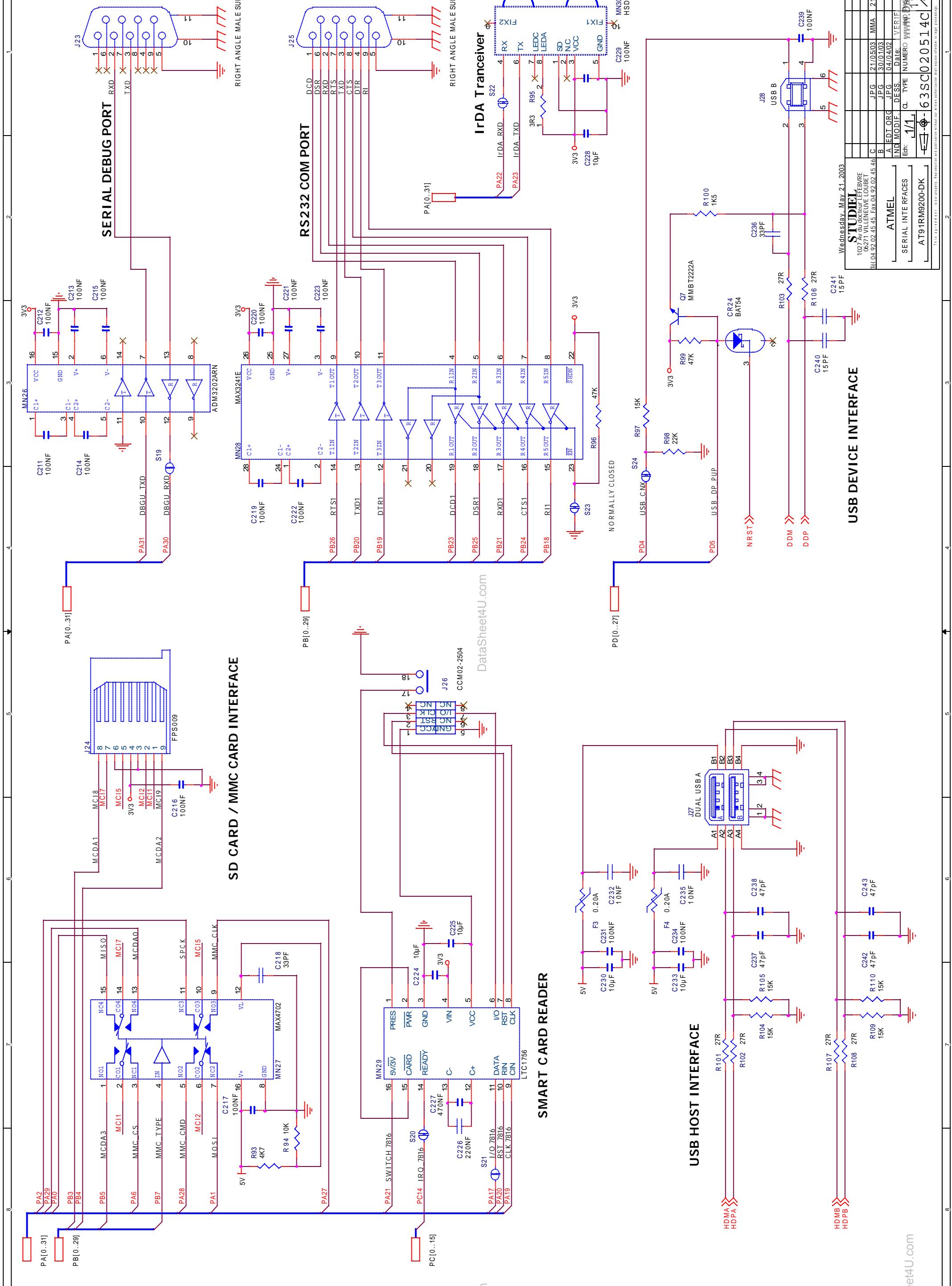
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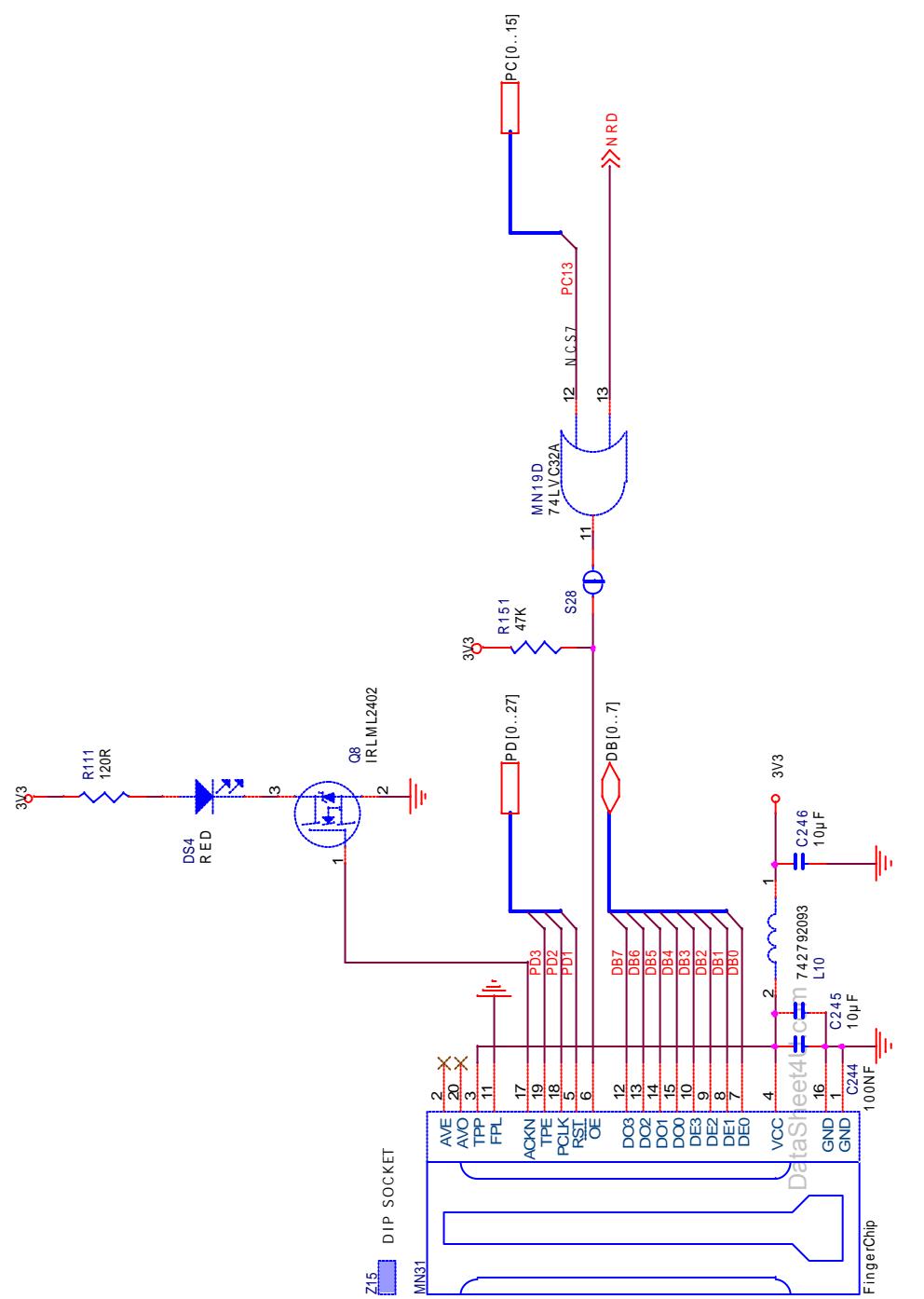
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| ATMEL AC97 ANALOG FRONT END | B | JPG | 30/01/03 | | |
| AT91RM9200-DK | A | DESS | 04/04/02 | VERIF | Date |
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Table 1: TABLEAU 1: TABLEAU DE POSITION DES DIFFÉRENTS CONNECTEURS



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| STUDIEL | 1027 Av du docteur LEFFEBRE 06271 VILLENEUVE LOUBET tel. 04 92 02 45 45 Fax 04 92 02 45 46 | C | JPG | 21/05/03 | MMA |
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