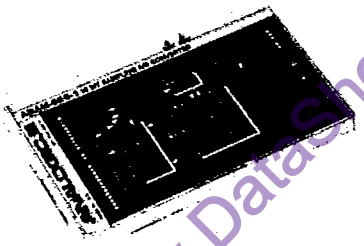

ANALOGIC

ADAM-826-1

16-Bit, 2.5 μs A/D Converter with Integral Sample-and-Hold

Description

Superior performance and relative ease of system implementation make the ADAM-826-1 the ideal solution for those applications requiring a sample-and-hold amplifier (S/H) directly at the input to the A/D Converter. The unit can be ordered with either a ±10V bipolar or 0-10V unipolar input and provides 16-bit two's complement or offset binary output data in 2.5 μs, including acquisition time. The differential linearity error of the ADAM-826-1 is typically less than ±1/4 LSB with a worst case maximum of less than ±3/4 LSB. The internal S/H represents a significant technical achievement in its own right, with an acquisition time of less than 1 μs for full scale input step change — extremely fast for an amplifier whose linearity is better than ±0.001%!

The selection of the ADAM-826-1, with its integral S/H, benefits overall system performance in at least two ways. First, the S/H has been designed specifically to match the requirements of the A/D Converter. For example, great care has been exercised in the internal timing to avoid overlap of critical functions which might impair system performance. Furthermore, S/H performance criteria such as acquisition time, hold mode settling, droop rate, and the like, have been optimized for the A/D Converter, resulting in exceptional combined overall performance as reflected in its specifications. The second benefit to the designer is that by selecting the ADAM-826-1, he can sidestep the sometimes costly iterations of printed circuit board layout often necessary to avoid degradation of 16-bit system performance due to ground loops, signal coupling, and digital noise introduced when separate S/H and A/D Converters are interconnected.

Using the ADAM-826-1

In most cases, the ADAM-826-1 will be connected as shown in the Block Diagram of Figure 6, in which case, a single trigger/start convert command will cause the S/H to go into the hold mode. Under control of the internal timing logic, the A/D Converter will then begin the conversion while hold mode settling takes place. At the completion of the conversion process, the S/H will automatically be returned to the sample mode to await the next trigger/start convert command. Please refer to the Timing Diagram of Figure 7 and to the section on Timing. It is important to note that the connection to the TRANSFER line must be kept as short as possible, or alternatively, buffered prior to connection to external circuitry.

If external system considerations so dictate, control of the S/H and A/D Converter may be accomplished independently through external logic provided by the user. This is achieved by disconnecting the S/H CONTROL OUT pin from the S/H CONTROL IN pin, as shown in the Block

(continued)

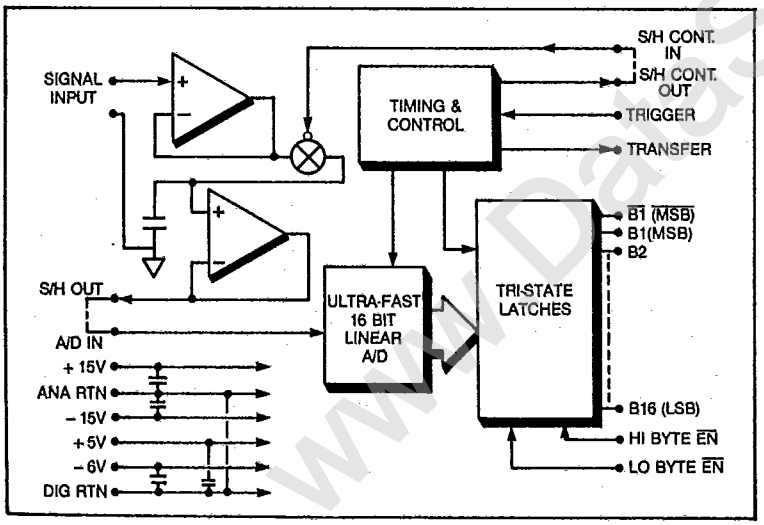

Figure 6. ADAM-826-1 Block Diagram.

SPECIFICATIONS T-51-10-16

(All specifications guaranteed at 25°C and nominal power supply voltages unless otherwise noted)

COMBINED S/H AND A/D CONVERTER PERFORMANCE (ADAM-826-1) (See Note 1.)

Note: These specifications represent the total error of all sources, including both the S/H and A/D Converter errors. As tabulated in subsequent sections, the specifications for the S/H and A/D by themselves are even better.

INPUT

Input Voltage Range
0V to +10V unipolar (See Note 2.) −10V to +10V bipolar

Maximum Input Without Damage
±Supply

Input Impedance
100 MΩ // 10 pF typical

Input Bias Current
±100 pA maximum (doubles every 10°C)

Initial Offset Voltage
±5 mV maximum, adjustable to zero

THROUGHPUT

Conversion Time
2.5 μs, maximum

Maximum Conversion Rate
400,000 samples per second

ACCURACY

Resolution
16 bits

Differential Non-Linearity
±1/4 LSB typical, ±3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
±1/2 LSB

Relative Accuracy
±0.0015% FSR typical (See Note 3.) ±0.003% FSR maximum (See Note 3.)

Absolute Accuracy (Includes Reference Accuracy)
±0.005% FSR maximum (See Note 4.) The Internal Reference (and offset) may be adjusted against a standard source traceable to the National Bureau of Standards for even better Absolute Accuracy

Noise
Unipolar: 60 μV rms maximum, Bipolar: 80 μV rms maximum

STABILITY

Differential Non-Linearity Tempco
±1 ppm FSR/°C maximum

Total Offset Tempco (Including Pedestal)
±5 ppm FSR/°C maximum

Gain Tempco
±5 ppm FSR/°C maximum

Warmup Time
10 minutes to specified accuracy (See Note 5.)

Power Supply Sensitivity Gain
±10 ppm/Δ1% each supply, maximum

Offset
±10 ppm/Δ1% each supply, maximum

Recommended Recalibration Interval
6 months

DIGITAL INPUTS/OUTPUTS INPUTS

Trigger
Negative edge triggered; 1 LSTTL load; 100 ns pulse width minimum, 200 ns maximum; (See Note 9.) CMOS and 74LSTTL Compatible

S/H Mode Control
Logic 1 is HOLD mode, logic 0 is SAMPLE, Logic 1 must be +5V, drive with CMOS gate or TTL gate with <470Ω pullup

Tri-state Control
HI Byte Enable
Logic 1 produces high impedance

LO Byte Enable
Logic 1 produces high impedance, CMOS and 74LSTTL Compatible

OUTPUTS

Data
16 bits data plus B1; Offset Binary or two's complement; See Coding Table; Tri-state CMOS latch (Silicon gate)

Data Output Loading Transfer (XFER)
1 LSTTL load, positive edge loads output data latches; data ready after 50 ns delay

Transfer (XFER) Loading
1 LSTTL Load

POWER REQUIREMENTS

+15V ±0.5V
90 mA, typical

−15V ±0.5V
100 mA, typical

+5V ±0.25V
95 mA, typical

−6V ±0.25V
140 mA, typical (See Note 8.)

Note: At power on, a 200 mA maximum current surge on the ±15V supply lines will occur, and will last for no more than 5 seconds. This surge is caused by the Reference heater circuit when starting "cold".

Note: The ±15V power supplies must have no more than 5 mV p-p ripple.

ENVIRONMENTAL AND MECHANICAL

Operating Temperature Range
0°C to +60°C

Storage Temperature Range
−25°C to +70°C

Relative Humidity
0 to 85%, non condensing

Dimensions and Shielding
Modupac
3.00" x 5.00" x 0.44"
(76.2 x 127.0 x 11.17 mm)
RFI 6 sides, EMI 5 sides

SAMPLE-AND-HOLD AMPLIFIER ONLY

INPUT

Input Voltage Range
±10V, (See Note 2.)

Maximum Input Without Damage
±Supply

Input Impedance
100 MΩ // 10 pF typical

Input Bias Current
±100 pA maximum (doubles every 10°C)

Initial Offset Voltage
±5 mV maximum, adjustable to zero

SAMPLE MODE

Gain
+1

Small Signal Bandwidth
5 MHz typical

Full Power Bandwidth
250 kHz

Acquisition Time
1 μs maximum to 0.0015% for 20V full scale step. Acquisition time for smaller steps will be less.

Non-Linearity
±0.001% (20V input)

Noise
40μV rms typ., 50 μV rms max. Unipolar or Bipolar

SAMPLE-TO-HOLD SWITCHING

Aperture Uncertainty
150 ps typical

Aperture Time
15 ns typical

Switching Transient Settling Time
150 ns maximum (See Note 6.) to ±0.0015% FSR

HOLD MODE

Output Drive Capability
1 kΩ // 50 pF Short-circuit protected

Droop Rate
5 μV/μs maximum (See Note 7.)

Dielectric Absorption
±0.001% of voltage change, typical (800 ns Sample, 1.5 μs Hold)

Pedestal Non-Linearity
±0.0015% FSR maximum

A/D CONVERTER ONLY T-51-10-16

Input Voltage
0V to +10V unipolar; −10V to +10V bipolar, Factory configured

Input Impedance
1.4 kΩ unipolar, 2.8 kΩ bipolar

ACCURACY

Resolution
16 bits

Differential Non-Linearity
±1/4 LSB typical, ±3/4 LSB maximum

Monotonicity
Guaranteed; no missing codes

Quantization Error
±1/2 LSB

Relative Accuracy
±0.0015% FSR maximum

Absolute Accuracy
±0.003% FSR maximum

Noise (Including Ref.)
Unipolar: 30 μV rms, maximum, Bipolar: 60 μV rms, maximum

STABILITY

Differential Non-Linearity
±1 ppm/°C maximum

Tempco
±5 ppm/°C maximum

Gain Tempco
Unipolar: ±1.5 ppm/°C maximum,
Bipolar: ±4.5 ppm/°C maximum

Warmup Time
10 minutes to specified accuracy

Recommended Recalibration Interval
6 months

THROUGHPUT

Conversion Time
1.5 μs maximum

Note 1: Specifications apply when S/H control is internally generated. See text and Figure 5.
Note 2: Input voltage range is determined by the A/D Converter. The S/H is a unity gain device.
Note 3: Specified as the maximum deviation from a best fit line. Maximum deviation from straight line drawn through full scale end points is 0.004%.
Note 4: Absolute Accuracy is the worst case summation of all error sources for both the Analog-to-Digital Converter and the Sample-and-Hold Amplifier.
Note 5: Time required for internal reference heater to stabilize.
Note 6: Specified for completeness only — this settling time is overlapped by the A/D conversion time and does not affect throughput.
Note 7: Specified for completeness only — droop rate does not affect the accuracy of the 1.5 μs conversion process.
Note 8: −6V may be readily derived from the −15V power supply using a 7906-type three-terminal regulator. See Figure 1.
Note 9: The 100 ns pulse width is recommended where possible.

Using the ADAM-826-1 (cont.)

Diagram of Figure 6, and supplying an external S/H mode control signal to the S/H CONTROL IN pin. This signal should be provided by a HCMOS driver so that the logic "1" (HOLD mode) is a solid +5V.

In some system architectures, it may be desirable to introduce a signal, such as a digitally controlled overall system offset correction, between the S/H output and the A/D Converter input. A provision for this is made in the ADAM-826-1 allowing the user to add appropriate circuitry between the S/H OUT and A/D IN pins. If this offset correction signal is changed when the ADAM-826-1 is in the sample mode, then the timing as shown in Figure 7 will not be affected, provided the D/A converter supplying the correction voltage is completely settled prior to the next trigger/start convert command. The connection to the S/H OUT-A/D IN pins from the D/A must be as short as possible; refer to the sections on pc board layout, and the text on the ADAM-826-3.

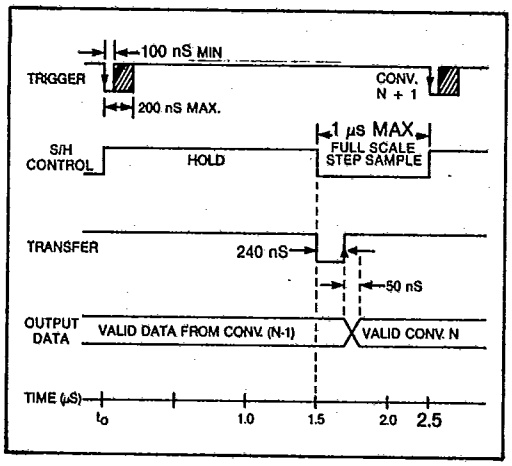

Figure 7. Typical Timing - ADAM-826-1

T-51-10-16

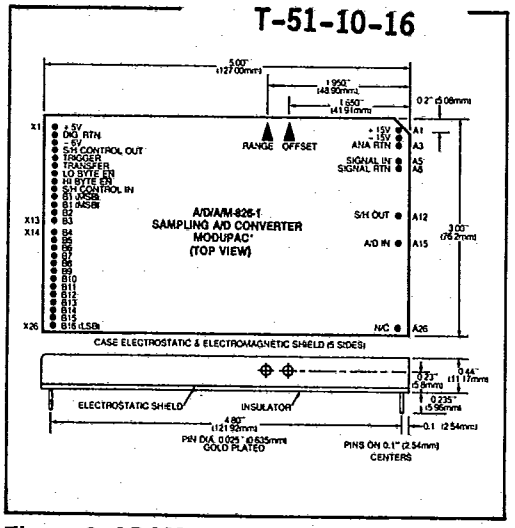

Figure 8. ADAM-826-1 Mechanical & Pinout