Precision, Low Noise, Low Input Bias Current, Wide Bandwidth JFET Operational Amplifiers

Preliminary Technical Data

ADA4610-2

FEATURES

Low T_CV_{OS}: 1 µV/°C typical
Low input bias current: 5 pA typical at V_S = ±15 V
Dual-supply operation: ±4.5 V to ±18 V
Low noise:
7.2 nV/√Hz typical at f = 1 kHz
0.7 μV_{P-P} at 0.1 Hz to 10 Hz
Low distortion: 0.000005%
No phase reversal
Rail-to-Rail Output
Unity gain stable

APPLICATIONS

Instrumentation
Medical Instruments
Multipole filters
Precision current measurement
Photodiode amplifiers
Sensors
Audio

PIN CONFIGURATIONS

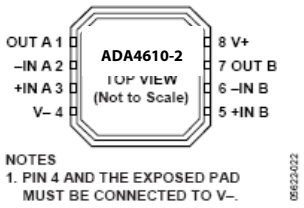

Figure 1. 8-Lead LFCSP (CP Suffix)

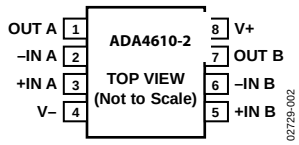

Figure 2. 8-Lead SOIC_N (R Suffix) & 8-Lead MSOP (RM Suffix)

GENERAL DESCRIPTION

The ADA4610-2 is a dual channel, precision JFET amplifier that feature low offset voltage, input bias current, input voltage noise, input current noise, and rail-to-rail output.

The combination of low offsets, low noise, and very low input bias currents makes these amplifiers especially suitable for high impedance sensor amplification and precise current measurements using shunts. The combination of dc precision, low noise, and fast settling time results in superior accuracy in medical instruments, electronic measurement, and automated test equipment. Unlike many competitive amplifiers, the ADA4610 maintain their fast settling performance even with substantial capacitive loads. Unlike many older JFET amplifiers, the ADA4610-2 does not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

Fast slew rate and great stability with capacitive loads make the ADA4610-2 a perfect fit for high performance filters. Low input bias currents, low offset, and low noise result in a wide dynamic range of photodiode amplifier circuits. Low noise and distortion, high output current, and excellent speed make the ADA4610-2 a great choice for audio applications.

The ADA4610-2 is specified over the −40°C to +125°C extended industrial temperature range.

The ADA4610-2A is available in 8-lead narrow SOIC, 8-lead MSOP, and 8-lead LFCSP packages. The ADA4610-2B is available in 8-lead narrow SOIC package.

Rev. PrA

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SPECIFICATIONS

@ V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	B-Grade		TBD	0.4	mV
		−40°C < T_A < +125°C			TBD	mV
		A-Grade		TBD	1	mV
		−40°C < T_A < +125°C			TBD	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	(B-Grade) −40°C < T_A < +125°C		0.5	TBD	µV/°C
		(A-Grade) −40°C < T_A < +125°C		1	TBD	µV/°C
Input Bias Current	I_B			5	TBD	pA
		−40°C < T_A < +85°C			TBD	pA
		−40°C < T_A < +125°C			TBD	nA
Input Offset Current	I_{OS}			2	TBD	pA
		−40°C < T_A < +85°C			TBD	pA
		−40°C < T_A < +125°C			TBD	nA
Input Voltage Range			−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12.5V	TBD	113		dB
		−40°C < T_A < +125°C	TBD			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = ±13.5 V	TBD	107		dB
		−40°C < T_A < +125°C	TBD			dB
Input Resistance	R_{IN}			TBD		Ω
Input Capacitance, Differential Mode	C_{INDM}			2.5		pF
Input Capacitance, Common Mode	C_{INCM}			5.4		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	14.8	14.9		V
		−40°C < T_A < +125°C	TBD			V
		R_L = 600 Ω	14.2	14.3		V
		−40°C < T_A < +125°C	TBD			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		−14.8	−14.7	V
		−40°C < T_A < +125°C			TBD	V
		R_L = 600 Ω		-14.7	-14.6	V
		−40°C < T_A < +125°C			TBD	V
Output Current	I_{OUT}			±40		mA
Closed-Loop Output Impedance	Z_{OUT}	TBD		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	TBD	106		dB
		−40°C < T_A < +125°C	TBD			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		1.85	2	mA
		−40°C < T_A < +125°C			TBD	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		20		V/µs
Gain Bandwidth Product	GBP			10		MHz
Settling Time	t_S	To 0.1%, 0 V to 10 V step, G = +1		TBD		µs
		To 0.01%, 0 V to 10 V step, G = +1		TBD		µs
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, G = +1, R_L = 2 kΩ		0.000005		%
Phase Margin	φ_M			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth		0.7	TBD	µV p-p
Voltage Noise Density	e_n	f = 10 Hz		18		nV/√Hz
		f = 100 Hz		9.2		nV/√Hz
		f = 1 kHz		7.2	TBD	nV/√Hz
		f = 10 kHz		7.7		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		TBD		fA/√Hz

SPECIFICATIONS

@ V_S = ±5 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	B-Grade		TBD	0.4	mV
		−40°C < T_A < +125°C			TBD	mV
		A-Grade		TBD	1	mV
		−40°C < T_A < +125°C			TBD	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	(B-Grade) −40°C < T_A < +125°C		0.5	TBD	µV/°C
		(A-Grade) −40°C < T_A < +125°C		1	TBD	µV/°C
Input Bias Current	I_B			TBD	TBD	pA
		−40°C < T_A < +85°C		5	TBD	pA
		−40°C < T_A < +125°C			TBD	nA
Input Offset Current	I_{OS}			2	TBD	pA
		−40°C < T_A < +85°C			TBD	pA
		−40°C < T_A < +125°C			TBD	nA
Input Voltage Range			−2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±2.5V	TBD	110		dB
		−40°C < T_A < +125°C	TBD			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = ±3.5 V	TBD	107		dB
		−40°C < T_A < +125°C	TBD			dB
Input Resistance	R_{IN}			TBD		Ω
Input Capacitance, Differential Mode	C_{INDM}			2.5		pF
Input Capacitance, Common Mode	C_{INCM}			5.4		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	4.8	4.9		V
		−40°C < T_A < +125°C	TBD			V
		R_L = 600 Ω	4.2	4.3		V
		−40°C < T_A < +125°C	TBD			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		−4.8	−4.7	V
		−40°C < T_A < +125°C			TBD	V
		R_L = 600 Ω		-4.7	-4.6	V
		−40°C < T_A < +125°C			TBD	V
Output Current	I_{OUT}			TBD		mA
Closed-Loop Output Impedance	Z_{OUT}	TBD		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	TBD	106		dB
		−40°C < T_A < +125°C	TBD			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		1.85	2	mA
		−40°C < T_A < +125°C			TBD	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		20		V/µs
Gain Bandwidth Product	GBP			10		MHz
Settling Time	t_S	To 0.1%, 0 V to 4 V step, G = +1		TBD		µs
		To 0.01%, 0 V to 4 V step, G = +1		TBD		µs
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, G = +1, R_L = 2 kΩ		0.000005		%
Phase Margin	φ_M			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth		0.7	TBD	µV p-p
Voltage Noise Density	e_n	f = 10 Hz		18		nV/√Hz
		f = 100 Hz		9.2		nV/√Hz
		f = 1 kHz		7.2	TBD	nV/√Hz
		f = 10 kHz		7.7		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		TBD		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$\pm V_S$
Output Short-Circuit Duration to GND	Observe derating curves
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Electrostatic Discharge (Human Body Model)	2000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead MSOP (RM)	142	45	°C/W
5-Lead SOT23 (RJ)	190	92	°C/W
8-Lead LFCSP (CP)	TBD	TBD	°C/W
8-Lead SOIC_N (R)	120	45	°C/W
14-Lead SOIC_N (R)	115	36	°C/W
16-Lead LFCSP (CP)	TBD	TBD	°C/W

[1] θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages. This was measured using a standard 4-layer board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.