M54992P/FP

Bi-CMOS 24-BIT SERIAL-INPUT LATCHED DRIVER

DESCRIPTION

The M54992 is a semiconductor integrated circuit consisting of 24 stages of CMOS shift registers and latches with serial inputs and serial or parallel outputs. It is based on Bi-CMOS process technology, and has 24 bipolar drivers at the parallel outputs.

FEATURES

- Serial input and serial or parallel output
- Serial output enables cascade connection
- Built-in latch for each stage
- Enable input provides output control
- Low supply current (standby current $I_{CC} \leq 1mA$)
- Serial I/O level is compatible with typical CMOS devices
- Driver features: High withstand voltage ($BV_{CEO} \geq 30V$)
  Capable of large drive currents ($I_{O(max)}=100mA$)
- Wide operating temperrature range T_a=-10 – +75°C

APPLICATION

Dot drivers of thermal printer heads, serial/parallel conversion. Drivers for relays and solenoids.

FUNCTION

The M54992 consists of 24 stages of D-type flip flops connected to 24 latches.

Data is input to serial input S-IN, and clock pulses are input to clock input T. When the clock changes from low to high, the input data enters the first shift register and data already in the shift registers is shifted sequentially.

The serial output S-OUT is used to connect multiple M54992 to expand the number of parallel outputs. S-OUT is connected to S-IN of the next stage.

For parallel output. When the clock pulse changes from low to high, latch input (LATCH) is high and output enable input ($\overline{EN}$) is low the serial input data at S-IN appears at output $\overline{O_1}$ and the other data already present is shifted sequentially to outputs $\overline{O_2}$ through $\overline{O_{24}}$.

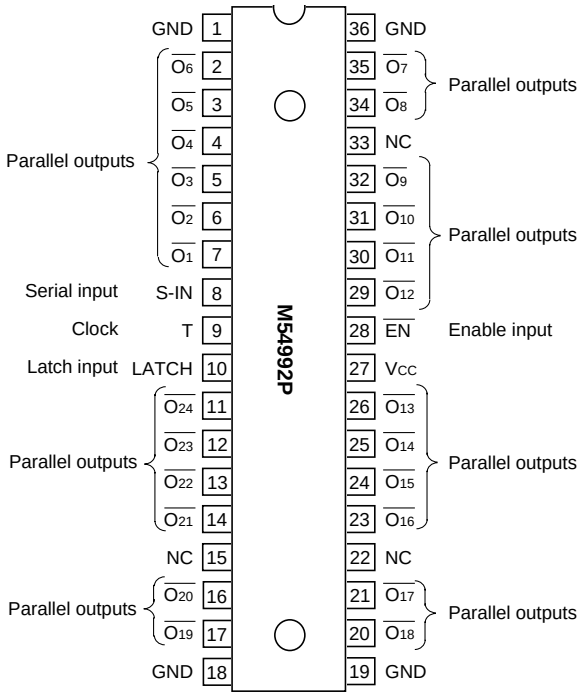
The parallel outputs are inverted.

When the latch input is held low, the latch retains the stored data. When the $\overline{EN}$ input is high, outputs $\overline{O_1}$ through $\overline{O_{24}}$ all turn off. As the internal logic is unstable when the power is turned on, the $\overline{EN}$ input should be kept high (setting outputs $\overline{O_1}$ through $\overline{O_{24}}$ off) until input data is set and the internal logic is initialized.

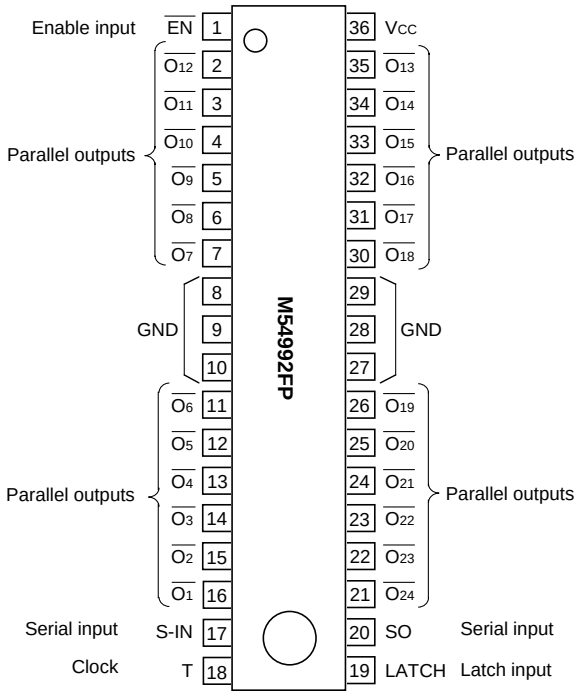
L-GND is the GND of CMOS logic circuit and P-GND is the GND of output driver circuits $\overline{O_1}$ through $\overline{O_{24}}$ which employ bipolar transistors capable of large drive currents.

An output load prevention circuit is built in this IC to prevent misoperation at power ON/OFF. Therefore, when V_{CC} falls short of the fixed level, all outputs ($\overline{O_1}$ – $\overline{O_{24}}$) are compulsorily set to the OFF state.

PIN CONFIGURATION (TOP VIEW)



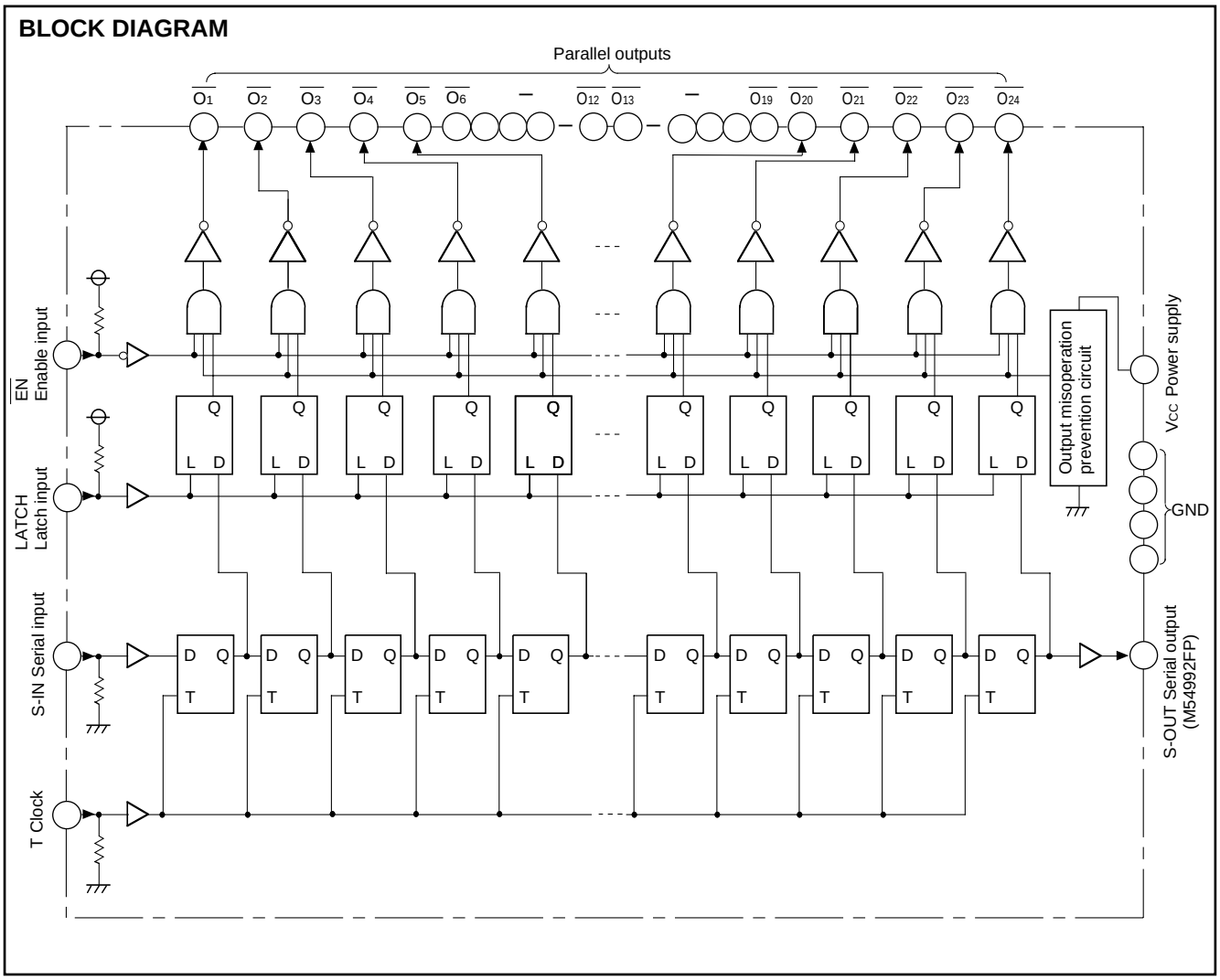
Outline 36P4E



Outline 36P2R-A

NC: no connection

BLOCK DIAGRAM



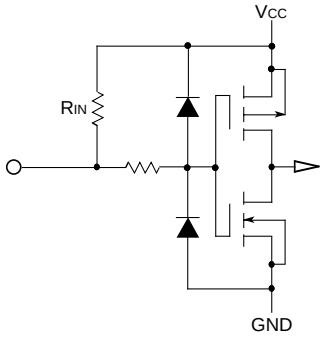
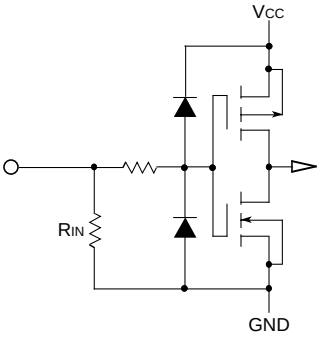
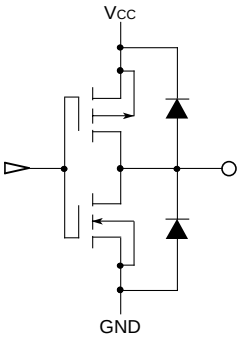
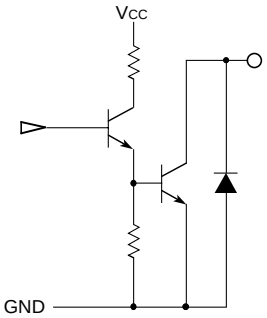
TRUTH TABLE

Input				Output	
S-IN	T	LATCH	$\overline{EN}$	$\overline{O1}$–$\overline{O24}$	S-OUT
L	IN	L	L	t-1	L
L	IN	H	L	L	L
H	IN	L	L	t-1	H
H	IN	H	L	H	H
H	IN	H	H	L	H

T: IN means to input following signal

L : low level
H : high level
t-1 : previous state
H output : OFF state
L output : ON state

INPUT/OUTPUT CIRCUIT DIAGRAM

1 Inputs with pullup resistor ($\overline{EN}$, LATCH) 	2 Inputs with pulldown resistor (T, S-IN) 
3 Serial output (M54992FP) (S-OUT) 	4 Parallel outputs ($\overline{O1}$ – $\overline{O24}$) 

ABSOLUTE MAXIMUM RATINGS (Ta=-10 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions		Ratings	Unit
V_{CC}	Supply voltage			-0.5 – 8	V
V_I	Input voltage			-0.5 – V_{CC}+0.5	V
V_O	Output voltage	S-OUT	M54992FP	-0.5 – V_{CC}+0.5	V
		$\overline{O_1}$ – $\overline{O_{24}}$: OFF		-0.5 – 30	V
I_O	Output current			120	mA
P_d	Power dissipation	Ta=25°C Mounted on a board	M54992P	2.0	W
			M54992FP	1.9	W
T_{opr}	Operating temperature			-10 – 75	°C
T_{stg}	Storage temperature			-55 – 125	°C

RECOMMENDED OPERATING CONDITION (Ta=-10 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4	5	6	V
V_O	Output apply voltage	$\overline{O_1}$ – $\overline{O_{24}}$: OFF			30	V
I_O	Output current (per circuit)	$\overline{O_1}$ – $\overline{O_{24}}$: ON Duty cycle : 50% or below			100	mA

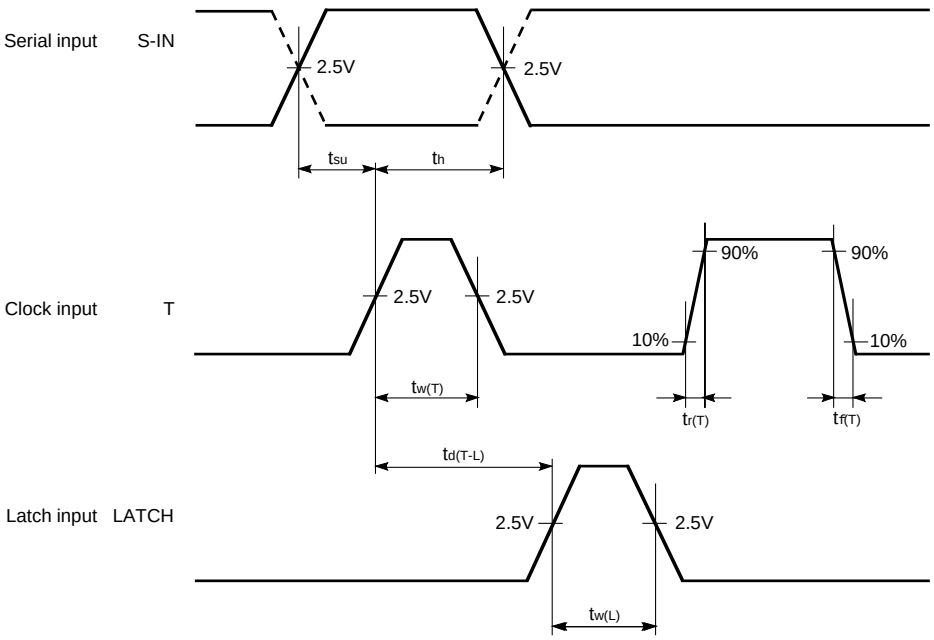
ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage	Ta=-10 – 75°C, V_{CC}=4 – 6V		0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
I_{IH}	High-level input current	T, S-IN	V_{IH}=5V	—		25	μA
I_{IL}	Low-level input current	$\overline{EN}$, LATCH	V_{IL}=0V	—		-25	μA
V_{OH}	High-level output voltage	|I_O|≤1μA	M54992FP (S-OUT)	4.9		—	V
V_{OL}	Low-level output voltage			—		0.1	V
I_{OH}	High-level output current	V_{OH}=4.5V		-100		—	μA
I_{OL}	Low-level output current	V_{OL}=0.4V		400		—	μA
V_{OL1}	Low-level output voltage	I_{OL}=100mA	$\overline{O_1}$ – $\overline{O_{24}}$	—		0.55	V
V_{OL2}		I_{OL}=80mA	$\overline{O_1}$ – $\overline{O_{24}}$	—		0.4	V
I_{OLK}	Output leak current	V_O=30V(output: OFF)	$\overline{O_1}$ – $\overline{O_{24}}$	—		50	μA
I_{CC1}	Supply current	Input: open All driver outputs are OFF.		—		1	mA
I_{CC2}		One driver output is ON.		—	3.5	5.0	mA
V_{T+}	Misoperation prevention supply voltage.			2.9	3.4	3.9	V
V_{T-}				2.6	3.1	3.6	V

TIMING REQUIREMENTS (Ta=-10 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$f_{(T)}$	Clock frequency	Input duty cycle: 45 – 55%			4	MHz
$t_{w(T)}$	Clock pulse width		100			ns
$t_{w(L)}$	Latch pulse width		100			ns
t_{su}	Data setup time		50			ns
t_h	Data hold time		20			ns
$t_{d(T-L)}$	Clock-latch time		400			ns
$t_{r(T)}$	Clock pulse rise time				500	ns
$t_{f(T)}$	Clock pulse fall time				500	ns

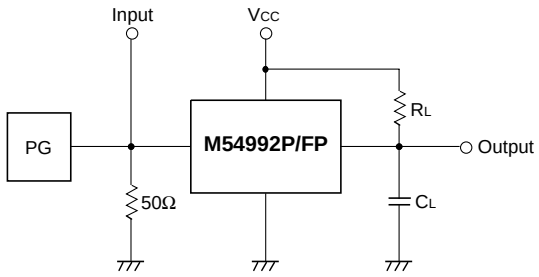
TIMING CHART



SWITCHING CHARACTERISTICS (Ta=25°C, VCC=5V, unless otherwise noted)

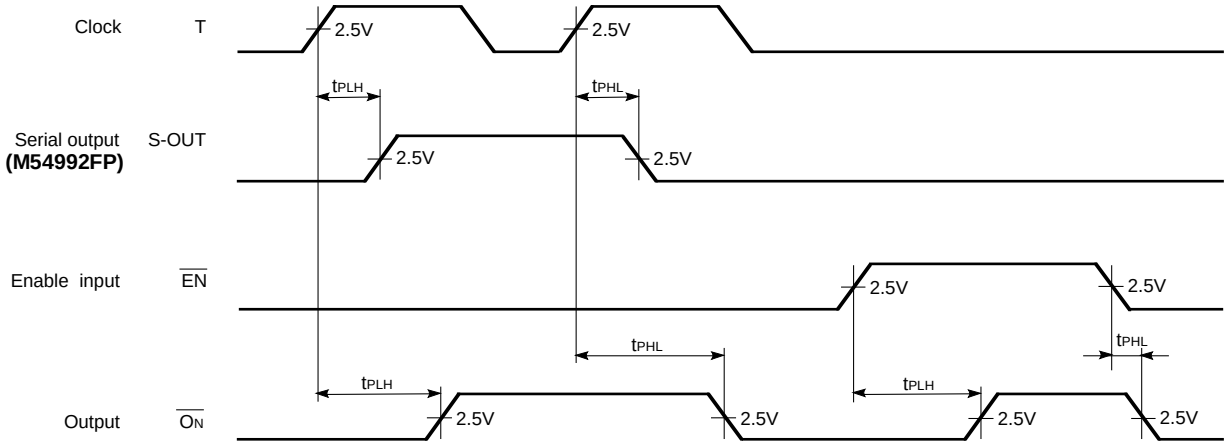
Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
t_{PLH}	Low-to-high-level output propagation time From input T to output S-OUT	V_{IH}=5V V_{IL}=0V $R_{L(S\text{-}OUT)}=\infty$ $R_{L(\overline{ON})}$=100Ω (N=1–24) C_L=15pF	M54992FP			0.2	µs
t_{PHL}	High-to-low-level output propagation time From input T to output S-OUT					0.2	µs
t_{PLH}	Low-to-high-level output propagation time From input T to output $\overline{ON}$					10	µs
t_{PHL}	High-to-low-level output propagation time From input T to output $\overline{ON}$					5	µs
t_{PLH}	Low-to-high-level output propagation time From input $\overline{EN}$ to output $\overline{ON}$					10	µs
t_{PHL}	High-to-low level output propagation time From input $\overline{EN}$ to output $\overline{ON}$					5	µs

TEST CIRCUIT



- The input waveform: $t_r \leq 20ns$, $t_f \leq 20ns$
- The capacitance C_L includes the wiring stray capacitance and probe input capacitance.

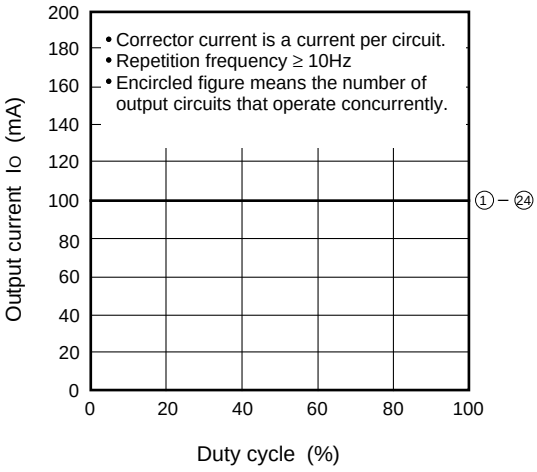
TIMING CHART



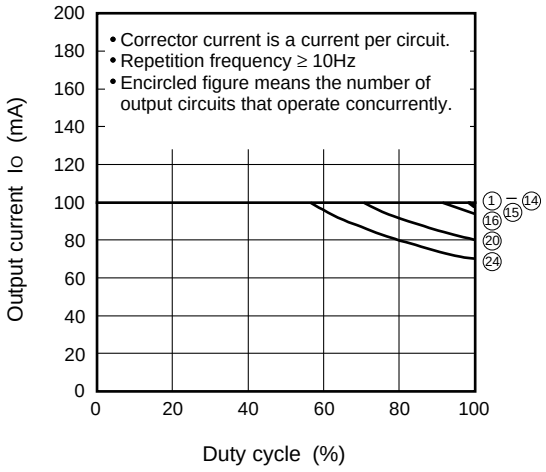
(N=1 – 24)

TYPICAL CHARACTERISTICS (V_{CC}=5V, unless otherwise noted)

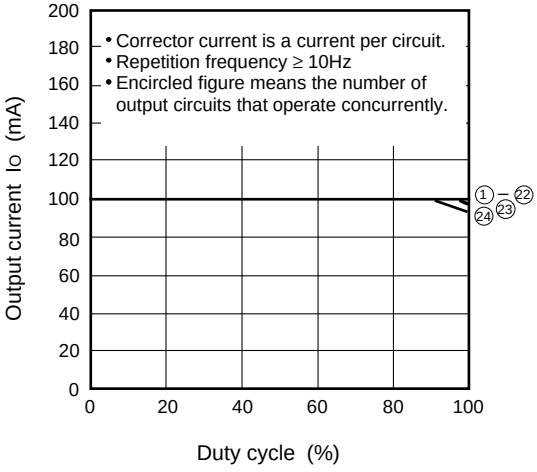
Duty cycle vs. allowable output current
(M54992P)



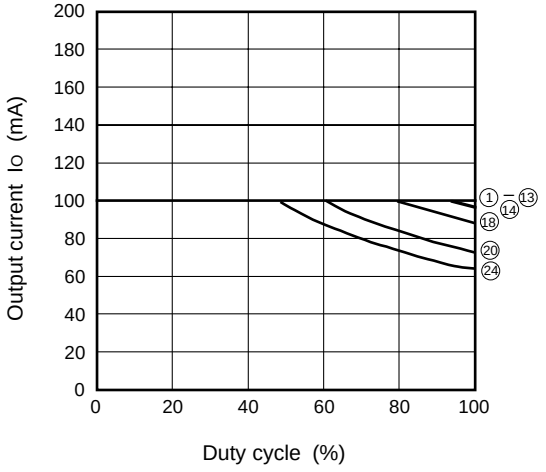
Duty cycle vs. allowable output current
(M54992P)



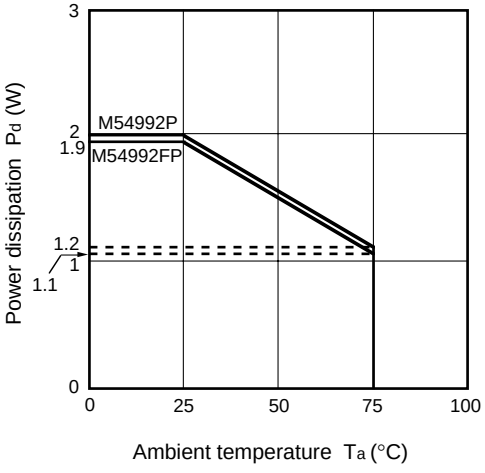
Duty cycle vs. allowable output current
(M54992FP)



Duty cycle vs. allowable output current
(M54992FP)



Thermal derating
(Absolute maximum ratings)



Driver output V_{OL} vs. I_{OL}