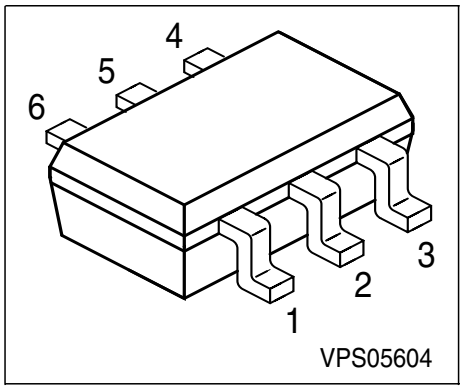
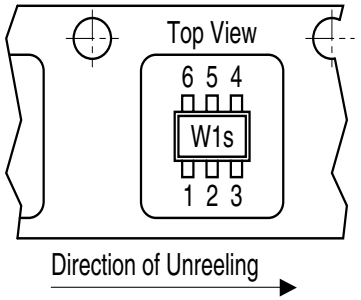
Si-MMIC-Amplifier **in SIEGET 25-Technologie**



- Multifunctional casc. 50 Ω block (LNA / MIX)
- Unconditionally stable
- Gain $|S_{21}|^2$ = 18.5 dB at 1.8 GHz (Appl.1)
  gain $|S_{21}|^2$ = 22 dB at 1.8 GHz (Appl.2)
  IP_{3out} = +7 dBm at 1.8 GHz (V_D=3V,I_D=9.5mA)
- Noise figure *NF* = 2.2 dB at 1.8 GHz
- Reverse isolation >28 dB (appl.1) >35 dB (Appl.2)
- Typical device voltage V_D = 2 V to 5 V

Tape loading orientation

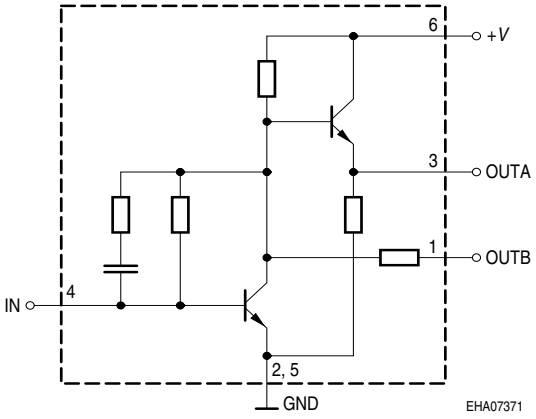


Marking on SOT-363 package
(for example W1s)
corresponds to pin 1 of device

Position in tape: pin 1
opposite of feed hole side

EHA07193

Circuit Diagram



ESD: **E**lectro**s**tatic **d**ischarge sensitive device,
observe handling precaution!

Type	Marking	Pin Configuration						Package
BGA 425	BMs	1,OutB	2,GND	3,OutA	4,IN	5,GND	6,+V	SOT-363

Maximum Ratings

Parameter	Symbol	Value	Unit
Device current	I_D	25	mA
Device voltage	V_D,+V	6	V
Total power dissipation, T_S = 120 °C [1)]	P_{tot}	150	mW
RF input power	P_{RFin}	-10	dBm
Junction temperature	T_j	150	°C
Ambient temperature	T_A	-65 ... 150	
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Junction - soldering point	R_{thJS}	≤ 335	K/W

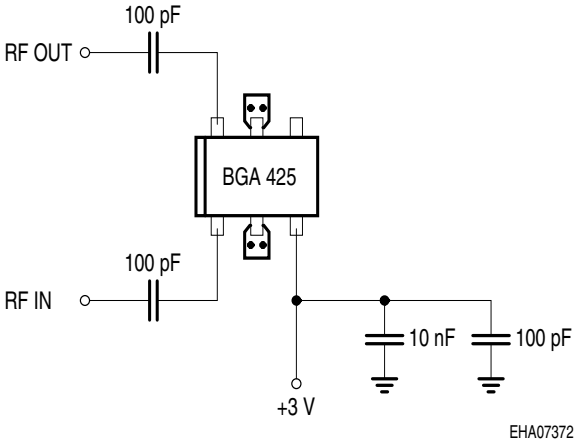
[1] T_S is measured on the ground lead at the soldering point to the pcb

Electrical Characteristics at T_A = 25 °C, unless otherwise specified.

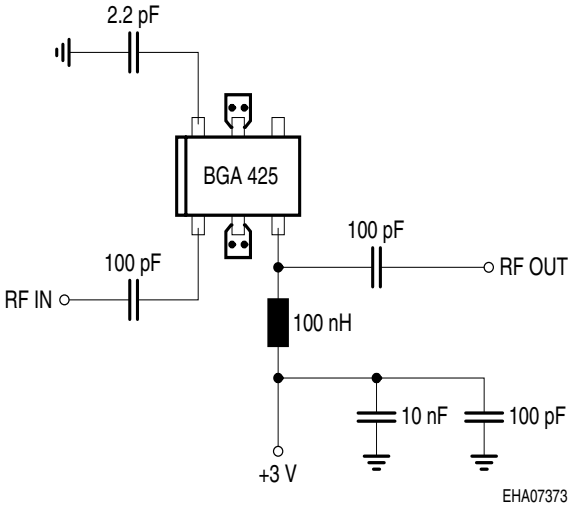
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC characteristics V_D = 3V, Z_o = 50Ω, Testfixture Appl.1					
Device current	I_D	8.5	9.5	10.5	mA
Insertion power gain	$\|S_{21}\|^2$				dB
f = 0.1 GHz		-	27	-	
f = 1 GHz		-	22	-	
f = 1.8 GHz		-	18.5	-	
Reverse isolation f = 1.8 GHz	S12	-	28	-	
Noise figure	NF				
f = 0.1 GHz		-	1.9	-	
f = 1 GHz		-	2	-	
f = 1.8 GHz		-	2.2	-	
Intercept point at the output f = 1.8 GHz	IP_{3out}	-	+ 7	-	dBm
Return loss input f = 1.8 GHz	RL_{in}	-	>13	-	dB
Return loss output f = 1.8 GHz	RL_{out}	-	>7	-	

Typical configuration
Application 1 - 3 (LNA)
Application 4 (Mix)

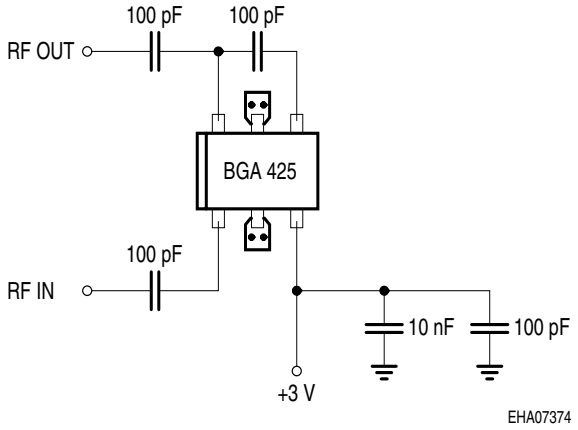
Appl.1



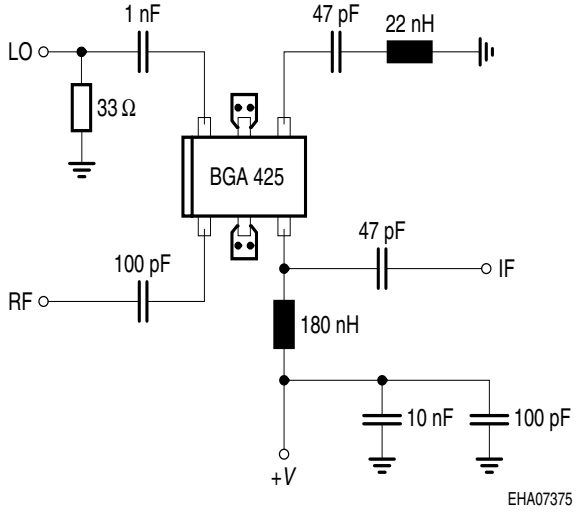
Appl.2



Appl.3



Appl.4



Note: 1) Large-value capacitors should be connected from pin 6 to ground right at the device to provide a low impedance path! (appl. 1)

2) The use of plated through holes right at pin 2 and 5 is essential for pc-board-applications. Thin boards are recommended to minimize the parasitic inductance to ground!

3) For more information please see application note 028 and 030.

Electrical characteristics at T_A = 25 °C, unless otherwise specified.
VD = 3 V
Application 1 to 4

Applic.	**Insertion Gain $\|S_{21}\|^2$ (dB) Frequ. (GHz)**			**Noise Figure *NF* (dB) Frequ. (GHz)**			**Reverse Isol. S12 (dB) Frequ. (GHz)**			**Return Loss Input RL_{in} (dB) Frequ. (GHz)**			**Return Loss Output RL_{out} (dB) Frequ. (GHz)**		
	0.1	1	1.8	0.1	1	1.8	0.1	1	1.8	0.1	1	1.8	0.1	1	1.8
1 (LNA)	27	22	18.5	1.9	2	2.2	46	32	28	19	19	18	10	12	13
2 (LNA)	10	22	22	-	1.9	2.1	35	35	37	13	15	8	5	10	11 *)
3 (LNA)	24	20	16	1.9	2	2.2	34	30	26	8	10	14	15	17	11
4 (MIX)	e.g.: RF = 900 MHz, IF = 100 MHz, VD = 3 V Conversion gain: 20 dB Intercept point output: 0 dBm Noise figure: < 5 dB LO-power: +3 dBm														

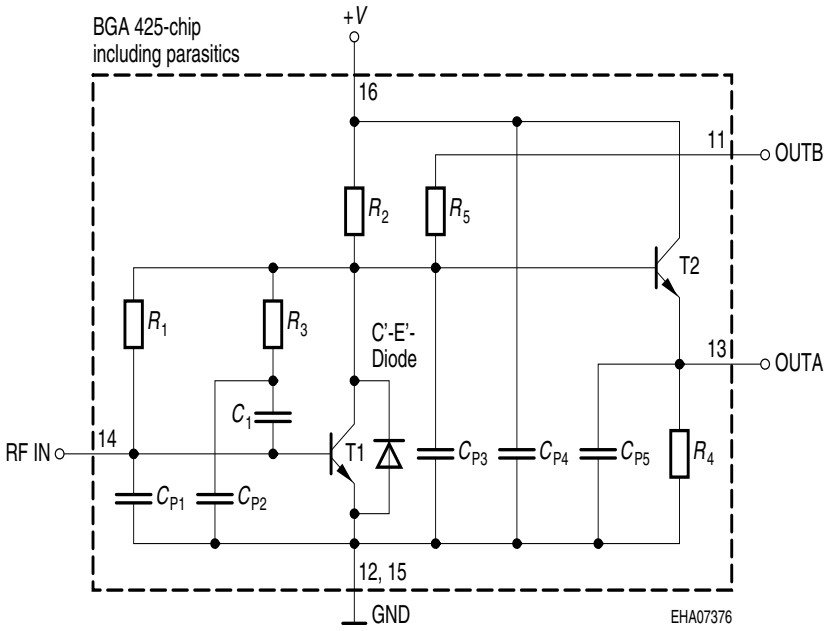
*) 2.2 pF by-pass capacitance and 100 nH bias-inductance

For linear simulation please use on-wafer measurement data of our T501 chip an add resistive and capacitive elements, parasitics and package equivalent circuit.

S-Parameters at T_A = 25 °C (On-wafer measurement data T501)

f	S_{11}		S_{21}		S_{12}		S_{22}	
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
T1, V_{CE} = 1.7 V, I_C = 4.7 mA								
0.1	0.7996	-8	11.8466	172.4	0.0111	118	0.9942	0
0.3	0.8223	-15.5	11.9814	169	0.0126	90.9	0.9853	-5.7
0.5	0.8294	-26.3	11.9702	162.6	0.0163	75.9	0.9675	-9.6
0.7	0.8162	-34.4	11.4624	156.8	0.019	72.4	0.9529	-13.5
0.9	0.81	-44.5	11.1452	149.5	0.0208	64.7	0.9286	-17.2
1.1	0.793	-52.8	10.739	144.6	0.0281	62.4	0.9094	-20.4
1.3	0.7884	-61.8	10.3219	138.9	0.0332	58.2	0.8842	-23.5
1.5	0.7651	-69.1	9.7368	134	0.0373	54	0.8523	-25.9
1.7	0.7534	-75.9	9.3137	130.2	0.0383	49.3	0.8221	-28.2
1.9	0.74	-81.8	8.8247	126	0.0404	45.6	0.7939	-30.2
2.1	0.7391	-88.4	8.4426	121.9	0.0417	44.1	0.7721	-32.7
2.3	0.7335	-96	8.089	118	0.0451	41.6	0.7476	-34.5
2.5	0.7186	-98.4	7.6674	115.5	0.0465	40.8	0.7339	-35.7
2.7	0.7193	-103.1	7.3034	113.2	0.049	40	0.716	-37.3
2.9	0.702	-108	6.7988	109.9	0.0492	37	0.6885	-38.6
3.1	0.6897	-112.6	6.4921	107.4	0.0501	36.7	0.6743	-39.7
T2, V_{CE} = 2.2 V, I_C = 4.7 mA								
0.1	0.8144	-8.3	11.9941	172.1	0.0154	129.2	0.985	-0.5
0.3	0.8094	-15.3	12.1389	169	0.01	80.7	0.9906	-5.6
0.5	0.8251	-25.8	12.1376	162.7	0.0129	76.3	0.9728	-0.1
0.7	0.8171	-34.4	11.6229	157	0.0183	70.8	0.9557	-12.7
0.9	0.7957	-44.9	11.3048	149.7	0.0227	70.7	0.9375	-16
1.1	0.7952	-52.5	10.8874	144.8	0.0261	64.2	0.9147	-19
1.3	0.7953	-61.9	10.4735	139.2	0.0307	60.7	0.8916	-22.4
1.5	0.767	-68.6	9.8866	134.3	0.0325	54	0.8595	-24.5
1.7	0.7618	-75.5	9.4501	130.5	0.0361	48	0.8322	-26.6
1.9	0.7384	-81.3	8.9757	126.3	0.0374	49.2	0.8019	-28.6
2.1	0.739	-88.7	8.5788	122.1	0.04	44.3	0.7857	-30.9
2.3	0.7285	-95.8	8.2231	118.2	0.0416	39.7	0.7625	-32.9
2.5	0.718	-97.9	7.7991	115.5	0.0463	40.4	0.7467	-33.7
2.7	0.7294	-102.9	7.429	113.4	0.043	38.8	0.7273	-35.8
2.9	0.6955	-107.8	6.9444	110	0.0468	35.7	0.7077	-36.7
3.1	0.6868	-111.9	6.6064	107.6	0.0481	34.2	0.689	-37.6

Spice model



T1	T501
T2	T501
R_1	14.5kΩ
R_2	280Ω
R_3	2.4kΩ
R_4	170Ω
R_5	22Ω
R_{P1}	1kΩ
C_1	2.3pF
C_{P1}	0.2pF
C_{P2}	0.2pF
C_{P3}	0.6pF
C_{P4}	0.1pF
C_{P5}	0.1pF
C'-E'-diode	T1

Transistor Chip Data T1 (Berkley-SPICE 2G.6 Syntax) :

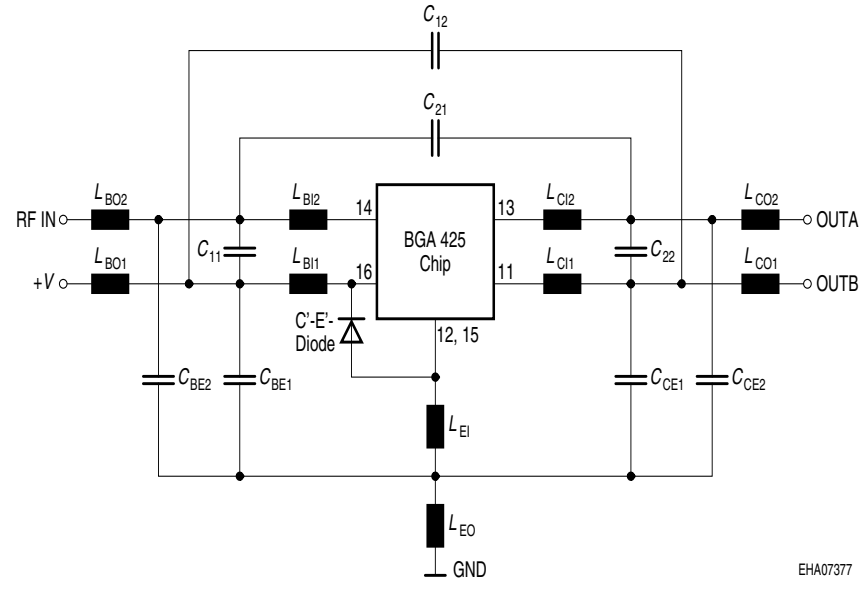
IS =	0.21024	fA	BF =	83.23	-	NF =	1.0405	-
VAF =	39.251	V	IKF =	0.16493	A	ISE =	15.761	fA
NE =	1.7763	-	BR =	10.526	-	NR =	0.96647	-
VAR =	34.368	V	IKR =	0.25052	A	ISC =	0.037223	fA
NC =	1.3152	-	RB =	15	Ω	IRB =	0.21215	A
RBM =	1.3491	Ω	RE =	1.9289		RC =	0.12691	Ω
CJE =	3.7265	fF	VJE =	0.70367	V	MJE =	0.37747	-
TF =	4.5899	ps	XTF =	0.3641	-	VTF =	0.19762	V
ITF =	1.3364	mA	PTF =	0	deg	CJC =	96.941	fF
VJC =	0.99532	V	MJC =	0.48652	-	XCJC =	0.08161	-
TR =	1.4935	ns	CJS =	0	fF	VJS =	0.75	V
MJS =	0	-	XTB =	0	-	EG =	1.11	eV
XTI =	3	-	FC =	0.99469	-	TNOM	300	K

C'-E'-Diode Data (Berkley-SPICE 2G.6 Syntax) :

IS =	2	fA	N =	1.02	-	RS =	20	Ω

All parameters are ready to use, no scaling is necessary

Package Equivalent Circuit:



L_{BI1} =	0.4	nH
L_{BI2} =	0.7	nH
L_{BO1} =	0.3	nH
L_{BO2} =	0.3	nH
L_{EI} =	0.3	nH
L_{EO} =	0.1	nH
L_{CI1} =	0.4	nH
L_{CI2} =	0.4	nH
L_{CO1} =	0.3	nH
L_{CO2} =	0.3	nH
C_{BE1} =	200	fF
C_{BE2} =	200	fF
C_{CE1} =	200	fF
C_{CE2} =	200	fF
C_{11} =	5	fF
C_{22} =	5	fF
C_{12} =	50	fF
C_{21} =	50	fF

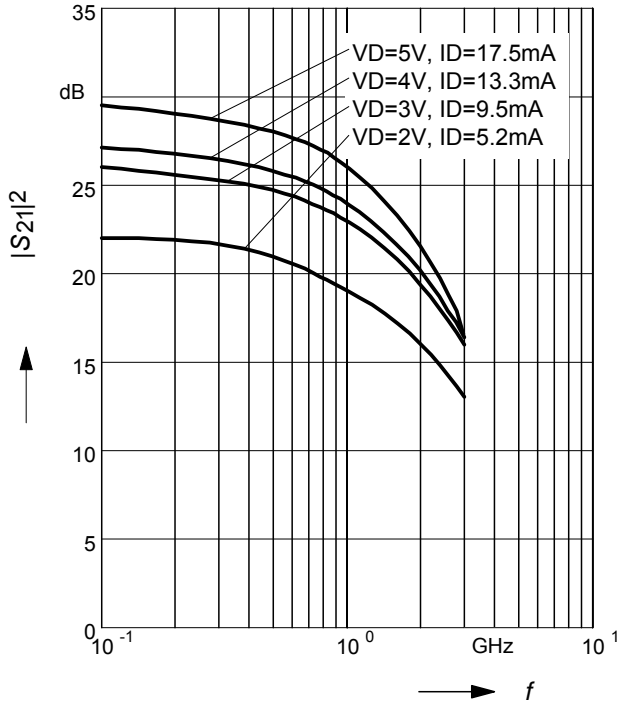
Valid up to 3GHz

Extracted on behalf of SIEMENS Small Signal Semiconductors by:
Institut für Mobil-und Satellitentechnik (IMST)

For examples and ready to use parameters please contact your local Infineon Technologies distributor or salesoffice to obtain a Infineon Technologies CD-ROM or see Internet: http://www.infineon.com/products/discrete/index.htm

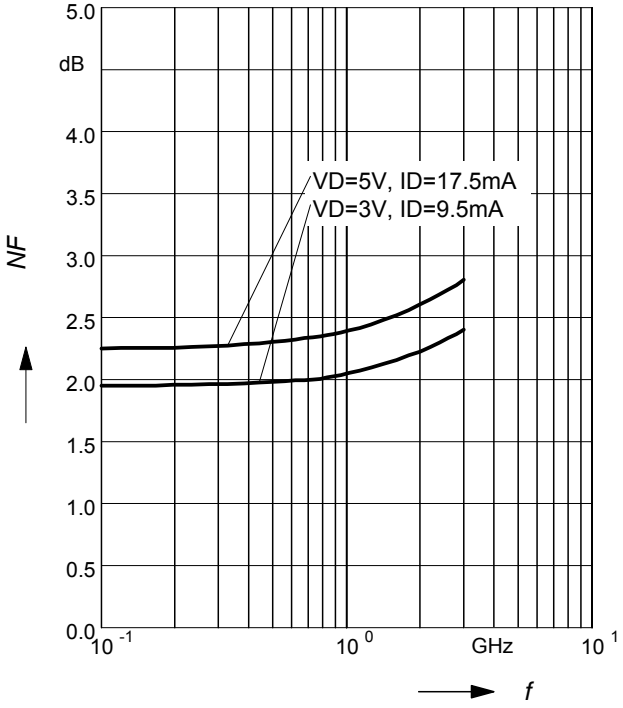
Insertion power gain $|S_{21}|^2 = f(f)$

V_D, I_D = parameter



Noise figure $NF = f(f)$

V_D,I_D = parameter



Intercept point at the output

$IP_{3out} = f(f)$

V_D,I_D = parameter