# ANALOG DEVICES

# Rigid Disk Data Channel Qualifier

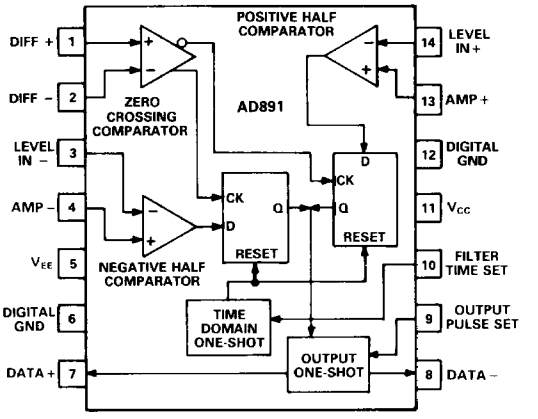
# AD891

**FEATURES**

**Three Matched, Offset-Trimmed Comparators**
**3.1 ns (typ) Comparator Propagation Delay**
**ECL Logic Permits 50 Mb/s Transfer Rates**
**6.8 ns Delay (typ) from Inputs to Data Output**
**500 ps (typ) Additional Pulse Pairing**
**Temperature-Compensated Operation**
**Compatible with 10 KH ECL Logic**
**Two Temperature-Compensated One-Shots**
**One-Shot Periods Set Using External Resistors**

AD891 FUNCTIONAL BLOCK DIAGRAM

Cerdip (Q) Package




## PRODUCT DESCRIPTION

The AD891 disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891 provides both level and time-domain qualification. Level qualification is performed on alternating half cycles of the data waveform using a user-defined threshold level which is applied to each of two 3.1 ns propagation delay comparators. This technique prevents single bit errors from being propagated into two bit errors. A third comparator is used to provide zero-crossing detection. Factory trimmed offsets and a careful internal layout ensure symmetric operation and low pulse pairing with a differential input waveform.

An external RLC passive delay-line differentiator should be used with the AD891; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

The outputs from the amplitude-qualification comparators are applied to the "D" inputs of two master-slave D-type flip-flops which are then clocked by the outputs from the zero-crossing comparator. Each valid zero-crossing event causes a one-shot with a user-definable period to be triggered. This disables the operation of the flip-flops, thus preventing the detection of additional zero-crossing events during the one-shot period.

Simultaneously, an output one-shot is activated, the leading edge of which is synchronous with the change in the flip-flop outputs. The period of this one-shot is also user-definable and is intended to ensure adequate output pulse duration for transmission within the external environment. Each one-shot requires a single metal-film resistor to set its period. All one-shots have trimmed pulse periods; temperature stability is maintained by the use of an internal bandgap reference.

The AD891's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600 ps per gate. The output data conforms to standard 10 KH ECL logic levels. The AD891 can drive a properly terminated 75 Ω transmission line.

The AD891 is specified to operate over the commercial (0 to +70°C) temperature range. It is available either in a 14-pin cerdip package or in a 20-pin PLCC package.

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# SPECIFICATIONS (@ +25°C and 5 V dc, unless otherwise noted)

| Model | Conditions | AD891J Min | Typ | Max | Units |
|---|---|---|---|---|---|
| COMPARATOR SPECIFICATIONS | | | | | |
| Propagation Delay | 20 mV Overdrive | | 3.3 | | ns |
| | 200 mV Overdrive | | 3.1 | | ns |
| Comparator Mismatch | | | | 300 | ps |
| Input Offset Voltage | | | 0.25 | **1.0** | mV |
| Noise Induced Offset Voltage | $10^8$ Error Rate | | ±300 | | μV |
| Input Offset Current | | | 100 | | nA |
| Input Bias Current | | | 1.6 | 3 | μA |
| Open-Loop Gain | f = 10 MHz | | 66 | | dB |
| Input Resistance | Differential | | 500 | | kΩ |
| Input Capacitance | Differential | | **1** | 5 | pF |
| Input Common-Mode Range | Referred to Digital GND | −1.5 | | +2.2 | V |
| INTERNAL LOGIC SPECIFICATIONS | | | | | |
| Logic "1" Level | | −0.98 | −0.85 | −0.81 | V |
| Logic "0" Level | | −1.95 | −1.85 | −1.63 | V |
| Rise Time | | | 1.2 | | ns |
| Fall Time | | | 1.0 | | ns |
| D-Type Flip-Flops | | | | | |
| Clock – Q Delay | | | 1.3 | | ns |
| Clock – $\overline{Q}$ Delay | | | 1.2 | | ns |
| Reset – Q Delay | | | 0.6 | | ns |
| Reset – $\overline{Q}$ Delay | | | 0.55 | | ns |
| ONE-SHOT SPECIFICATIONS | | | | | |
| Resistor Scaling[1] | | One-Shot Pulse ≈ 7+3.1 $R_{SET}$ | | | |
| Pulse Duration | $R_{SET} = R_{min}$ to $R_{max}$ | 9 | | 180 | ns |
| | $R_{SET}$ = 30 kΩ | **95** | 100 | **105** | ns |
| | $R_{SET}$ = 10 kΩ | **35** | 38 | **41** | ns |
| Resistor Range | $R_{SET} = R_{min}$ to $R_{max}$ | 0.75 | | 56 | kΩ |
| EXTERNAL LOGIC SPECIFICATIONS[2] | $T_J$ = +25°C | | | | |
| Output Logic "1" | | −0.98 | −0.85 | −0.81 | V |
| Output Logic "0" | | −1.95 | −1.85 | −1.63 | V |
| Rise Time | | | 1.4 | | ns |
| Fall Time | | | 1.2 | | ns |
| DATA THROUGHPUT SPECIFICATIONS | | | | | |
| Propagation Delay[3] | Differentiator Input to Data Output | | 6.8 | | ns |
| Additional Pulse Pairing[4] | 200 mV Overdrive 5 ns Input Rise Time | **0** | 500 | **1000** | ps |
| Max Transfer Rate | | 50 | | | Mb/s |
| Min Transfer Rate[5] | | | | 1 | Mb/s |
| POWER SUPPLY REQUIREMENTS | | | | | |
| Operating Range | | | | | |
| $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| $V_{EE}$ | | −4.68 | −5.2 | −5.72 | V |
| Quiescent Current | $T_{min}$ to $T_{max}$ | | | | |
| $V_{CC}$ | | 15 | 23 | 35 | mA |
| $V_{EE}$ | | 55 | 68 | 85 | mA |

NOTES

[1]One-shot pulse in ns; $R_{SET}$ specified in kΩ.

[2]Logic specifications obtained for the "Data +" and "Data −" outputs using 1 kΩ pull-down resistors tied to $V_{EE}$ and 100 Ω resistors connected to −2 V.

[3]Propagation delay is measured from the zero-crossing comparator input to the "Data +" output with 200 mV overdrive.

[4]Measurements were performed using a ±100 mV square wave having a rise time under 5 ns; this was applied to the input of the zero-crossing comparator. The resultant pulse pairing is the difference in delay times for two consecutive output pulses.

[5]The minimum transfer rate is limited only by the maximum recommended one-shot period of 180 ns.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

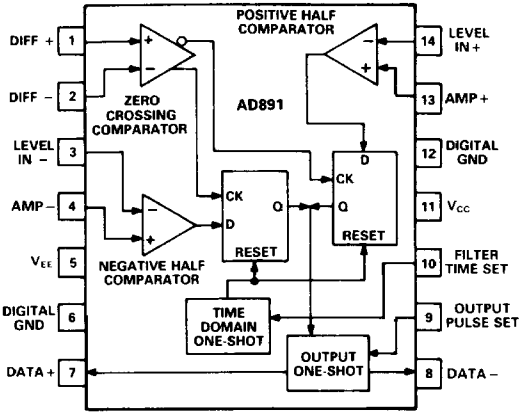
## ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±7.5 V
Comparator Differential Input Voltage . . . . . ±5.6 V
Storage Temperature Range P, Q . . . . . −65°C to +150°C
Operating Temperature Range[2]
AD891P, AD891Q . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

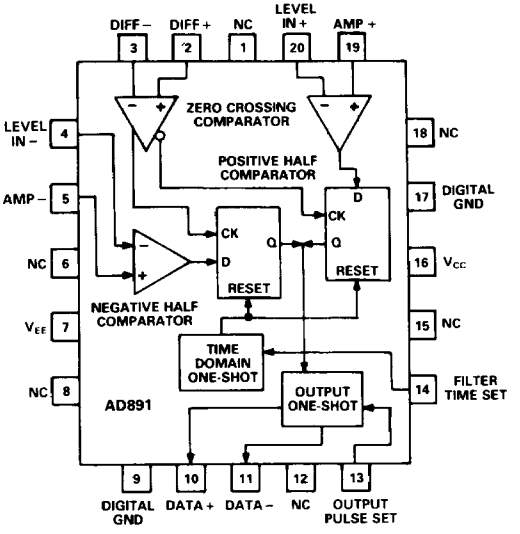
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]20-pin PLCC package: $\theta_{JA}$ = +70°C/Watt;
14-pin cerdip package: $\theta_{JA}$ = +105°C/Watt.

## PIN CONFIGURATIONS

### 14-Pin Cerdip (Q) Package




### 20-Pin PLCC (P) Package




### ORDERING GUIDE*

| Model No. | Description | Package Option |
|---|---|---|
| AD891JQ | 14-Pin Cerdip | Q-14 |
| AD891JP | 20-Pin PLCC | P-20A |

*See Section 20 for package outline information.

## Typical Characteristics (@ +25°C with ±5 V Supplies)

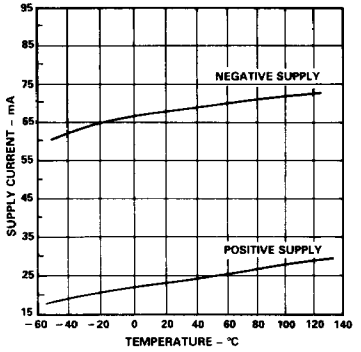



*Figure 1. Supply Current vs. Temperature*

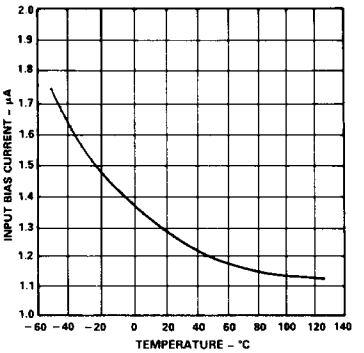



*Figure 2. Comparator Input Bias Current vs. Temperature*

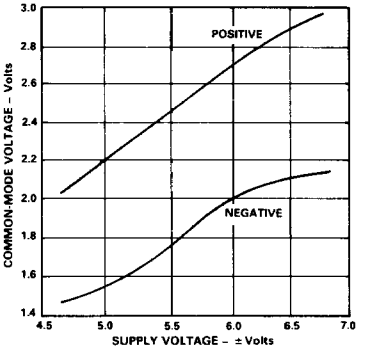



*Figure 3. Comparator Common-Mode Voltage vs. Supply Voltage*

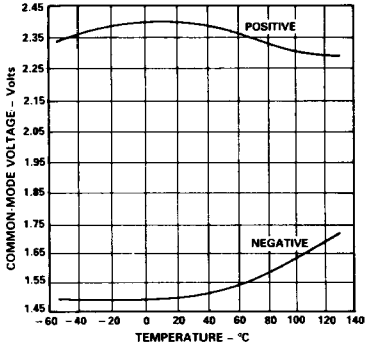



*Figure 4. Comparator Common-Mode Voltage vs. Temperature*

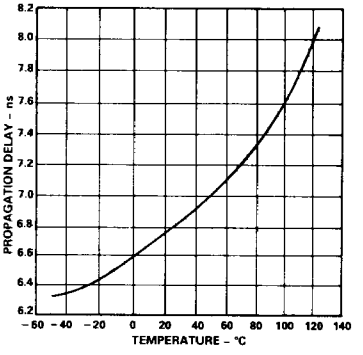



*Figure 5. Propagation Delay vs. Temperature*

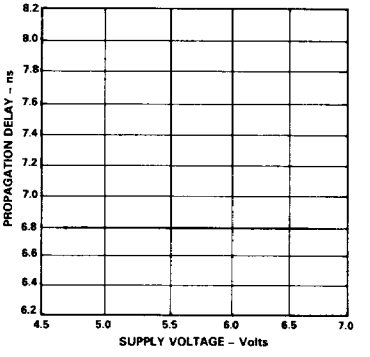



*Figure 6. Propagation Delay vs. Power Supply Voltage*

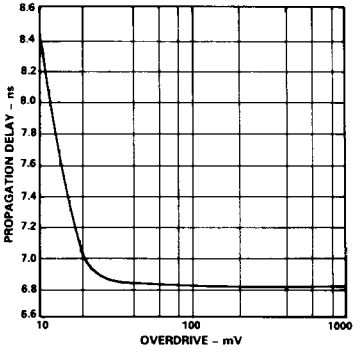



*Figure 7. Propagation Delay vs. Overdrive*

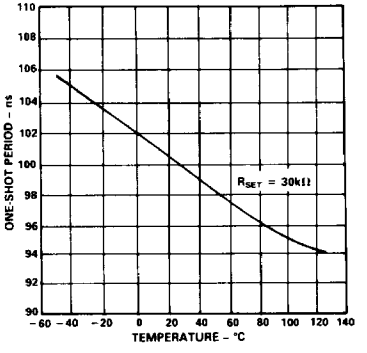



*Figure 8. One-Shot Period vs. Temperature*

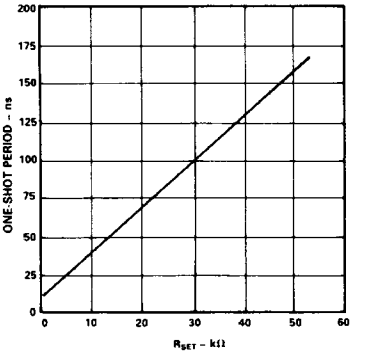



*Figure 9. One-Shot Period vs. $R_{SET}$*

## THEORY OF OPERATION

The AD891 consists of three comparators, two D-type flip-flops, an internal bandgap reference and a pair of externally adjustable one-shots. Two comparators are used to provide data amplitude qualification, and the third acts as a zero-crossing detector when used with an external passive differentiator circuit. (Refer to the AD891 block diagram and Figure 11.)

Figure 10 illustrates the operation of the AD891, using the recommended passive delay-line differentiator described in the following section. Sequence "A" represents the pattern written on the disk where a logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the AD891 consists of a sequence of alternating pulses "B." The data pattern shown is worst case for a 1-7 code input. "C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in state of this output are used to clock the two internal D-type flip-flops. The flip-flops are enabled using the output "E" from the positive and negative threshold comparators, such that the flip-flop outputs change state only when the analog input exceeds the programmed threshold levels (positive or negative). When the threshold levels are exceeded and a zero-crossing event occurs, the flip-flops change state, producing an output pulse "F." The duration of this pulse, seen at the Data+/Data− outputs, is set using an external resistor, as is the internal time-out which is used to prevent noise induced retriggering. The final output data sequence is shown in "G." As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a time-shifted version of the write data.

Since the 1-7 code input is the most demanding of the popular encoding schemes to qualify, the AD891 is clearly suitable for other codes, such as MFM and 2-7. The recommended time domain filter one-shot period for MFM and 1-7 code is equal to 75% of the bit cell clock period. For 2-7 code the one-shot period can be increased to 150% of the bit cell clock period.

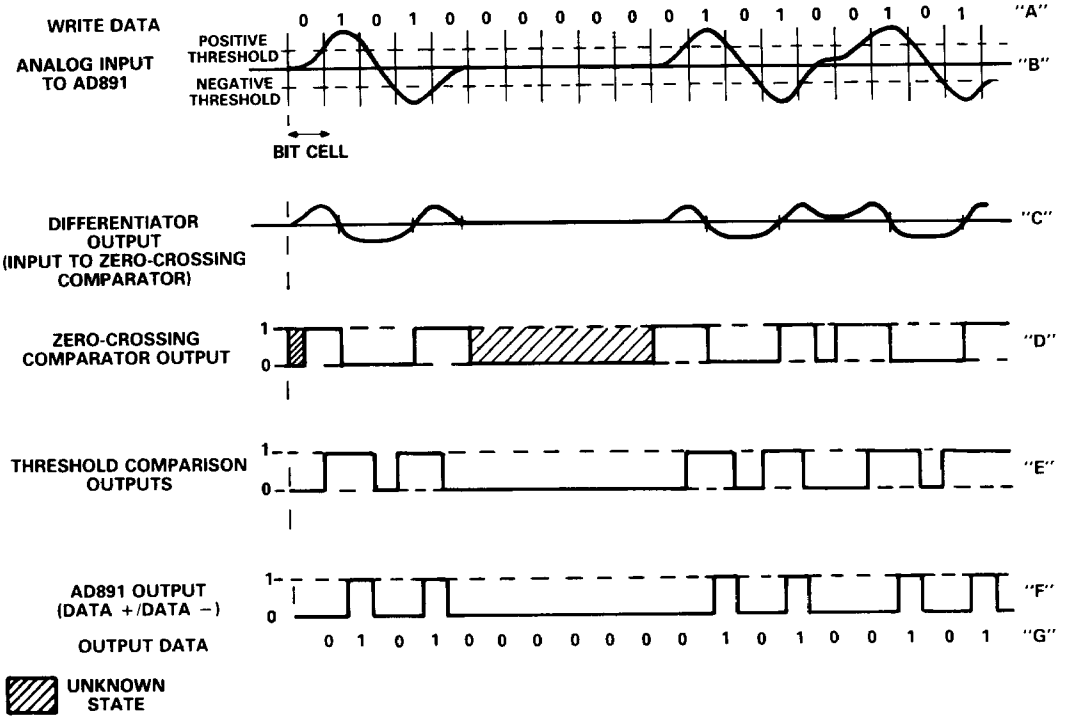



*Figure 10. AD891 Operation for Worst Case 1-7 Code Pattern*

## DESIGN CONSIDERATIONS

In designing a suitable passive delay-line differentiator, either the fully differential (Figure 11a) or single-ended (Figure 11b) configuration can be used. The equations governing component selection for both connections are as shown.

If the single-ended configuration is employed, then the inputs to the negative half-cycle comparator need to be biased such that the comparator is turned off. This can be accomplished by placing the "Amp−" input at a potential at least 100 mV more negative than the "Level In−" input. The "Amp−" pin may be connected to the "$V_{EE}$" pin and the "Level In−" pin may be connected to the "Digital GND" pin, provided that the potential difference does not exceed 5.6 volts, which is the absolute maximum differential input rating of the device.

Good RF layout practice should be obeyed, with decoupling networks of 0.1 μF in parallel with 0.01 μF at both the "$V_{CC}$" and "$V_{EE}$" pins. A ground plane should be used extensively. Two digital grounds are supplied: Pin 12 is for the internal logic while Pin 5 is provided for the cerdip package; the corresponding PLCC package pins are 17 and 9, respectively.) The filter time and output pulse setting resistors should be tied, as directly as possible, to the "Digital GND" pin.

The "Data−" and "Data+" pins require pull-down resistors to "$V_{EE}$" as per normal practice in ECL. The use of 30 kΩ resistors connected between the "Filter Time Set" and "Output Pulse Set" pins and digital ground will produce a nominal 100 ns one-shot period; 10 kΩ resistors will nominally produce 38 ns one-shot periods. The timing of the two one-shots may be set independently.

For best performance, the three input comparators should be operated at a common-mode potential close to digital ground. The digital ground should be connected to the analog ground as near to the power supply as possible to minimize noise injection.

## INTEGRATING WITH THE AD890 WIDEBAND CHANNEL PROCESSING ELEMENT

Figure 12 shows a typical application using the AD891 and AD890 connected together to create a 30 MHz channel (cerdip connections shown). This circuit includes a 5-pole 30 MHz Gaussian-to-6 dB transitional filter plus a second-order RLC time domain equalizer. The fully differential passive delay-line differentiator previously discussed is also included. The analog and digital grounds should be connected only to the power supply common.

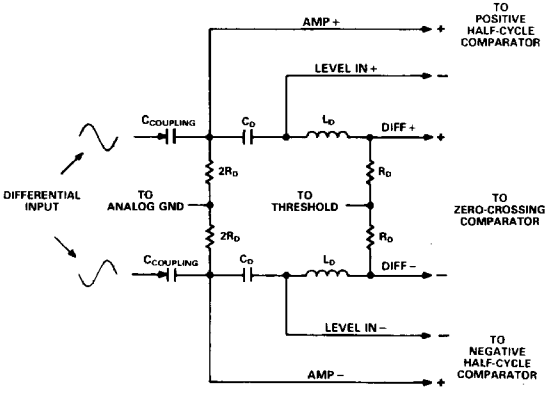



*Figure 11a. Fully Differential Configuration of Passive Delay-Line Differentiator*

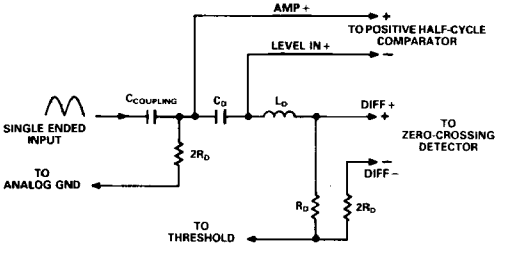



*Figure 11b. Single-Ended Configuration of Passive Delay-Line Differentiator*

## RECOMMENDED COMPONENTS

$$f_D = \frac{1}{2\pi\sqrt{L_D C_D}}$$

f = 1.5 Times the Maximum Desired Differentiated Frequency

$$R_D = K\left[\sqrt{\frac{L_D}{C_D}}\right]$$

$R_D$ Minimum Value: 120 Ω
150 Ω or Greater Is Recommended

1.3 (Best Magnitude Response) ≤K ≤1.7 (Best Group Delay Response)

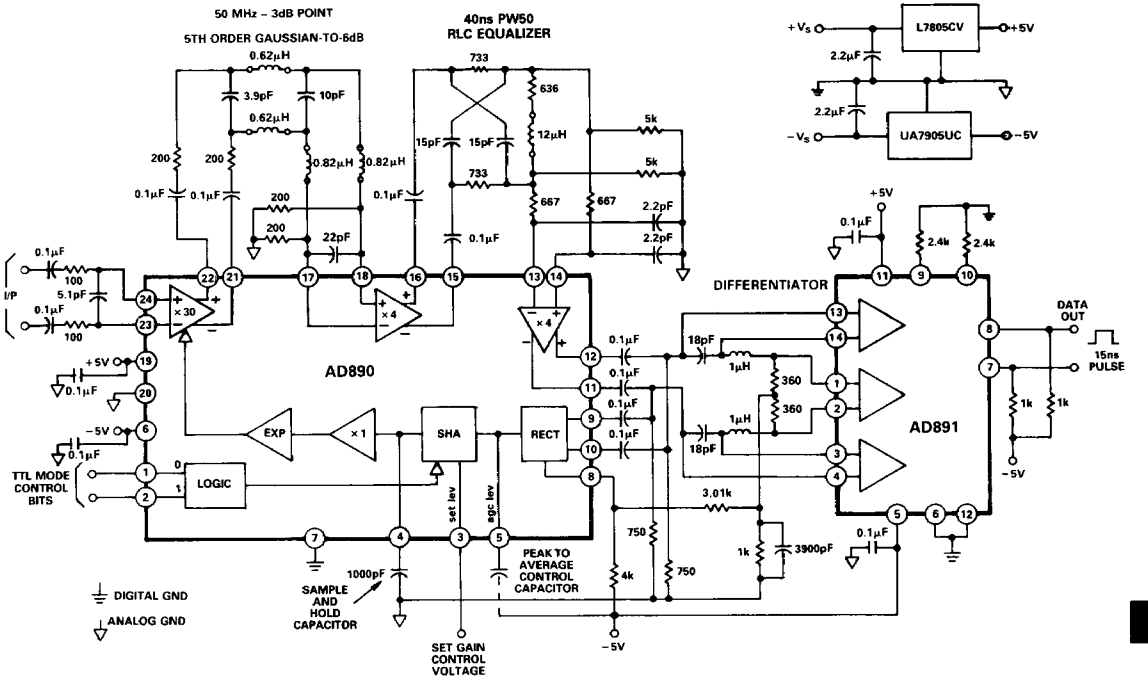



*Figure 12. Typical AD890/AD891 Connection for a 30 MHz Channel*

## OPERATION WITH +5 V, +12 V SUPPLIES

Operation with +5 V (±0.5 V) and +12 V (±0.6 V) supplies is readily achieved. The digital ground pins must be connected to the +5 V line or to an available center tap of the +12 V supply. The specified output ECL logic levels are therefore referred to the +5 V supply. Pull-down resistors for the "Data+" and "Data−" pins should be connected to $V_{EE}$. Thus connected, a current of approximately 23 mA will flow in the +5 V supply under normal operation.

In order to ensure correct comparator operation, a pair of 100 mA diodes should be added in series with the +12 V supply which is connected to the $V_{CC}$ terminal. This connection is shown in Figure 13 (shown for cerdip package).

Both the +5 V and +12 V supplies should be RF bypassed to ground; the values of 0.1 μF and 0.01 μF in parallel are recommended. In addition, some higher value of decoupling capacitance – such as 3.3 μF – may be desirable. This decoupling should be applied directly at the AD891 "$V_{CC}$" and "Digital GND" pins. Finally, the common-mode range for the comparators is now referred to the +5 V supply line, and care must be taken to operate within the common-mode limits.

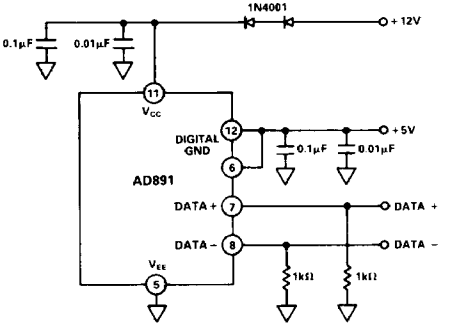



*Figure 13. AD891 Connection for +5 V, +12 V Operation*

## RESPONSE CHARACTERISTICS OF THE FULLY DIFFERENTIAL DELAY-LINE DIFFERENTIATOR

Figures 14 through 17 show typical performance to be expected from the recommended passive, fully differential, delay-line differentiator previously discussed. Figures 14 and 15 depict magnitude and phase response for the undifferentiated output, respectively. Figure 16 shows magnitude response for the differentiated output, and Figure 17 shows phase error between the two outputs.

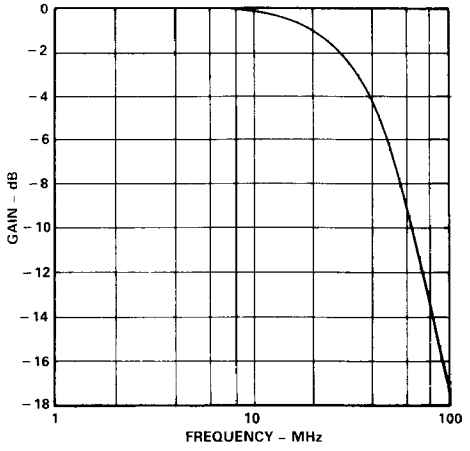



*Figure 14. Magnitude Response of Undifferentiated Output*

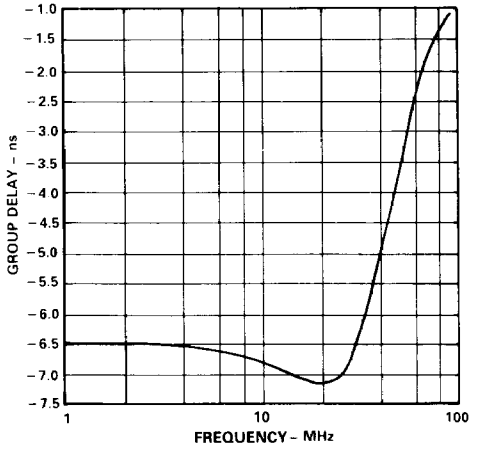



*Figure 15. Group Delay Characteristics of Undifferentiated Output*

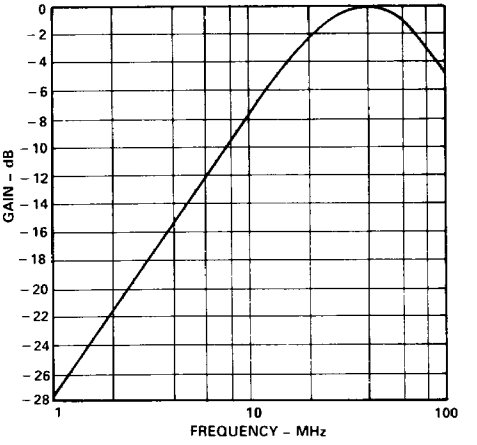



*Figure 16. Magnitude Response of Differentiated Output*

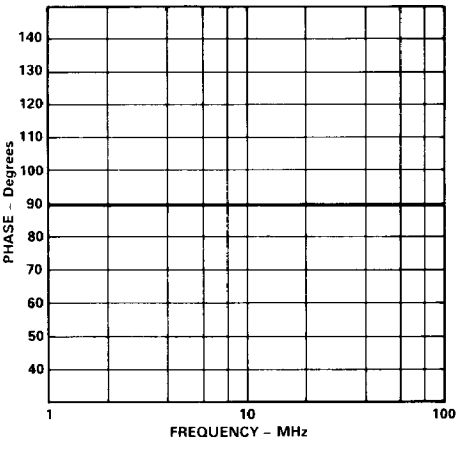



*Figure 17. Relative Phase Between Differentiated and Undifferentiated Outputs*