

### FEATURES

- 4 Matched Transimpedance Amplifiers
- 40 MHz Bandwidth
- Selectable 40 kΩ/120 kΩ Transimpedance
- Continuous or Sampled Servo Capability
- Outputs:
  - Quad Sum
  - Track
  - Normalized Track
  - Focus
  - Normalized Focus
- 10 MHz Normalization Dividers
- 10 ns Write Recovery with Sampling
- Low Output Noise

### PRODUCT DESCRIPTION

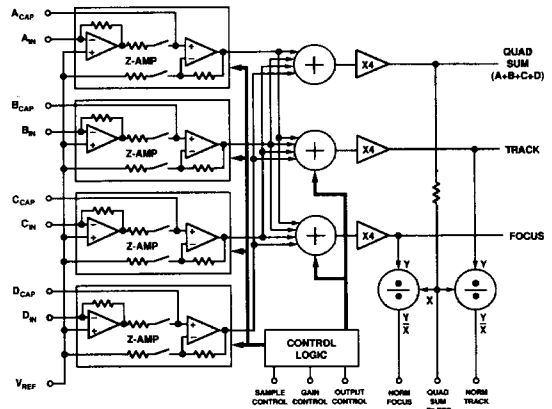
The AD880 is a monolithic integrated circuit intended for applications in the servo/read systems of an optical disk drive product.

The AD880 consists of four matched transimpedance amplifiers (A, B, C, D) with selectable 40 kΩ or 120 kΩ transimpedance. The basic transimpedance stage consists of a 10 kΩ transimpedance front end that drives a programmable ×1 or ×3 buffer. Each stage has been configured to minimize noise and noise peaking. To further enhance overall signal to noise performance, an external capacitor may be added between the transimpedance amplifier and the programmable buffer to implement a first order low-pass filter.

The AD880 is stable over the full range of input source capacitances. To ensure stability and maximize available bandwidth in both transimpedance modes, the internal compensation capacitor in the programmable buffer is appropriately modified for each mode.

Fast read after write recovery is implemented through the transimpedance sample function. Use of the sample function allows for a read-after-write recovery in approximately 10 ns. The "sample capacitor" also serves the dual purpose of providing the low-pass filter.

AD880 FUNCTIONAL BLOCK DIAGRAM



In addition, the part contains three offset trimmed summing amplifiers with 40 MHz bandwidth. One amplifier provides the quad sum output. This output can be low pass filtered prior to driving the normalization dividers. Two other summing amplifiers generate the track and focus outputs.

- Quad Sum :  $(A+B+C+D)$
- Track :  $(A+D) - (B+C)$  or  $(A-B)$
- Focus :  $(A+C) - (B+D)$  or  $(C-D)$

The selectable outputs are programmed through a CMOS compatible control line.

Finally, a pair of two quadrant dividers are provided. These generate the normalized focus and track signals with an accuracy of 10%, and have bandwidths in excess of 10 MHz.

The AD880 is available in a 20-pin SOIC package and is specified to operate over the 0 to +70°C commercial temperature range.

# SPECIFICATIONS (@ + 25°C and +12 V dc, unless otherwise noted)

Parameter	Conditions	AD880J			Units	
		Min	Typ	Max		
<b>TRANSIMPEDANCE AMPLIFIER</b>						
Transimpedance	Channel to Channel @ 30 MHz Input Signal $AV_0$		10		k $\Omega$	
Transimpedance Matching				$\pm 1$	%	
Channel to Channel Crosstalk				-40	dB	
Open-Loop Gain			20		V/V	
Open-Loop Bandwidth			40		MHz	
Input Capacitance			2		pF	
Input Offset Current			TBD		nA	
Input Offset Voltage			TBD		mV	
Input Current Noise			1		pA/ $\sqrt{\text{Hz}}$	
Input Voltage Noise			1.5		nV/ $\sqrt{\text{Hz}}$	
Feedback Resistor Noise			13		nV/ $\sqrt{\text{Hz}}$	
Output Impedance		@ Filter Capacitor Pin (Active)	1		k $\Omega$	
Output Impedance		@ Filter Capacitor Pin (Sampled)	250		M $\Omega$	
Max Output Voltage Swing			$\pm 0.7$		V	
Max Output Current			TBD		mA	
$V_{\text{REF}}$ Range		+4.5		V		
$V_{\text{REF}}$ Input Current		-5		5	mA	
<b>PROGRAMMABLE BUFFER</b>						
Gain	Gain Control = 0		10		dB	
Gain Matching	Gain Control = 0, Channel to Channel		TBD		dB	
3 dB Bandwidth	Gain Control = 0		40		MHz	
Gain	Gain Control = 1		0		dB	
Gain Matching	Gain Control = 1, Channel to Channel		TBD		dB	
3 dB Bandwidth	Gain Control = 1		60		MHz	
Input Bias Current				0.1	pA	
Input Offset Voltage			TBD		$\mu$ V	
Input Current Noise			1		pA/ $\sqrt{\text{Hz}}$	
Input Voltage Noise			13		nV/ $\sqrt{\text{Hz}}$	
Max Output Voltage Swing	Relative to $V_{\text{REF}}$	$\pm 1$			V	
<b>SUMMING AMPLIFIER</b>						
Gain	Input to Input		12		dB	
Gain Matching				TBD		%
3 dB Bandwidth	Relative to $V_{\text{REF}}$		40		MHz	
Output DC Voltage			0		V	
Output Voltage Offset				TBD		V
Output Impedance	Relative to $V_{\text{REF}}$		TBD		$\Omega$	
Max Output Voltage			$\pm 2.5$		V	
Max Output Current			20		mA	
<b>NORMALIZATION DIVIDERS</b>						
Division Error	$0.5 \leq Y \leq X \leq 1.5$			$\pm 10$	%	
3 dB Bandwidth			10		MHz	
Output Voltage Range		Relative to $V_{\text{REF}}$		2		V
Output Current		Division Ratio = 1		200		$\mu$ A
<b>QUAD SUM FILTER</b>						
Resistance	Quad Sum to Quad Sum Filter	8	10	12	k $\Omega$	
<b>MODE CONTROL SECTION</b>						
$V_{\text{IH}}$	(CMOS Compatible)	4.0		$V_{\text{CC}}$	V	
$V_{\text{IL}}$		0		1	V	
$I_{\text{IH}}$				0.1	pA	
$I_{\text{IL}}$				0.1	pA	
Mode Switching Times		Gain Control		10		ns
		Output Mode		10		ns
	Sample Mode		10		ns	

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Conditions	AD880J			Units
		Min	Typ	Max	
<b>POWER SUPPLY REQUIREMENTS</b>					
Supply Voltage $V_{CC}$	$T_{min}$ to $T_{max}$	10.8	12	13.2	V
Supply Voltage $V_{EE}$			0		V
Quiescent Current $I_{CC}$		50	60	70	mA
<b>ABSOLUTE MAXIMUM RATINGS<sup>1</sup></b>					
Supply Voltage $V_{CC}$	Soldering 60 Sec			14.5	V
$V_{REF}$ Input Voltage		-0.8		7.0	V
Storage Temperature Range		-65		130	°C
Operating Temperature Range <sup>2</sup>		0		70	°C
Lead Temperature Range				+300	°C

NOTES

<sup>1</sup>Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.

<sup>2</sup>20-pin wide body SO package:  $\theta_{JA} = +65^{\circ}\text{C}/\text{watt}$ .

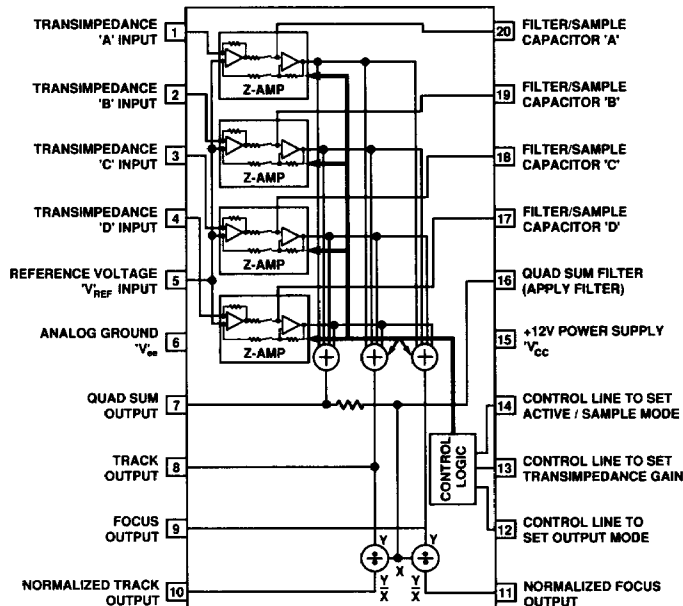
Specifications subject to change without notice.

Logic Assignments	Sample Control	Gain Control	Output Control	Logic Assignments	Sample Control	Gain Control	Output Control
Transimpedance Amplifiers Active	0	X	X	Track Output = (A+D) - (B+C)			
Transimpedance Amplifiers Sampled	X	X	X	and Focus Output = (A+C) - (B+D)	X	X	0
Select 120 k $\Omega$ Transimpedance	X	0	X	Track Output = (A-B)			
Select 40 k $\Omega$ Transimpedance	X	X	X	and Focus Output = (C-D)	X	X	1

X = Do Not Care.

Table 1. AD880 Logic Assignments

PIN ASSIGNMENTS



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

## THEORY OF OPERATION

### Transimpedance Stage

The transimpedance stage is configured as a fixed 10 k $\Omega$  transimpedance amplifier followed by a programmable buffer (Figure 1). The source capacitance  $C_S$  coupled with the transimpedance feedback resistor,  $R_F = 10$  k $\Omega$ , determines the bandwidth of the transimpedance amplifier.

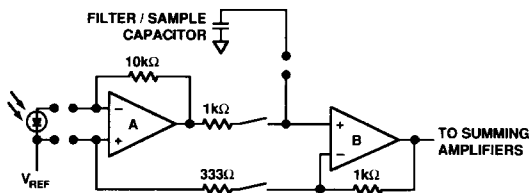


Figure 1.

To optimize the signal to noise performance the input amplifier uses a bipolar input stage. This allows for a significantly lower input voltage noise figure at the expense of input bias and noise current. To compensate for the output offset voltage created by the input bias current, the programmable buffer mirrors and cancels the offset voltage created in the transimpedance cell. The overall output voltage offset through the complete transimpedance stage is less than 5 mV.

By keeping the transimpedance of the first stage relatively low, 10 k $\Omega$ , and limiting the open-loop gain of amplifier "A" to 20, noise peaking is limited. To further limit noise and noise peaking, the output of the first stage may be low pass filtered by applying a capacitor, see Figure 1, at the appropriate pins (Pins 17, 18, 19 and 20). The capacitor forms a first order low-pass filter with a cut-off frequency  $f = 1/(2\pi \cdot 1000 \cdot C_{FILTER})$ . The complete noise model for the front-end transimpedance stage is shown in Figure 2.

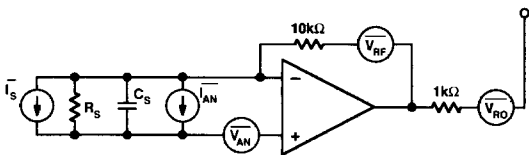


Figure 2.

To ensure stability of the complete transimpedance stage over the full range of source capacitances, the programmable buffer is internally compensated. To maintain the stability and maximize available bandwidth, the compensation capacitor is internally modified for each transimpedance mode. Also, depending upon the buffer gain of  $\times 1$  or  $\times 3$ , programmable through the "Gain Control" line (Pin 13), the input noise is amplified by a factor of 1 or 3, respectively.

Logic Assignments	Gain Control
Select 120 k $\Omega$ Transimpedance	0
Select 40 k $\Omega$ Transimpedance	1

To improve read-after-write recovery the AD880 offers an input sample function, programmable through the "Sample Control" line (Pin 14).

Logic Assignments	Sample Control
Transimpedance Amplifier Active	0
Transimpedance Amplifier Sampled	1

The sample capacitor also serves as the low-pass filter for the transimpedance stage. The FET input on the programmable buffer ensures an excellent droop-rate in the sample mode.

### Summing Amplifiers

The summing amplifiers provide the Quad Sum, Focus and Track outputs with a gain of X4. The X4 amplification through the summers provide the final gain for achieving a 40 k $\Omega$  or 120 k $\Omega$  overall transimpedance.

The output of both the Focus and Track summing amplifiers are programmable through the CMOS compatible "Output Control" line (Pin 12).

Logic Assignments	Output Control
Track Output = (A+D) - (B+C) and Focus Output = (A+C) - (B+D)	0
Track Output = (A - B) and Focus Output = (C - D)	1

### Normalization Dividers

The normalization dividers provide current output of the Normalized Focus and Track signals. A low-pass filter capability is provided at the "Quad Sum Filter" pin (Pin 16). The Quad Sum Filter Resistance is 10 k $\Omega$ , and thereby offers the user the capability to implement a RC filter prior to the applying the Quad Sum signal to the normalization dividers.

### General Layout Requirements

Care must be taken to ensure good  $R_F$  practice in the PC layout to avoid oscillations. A parallel combination of 0.1  $\mu$ F and 0.01  $\mu$ F ceramic capacitors should be used as close to the  $V_{CC}$  (Pin 6) and  $V_{REF}$  (Pin 5) pins as possible. Also, a current path to  $V_{REFERENCE}$  must be provided for the outputs of the normalization dividers.

## ORDERING GUIDE

Model	Description	Package Option*
AD880JR	20-Pin Small Outline	R-20

\*See Section 20 for package outline information.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.