WM8750-EV1M

Evaluation Board User Handbook

Rev 2.0

TABLE OF CONTENTS

INTRODUCTION

The WM8750 is a stereo CODEC for portable audio applications.

This evaluation platform and documentation should be used in conjunction with the latest version of the WM8750 datasheet. The datasheet gives device functionality information as well as timing and data format requirements.

This evaluation platform has been designed to allow the user ease of use and give optimum performance in device measurement as well as providing the user with the ability to listen to the excellent audio quality offered by the WM8750.

GETTING STARTED

EVALUATION BOARD CHECKLIST

The following items are available from Wolfson:

- WM8750-EV1B Evaluation Board - 6097_QFN32_EV1_REV1
- WM8750-EV1S Control Software (download from http://www.wolfsonmicro.com)
- WM8750-EV1M User Handbook (download from http://www.wolfsonmicro.com)

CUSTOMER REQUIREMENTS

Minimum customer requirements are:

- D.C. Power supply of +5V
- D.C. Power supply of +1.8V to +3.6V
- PC and printer cable (for software control)

Minimum PC spec requirements are:

- Win95/98/NT/2000/XP
- 486 Processor
- Approximately 1.5Mb of free hard disk space

DAC Signal Path Requires:

- Digital coaxial or optical data source
- One set of active stereo speakers

ADC Signal Path Requires:

- Analogue coaxial or 3.5mm jack plug signal source
- Digital coaxial or optical data receiving unit

Analogue Signal Path Requires:

- Analogue coaxial or 3.5mm jack plug signal source
- One set of active stereo speakers

POWER SUPPLIES

Using appropriate power leads with 4mm connectors, power supplies should be connected as described in Table 1.

REF-DES	SOCKET NAME	SUPPLY
J8	+5V	+5V
J2	DBVDD	+1.8V to +3.6V
J4	AVDD	+1.8V to +3.6V
J10	DCVDD	+1.42V to +3.6V
J47	HPVDD	+1.8V to +3.6V
J1	DGND	0V
J5	AGND	0V

Table 1 Power Supply Connections

The DGND and AGND connections may be connected to a common GND on the supply with no reduction in performance.

To reduce the supply connections that need to be attached to the EVB, sites L1 and L8 are populated with 0R resistors shorting AVDD, HPVDD and DBVDD. In this configuration it is recommended that the supply only be attached to AVDD. If separate supplies are required the 0R resistors should be removed from sites L1 and L8.

Note: Refer to WM8750 datasheet for limitations on individual supply voltages.

Important: Exceeding the recommended maximum voltage can damage EVB components. Under voltage may cause improper operation of some or all of the EVB components.

BOARD FUNCTIONALITY

There are three options for inputting digital data into the WM8750 evaluation board. There is a coaxial input (J19) via a standard phono connector or an optical input (U3) via a standard optical receiver module. A direct digital input is also available via one side of a 2x8 pin header (H1).

The analogue input signals are applied to the evaluation board via phono connectors J7 (RLINE_IN1), J12 (LLINE_IN1), J14 (RLINE_IN2), J22 (LLINE_IN2), J26 (RLINE_IN3) and J45 (LLINE_IN3). Analogue inputs can also be applied to the evaluation board via 3.5mm jack sockets J9 (MIC_IN1); J16 (MIC_IN2) and J30 (MIC_IN3).

There are two options for outputting digital data from the WM8750 evaluation board. There is a coaxial output (J29) via a standard phono connector. The digital signals may also be accessed via one side of a 2x8 pin header (H2).

The analogue outputs of the board are via phono connectors J43 (ROUT1), J44 (LOUT1), J41 (LOUT2), J42 (ROUT2), J39 (MONO OUT) and J40 (OUT3). There is also an analogue output via a 3.5mm jack socket J46 (HP_OUT).

All WM8750 device pins are accessible for easy measurement via the 2x4 pin headers (J13, J15, J17 and J21) running up each side of the device.

Level-shift IC (U4) is used to shift the fixed +5V digital input from the CS8427 (U5) down to the same level as DBVDD and vice-versa.

BOARD INPUT

REF-DES	SOCKET NAME	SIGNAL
J19	SPDIF_IN	Digital (AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201) signal.
U3	OPTICAL_IN	Digital (AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201) optical signal.

Table 2 Digital Inputs

REF-DES	SOCKET NAME	SIGNAL
J7	RLINE_IN1	Analogue signal
J12	LLINE_IN1	Analogue signal
J14	RLINE_IN2	Analogue signal
J22	LLINE_IN2	Analogue signal
J26	RLINE_IN3	Analogue signal
J45	LLINE_IN3	Analogue signal
J9	MIC_IN1	Analogue signal (MIC Input)
J16	MIC_IN2	Analogue signal (MIC Input)
J30	MIC_IN3	Analogue signal (MIC Input)
Analogue signals applied to these connectors are AC coupled before being input to the WM8750.		

Table 3 Analogue Inputs

Note: When used in Master Mode, an SPDIF signal must still be applied to phono connector J19. This input signal is used to allow correct operation of the CS8427 as well as being used to generate the MCLK for the WM8750.

BOARD OUTPUT

REF-DES	SOCKET NAME	SIGNAL
J29	SPDIF_OUT	Digital (AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201) signal.

Table 4 Digital Output

REF-DES	SOCKET NAME	SIGNAL
J43	ROUT1	Line/Headphone Output
J44	LOUT1	Line/Headphone Output
J42	ROUT2	Speaker Output
J41	LOUT2	Speaker Output
J39	MONO OUT	Mono Output
J40	OUT3	ROUT1/VREF/MONO OUT
J46	HP_OUT	Headphone Output

Table 5 Analogue Outputs

INTERFACES

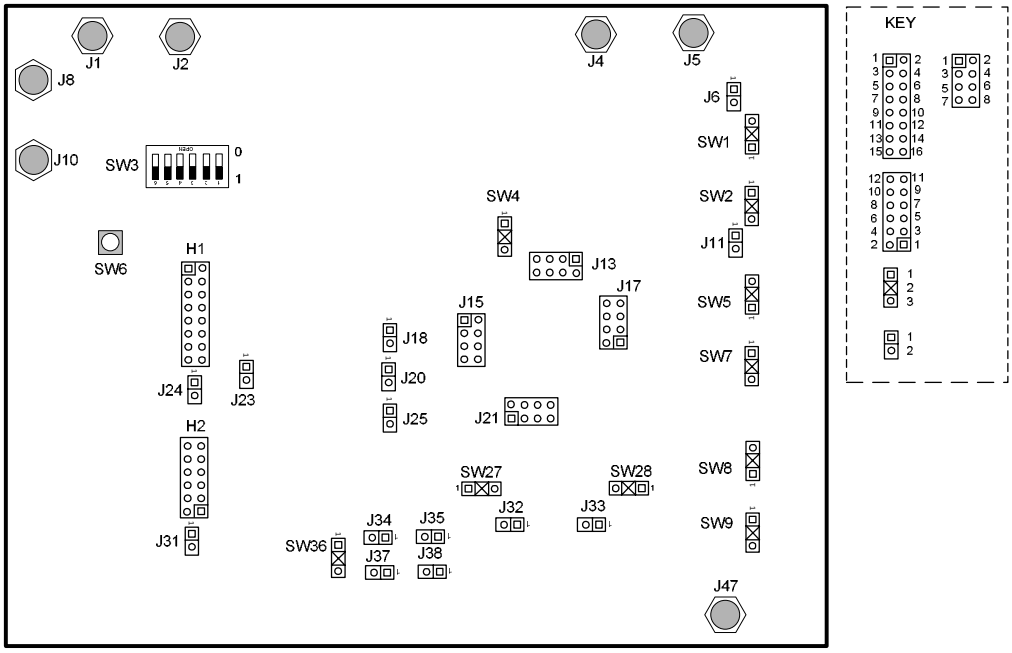

Figure 1 Interfaces

HEADERS

H1	SIGNAL
1/2	MCLK
3/4	GND
5/6	DACDAT
7/8	GND
9/10	DACLRC
11/12	GND
13/14	BCLK
15/16	GND

J24	SIGNAL
1	ADCLRC_IN
2	GND

H2	SIGNAL
12/11	GND
10/9	ADCDAT
8/7	GND
6/5	ADCLRC
4/3	GND
2/1	BCLK

J31	SIGNAL
1	DACLRC_OUT
2	GND

J15	WM8750	PIN NAME
1	1	MCLK
2	2	DCVDD
3	3	DBVDD
4	4	DGND
5	5	BCLK
6	6	DACDAT
7	7	DACLRC
8	8	ADCDAT

J17	WM8750	PIN NAME
1	17	HPVDD
2	18	AVDD
3	19	AGND
4	20	VREF
5	21	VMID
6	22	MICBIAS
7	23	RINPUT3/HPDETECT
8	24	LINPUT3

J21	WM8750	PIN NAME
1	9	ADCLRC
2	10	MONOOUT
3	11	OUT3
4	12	ROUT1
5	13	LOUT1
6	14	HPGND
7	15	ROUT2
8	16	LOUT2

J13	WM8750	PIN NAME
1	25	RINPUT2
2	26	LINPUT2
3	27	RINPUT1
4	28	LINPUT1
5	29	MODE
6	30	CSB
7	31	SDIN
8	32	SCLK

Table 6 Headers

LINKS, JUMPERS AND SWITCHES

LINKS AND JUMPERS	LINK/JUMPER STATUS	DESCRIPTION
J18 (BCLK)	OPEN SHORT	Master mode Slave mode [default setting]
J20 (ADCLRC)	OPEN SHORT	Master mode Slave mode [default setting]
J25 (DACLRC)	OPEN SHORT	Master mode Slave mode [default setting]
J23	OPEN SHORT	Master mode Slave mode (Ties ADCLRC to DACLRC) [default setting]
J32, J33, J34 and J35	OPEN SHORT	OUT signals are AC coupled [default setting] OUT signals are not AC coupled
J37 (external speaker connection)		Pin 1 – AGND Pin 2 – +ve speaker connection
J38 (external speaker connection)		Pin 1 – AGND Pin 2 – -ve speaker connection
J6 (DC input connection)		Pin 1 – DC signal input Pin 2 – AGND
J11 (DC input connection)		Pin 1 – DC signal input Pin 2 – AGND

Table 7 Links

SWITCHES	SWITCH STATUS	DESCRIPTION
SW6		After an input data format change has been made using SW3, the CS8427 will only latch the new settings after SW6 has been pressed and released.
SW3 (DATA FORMAT)		1 2 3 4 5 6 DATA FORMAT 1 0 0 1 0 0 I2S Compatible [default setting] 1 0 0 0 0 1 24-bit Right Justified 1 0 0 0 0 0 Left Justified
SW4 (Software Control)	Pins 1 and 2 SHORT Pins 2 and 3 SHORT	3-wire (SPI) Control Mode [default setting] 2-wire Control Mode
SW1, SW2 (R/Line Input 1 Select)	Pins 1 and 2 SHORT Pins 2 and 3 SHORT	MIC Input Select (3.5mm Jack Socket) Line Input Select (Phono Socket) [default setting]
SW5, SW7 (R/Line Input 2 Select)	Pins 1 and 2 SHORT Pins 2 and 3 SHORT	MIC Input Select (3.5mm Jack Socket) Line Input Select (Phono Socket) [default setting]
SW8, SW9 (R/Line Input 3 Select)	Pins 1 and 2 SHORT Pins 2 and 3 SHORT	MIC Input Select (3.5mm Jack Socket) Line Input Select (Phono Socket) [default setting]
SW27, SW28 (R/LOUT 1 Select)	Pins 1 and 2 SHORT Pins 2 and 3 SHORT	HP Output Select (3.5mm Jack Socket) Line Output Select (Phono Socket) [default setting]
SW36	Pins 1 and 2 SHORT Pins 2 and 3 SHORT	Connects to OUT3 for HP output DC reference Connects to GND for HP output reference [default setting]

Table 8 Switches

WM8750 OPERATION

SOFTWARE CONTROL

There are two possible serial software control modes that may be selected to operate the WM8750. The standard SPI user interface is a 3-wire solution with the second option being a 2-wire solution.

3-WIRE MODE

To operate the WM8750 in SPI (3-wire) mode, jumper switch SW4 must be set so that pins 1 and 2 are SHORT. The 3-wire serial interface then becomes active on pins 30(CSB), 31(SDIN) and 32(SCLK). The serial interface on the board can be connected to a PC via the printer port or any other standard parallel port. The port used can be selected through the software provided. The software supplied with this kit gives the user access to all the possible features provided by the WM8750. The 3-wire latch, data and clock lines may also be connected to the board via the test points TP2 (CSB), TP4 (SDIN) and TP3 (SCLK).

Please refer to the WM8750 datasheet for full details of the serial interface timing and all register features.

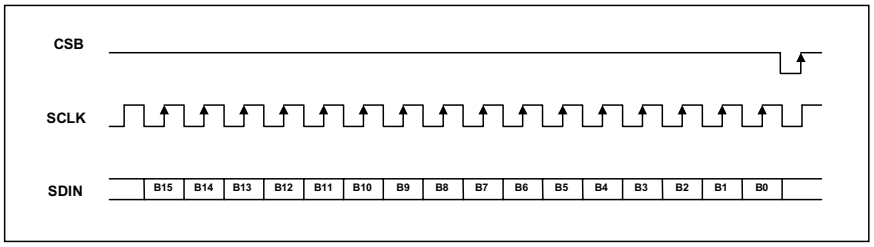

Figure 2 3-Wire Serial Interface

2-WIRE MODE

To operate the WM8750 in 2-wire mode, jumper switch SW4 must be set so that pins 2 and 3 are SHORT. The 2-wire serial interface becomes active on pins 31(SDIN) and 32(SCLK). The serial interface on the board can be connected to a PC via the printer port or any other standard parallel port. **Note: a bi-directional parallel port is required for 2-wire operation[1].** The 2-wire data and clock lines may also be connected to the board via the test points TP4 (SDIN) and TP3 (SCLK).

When used in 2-wire mode, the WM8750 has two possible addresses (0011010 [0x34h] or 0011011 [0x36h]) that are selectable by pulling CSB low or high. If connecting a probe to the Test Points it must be noted that the CSB line is pulled high on the WM8750 evaluation board selecting address 0011011. CSB must be pulled low or driven low through the software writes if address 0011010 is used (as is done in the WM8750-EV1S software provided).

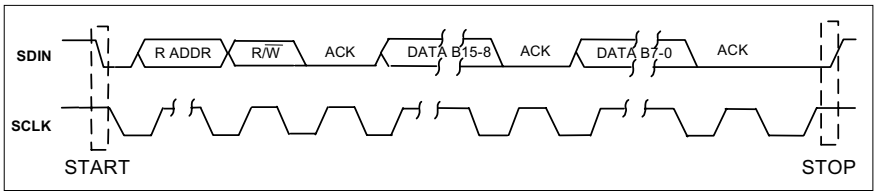

Figure 3 2-Wire Serial Interface

Note: [1]If the 2-wire mode does not operate as expected, the likely cause is the configuration of the parallel port interface mode. Check that the port is configured for bi-directional communication. Most PCs allow the parallel port to be configured in the BIOS settings during initial PC power up.

REGISTER	ADDRESS (Bit 15 – 9)	remarks	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	default
R0 (00h)	0000000	Left Input volume	LIVU	LINMUTE	LIZC	LINVOL						010010111
R1 (01h)	0000001	Right Input volume	RIVU	RINMUTE	RIZC	RINVOL						010010111
R2 (02h)	0000010	LOUT1 volume	LO1VU	LO1ZC	LOUT1VOL[6:0]							001111001
R3 (03h)	0000011	ROUT1 volume	RO1VU	RO1ZC	ROUT1VOL[6:0]							001111001
R4 (04h)	0000100	Reserved	0	0	0	0	0	0	0	0	0	000000000
R5 (05h)	0000101	ADC & DAC Control	ADCDIV2	DACDIV2	ADCPOL[1:0]		HPOR	DACMU	DEEMPH[1:0]		ADCHPD	000001000
R6 (06h)	0000110	Reserved	0	0	0	0	0	0	0	0	0	000000000
R7 (07h)	0000111	Audio Interface	0	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]		000001010
R8 (08h)	0001000	Sample rate	BCM[1:0]		CLKDIV2	SR[4:0]					USB	000000000
R9 (09h)	0001001	Reserved	0	0	0	0	0	0	0	0	0	000000000
R10 (0Ah)	0001010	Left DAC volume	LDVU	LDACVOL[7:0]								011111111
R11 (0Bh)	0001011	Right DAC volume	RDVU	RDACVOL[7:0]								011111111
R12 (0Ch)	0001100	Bass control	0	BB	BC	0	0	BASS[3:0]				000001111
R13 (0Dh)	0001101	Treble control	0	0	TC	0	0	TRBL[3:0]				000001111
R15 (0Fh)	0001111	Reset	writing to this register resets all registers to their default state									not reset
R16 (10h)	0010000	3D control	0	MODE3D	3DUC	3DLC	3DDEPTH[3:0]				3DEN	000000000
R17 (11h)	0010001	ALC1	ALCSEL[1:0]		MAXGAIN[2:0]			ALCL[3:0]				001111011
R18 (12h)	0010010	ALC2	0	ALCZC	0	0	0	HLD[3:0]				000000000
R19 (13h)	0010011	ALC3	0	DCY[3:0]				ATK[3:0]				000110010
R20 (14h)	0010100	Noise Gate	0	NGTH[4:0]					NGG[1:0]		NGAT	000000000
R21 (15h)	0010101	Left ADC volume	LAVU	LADCVOL[7:0]								011000011
R22 (16h)	0010110	Right ADC volume	RAVU	RADCVOL[7:0]								011000011
R23 (17h)	0010111	Additional control(1)	TSDEN	VSEL[1:0]		DMONOMIX[1:0]		DATSEL[1:0]		DACINV	TOEN	011000000
R24 (18h)	0011000	Additional control(2)	OUT3SW[1:0]		HPSWEN	HPSWPOL	ROUT2INV	TRI	LRCM	ADCOSR	DACOSR	000000000
R25 (19h)	0011001	Pwr Mgmt (1)	VMIDSEL[1:0]		VREF	AINL	AINR	ADCL	ADCR	MICB	DIGENB	000000000
R26 (1Ah)	0011010	Pwr Mgmt (2)	DACL	DACR	LOUT1	ROUT1	LOUT2	ROUT2	MONO	OUT3	0	000000000
R27 (1Bh)	0011011	Additional Control (3)	ADCLRM[1:0]		VROI	0	0	0	0	0	0	000000000
R31 (1Fh)	0011111	ADC input mode	DS	MONOMIX[1:0]		RDCM	LDCM	0	0	0	0	000000000
R32 (20h)	0100000	ADCL signal path	0	LINSEL[1:0]		LMICBOOST[1:0]		0	0	0	0	000000000
R33 (21h)	0100001	ADCR signal path	0	RINSEL[1:0]		RMICBOOST[1:0]		0	0	0	0	000000000
R34 (22h)	0100010	Left out Mix (1)	LD2LO	LI2LO	LI2LOVOL[2:0]			0	LMIXSEL[2:0]			001010000
R35 (23h)	0100011	Left out Mix (2)	RD2LO	RI2LO	RI2LOVOL[2:0]			0	0	0	0	001010000
R36 (24h)	0100100	Right out Mix (1)	LD2RO	LI2RO	LI2ROVOL[2:0]			0	RMIXSEL[2:0]			001010000
R37 (25h)	0100101	Right out Mix (2)	RD2RO	RI2RO	RI2ROVOL[2:0]			0	0	0	0	001010000
R38 (26h)	0100110	Mono out Mix (1)	LD2MO	LI2MO	LI2MOVOL[2:0]			0	0	0	0	001010000
R39 (27h)	0100111	Mono out Mix (2)	RD2MO	RI2MO	RI2MOVOL[2:0]			0	0	0	0	001010000
R40 (28h)	0101000	LOUT2 volume	LO2VU	LO2ZC	LOUT2VOL[6:0]							001111001
R41 (29h)	0101001	ROUT2 volume	RO2VU	RO2ZC	ROUT2VOL[6:0]							001111001
R42 (2Ah)	0101010	MONOOUT volume	0	MOZC	MOUTVOL[6:0]							001111001

Table 9 Mapping of Program Registers

Please refer to the WM8750 datasheet for full details of the serial interface timing and all register features.

SERIAL INTERFACE SOFTWARE DESCRIPTION

The following section will detail the downloading and installation of evaluation software and also the operation of the software and the functionality of each control button.

SOFTWARE DOWNLOAD

The current evaluation board control software WM8750-EV1S should be downloaded from the Wolfson website [www.wolfsonmicro.com].

From the homepage it is recommended to carry out a search for 'WM8750' and select the evaluation board *'more'* button. Select *'download'* from the top right hand corner under the software label. Once the licence agreement has been accepted, select the WM8750_EV1S_REVx.x.ZIP link and download to your hard drive.

SOFTWARE INSTALLATION

Once the .zip file has been downloaded, to install the software:

- Open the .zip file.
- Double click on the setup.exe file.
- Follow the on-screen installation instructions and save to the desired location.

The software can then be opened by either running the extracted WM8750_EV1_REVx.x.exe file from the saved location or alternatively, selecting: Start > Programs > WM8750-EV1S-REVx.x > WM8750-EV1S.

SOFTWARE OPERATION

Due to the many features offered by the WM8750, the software has been split into five different panels. This eases the complexity of the software making each panel less busy, the panels have also been grouped so that it makes it simple to control each section of the device.

The main menu panel shown in Figure 4 is used to call up the other panels as well as offering a number of pull-down menus.

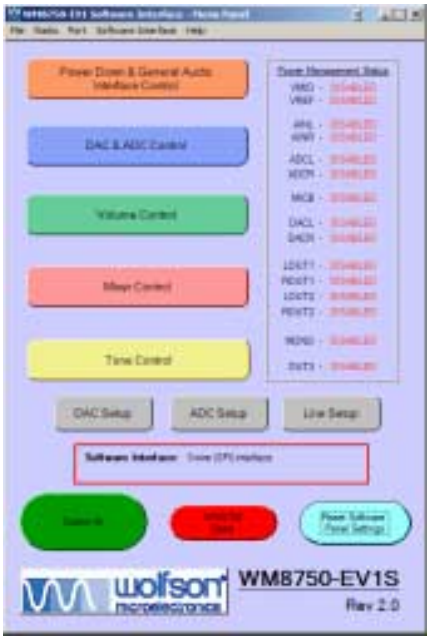

Figure 4 Software Menu Panel

The 'Submit All' button will submit values to every register of the WM8750. The 'Reset' button writes to the reset register (R15) but does not reset the control panel values. If the previous values are to be resubmitted then the 'Submit All' button should be pressed, if the user would like to start afresh then the 'Reset Software Panel Settings' button should also be pressed. Pressing this button does not write to the device, it only resets the panel settings to their default state. Left clicking on the Wolfson logo will open the PCs default web browser and go to the Wolfson Microelectronics website ('www.wolfsonmicro.com'). The DAC, ADC and Line setup buttons have also been provided as a quick start approach. Pressing either of these buttons will power up the DAC, ADC or Line signal paths in a known state as described in the following pages.

Important: The CS8427 SPDIF decoder IC will only work at a rate of 256fs. This will limit the sample rates that may be set using the WM8750 unless an external source is used to supply signals directly to the relevant pins of header H1 or taking the signals from the relevant pins of header H2.

DAC SUBMIT SETUP

By pressing the 'DAC Setup' button, the software writes to the device setting the following path: SPDIF_In through the DAC to the L/ROUT1 and L/ROUT2 outputs. The default format setting is 24-bit, I^2S. Table 6 lists the required board settings to allow this signal path to be used. This button is intended to ease the initial use of the WM8750 until the user becomes familiar with both device and software operation.

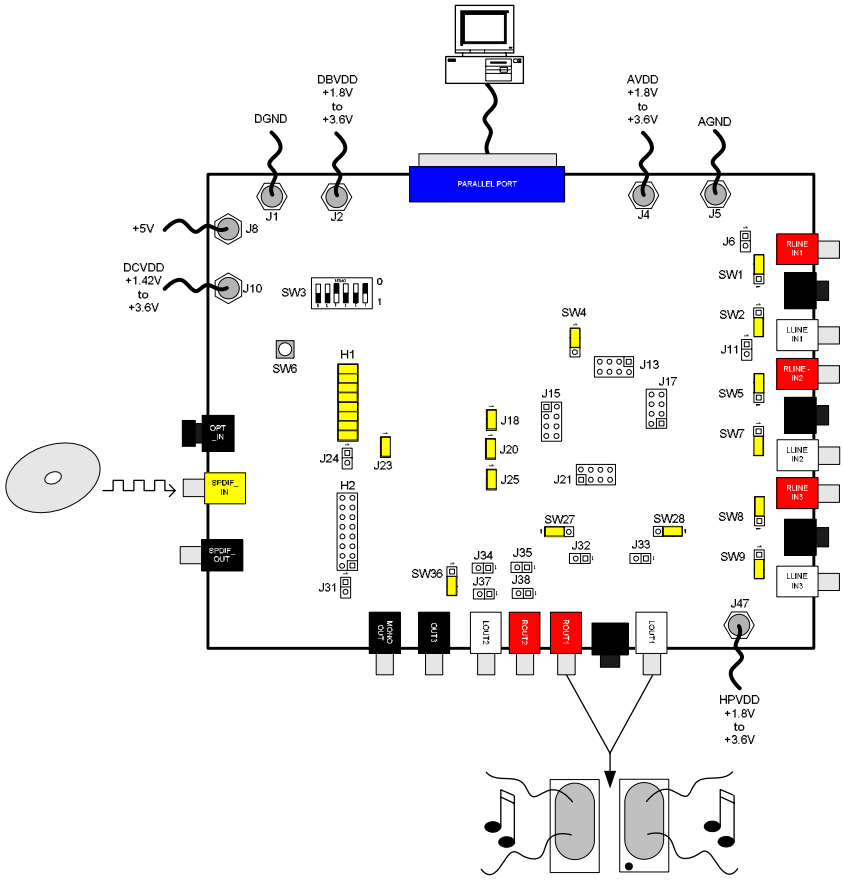

Figure 5 Recommended DAC Setup

LINKS AND JUMPERS	LINK/JUMPER STATUS	DESCRIPTION
H1	All jumpers in place	DAC clocks and data input
H2	No jumpers in place	ADC clocks and data output
SW36	Pins 2 and 3 SHORT	Connects to GND for HP output reference
J18 (BCLK)	SHORT	Slave mode
J20 (ADCLRC)	SHORT	Slave mode
J25 (DACLRC)	SHORT	Slave mode
J23	SHORT	Slave mode
J32, J33, J34 and J35	OPEN	OUT signals are AC coupled
SW3		1 2 3 4 5 6 DATA FORMAT 1 0 0 1 0 0 I2S Compatible
SW4	Pins 1 and 2 SHORT	3-wire (SPI) Control Mode
SW1, SW2	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW5, SW7	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW8, SW9	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW27, SW28	Pins 2 and 3 SHORT	Line Output Select (Phono Socket)

Table 10 DAC Setup Jumper Settings (Slave Mode)

ADC SUBMIT SETUP

By pressing the 'ADC Setup' button, the software writes to the device setting the L/RLINE_IN1 through ADC to SPDIF_Out path active. As with the DAC setup described previously, this is to ease the initial use of the WM8750 until the user becomes familiar with both device and software operation. It should be noted that the SPDIF_In connection is still required to provide the necessary clocks to the WM8750 in this mode.

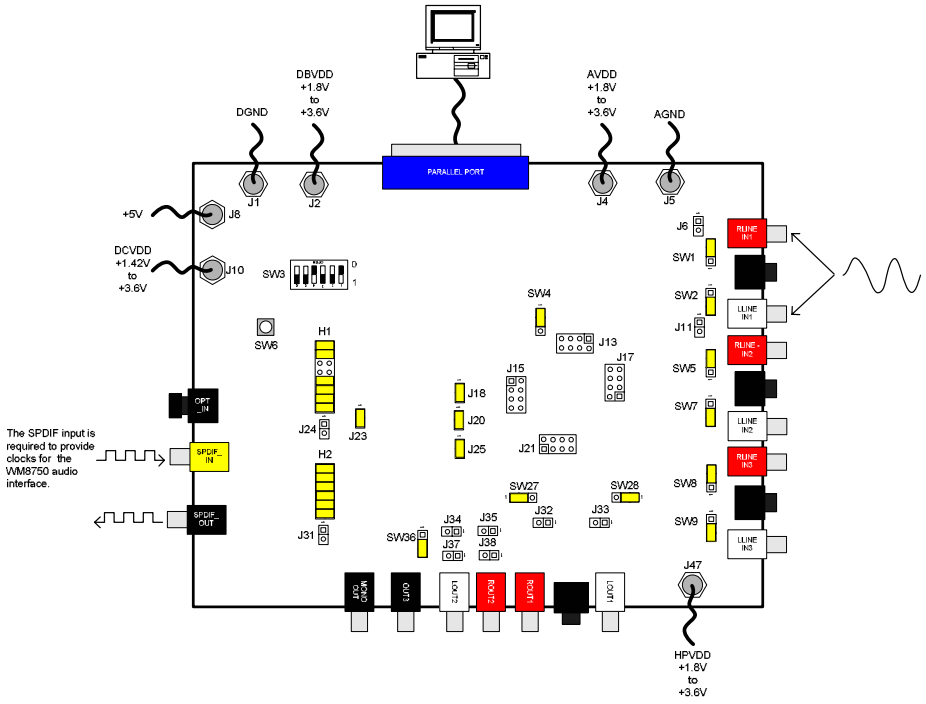

Figure 6 Recommended ADC Setup

LINKS AND JUMPERS	LINK/JUMPER STATUS	DESCRIPTION
H1	All jumpers in place except for the jumper connecting pins 5 and 6 and 7 and 8.	DAC clocks and data input
H2	All jumpers in place	ADC clocks and data output
SW36	Pins 2 and 3 SHORT	Connects to GND for HP output reference
J18 (BCLK)	SHORT	Slave mode
J20 (ADCLRC)	SHORT	Slave mode
J25 (DACLRC)	SHORT	Slave mode
J23	SHORT	Slave mode
J32, J33, J34 and J35	OPEN	OUT signals are AC coupled
SW3		1 2 3 4 5 6 DATA FORMAT 1 0 0 1 0 0 I2S Compatible
SW4	Pins 1 and 2 SHORT	3-wire (SPI) Control Mode
SW1, SW2	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW5, SW7	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW8, SW9	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW27, SW28	Pins 2 and 3 SHORT	Line Output Select (Phono Socket)

Table 11 ADC Setup Jumper Setup (Slave Mode)

LINE SUBMIT SETUP

By pressing the 'Line Setup' button, the software writes to the device setting the L/RLINE_IN1 through the analogue path to the L/ROUT1 and L/ROUT2 outputs. As with the setups previously described, this is to ease the initial use of the WM8750 until the user becomes familiar with both device and software operation.

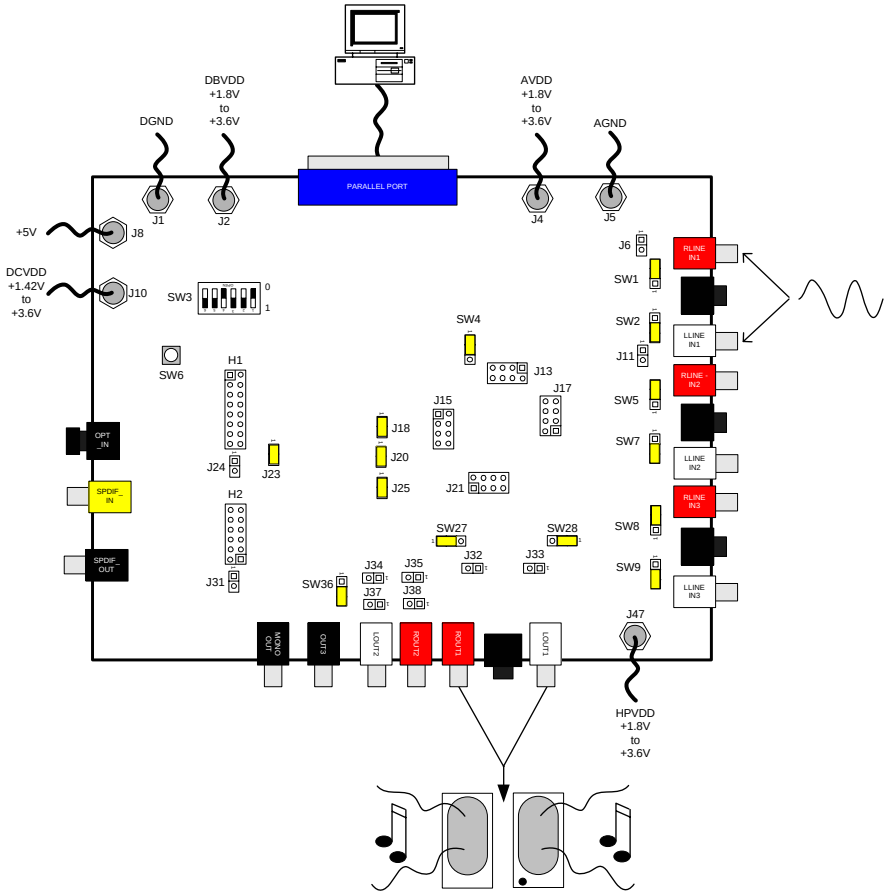

Figure 7 Recommended Line Setup

LINKS AND JUMPERS	LINK/JUMPER STATUS	DESCRIPTION
H1	No jumpers in place	DAC clocks and data input
H2	No jumpers in place	ADC clocks and data output
SW36	Pins 2 and 3 SHORT	Connects to GND for HP output reference
J18 (BCLK)	SHORT	Slave mode
J20 (ADCLRC)	SHORT	Slave mode
J25 (DACLRC)	SHORT	Slave mode
J23	SHORT	Slave mode
J32, J33, J34 and J35	OPEN	OUT signals are AC coupled
SW3		1 2 3 4 5 6 DATA FORMAT 1 0 0 1 0 0 I2S Compatible
SW4	Pins 1 and 2 SHORT	3-wire (SPI) Control Mode
SW1, SW2	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW5, SW7	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW8, SW9	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW27, SW28	Pins 2 and 3 SHORT	Line Output Select (Phono Socket)

Table 12 Line Setup Jumper Setup (Slave Mode)

POWER DOWN AND INTERFACE CONTROL

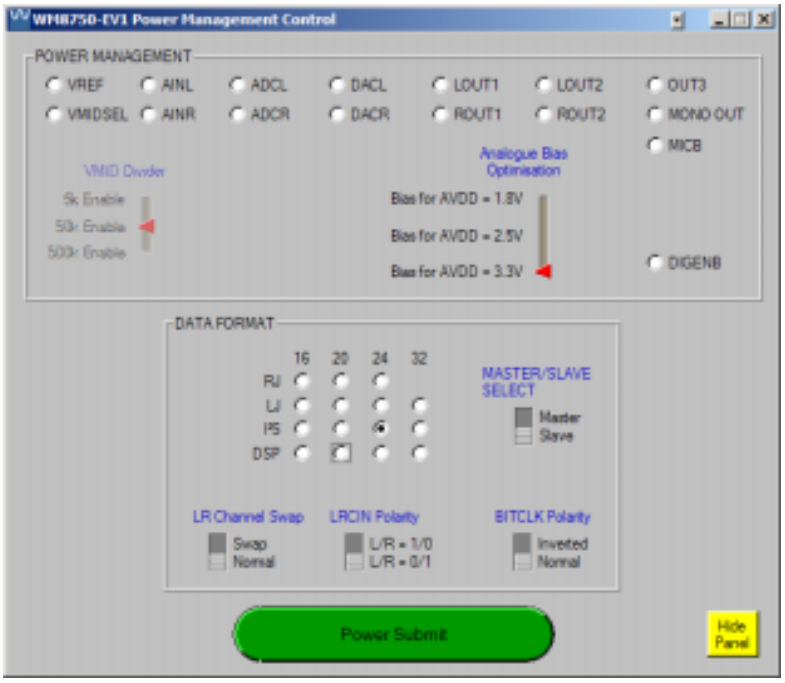

Figure 8 Power and Interface Control

The Power Down and Interface Control panel is used to enable/disable the various sections of the WM8750. It is also used to set the audio interface to the required data format. Pressing the 'Power Submit' button will cause the settings shown on this panel to be written to the WM8750. A full device register write is not sent.

DAC AND ADC CONTROL

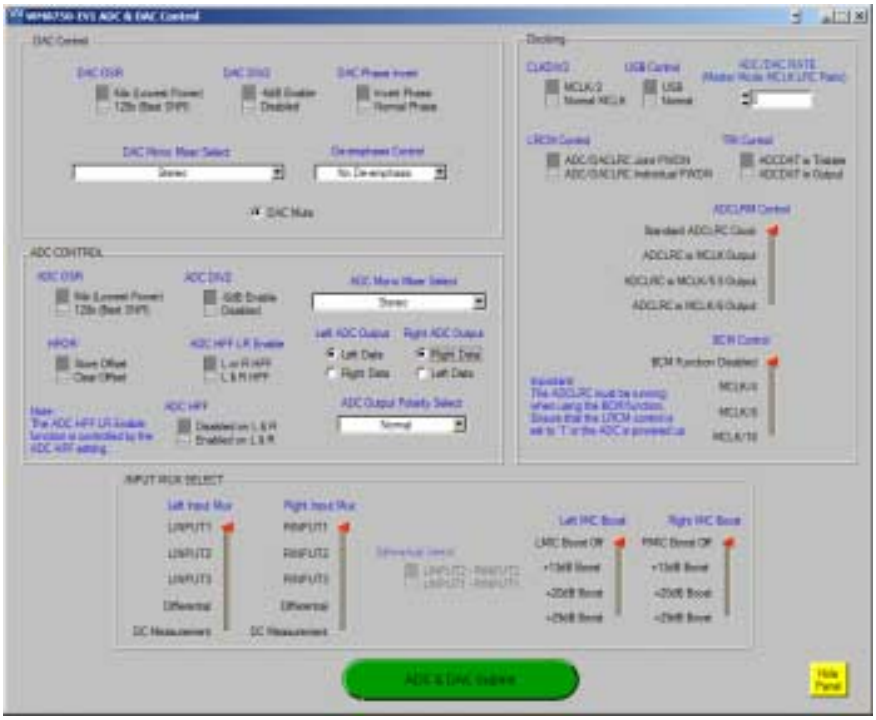

Figure 9 DAC and ADC Control

The DAC and ADC Control panel is used to control the many DAC and ADC related features of the WM8750. Pressing the 'ADC and DAC Submit' button will cause the settings shown on this panel to be written to the WM8750. A full device register write is not sent.

VOLUME CONTROL

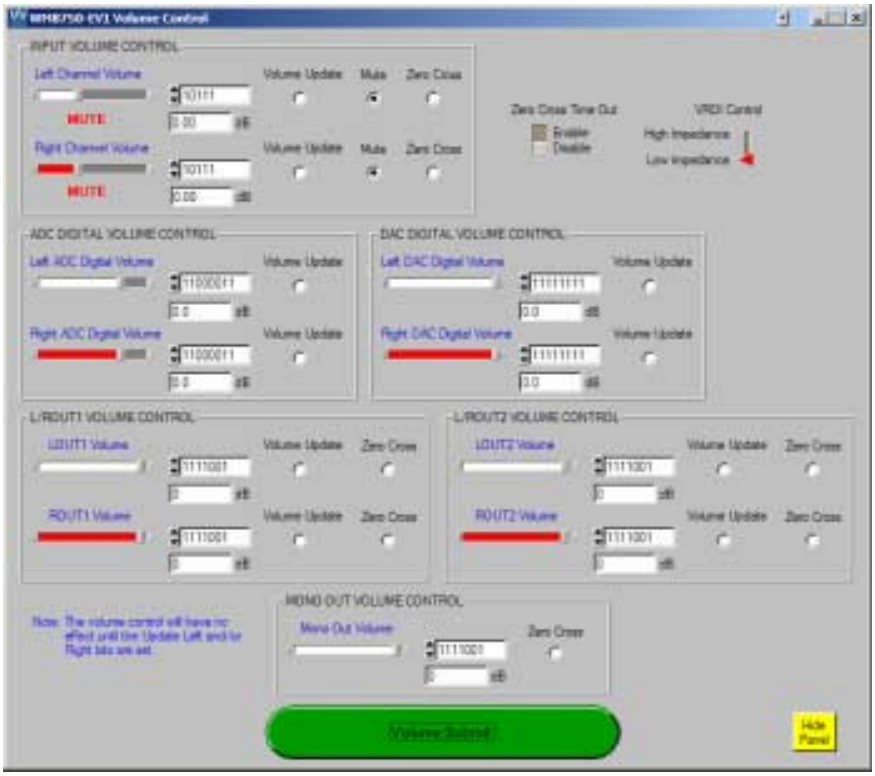

Figure 10 Volume Control

The Volume Control panel is used to control both analogue and digital volume settings of the WM8750. The volume sliders update in 'real' time (i.e. the 'Volume Submit' button does not have to be pressed to update the output volume level) but will only have an effect on the output if the Volume Update bits are set. Once changes are made to the Volume Update bits, the 'Volume Submit' button must be left clicked for the change to take effect. Pressing the 'Volume Submit' button will cause the settings shown on this panel to be written to the WM8750. A full device register write is not sent.

MIXER CONTROL

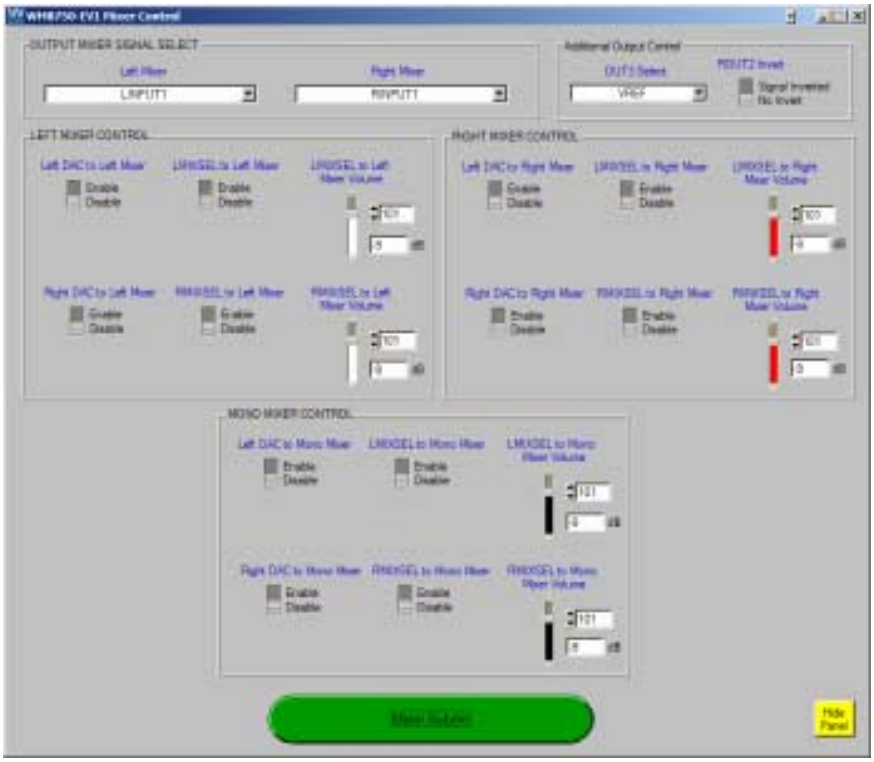

Figure 11 Mixer Control

The Mixer Control panel is used to control the many signal mixing options offered by the WM8750. The volume sliders update in 'real' time (i.e. the 'Mixer Submit' button does not have to be pressed to update the mixer volume level). Pressing the 'Mixer Submit' button will cause the settings shown on this panel to be written to the WM8750. A full device register write is not sent.

TONE CONTROL

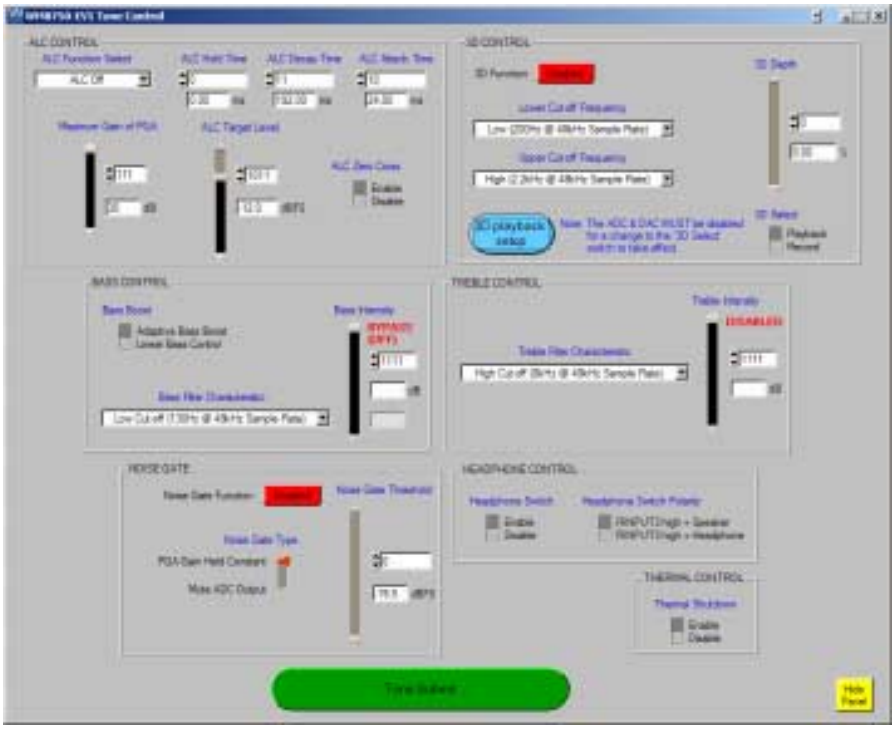

Figure 12 Tone Control

The Tone Control panel is used to control the various tone options (3D, Bass, Treble, etc) offered by the WM8750. The sliders update in 'real' time (i.e. the 'Tone Submit' button does not have to be pressed to update the relevant tone slider level). Pressing the 'Tone Submit' button will cause the settings shown on this panel to be written to the WM8750. A full device register write is not sent.

It is important to note that to change the '3D Select' control setting from Record to Playback, the ADC and DAC must be set to a power down state in the Power Down and Interface Control panel. After the '3D Select' setting has been made and written to the WM8750 the ADC and DAC should be powered up.

Once any of the WM8750 default settings are changed on the control panel, the relevant section is highlighted in blue to show the section where the setting has changed. The highlight around the relevant section also has the purpose of letting the user know that they have not yet submitted the required changes to the WM8750. After a Submit from the relevant panel or a main panel Submit, the sections will default back to their original 'panel grey' colour. The Submit button also becomes inactive until another change is made to the register settings.

Refer to the Appendix Section of this user manual for additional evaluation board setup details.

SCHEMATIC LAYOUT

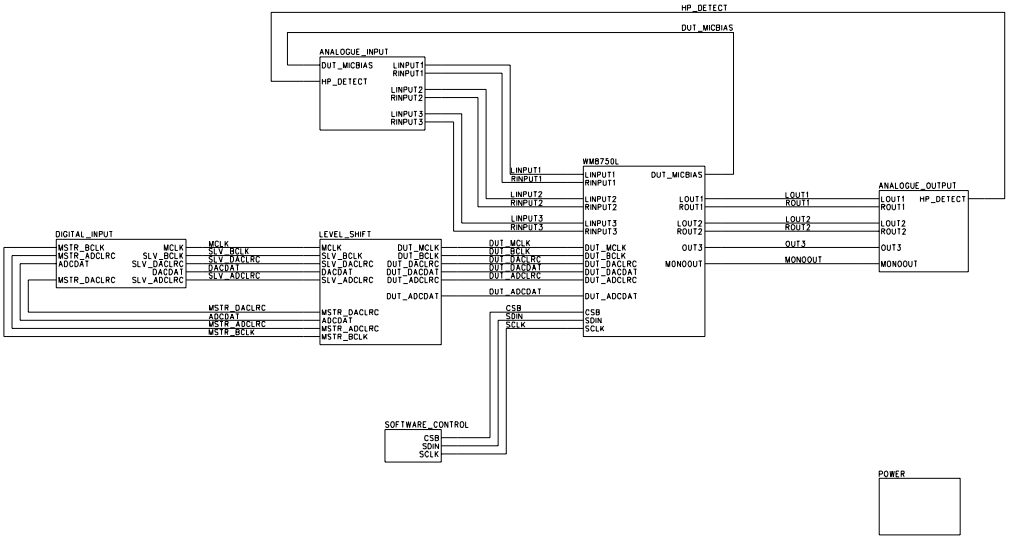

Figure 13 Functional Diagram

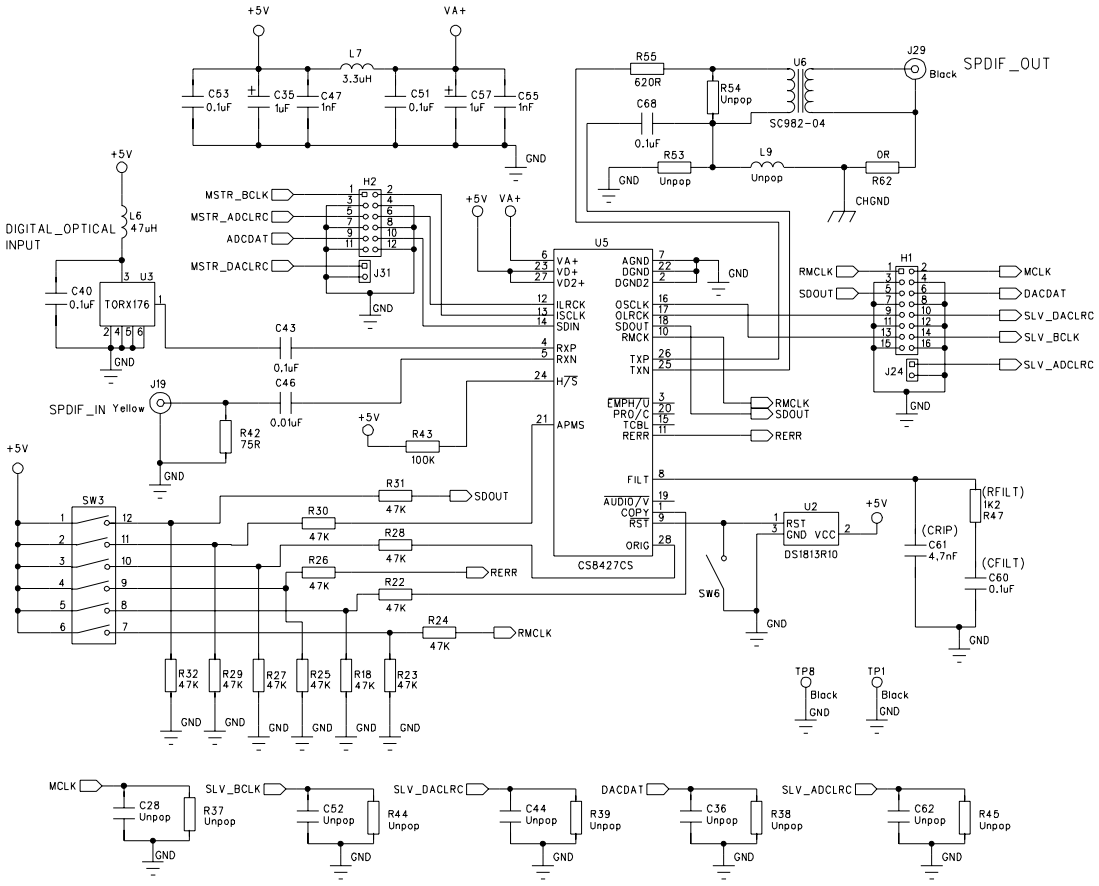

Figure 14 Digital Input

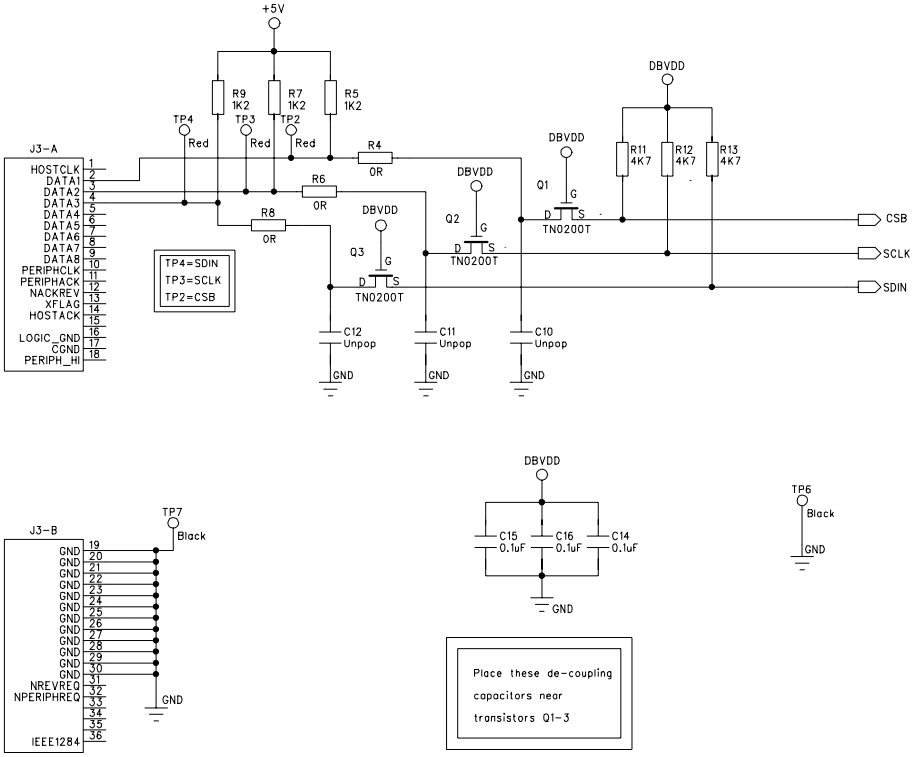

Figure 15 Software Control

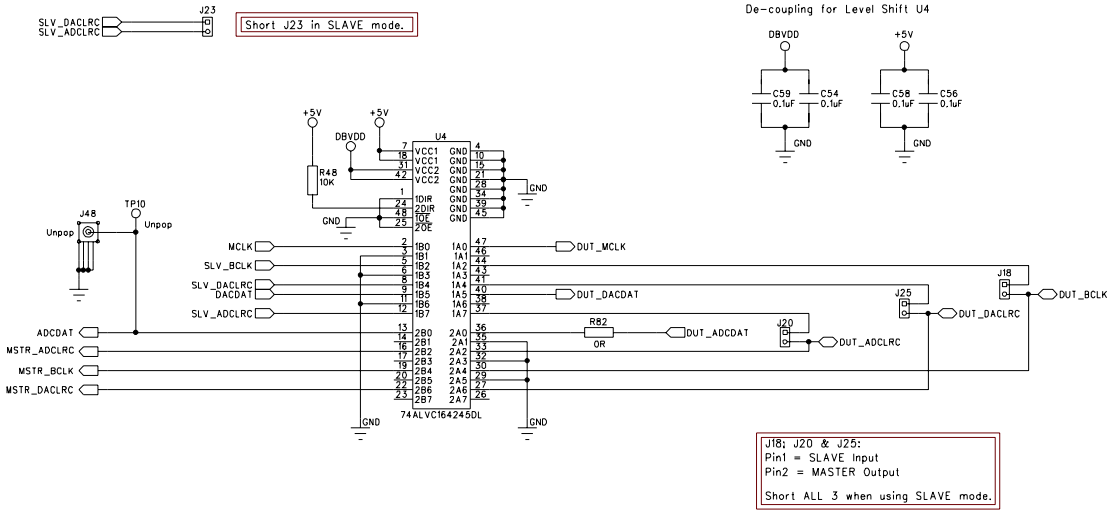

Figure 16 Level Shift

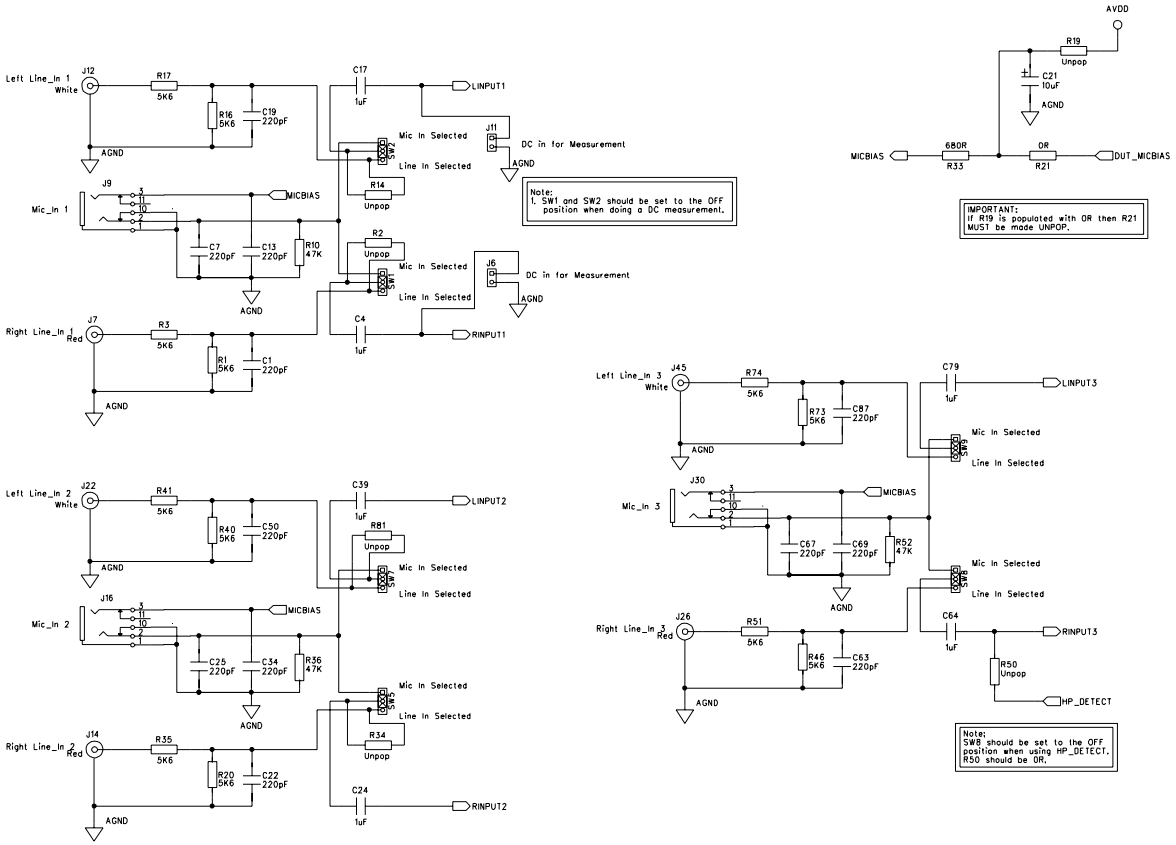

Figure 17 Analogue Input

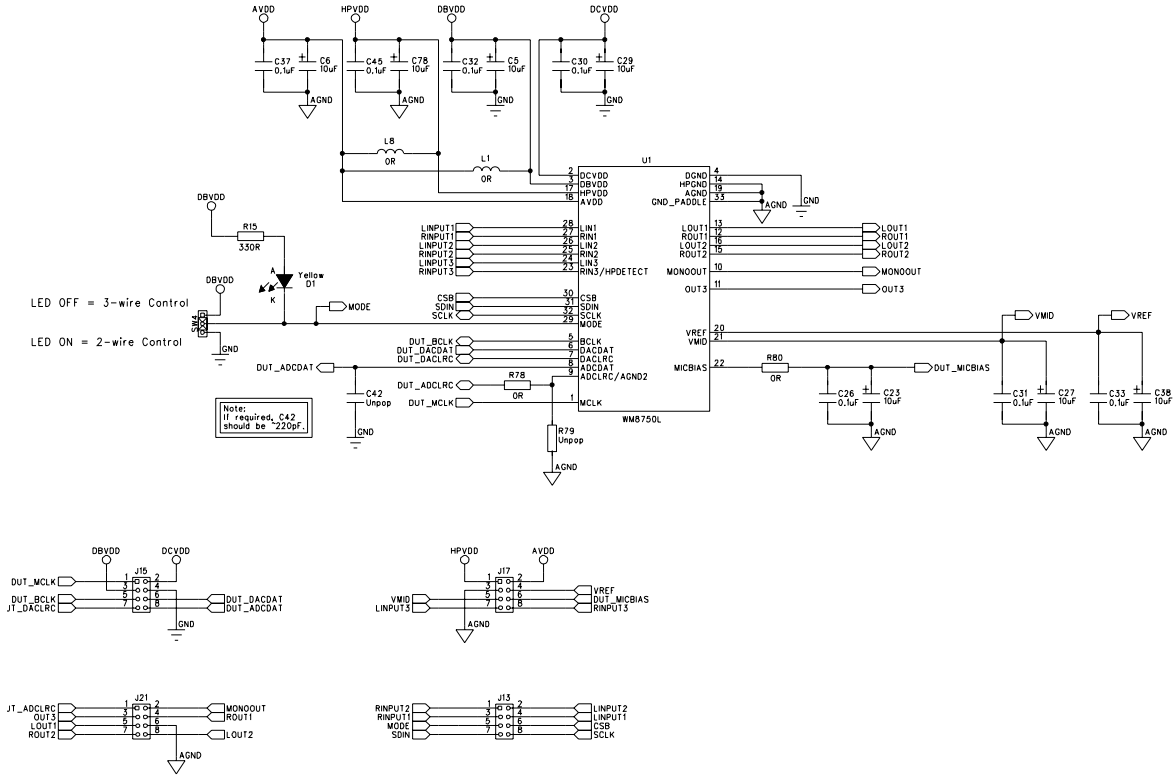

Figure 18 WM8750

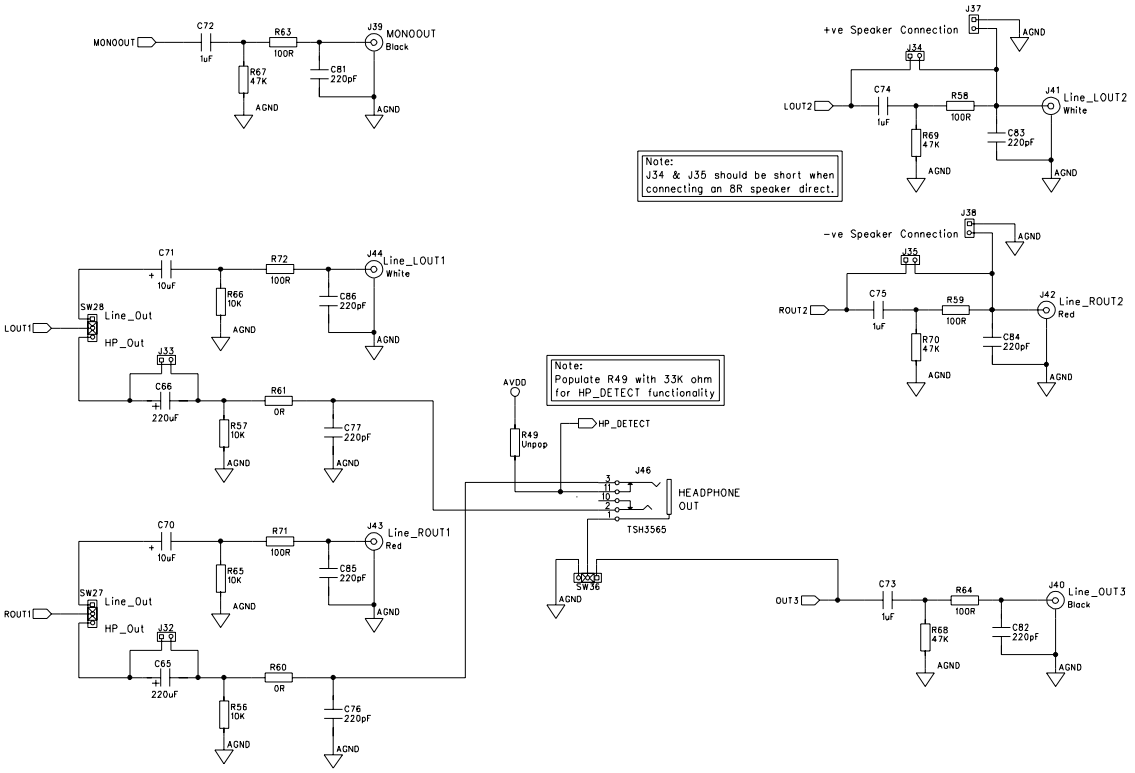

Figure 19 Analogue Output

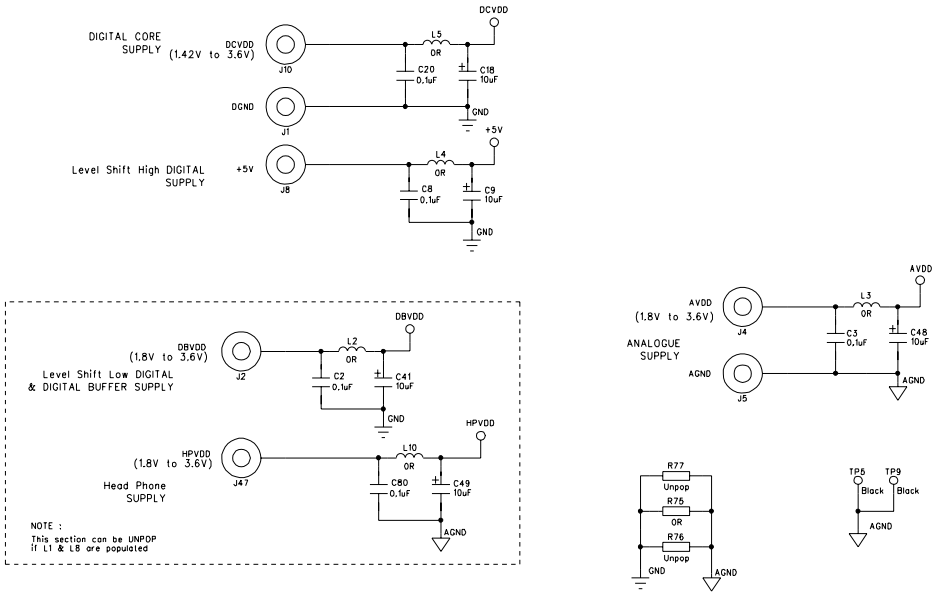

Figure 20 Power

WM8750-EV1B PCB LAYOUT

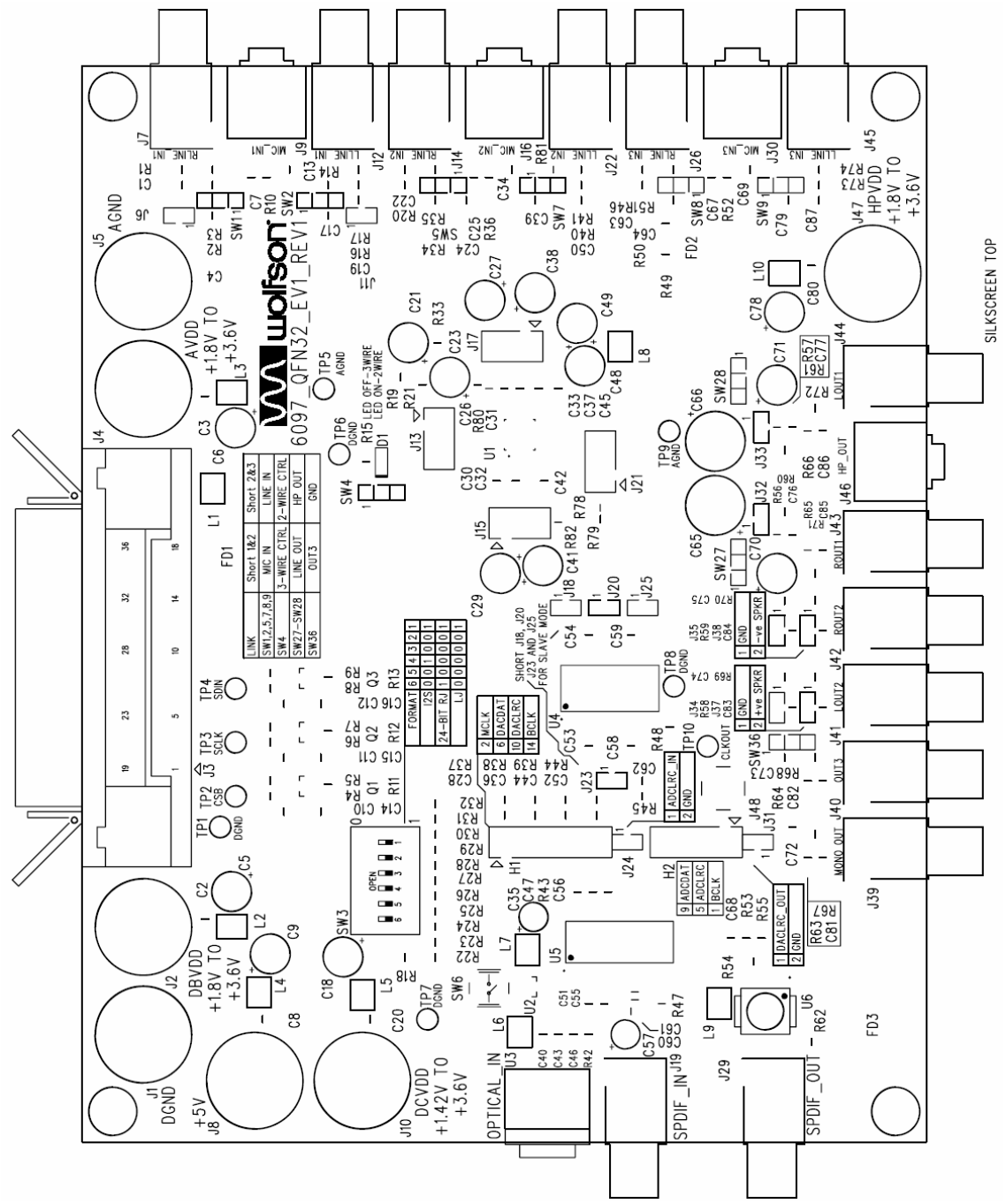

Figure 21 Top Layer Silkscreen

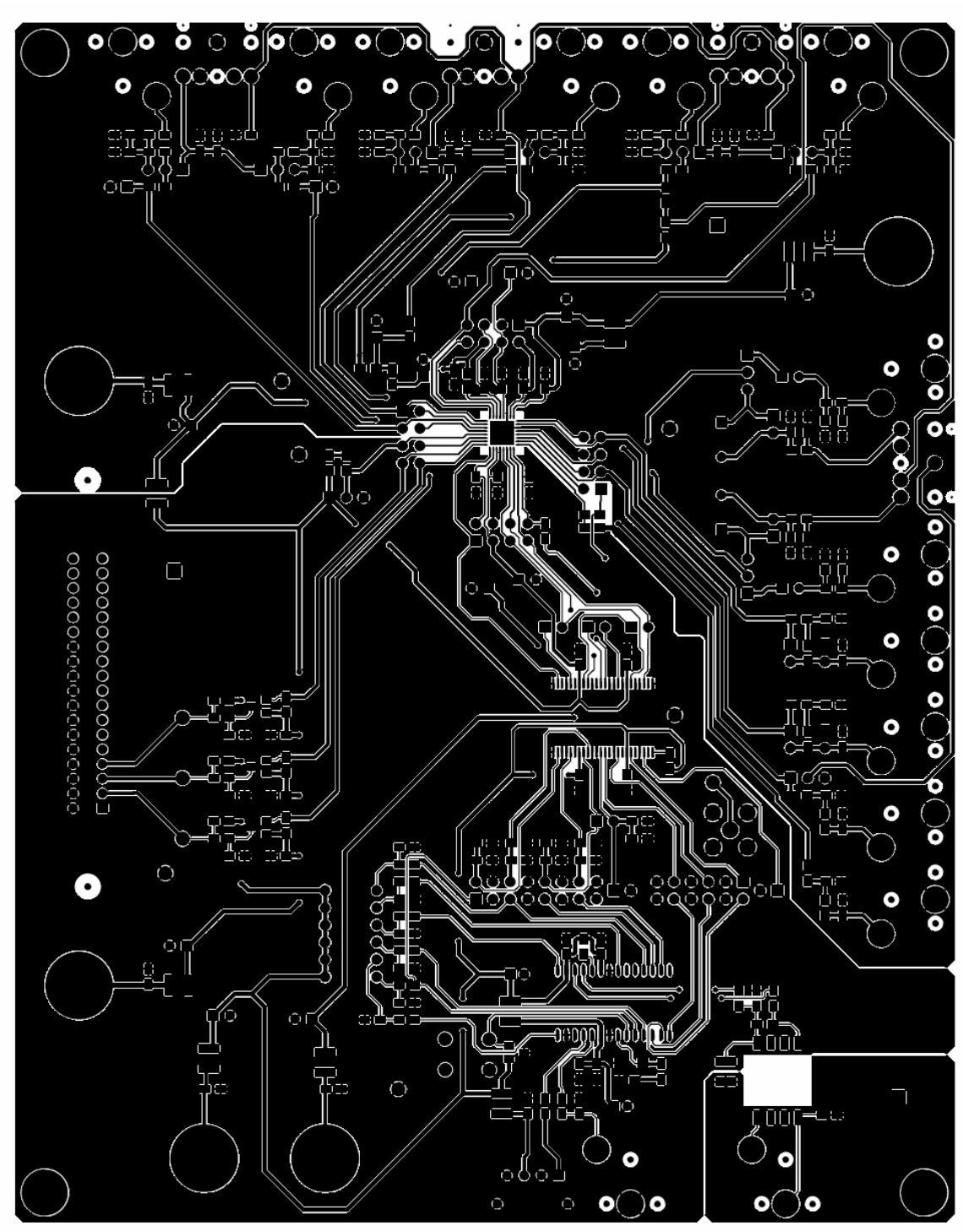

Figure 22 Top Layer

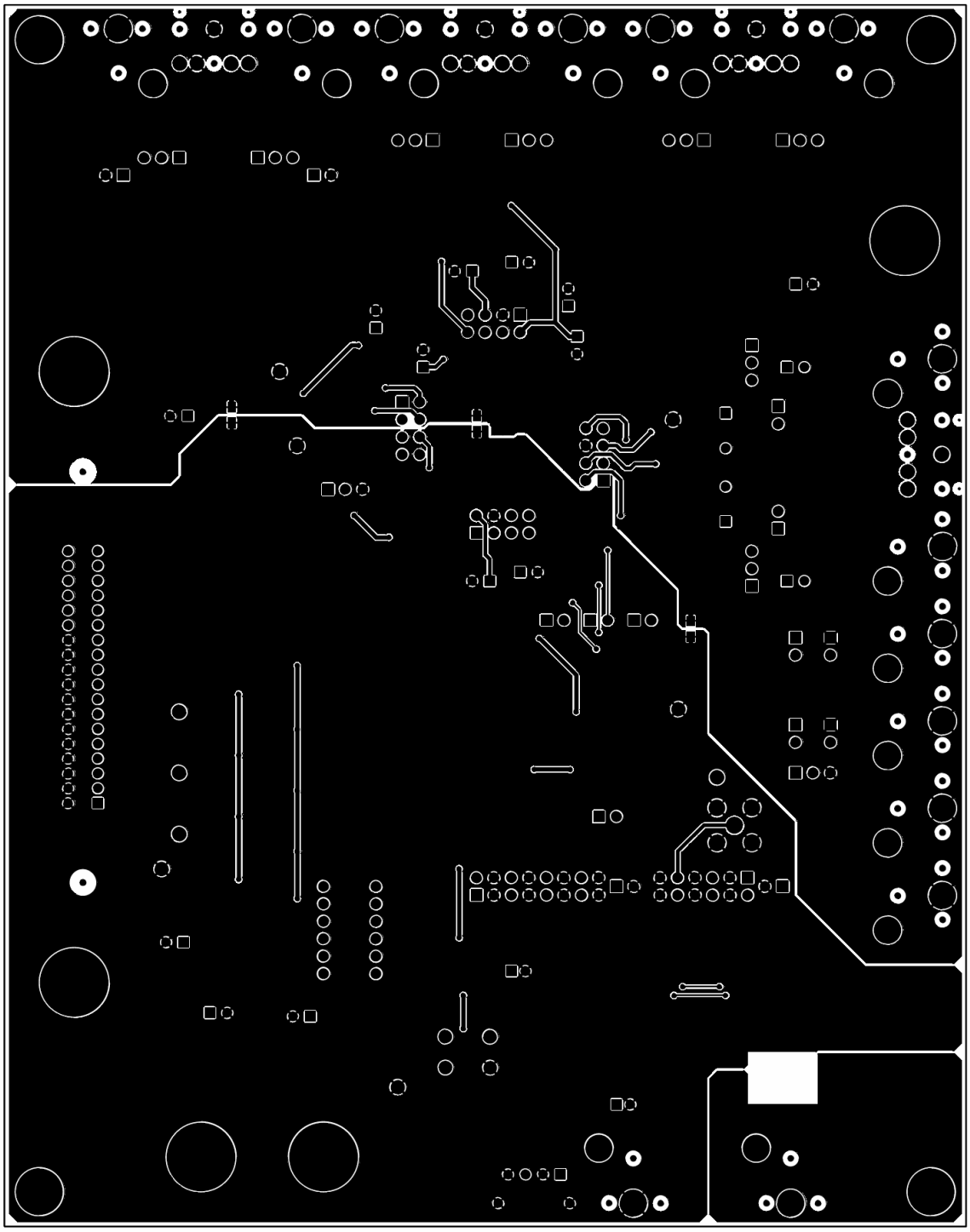

Figure 23 Bottom Layer

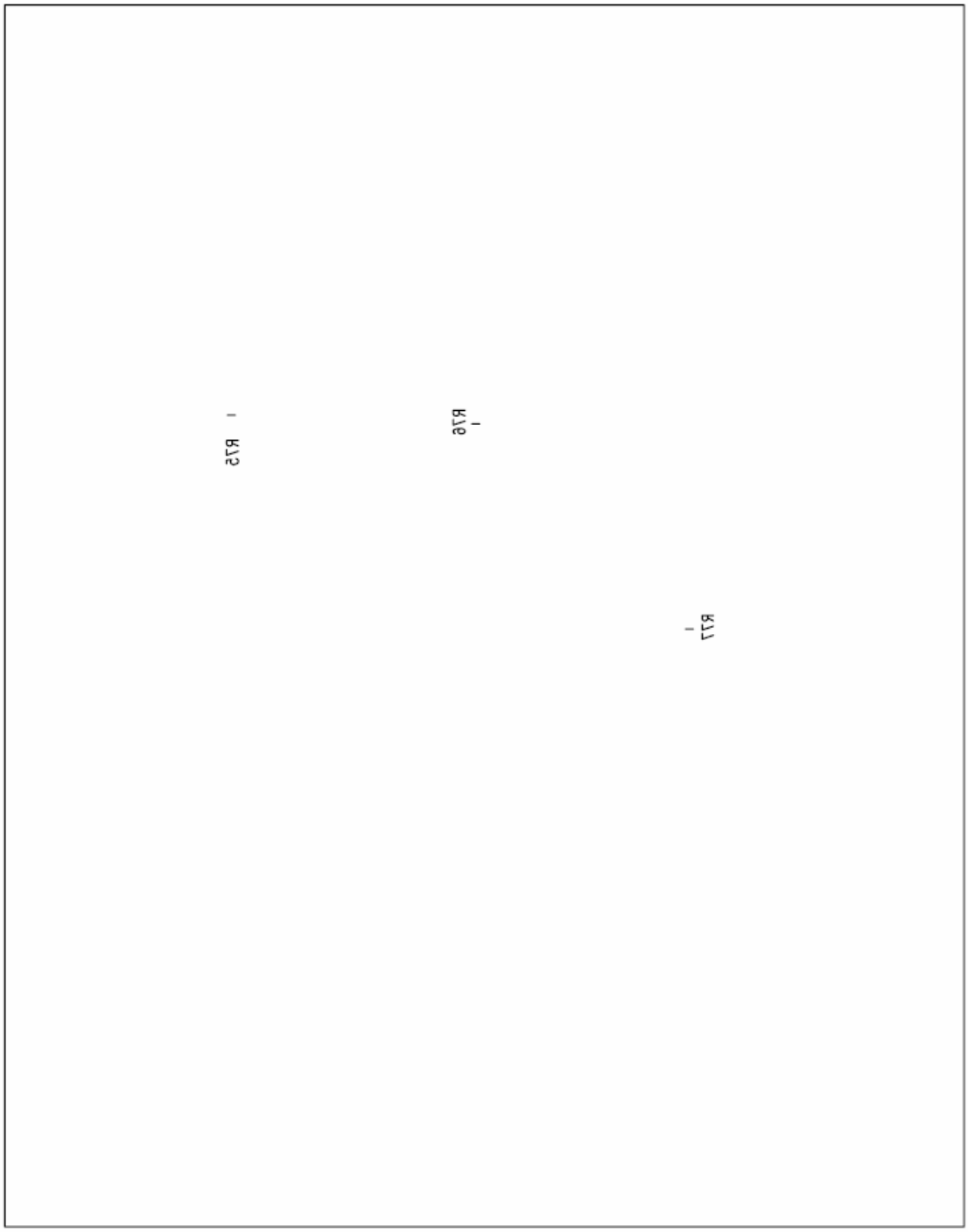

Figure 24 Bottom Layer Silkscreen

WM8750-EV1B BILL OF MATERIAL

DESCRIPTION	REFERENCE	QUANTITY
74ALVC164245 16 Bit Dual Supply Bus Transceiver SSO	U4	1
10uF 6.3 Dia 2.5 pitch Oscon Through Hole Cap. 16V 20%	C5-6 C9 C18 C21 C23 C27 C29 C38 C41 C48-49 C70-71 C78	15
1uF 4 Dia 2 pitch Oscon Through Hole Cap. 25V 20%	C35 C57	2
220uF 10 Dia 5 pitch Oscon Through Hole Cap. 10V 20%	C65-66	2
0.01uF 0805 SMD Ceramic Capacitor 50V X7R	C46	1
0.1uF 0805 SMD Ceramic Capacitor 50V X7R	C2-3 C8 C14-16 C20 C26 C30-33 C37 C40 C43 C45 C51 C53-54 C56 C58-60 C68 C80	25
1nF 0805 SMD Ceramic Capacitor 50V NPO	C47 C55	2
1uF 0805 SMD Ceramic Capacitor 10V X7R	C4 C17 C24 C39 C64 C72-75 C79	10
220pF 0805 SMD Ceramic Capacitor 50V X7R	C1 C7 C13 C19 C22 C25 C34 C50 C63 C67 C69 C76-77 C81-87	20
Unpop 0805 SMD Ceramic Capacitor site	C10-12 C28 C36 C42 C44 C52 C62	9
4.7nF 1206 SMD Ceramic Capacitor 50V COG	C61	1
3.5mm Jack Socket 6.5mm Centre Height	J9 J16 J30 J46	4
2x4 2.54mm pitch PCB Pin Header VERTICAL	J13 J15 J17 J21	4
2x6 2.54mm pitch PCB Pin Header VERTICAL	H2	1
2x8 2.54mm pitch PCB Pin Header VERTICAL	H1	1
36-way Centronics/IEE488 PCB mountable Connector	J3	1
JSK9-16-G0 PCB 1x3 Jumper Switch 0.1" Center-off VERTICAL	SW1-2 SW4-5 SW7-9 SW27-28 SW36	10
4mm Non-Insulated Panel Socket 16A	J1-2 J4-5 J8 J10 J47	7
Phono Socket PCB mount BLACK	J29 J39-40	3
Phono Socket PCB mount RED	J7 J14 J26 J42-43	5
Phono Socket PCB mount WHITE	J12 J22 J41 J44-45	5
Phono Socket PCB mount YELLOW	J19	1
Unpop SMB Connector PCB Mount	J48	1
CS8427 96KHz Audio Transceiver	U5	1
DS1813 5V active Low Power-On-Reset chip SOT	U2	1
0R 1206 Resistor on 1210 Inductor site	L1-5 L8 L10	7
3.3uH 1210 Surface Mount Inductor '1210A series'	L7	1
47uH 1210 Surface Mount Inductor 'PA series'	L6	1
Unpop 1210 Surface Mount Inductor site	L9	1
HSMY-C670 0805 SMD Chip LED YELLOW	D1	1
1x2 PCB Pin Header 0.1" VERTICAL	J6 J11 J18 J20 J23-25 J31-35 J37-38	14
Slotted Panhead Screw - M3 thread; 12mm long	SC1-4	4
Hexagonal brass M3 size spacer 20mm length	P1-4	4
Plain M3 size washer	W1-4	4
0R 0805 SMD chip resistor 1% 0.1W	R4 R6 R8 R21 R60-62 R75 R78 R80 R82	11
100K 0805 SMD chip resistor 1% 0.1W	R43	1
100R 0805 SMD chip resistor 1% 0.1W	R58-59 R63-64 R71-72	6
10K 0805 SMD chip resistor 1% 0.1W	R48 R56-57 R65-66	5
1K2 0805 SMD chip resistor 1% 0.1W	R5 R7 R9 R47	4
330R 0805 SMD chip resistor 1% 0.1W	R15	1
47K 0805 SMD chip resistor 1% 0.1W	R10 R18 R22-32 R36 R52 R67-70	19

DESCRIPTION	REFERENCE	QUANTITY
4K7 0805 SMD chip resistor 1% 0.1W	R11-13	3
5K6 0805 SMD chip resistor 1% 0.1W	R1 R3 R16-17 R20 R35 R40-41 R46 R51 R73-74	12
620R 0805 SMD chip resistor 1% 0.1W	R55	1
680R 0805 SMD chip resistor 1% 0.1W	R33	1
75R 0805 SMD chip resistor 1% 0.125W	R42	1
Unpopulated 0805 resistor site	R2 R14 R19 R34 R37-39 R44-45 R49-50 R53-54 R76-77 R79 R81	17
DIL Switch 6-Way Rocker	SW3	1
B3F1000 SPNO PCB mount switch	SW6	1
1.32mm PCB Test Terminal BLACK	TP1 TP5-9	6
1.32mm PCB Test Terminal RED	TP2-4	3
Unpop 1.32mm PCB Test Terminal	TP10	1
TORX176 Digirtal Audio Optical Receiver	U3	1
2:1 Ratio 96KHz SPDIF Digital Audio transformer SOIC(1)	U6	1
TN0200T N- Channel MOSFET SOT23	Q1-3	3
WM8750L Stereo CODEC for Portable Audio QFN	U1	1

Table 13 WM8750-EV1M Bill of Materials

Note: [1] The audio transformer used on this board is manufactured by Scientific Conversion Inc. (www.scientificonversion.com).

APPENDIX

EXTERNAL DSP CONNECTION TO THE WM8750-EV1B

The WM8750-EV1B evaluation board has been designed to allow it to be easily connected to an external DSP platform with error free operation.

The following information is provided to ease the connection process and ensure that all signals sent and received by the WM8750-EV1B are reliable and at the correct voltage levels.

AUDIO INTERFACE CONNECTIONS

It is recommended that twisted pair (signal twisted with GND) or shielded wires are used to make the audio interface connections between the DSP and WM8750-EV1B platforms. This is to ensure that no interference or noise is picked up by the clocks or data lines, thus reducing performance and reliability.

When the WM8750 is set in **Slave Mode**, the jumpers on header H1 should be removed, disconnecting the digital input section of the evaluation board. The audio interface timing and data signals from the DSP platform should then be connected as shown in Figure 25. The signals should be connected to H1 and not to the header strips J15 and J21 running up each side of the device. Connecting the signals to the output side of the level-shift IC (U4) will cause drive contention between U4 and the DSP and could result in damage to either or both devices. In most cases, the DSP supplies will be set around 3V for low power portable applications. The inputs to the level-shift IC (74ALVC164245) have a TTL threshold (i.e. Logic High = +2V(min); Logic Low = +0.8V(max)) and low input current requirements (i.e. 15uA max) allowing most DSPs to connect directly.

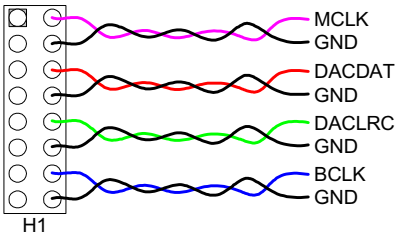

Figure 25 Connections from DSP Platform

The digital inputs to the WM8750 have a CMOS threshold (i.e. Logic High (min) = DBVDDx0.7; Logic Low (max) = DBVDDx0.3). These are met directly by the level shift IC outputs.

The jumpers on H2 should also be removed, disconnecting the digital output section of the WM8750 evaluation board. The ADCDAT data from the WM8750 should then be connected to the DSP via pin 8 of header strip J15 and the GND connection should be taken from pin 4 of header strip J15.

The ADCDAT signal should be taken direct from the WM8750 digital output as the output side of the level-shift IC (U4) from the WM8750 is pulled up to +5V which may overdrive and cause damage to the DSP inputs. The digital output levels of the WM8750 are Logic High (min) = DBVDDx0.9; Logic Low (max) = DBVDDx0.1 which should meet the input level requirements of most DSPs running at +3V supplies. If the DSP is running with +5V supplies then the connections to it should be made from the output side of the level-shift IC (U4), connecting the signals as shown in Figure 26.

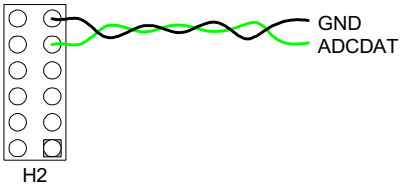

Figure 26 Data Connection to the DSP Platform (+5V tolerant input levels)

When the WM8750 is set to **Master Mode**, the jumpers on header H1 should be removed, disconnecting the digital input section of the evaluation board. If an external MCLK signal is being used (i.e. supplied by the DSP) then the DSP platform should be connected as shown in Figure 27. The signal should be connected to H1 and not to the header strip J15 running up the side of the device. Connecting the signal to the output side of the level-shift IC (U4) will cause drive contention between U4 and the DSP and could result in damage to either or both devices. In most cases, the DSP supplies will be set around +3V for low power portable applications. The inputs to the level-shift IC (74ALVC164245) have a TTL threshold (i.e. Logic High = +2V(min); Logic Low = +0.8V(max)) and low input current requirements (i.e. 15uA max) allowing most DSPs to connect directly.

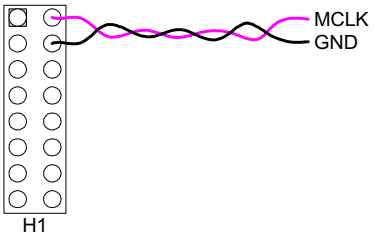

Figure 27 Timing Connections from DSP Platform

The digital inputs to the WM8750 have a CMOS threshold (i.e. Logic High (min) = DBVDDx0.7; Logic Low (max) = DBVDDx0.3). These are met directly by the level shift IC outputs.

The jumpers on H2 should also be removed, disconnecting the digital output section of the WM8750 evaluation board. The ADCDAT, BCLK and ADCLRC signals from the WM8750 should then be connected to the DSP from headers J15 and J21 running up each side of the WM8750.

The ADCDAT, BCLK and ADCLRC signals should be taken direct from the WM8750 digital output as the output side of the level-shift IC (U4) from the WM8750 is pulled up to +5V which may overdrive and cause damage to the DSP inputs. The digital output levels of the WM8750 are Logic High (min) = DBVDDx0.9; Logic Low (max) = DBVDDx0.1 which should meet the input level requirements of most DSPs running at +3V supplies. If the DSP is running with +5V supplies (and +5V tolerant inputs) then the connections from the WM8750 evaluation board to the DSP should be made from H2 on the output side of the level-shift IC from the WM8750 as shown in Figure 28.

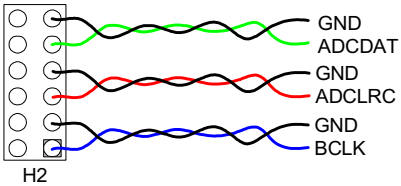

Figure 28 Connections to the DSP Platform (+5V tolerant input levels)

This will ensure that the DSP input level specifications are met.

SOFTWARE INTERFACE

When using the WM8750-EV1B evaluation board with a DSP platform, the registers may be set using the supplied software with a PC and parallel port cable as shown in Figure 29.

If the DSP is used to write to the WM8750 registers as well as supplying/receiving the audio interface timing and data signals, it is recommended that twisted pair or shielded wires are used to connect the DSP platform to the WM8750-EV1B. If the DSP supplies are set to the same voltage as the DBVDD supplies of the WM8750, a direct connection can be made to pin 6 (CSB), pin 7 (SDIN) and pin 8 (SCLK) of header strip J13 for 3-wire software mode as shown in Figure 30. If the DSP is running at a higher voltage (e.g. +5V) than the WM8750, the signals from the DSP platform should be connected to test points TP2 (CSB), TP4 (SDIN) and TP3 (SCLK). Connecting the higher voltage signals from the DSP to the test points will level shift through the transistors down to the same level as the DBVDD supply as shown in Figure 31. This will ensure that the WM8750 input CMOS thresholds (i.e. Logic High (min) = DBVDDx0.7; Logic Low (max) = DBVDDx0.3) are met and the device will not be damaged.

The same connections apply for controlling the WM8750 via 2-wire software mode (i.e. only pin 7 (SDIN) and pin 8 (SCLK) of header strip J13 are used). Pin 6 (CSB) can be pulled low on the board if device address 0011010 [0x34h] is required or pulled high address 0011011 [0x36h] is required.

CONNECTION DIAGRAMS

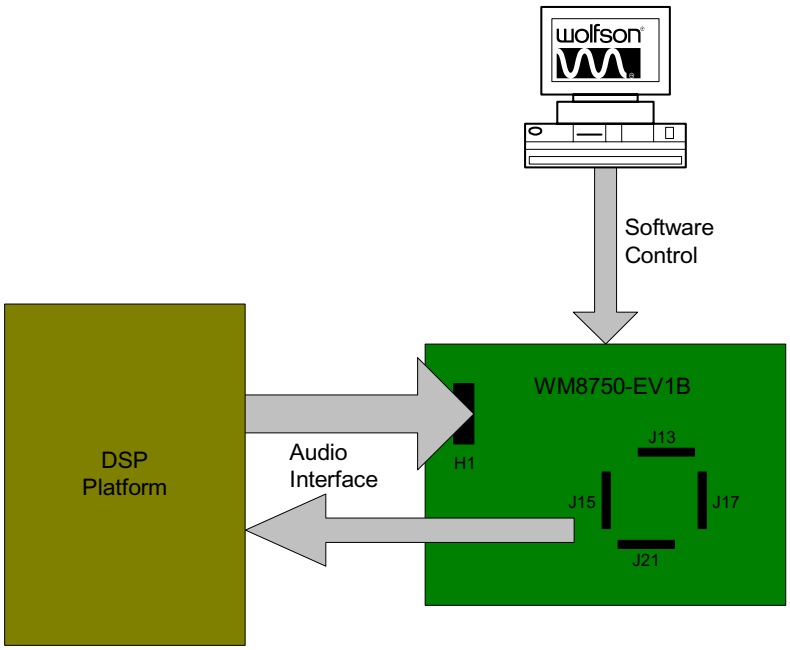

Figure 29 DSP Connection with PC Control using Wolfson Software

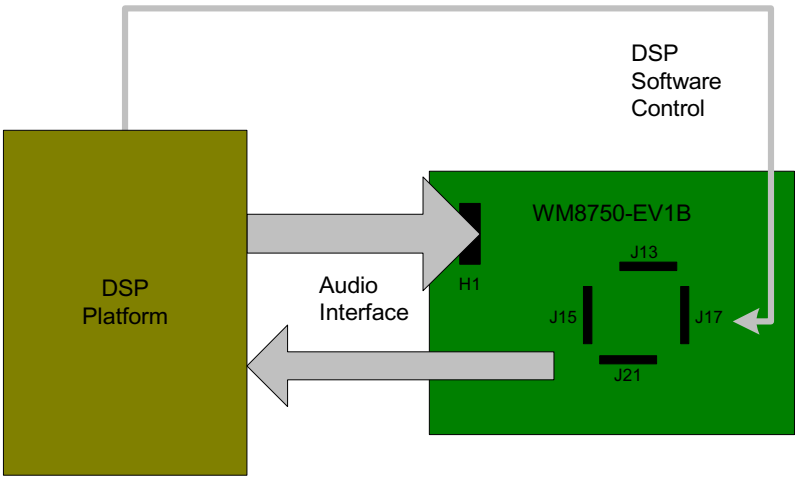

Figure 30 Full DSP Control with Equal Voltage Supplies for DSP and WM8750

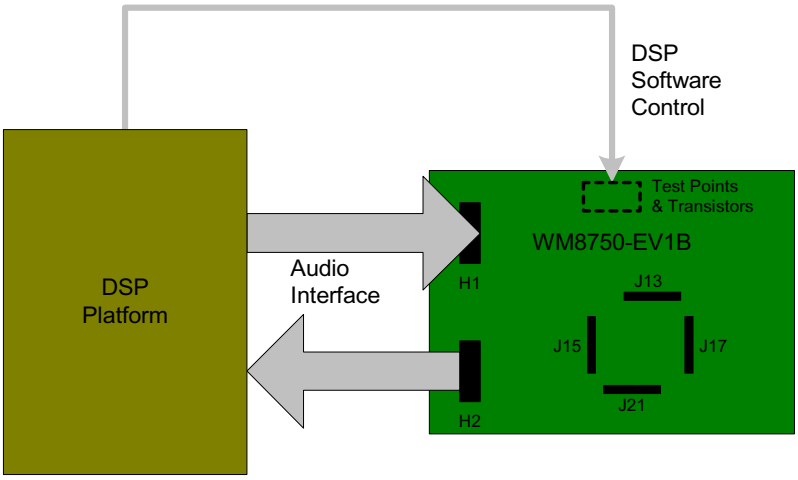

Figure 31 Full DSP Control with Higher Voltage DSP Supply than WM8750

ADDITIONAL WM8750-EV1B SETUP RECOMMENDATIONS

ADC TO DAC LOOPBACK

Setting up the WM8750-EV1 in loopback mode allows an analogue signal to be applied to L/RLINE_IN1, passed through the ADC, looped into the DAC and output on the L/ROUT outputs.

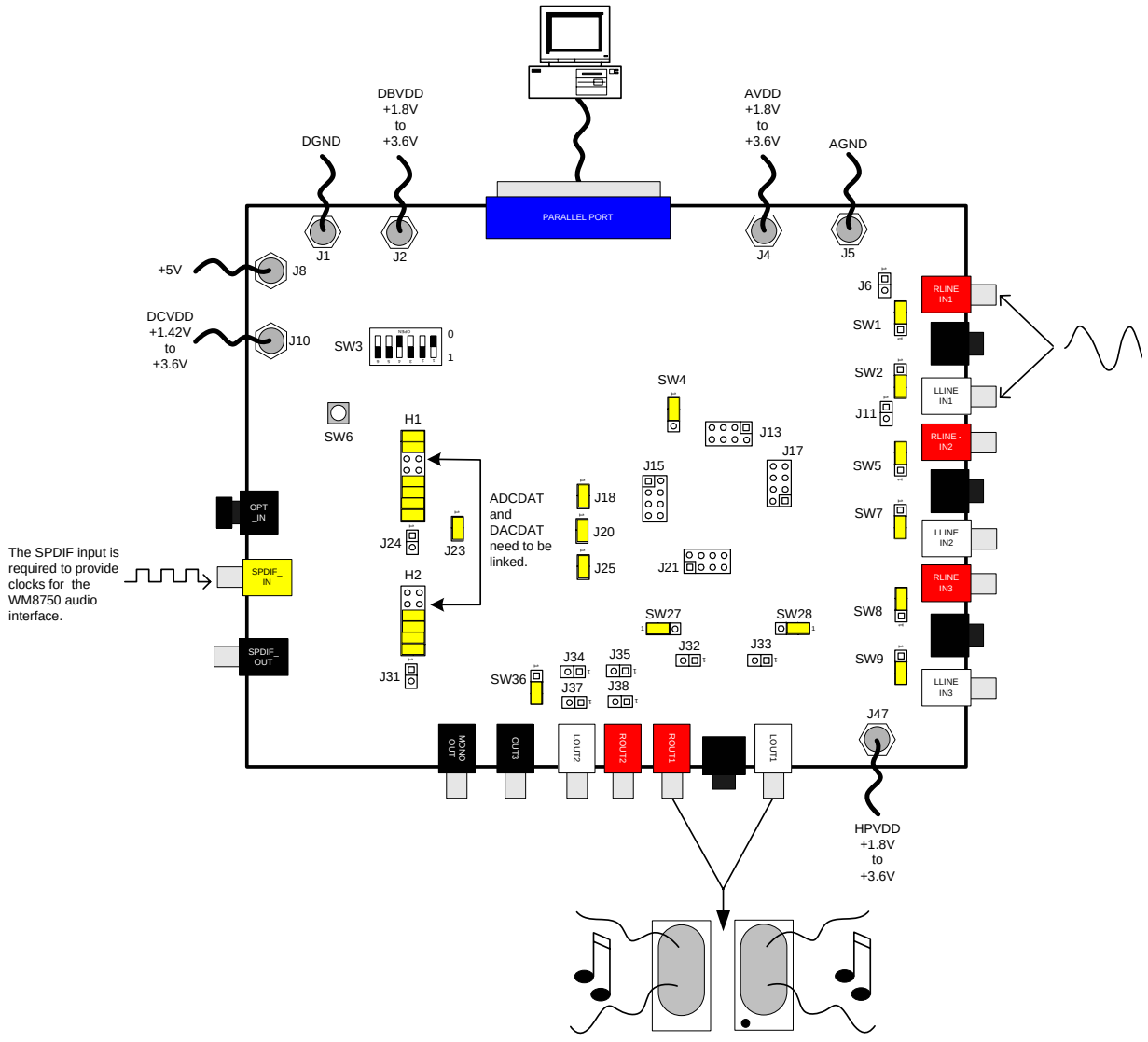

Figure 32 Recommended ADC to DAC Loopback Setup

Note: Pin 6 of H1 MUST be linked to pin 9 of H2. A digital input must also be applied to U3 or J19 so that the correct clocks are supplied to the WM8750.

LINKS AND JUMPERS	LINK/JUMPER STATUS	DESCRIPTION
H1	All jumpers in place except for links shorting pins 5 and 6 and 7 and 8.	DAC clocks and data input
H2	All jumpers in place except for links shorting pins 9 and 10 and 11 and 12.	ADC clocks and data output
SW36	Pins 2 and 3 SHORT	Connects to GND for HP output reference
J18 (BCLK)	SHORT	Slave mode
J20 (ADCLRC)	SHORT	Slave mode
J25 (DACLRC)	SHORT	Slave mode
J23	SHORT	Slave mode
J32, J33, J34 and J35	OPEN	OUT signals are AC coupled
SW3		1 2 3 4 5 6 DATA FORMAT 1 0 0 1 0 0 I^2S Compatible
SW4	Pins 1 and 2 SHORT	3-wire (SPI) Control Mode
SW1, SW2	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW5, SW7	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW8, SW9	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW27, SW28	Pins 2 and 3 SHORT	Line Output Select (Phono Socket)

Table 14 Loopback Setup Jumper Settings (Slave Mode)

SOFTWARE SETUP

1. Press the 'ADC Setup' button.
2. Open the Power Down Control panel and set the DAC and L/ROUT1 bits 'active'.
3. Open the ADC and DAC Control panel. Uncheck the DAC Mute button.
4. Open the Volume Control panel. Set the DAC and L/ROUT1 Volume Update buttons.
5. Open the Mixer Control panel. Set the Right DAC to Right Mixer and Left DAC to Left Mixer switches to 'Enable'.

CONNECTION OF AN 8Ω MONO SPEAKER

The WM8750-EV1 can be set up to drive an 8Ω mono speaker from the R/LOUT2 outputs. Figure 33 shows the setup required for a signal applied to the DAC signal path to be output on a speaker being driven from the phono connectors J41 and J42. As stated in Table 7, the speaker may also be attached to jumpers J37 and J38.

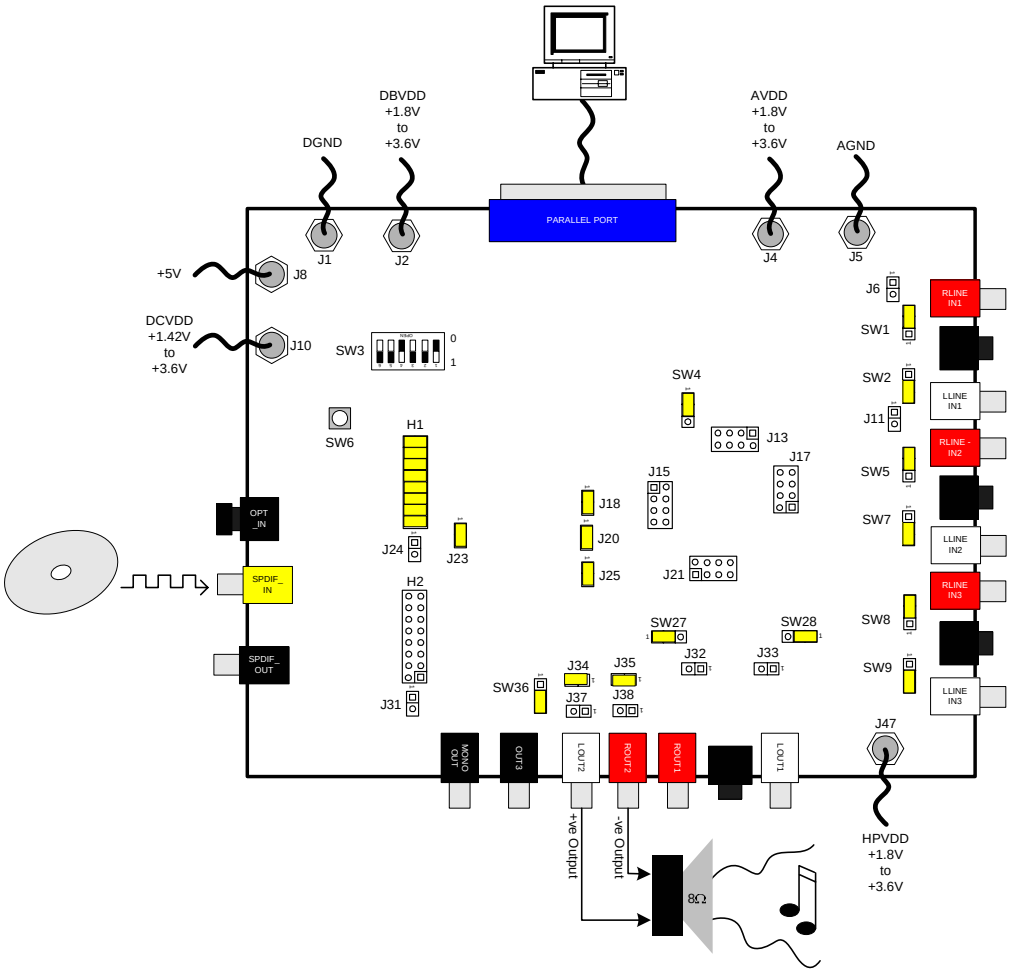

Figure 33 Recommended Mono Speaker Connection Setup

Note: LOUT2 = +ve output; ROUT2 = -ve output.

LINKS AND JUMPERS	LINK/JUMPER STATUS	DESCRIPTION
H1	All jumpers in place.	DAC clocks and data input
H2	No jumpers in place.	ADC clocks and data output
SW36	Pins 2 and 3 SHORT	Connects to GND for HP output reference
J18 (BCLK)	SHORT	Slave mode
J20 (ADCLRC)	SHORT	Slave mode
J25 (DACLRC)	SHORT	Slave mode
J23	SHORT	Slave mode
J32 and J33	OPEN	OUT signals are AC coupled
J34 and J35	SHORT	OUT signals are DC coupled
SW3		1 2 3 4 5 6 DATA FORMAT 1 0 0 1 0 0 I2S Compatible
SW4	Pins 1 and 2 SHORT	3-wire (SPI) Control Mode
SW1, SW2	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW5, SW7	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW8, SW9	Pins 2 and 3 SHORT	Line Input Select (Phono Socket)
SW27, SW28	Pins 2 and 3 SHORT	Line Output Select (Phono Socket)

Table 15 DAC to Mono Speaker Setup Jumper Settings (Slave Mode)

SOFTWARE SETUP

1. Press the 'DAC Setup' button.
2. Open the Mixer Control panel. Set the 'ROUT2 Invert' switch to Signal Inverted followed by the 'Mixer Submit' button.

HEADPHONE AUTO-DETECT FUNCTION

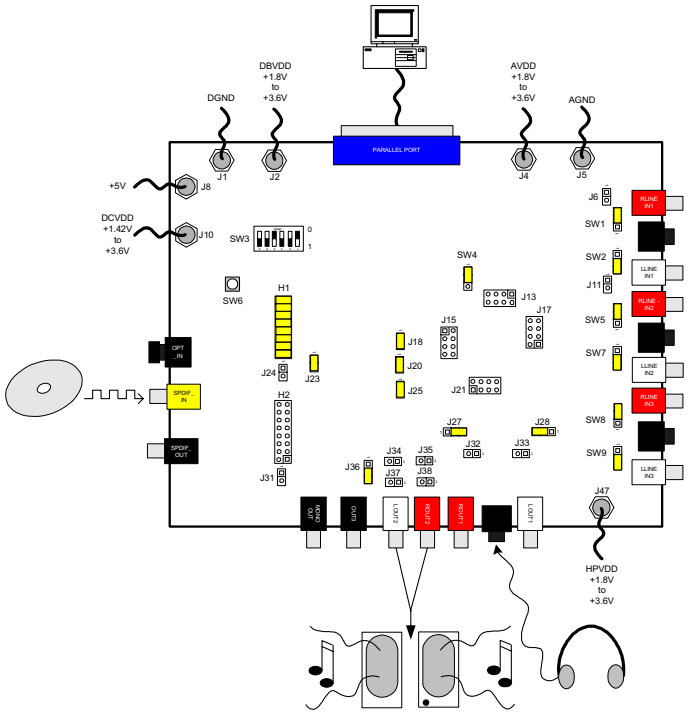

Figure 34 Headphone Auto Detect Setup

One of the features of the WM8750 is a headphone auto-detect function. This can be enabled on the WM8750-EV1B by the making the following hardware and software settings.

HARDWARE SETUP

1. Designator R50 should be populated with a 0R resistor.
2. Switch SW8 should be set to the OFF (centre) position.
3. Designator R49 should be populated with a 47K resistor.
4. Connect speakers to the R/LOUT2 outputs.
5. For this recommended setup the rest of the jumper and switch settings should be as shown in Table 7.

SOFTWARE SETUP

1. Press the 'DAC Setup' button.
2. Open the Tone Control panel and set the 'Headphone Switch' to Enable. Press the Tone Submit button.

The headphone auto-detect function should now be active. With no headphone connected to the 3.5mm jack socket (J46) audio should be output from the speakers connected to R/LOUT2. When the headphone is plugged into 3.5mm jack socket (J46), the audio should not be output from the speakers connected to R/LOUT2 and only be output from the headphones.

Refer to the WM8750 datasheet for further details of this, and all other functions offered by the WM8750.

EVALUATION SUPPORT

The aim of this evaluation kit is to help you to become familiar with the functionality and performance of the WM8750 CODEC.

If you require more information or require technical support please contact Wolfson Microelectronics Applications group through the following channels:

Email: apps@wolfsonmicro.com

Telephone Apps: (+44) 131 272 7070

Fax: (+44) 131 272 7001

Mail: Applications Department at address on last page.

or contact your local Wolfson representative.

Additional information may be made available from time to time on our web site at http://www.wolfsonmicro.com

IMPORTANT NOTICE

Wolfson Microelectronics plc (WM) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current. All products are sold subject to the WM terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

WM warrants performance of its products to the specifications applicable at the time of sale in accordance with WM's standard warranty. Testing and other quality control techniques are utilised to the extent WM deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

In order to minimise risks associated with customer applications, adequate design and operating safeguards must be used by the customer to minimise inherent or procedural hazards. Wolfson products are not authorised for use as critical components in life support devices or systems without the express written approval of an officer of the company. Life support devices or systems are devices or systems that are intended for surgical implant into the body, or support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided, can be reasonably expected to result in a significant injury to the user. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

WM assumes no liability for applications assistance or customer product design. WM does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of WM covering or relating to any combination, machine, or process in which such products or services might be or are used. WM's publication of information regarding any third party's products or services does not constitute WM's approval, license, warranty or endorsement thereof.

Reproduction of information from the WM web site or datasheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

Resale of WM's products or services with statements different from or beyond the parameters stated by WM for that product or service voids all express and any implied warranties for the associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

ADDRESS:

Wolfson Microelectronics plc

Westfield House

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: apps@wolfsonmicro.com