Ordering number : ENN7304

Thick-Film Hybrid IC

STK672-330

Unipolar Fixed-Current Chopper (External-Excited PWM) Scheme and Built-in Phase Signal Distribution IC

Two-Phase Stepping Motor Driver (Square Wave Drive) Output Current: 1.8 A

Overview

The STK672-330 is a unipolar fixed-current chopper type 2-phase stepping motor driver hybrid IC. It features power MOSFETs in the output stage and a built-in phase signal distribution IC. The incorporation of a phase distribution IC allows the STK672-330 to control the speed of the motor based on the frequency of an external input clock signal. It supports two types of excitation for motor control: 2-phase excitation and 1-2 phase excitation. It also provides a function for switching the motor direction. The STK672-330 features an ENABLE pin, a function not provided in the STK672-110. When the ENABLE pin is set low while the clock signal is being supplied, all MOSFET devices are forced to the off state. When ENABLE is set high again later, the IC resumes operation, continuing with the prior excitation timing.

Applications

- Two-phase stepping motor drive in send/receive facsimile units
- Paper feed in copiers, industrial robots, and other applications that require 2-phase stepping motor drive

Features

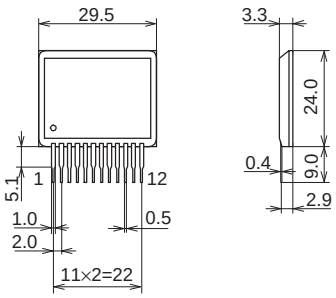
- The motor speed can be controlled by the frequency of an external clock signal (the CLOCK pin signal).
- The excitation type is switched according to the state (low or high) of the MODE pin. The mode is set to 2-phase or 1-2 phase excitation on the rising edge of the clock signal.
- A motor direction switching pin (the CWB pin) is provided.
- All inputs are Schmitt inputs.
- The motor current can be set by changing the Vref pin voltage. Since a 0.195-Ω current detection resistor is built in, a current of 1 A is set for each 0.195 V of applied voltage.
- The input frequency range for the clock signal used for motor speed control is 0 to 50 kHz.
- Supply voltage ranges: $V_{CC}1$ = 10 to 42 V, $V_{CC}2$ = 5.0 V ±5%
- This IC supports motor operating currents of up to 1.8 A at Tc = 105°C, and of up to 2.65 A at Tc = 25°C.
- Provides a function that, during clock input, forces all MOSFET devices to the off state when the ENABLE pin is set low, and then, when ENABLE is set high, resumes operation continuing with the prior excitation timing.

Package Dimensions

unit: mm

4192

[STK672-330]



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Specifications

Maximum Rating at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC} max	No signal	52	V
Maximum supply voltage 2	V_{DD} max	No signal	–0.3 to +7.0	V
Input voltage	V_{IN} max	Logic input pins	–0.3 to +7.0	V
Output current	I_{OH} max	V_{DD} = 5 V, CLOCK ≥ 200 Hz	2.65	A
Repeated avalanche capacity	Ear max		28	mJ
Power loss	Pd max	With an arbitrarily large heat sink. Per MOSFET	6.5	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

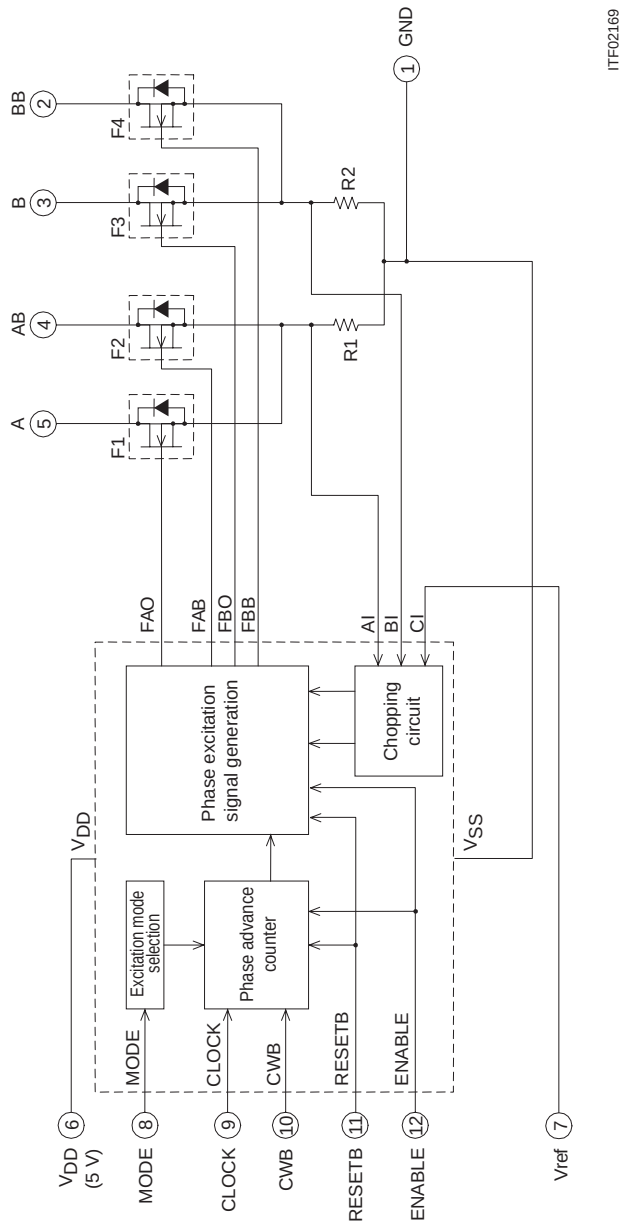
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}	With signals applied	10 to 42	V
Supply voltage 2	V_{DD}	With signals applied	5.0 ± 5%	V
Input voltage	V_{IH}		0 to V_{DD}	V
Phase current 1	$I_{OH}1$	Tc = 105°C, CLOCK ≥ 200 Hz	1.8	A
Phase current 2	$I_{OH}2$	Tc = 80°C, CLOCK ≥ 200 Hz See the motor current (I_{OH}) derating curve	2.1	A
Clock frequency	f_{CL}	Minimum pulse width: at least 10 µs	0 to 50	kHz
Phase driver withstand voltage	V_{DSS}	I_D = 1 mA (Tc = 25°C)	100 min	V
Recommended operating substrate temperature range	Tc	No condensation	0 to 105	°C

Electrical Characteristics at Tc = 25°C, V_{CC} = 24 V, V_{DD} = 5 V

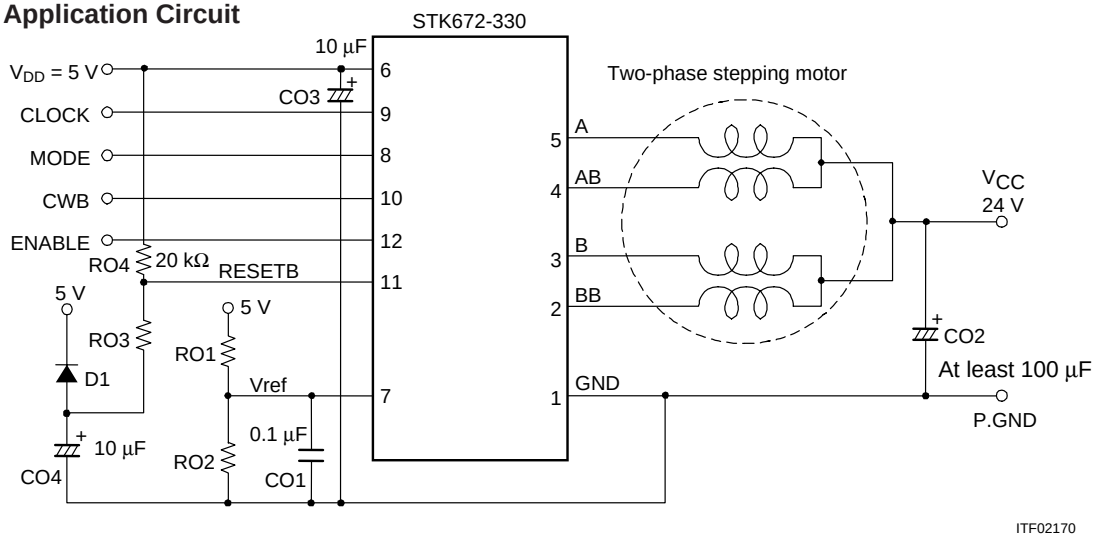
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{DD} supply current	I_{CCO}	CLOCK = GND		3.1	7	mA
Output current	I_{oave}	With R/L = 3 Ω/3.8 mH in each phase Vref = 0.137 V	0.36	0.40	0.44	A
FET diode forward voltage	Vdf	If = 1 A (R_L = 23 Ω)		1.2	1.8	V
Output saturation voltage	Vsat	R_L = 23 Ω		0.70	1.00	V
High-level input voltage	V_{IH}	Pins 8 to 12 (5 pins)	2.5			V
Low-level input voltage	V_{IL}	Pins 8 to 12 (5 pins)			0.6	V
Input current	I_{IL}	With pins 8 to 12 at the ground level.			10	µA
Vref input voltage	VrH	Pin 7	0		3.5	V
Vref input bias current	I_{IB}	With pin 7 at 1 V		50	500	nA
PWM frequency	fc		35	45	55	kHz

Note: A fixed-voltage power supply must be used.

Internal Equivalent Circuit Block Diagram



Sample Application Circuit



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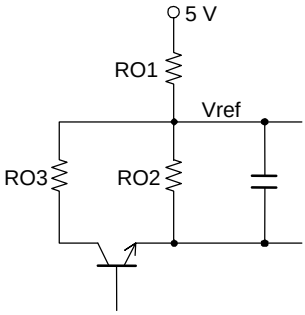
- To minimize noise in the 5-V system, locate the ground side of capacitor CO2 in the above circuit as close as possible to pin 1 of the IC. Also, if at all possible, the ground used for Vref must not be common to the P.GND pattern, but must be directly wired from pin 1.
- Insert resistor RO3 (47 to 100 Ω) so that the discharge energy from capacitor CO4 is not directly applied to the CMOS IC in this hybrid device. If the diode D1 has Vf characteristics with Vf less than or equal to 0.6 V (when If = 0.1 A), this will be smaller than the CMOS IC input pin diode Vf. If this is the case RO3 may be replaced with a short without problem.
- Both TTL and CMOS levels are used for the pin 8, 9, 10, 11 and 12 inputs.
- Since the input pins do not have built-in pull-up resistors, when the open-collector type pins 8, 9, 10, 11, and 12 are used as inputs, a 10 to 47 kΩ pull-up resistor (to V_{DD}) must be used.
- To prevent incorrect operation due to chopping noise, we recommend inserting 470 to 1000 pF capacitors between pin 1 and each of the pins 8, 9, 10, and 12.

(With the open-collector type IC, we also recommend inserting a 470 to 1000 pF capacitor between pin 11 (RESETB) and pin 1 when pin 11 is used as an input.)

- The following circuit (for a lowered current of over 0.2 A) is recommended if the application needs to temporarily lower the motor current. Here, a value of close to 100 kΩ must be used for resistor RO1 to make the transistor output saturation voltage as low as possible.



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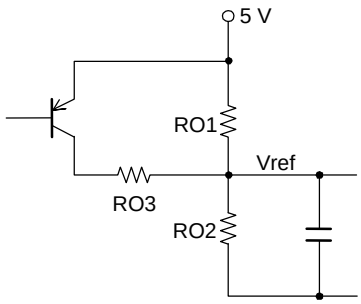

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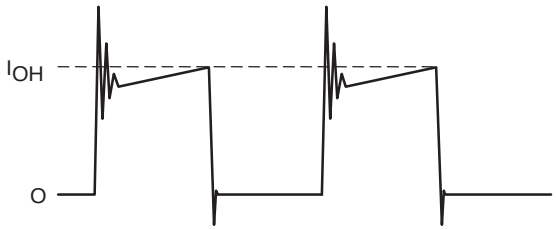
- Motor current peak value I_{OH} setting



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I_{OH} = Vref ÷ Rs
Vref = (R02 ÷ (R01 + R02)) × 5 V (or 3.3 V)
Rs is the hybrid IC internal current detection resistor.
In the STK672-330 (and STK672-350) Rs is 0.195 Ω.
(In the STK672-340 and STK672-360, Rs is 0.14 Ω.)

Input Pin Functions (TTL input levels)

Pin	Pin No.	Function	Input conditions when operating
CLOCK	9	Reference clock for motor phase current switching	Operates on the rising edge of the signal
MODE	8	Excitation mode selection	Low: 2-phase excitation High: 1-2 phase excitation
CWB	10	Motor direction switching	Low: CW (forward) High: CCW (reverse)
RESETB	11	System reset and A, AB, B, and BB outputs cutoff. Applications must apply a reset signal for at least 10 µs when V_{DD} is first applied.	A reset is applied by a low level
ENABLE	12	The A, AB, B, and BB outputs are turned off, and after operation is restored by returning the ENABLE pin to the high level, operation continues with the same excitation timing as before the low-level input.	The A, AB, B, and BB outputs are turned off by a low-level input.

- A simple reset function is formed from D1, CO4, RO3, and RO4 in this application circuit. With the CLOCK input held low, when the 5-V supply voltage is brought up a reset is applied if the motor output phases A and BB are driven. If the 5-V supply voltage rise time is slow (over 50 ms), the motor output phases A and BB may not be driven. Increase the value of the capacitor CO4 and check circuit operation again.
- See the timing chart for the concrete details on circuit operation.

Usage Notes

- STK672-330 input signal functions and timing (Specifications common to the STK672-340, 350, and 360 as well)
  (All inputs have no internal pull-up resistor and are TTL level Schmitt trigger inputs.)
  [RESETB and CLOCK (Input signal timing when power is first applied)]
  As shown in the timing chart, a RESETB signal input is required by the driver to operate with the timing in which the F1 gate is turned on first. The RESETB signal timing must be set up to have a width of at least 10 µs, as shown below. The capacitor CO4, and the resistors RO3 and RO4 in the application circuit form simple reset circuit that uses the RC time constant rising time. However, when designing the RESETB input based on V_{IH} levels, the application must have the timing shown in figure 1.

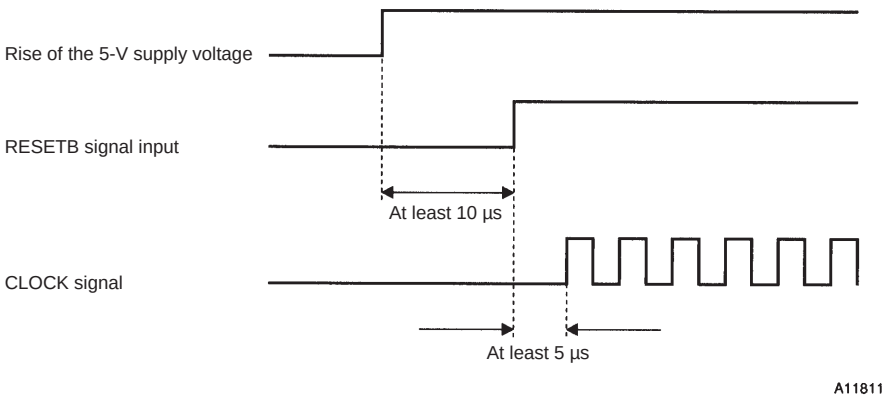


Figure 1 RESETB and CLOCK Signals Input Timing

Note: In the STK672-350 and 360, the RESETB signal must be input at least 10 μs after the rise of the motor power supply VCC level (10 V, minimum), not after the rise of the 5 V power supply (4.5 V, minimum).

CLOCK (Phase switching clock)
- Input frequency: DC to 50 kHz
- Minimum pulse width: 10 μs
- Signals are read on the rising edge.

CWB (Motor direction setting)
The direction of rotation is switched by setting CWB to 1 (high) or 0 (low). See the timing charts for details on the operation of the outputs.
Note: The state of the CWB input must not be changed during the 6.25 μs period before and after the rising edge of the CLOCK input.

ENABLE (Forcible on/off control of the A, AB, B, and BB outputs, and selection of the operate or hold state for hybrid IC internal operation)
ENABLE = 1 (high): Normal operation
ENABLE = 0 (low): Outputs A, AB, B, and BB forced to the off state.
If, during the state where CLOCK signal input is provided, the ENABLE pin is set to 0 (low) and then is later restored to the 1 (high) state, the IC will resume operation with the excitation timing continued from before the point ENABLE was set to 0 (low).

MODE (Excitation mode selection)
MODE = 0 (low): 2-phase excitation
MODE = 1 (high): 1-2 phase excitation
See the timing charts for details on output operation in these modes.
Note: The state of the MODE input must not be changed during the 5 μs period before and after the rising edge of the CLOCK input.

- Allowable motor current operating range
  The motor current (I_O) must be held within the range corresponding to the area under the curve shown in figure 3.
  For example, if the operating substrate temperature Tc is 105°C, then I_O must be held under I_O max = 1.8 A, and in hold mode I_O must be held under I_O max = 1.5 A.

• Thermal design

[Operating range in which a heat sink is not used]

The STK672-330 package has a structure that uses no screws, and is recommended for use without a heat sink. This section discusses the safe operating range when no heat sink is used.

In the maximum ratings specifications, Tc max is specified to be 105°C, and when mounted in an actual end product system, the Tc max value must never be exceeded during operation. Tc can be expressed by formula (A) below, and thus the range for ΔTc must be stipulated so that Tc is always under 105°C.

$Tc = Ta + \Delta Tc$ (A)

Ta: Hybrid IC (H-IC) ambient temperature, ΔTc: Temperature increase across the aluminum substrate

As shown in figure 5, the value of ΔTc increases as the hybrid IC internal average power dissipation P_D increases.

As shown in figure 4, P_D increases with the motor current. Here we describe the actual P_D calculation using the example shown in the motor current timing chart in figure 2.

Since there are periods when current flows and periods when the current is off during actual motor operation, P_D cannot be determined from the data presented in figure 4. Therefore, we calculate P_D assuming that actual motor operation consists of repetitions of the operation shown in figure 2.

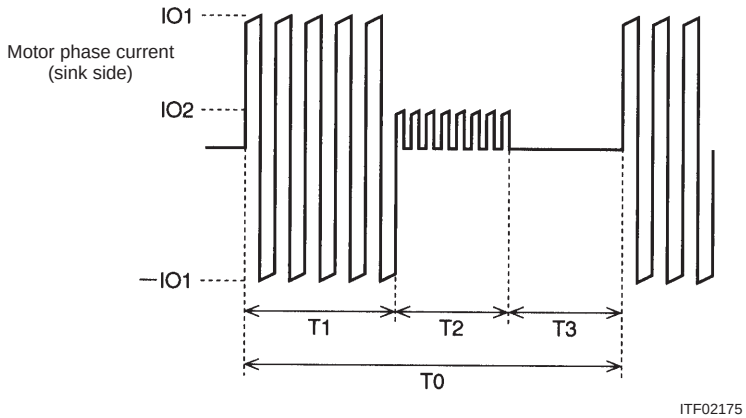


Figure 2. Motor Current Timing

T1: Motor rotation operation time
T2: Motor hold operation time
T3: Motor current off time
T2 may be reduced, depending on the application.
T0: Single repeated motor operating cycle
IO1 and IO2: Motor current peak values
Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.
Note that figure 2 presents the concepts here, and that the on/off duty of the actual signals will differ.

The hybrid IC (H-IC) internal average power dissipation P_D can be calculated from the following formula.

$P_D = (T1 \times P1 + T2 \times P2 + T3) \div T0$ (I)

(Here, P1 is the P_D for IO1 and P2 is the P_D for IO2)

If the value calculated in formula (I) above is under 1.5 W, then from figure 5 we see that operation is allowed up to an ambient temperature Ta of 60°C.

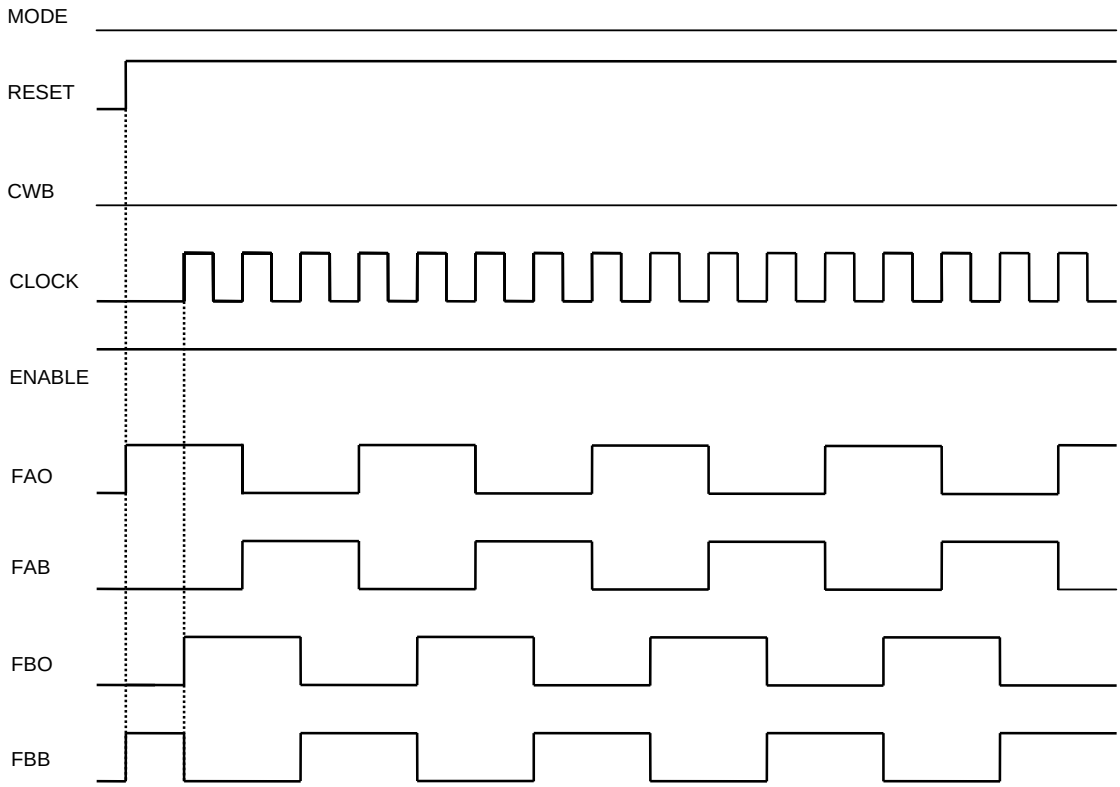
While the operating range when a heat sink is not used can be determined from formula (I) above, figure 4 is merely a single example of one operating mode for a single motor.

For example, while figure 4 shows a 2-phase excitation motor, if 1-2 phase excitation is used with a 500-Hz clock frequency, the drive will be turned off for 25% of the time and the dissipation P_D will be reduced to 75% of that in figure 4.

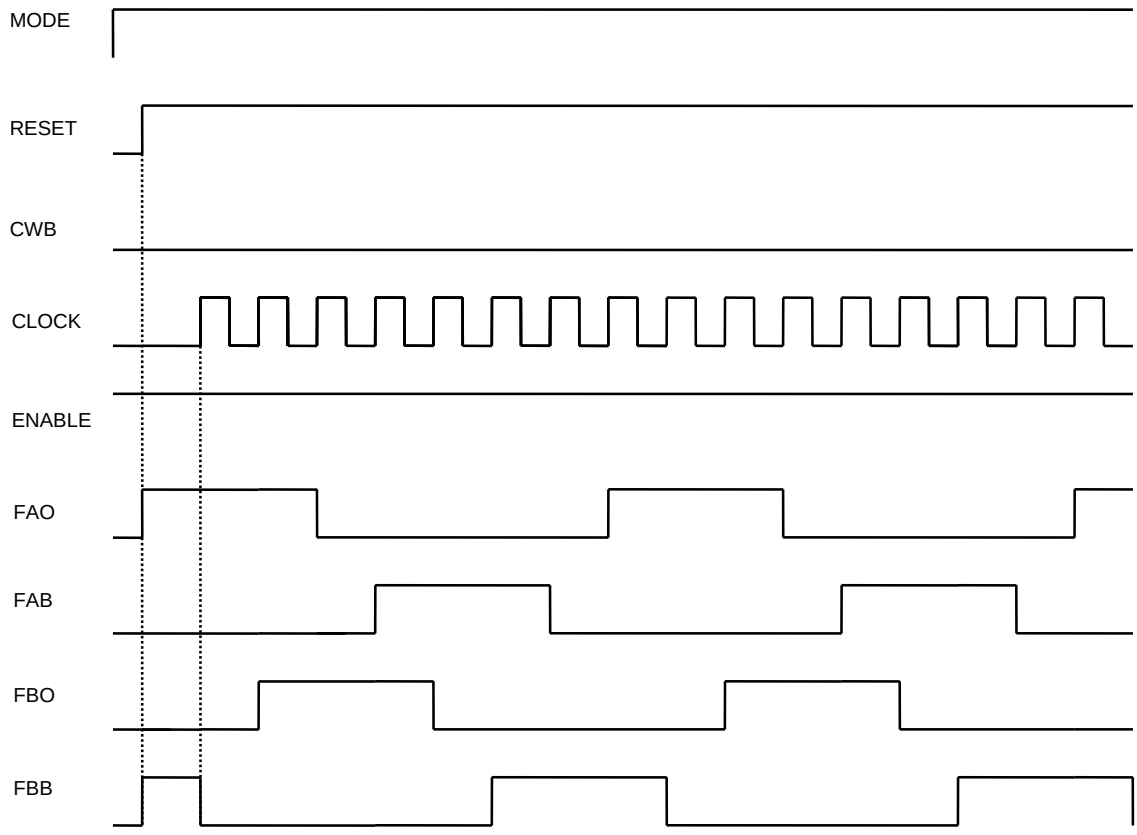
It is extremely difficult for SANYO to calculate the internal average power dissipation P_D for all possible end product conditions. After performing the above rough calculations, always install the hybrid IC (H-IC) in an actual end product and verify that the substrate temperature Tc does not rise above 105°C.

Timing Chart

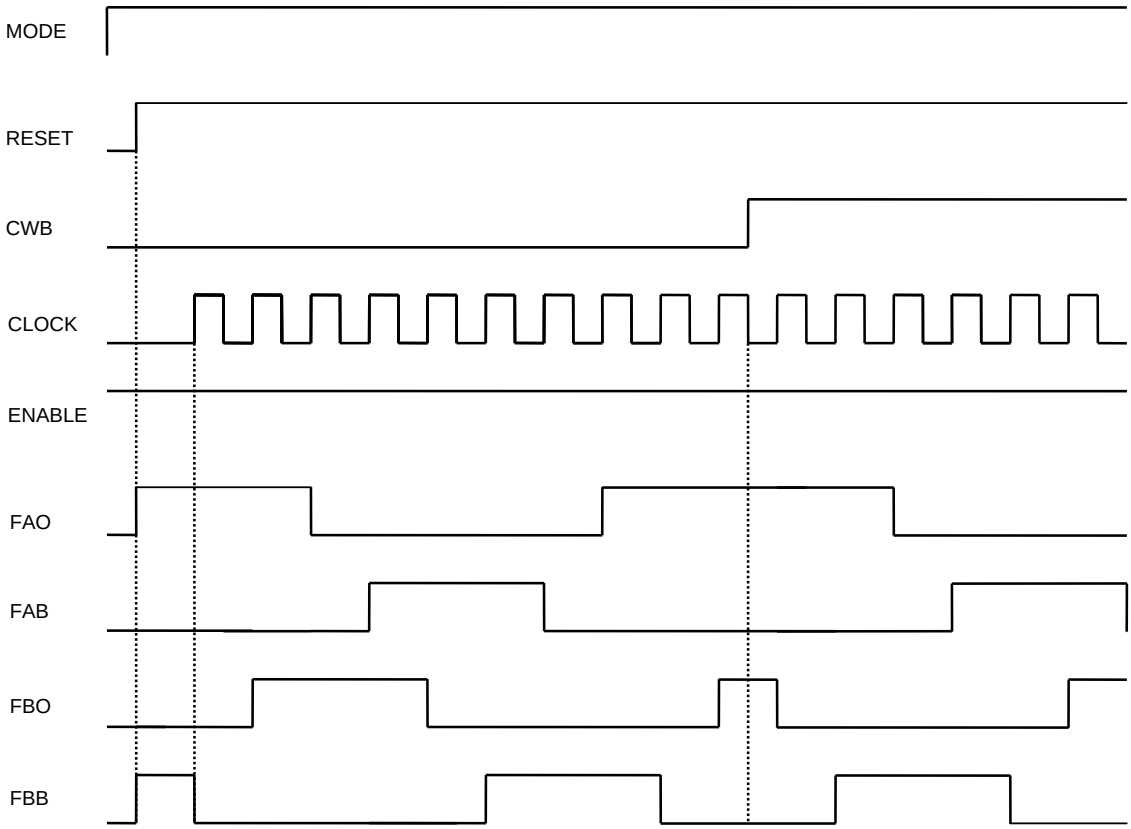
2-phase excitation



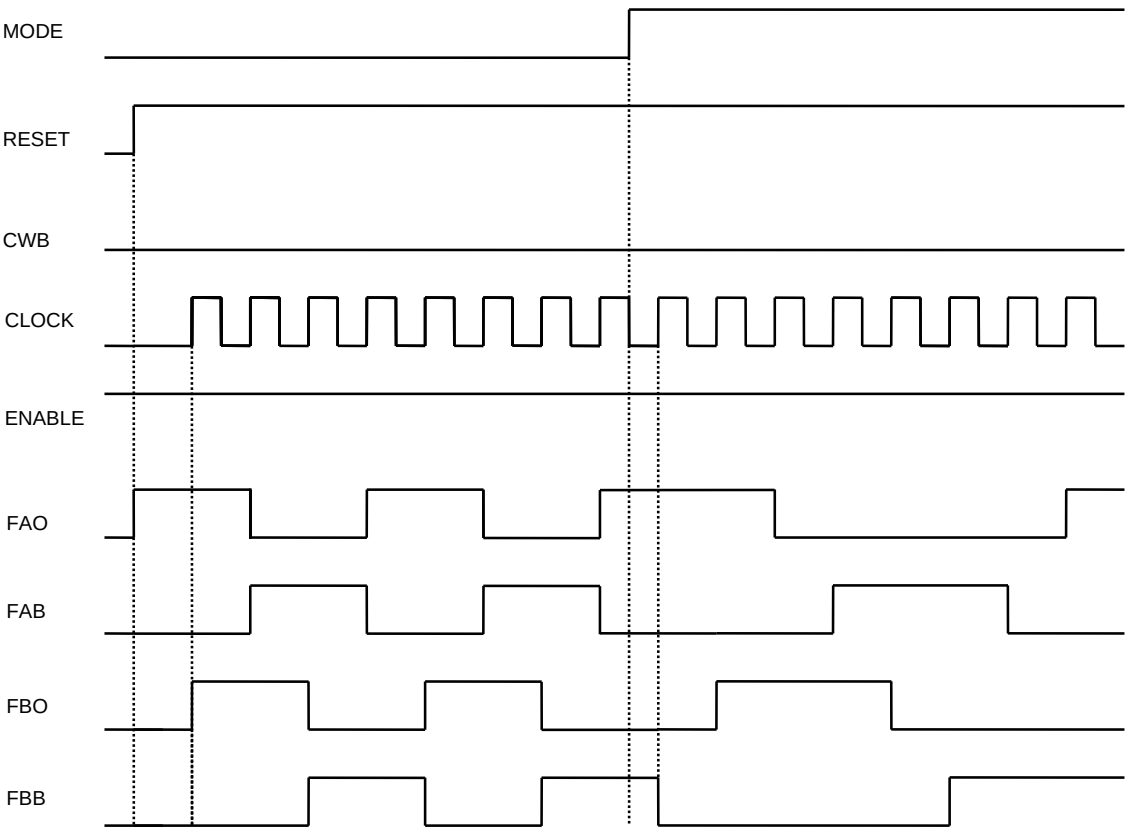
1-2 phase excitation



1-2 phase excitation (CWB)



Switching from 2-phase to 1-2 phase excitation



1-2 phase excitation (ENABLE)

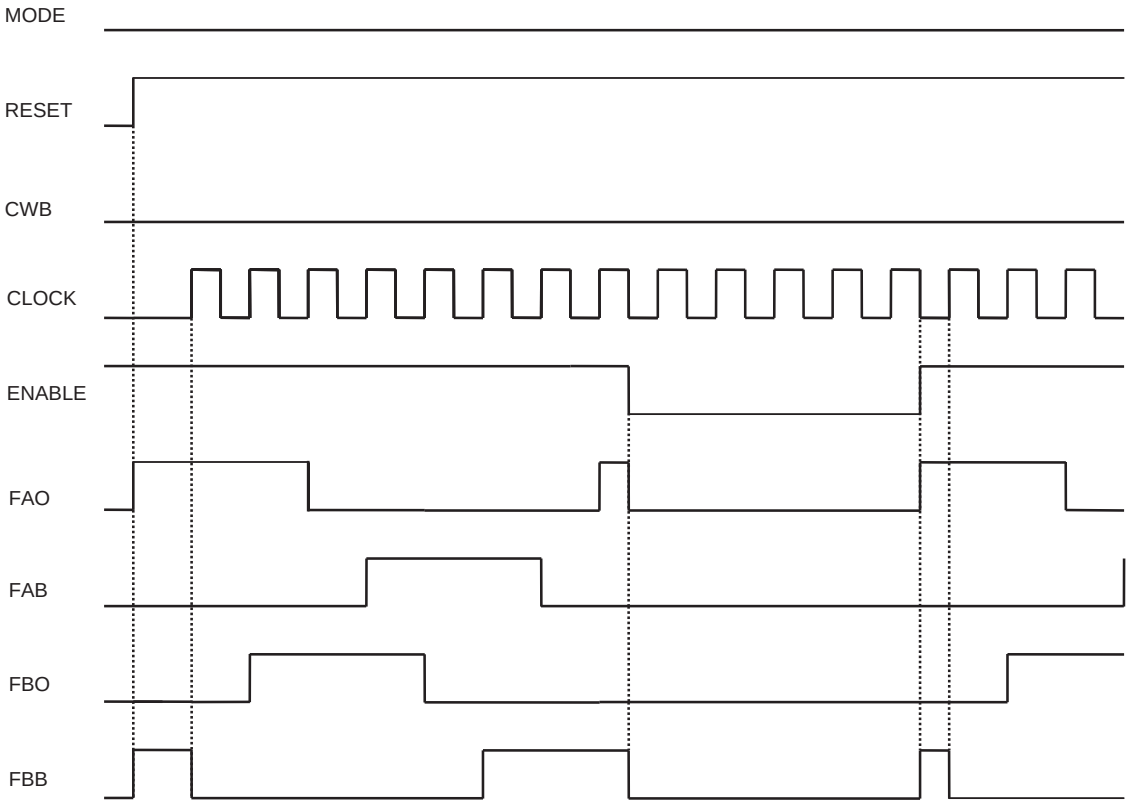


Figure 3

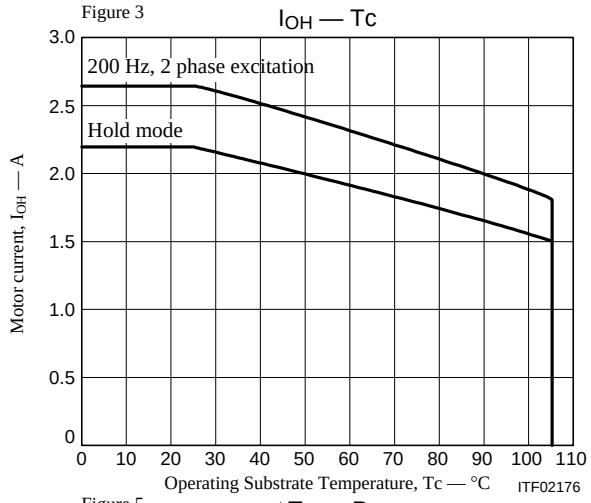


Figure 4

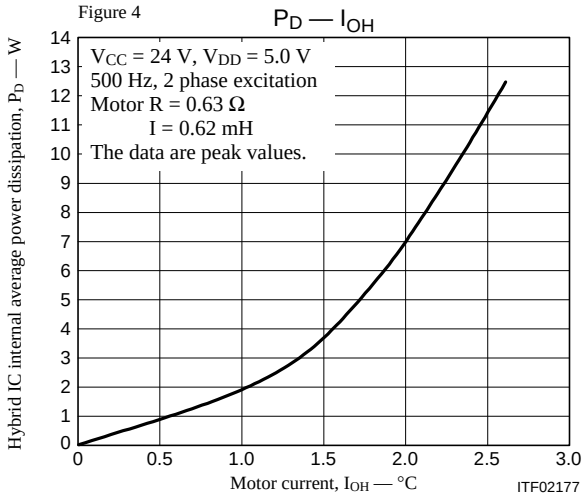


Figure 5