

# 433MHz Single Chip RF Transceiver **nRF401**

## FEATURES

- True single chip FSK transceiver
- Few external components required
- No set up or configuration
- No coding of data required
- 20kbit/s data rate
- 2 channels
- Wide supply range
- Very low power consumption
- Standby mode

## APPLICATIONS

- Alarm and Security Systems
- Automatic Meter Reading (AMR)
- Home Automation
- Remote Control
- Surveillance
- Automotive
- Telemetry
- Toys
- Wireless Communication

## GENERAL DESCRIPTION

nRF401 is a true single chip UHF transceiver designed to operate in the 433MHz ISM (Industrial, Scientific and Medical) frequency band. It features Frequency Shift Keying (FSK) modulation and demodulation capability. nRF401 operates at bit rates up to 20kbit/s. Transmit power can be adjusted to a maximum of 10dBm. Antenna interface is differential and suited for low cost PCB antennas. nRF401 features a standby mode which makes power saving easy and efficient. nRF401 operates from a single +3-5V DC supply.

As a primary application, nRF401 is intended for UHF radio equipment in compliance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1 V1.2.1.

## QUICK REFERENCE DATA

Parameter	Value	Unit
Frequency, Channel#1/Channel#2	433.92 / 434.33	MHz
Modulation	FSK	
Frequency deviation	±15	kHz
Max. RF output power @ 400Ω, 3V	10	dBm
Sensitivity @ 400Ω, BR=20 kbit/s, BER<10 <sup>-3</sup>	-105	dBm
Maximum bit rate	20	kbit/s
Supply voltage	2.7 – 5.25	V
Receive supply current	250*	μA
Transmit supply current @ -10 dBm output power	8	mA
Standby supply current	8	μA

Table 1. nRF401 quick reference data.

## ORDERING INFORMATION

Type number	Description	Version
nRF401-IC	20 pin SSOIC	A
nRF401-EVKIT	Evaluation kit with nRF401 IC	1.0

Table 2. nRF401 ordering information.

\* The PWR\_UP pin is used for power duty cycling. The duty-cycle is 2 % with a period of 200msec.



**BLOCK DIAGRAM**

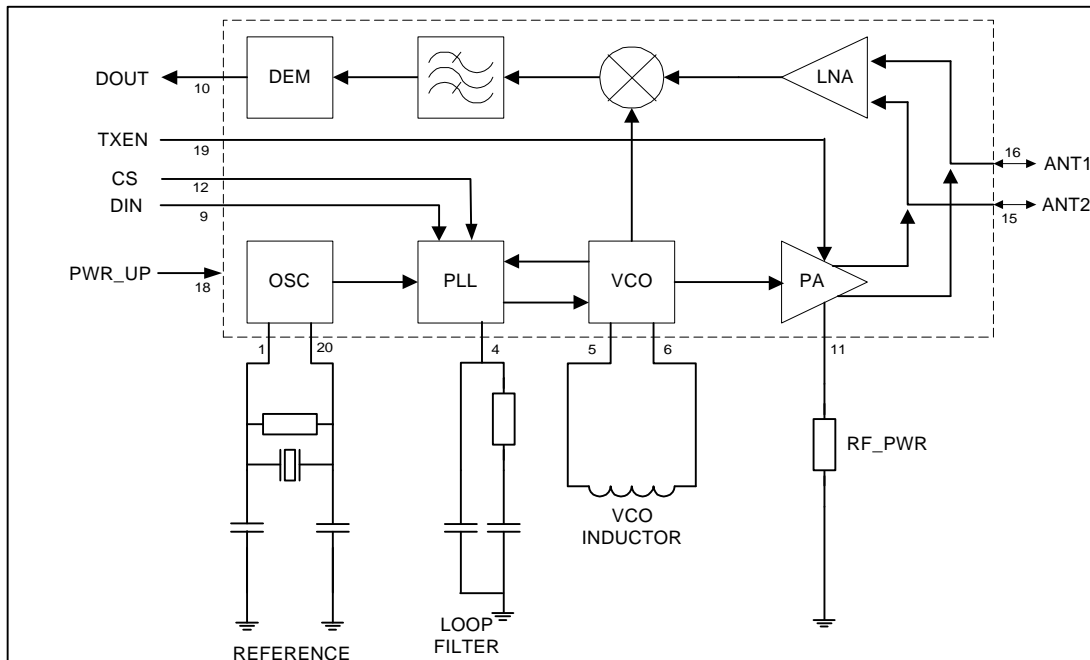


Figure 1. nRF401 block diagram with external components.

**PIN FUNCTIONS**

Pin	Name	Pin function	Description
1	XC1	Input	Crystal oscillator input
2	VDD	Power	Power supply (+3-5V DC)
3	VSS	Ground	Ground (0V)
4	FILT1	Input	Loop filter
5	VCO1	Input	External inductor for VCO
6	VCO2	Input	External inductor for VCO
7	VSS	Ground	Ground (0V)
8	VDD	Power	Power supply (+3-5V DC)
9	DIN	Input	Data input
10	DOUT	Output	Data output
11	RF_PWR	Input	Transmit power setting
12	CS	Input	Channel selection CS="0" ⇒ 433.92MHz (Channel#1) CS="1" ⇒ 434.33MHz (Channel#2)
13	VDD	Power	Power supply (+3-5V DC)
14	VSS	Ground	Ground (0V)
15	ANT2	Input/Output	Antenna terminal
16	ANT1	Input/Output	Antenna terminal
17	VSS	Ground	Ground (0V)
18	PWR_UP	Input	Power on/off PWR_UP = "1" ⇒ Power up (Operating mode) PWR_UP = "0" ⇒ Power down (Standby mode)
19	TXEN	Input	Transmit enable TXEN = "1" ⇒ Transmit mode TXEN = "0" ⇒ Receive mode
20	XC2	Output	Crystal oscillator output

Table 3. nRF401 pin functions.



**nRF401 Single Chip RF Transceiver**

**ELECTRICAL SPECIFICATIONS**

Conditions: V<sub>DD</sub> = +3V DC, V<sub>SS</sub> = 0V, T<sub>A</sub> = -25°C to +85°C

Symbol	Parameter (condition)	Min.	Typ.	Max.	Units
V <sub>DD</sub>	Supply voltage	2.7	3	5.25	V
V <sub>SS</sub>	Ground		0		V
I <sub>DD</sub>	Total current consumption				
	Receive mode		11		mA
	Transmit mode @ -10 dBm RF power		8		mA
	Stand by mode		8		µA
P <sub>RF</sub>	Max. RF output power @ 400Ω load		10		dBm
V <sub>IH</sub>	Logic "1" input voltage	0.7·V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>IL</sub>	Logic "0" input voltage	0		0.3·V <sub>DD</sub>	V
V <sub>OH</sub>	Logic "1" output voltage (I <sub>OH</sub> = - 1.0mA)	0.7·V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>OL</sub>	Logic "0" output voltage (I <sub>OL</sub> = 1.0mA)	0		0.3·V <sub>DD</sub>	V
I <sub>H</sub>	Logic "1" input current (V <sub>I</sub> = V <sub>DD</sub> )			+20	µA
I <sub>L</sub>	Logic "0" input current (V <sub>I</sub> = V <sub>SS</sub> )			-20	µA
f <sub>1</sub>	Channel#1 frequency		433.92		MHz
f <sub>2</sub>	Channel#2 frequency		434.33		MHz
	Dynamic range	90			dB
	Modulation type		FSK		
Δf	Frequency deviation		±15		kHz
f <sub>IF</sub>	IF frequency		400		kHz
BW <sub>IF</sub>	IF bandwidth	65		85	kHz
f <sub>X<sub>TAL</sub></sub>	Crystal frequency		4.0		MHz
	Crystal frequency stability requirement <sup>1)</sup>			±45	ppm
	Sensitivity @ 400Ω, BR=20 kbit/s, BER < 10 <sup>-3</sup>		-105		dBm
	Bit rate	0		20	kbit/s
Z <sub>I</sub>	Recommended antenna port differential impedance		400		Ω
	Spurious emission	Compliant with EN 300-220-1 V1.2.1 <sup>2)</sup>			

Table 4. nRF401 electrical specifications.

<sup>1)</sup> Maximum 5dB sensitivity degradation at temperature extremes. See also page 11.

<sup>2)</sup> With a PCB loop antenna or a differential to single ended matching network to a 50Ω antenna.

**ABSOLUTE MAXIMUM RATINGS**

**Supply voltages**

V<sub>DD</sub> ..... - 0.3V to +6V

V<sub>SS</sub> ..... 0V

**Power dissipation**

P<sub>D</sub> (T<sub>A</sub>=25°C)..... 250mW

**Input voltage**

V<sub>I</sub>..... - 0.3V to V<sub>DD</sub> + 0.3V

**Temperatures**

Operating Temperature.... -25°C to +85°C

Storage Temperature..... -40°C to +125°C

**Output voltage**

V<sub>O</sub>..... - 0.3V to V<sub>DD</sub> + 0.3V

*Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.*



**ATTENTION!**

Electrostatic Sensitive Device  
Observe Precaution for handling



**PIN ASSIGNMENT**

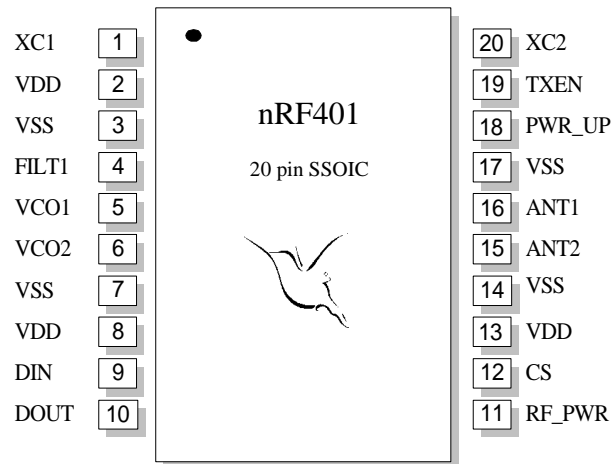
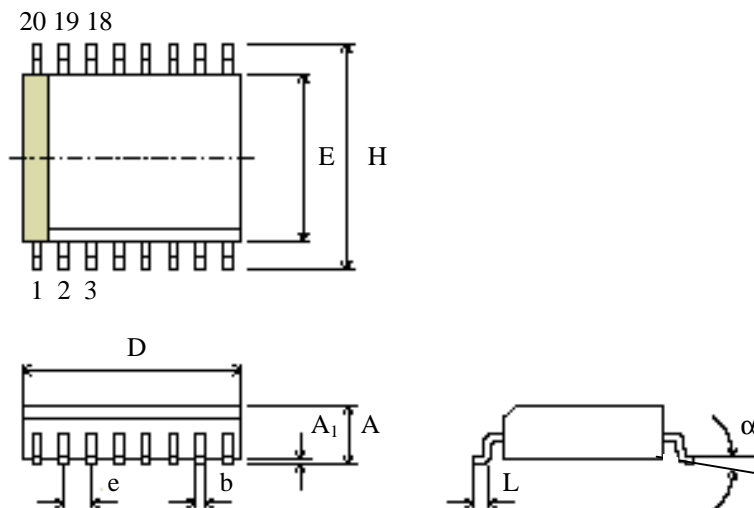


Figure 2. nRF401 pin assignment.

**PACKAGE OUTLINE**

nRF401, 20 pin SSOIC. (Dimensions in mm.)



Package Type		D	E	H	A	A <sub>1</sub>	e	b	L	Copl.	α
20 pin SSOIC (Wide)	Min	6.90	5.00	7.40		0.05	0.65	0.22	0.55	0.10	0°
	Max	7.50	5.60	8.20	2.00			0.38	0.95		8°

Figure 3. SSOIC-20 Package outline.



## IMPORTANT TIMING DATA

### Timing information

The timing information for the different operations is summarised in Table 5. (TX is transmit mode, RX is receive mode and Std.by is Standby mode.)

Change of Mode	Name	Max Delay	Condition
TX → RX	$t_{TR}$	3ms	Operational mode
RX → TX	$t_{RT}$	1ms	
Std.by → TX	$t_{ST}$	2ms	
Std.by → RX	$t_{SR}$	3ms	
$V_{DD}=0 \rightarrow TX$	$t_{VT}$	4ms	Start-up
$V_{DD}=0 \rightarrow RX$	$t_{VR}$	5ms	

Table 5 Switching times for nRF401.

### Switching TX ↔ RX (operational mode).

When switching from RX-mode to TX-mode data (DIN) may not be sent before the TXEN-input has been high for at least 1ms, see Figure 4(a).

When switching from TX-mode to RX-mode the receiver may not receive data (DOUT) before the TXEN-input has been low for at least 3ms, see Figure 4(b).

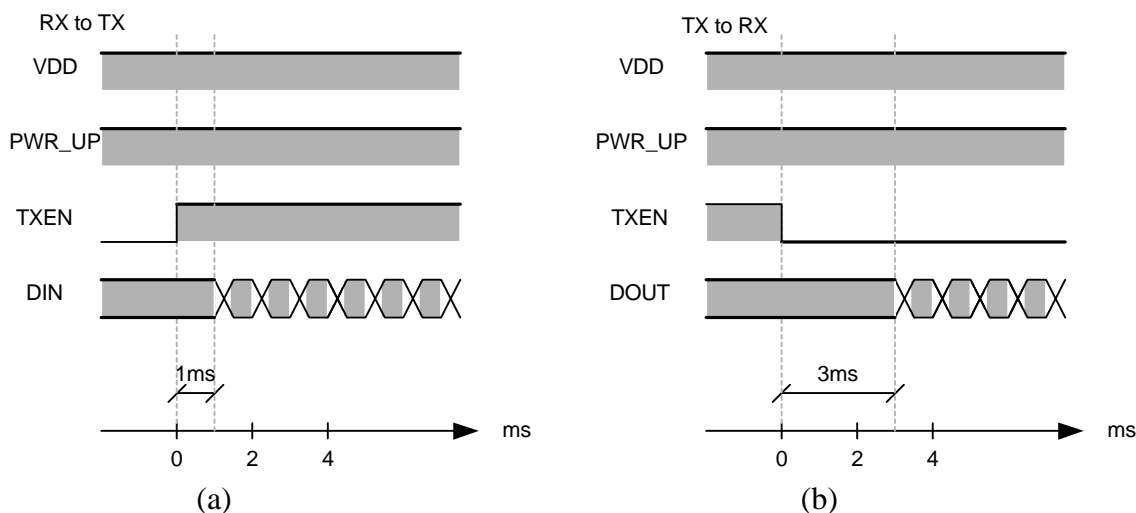


Figure 4. Timing diagram for nRF401 for switching from RX to TX (a) and TX to RX (b).

### Switching between standby and RX-mode (operational mode).

The time from the PWR\_UP input is set to "1", until the data (DOUT) is valid is  $t_{SR}$ , see Table 5. Worst case  $t_{SR}$  is 3ms for nRF401 as can be seen in Figure 5 (a).

### Switching between standby and TX-mode (operational mode).

The time from the PWR\_UP input is set to "1", until the synthesised frequency is stable is  $t_{ST}$ , see Table 5.

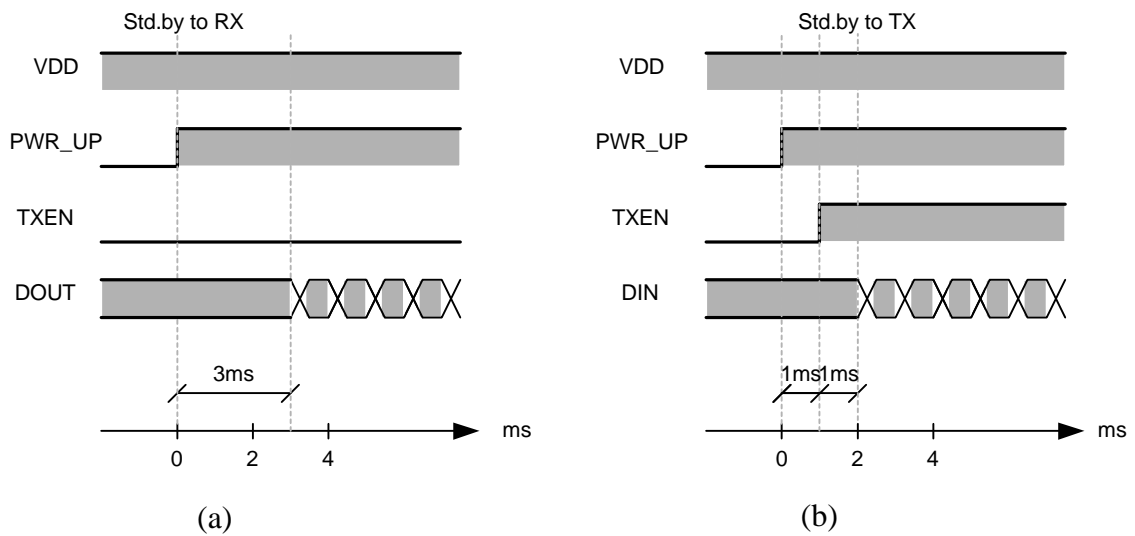


Figure 5 Timing diagram for nRF401 when going from standby to RX-mode (a) or TX-mode (b).

**Power up to transmit-mode (start-up).**

To avoid spurious emission outside the ISM-band when the power supply is switched on, the TXEN-input must be kept low until the synthesised frequency is stable, see Figure 6 (a).

When enabling transmit-mode, TXEN-input should be high for at least 1 ms before data (DIN) is transmitted, see Figure 6 (a).

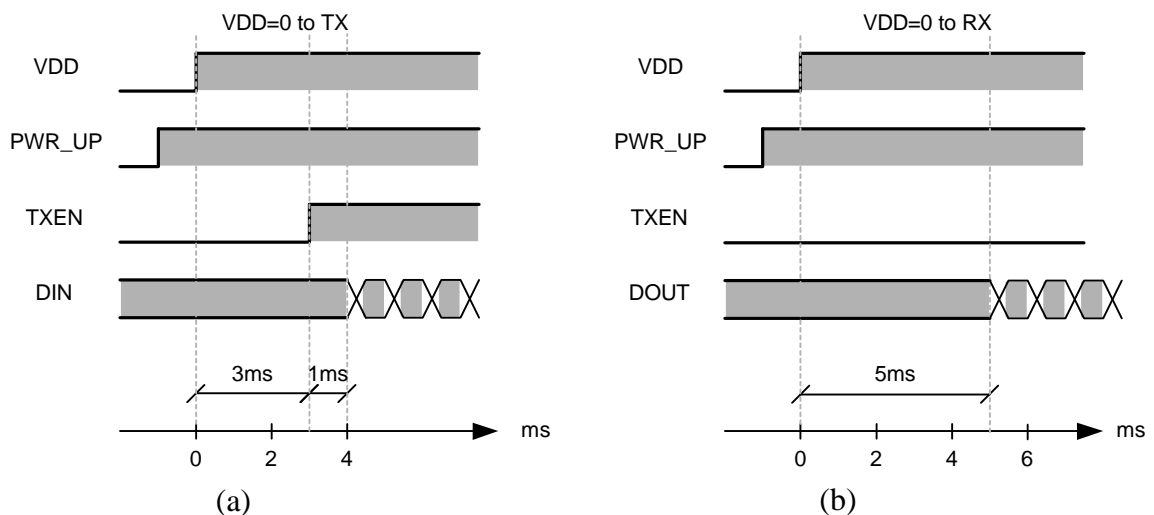


Figure 6. Timing diagram for nRF401 when powering up to TX-mode (a) or RX-mode (b).

**Power up to receive mode (start up).**

In transition from power up to receive mode, the receiver may not receive data (DOUT) until VDD has been stable ( $VDD > 2.7\text{ V}$ ) for at least 5ms, see Figure 6(b). If an external reference oscillator is used, the receiver may receive data (DOUT) after 3ms.



**APPLICATION INFORMATION**

**Antenna input/output**

The ANT1 and ANT2 pins provide RF input to the LNA (Low Noise Amplifier) when nRF401 is in receive mode, and RF output from the PA (Power Amplifier) when nRF401 is in transmit mode. The antenna connection to nRF401 is differential and the recommended load impedance at the antenna port is 400Ω.

Figure 12 shows a typical application schematic with a differential loop antenna on a Printed Circuit Board (PCB). The output stage (PA) consists of two open collector transistors in a differential pair configuration. VDD to the PA must be supplied through the collector load. When connecting a differential loop antenna to the ANT1/ANT2 pins, VDD should be supplied through the centre of the loop antenna as shown in Figure 12.

A single ended antenna or 50Ω test instrument may be connected to nRF401 by using a differential to single ended matching network (BALUN) as shown in Figure 7.

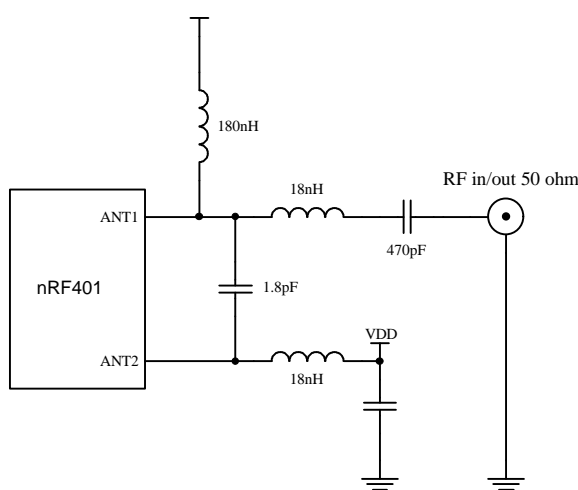


Figure 7. Connection of nRF401 to single ended antenna by using a differential to single ended matching network.

The 180nH inductor to VDD in Figure 7, need to have a Self-Resonance Frequency (SRF) above 433 MHz to be effective. Suitable inductors are listed in Table 6.

Vendors	WWW address	Part. no., 180 nH inductors, 0603 size
Stetco	<a href="http://www.stetco.com">http://www.stetco.com</a>	0603G181KTE
Coilcraft	<a href="http://www.coilcraft.com">http://www.coilcraft.com</a>	0603CS-R18XJBC
muRata	<a href="http://www.murata.com">http://www.murata.com</a>	LQW1608AR18J00

Table 6. Vendors and part. no. for suitable 180nH inductors.



**nRF401 Single Chip RF Transceiver**

An additional notch filter (L and C) at the 50Ω RF input/output may be necessary dependent on the application requirements (see application note nAN400-05).

A single ended antenna may also be connected to nRF401 using an 8:1 impedance RF transformer. The RF transformer must have a centre tap at the primary side for VDD supply.

**RF output power**

The external bias resistor R3 connected between the RF\_PWR pin and VSS sets the output power. The RF output power may be set to levels up to +10dBm. In Figure 8 the output power is plotted for power levels down to, but not limited to, -8.5dBm for a differential load of 400Ω. DC power supply current versus external bias resistor value is shown in Figure 9.

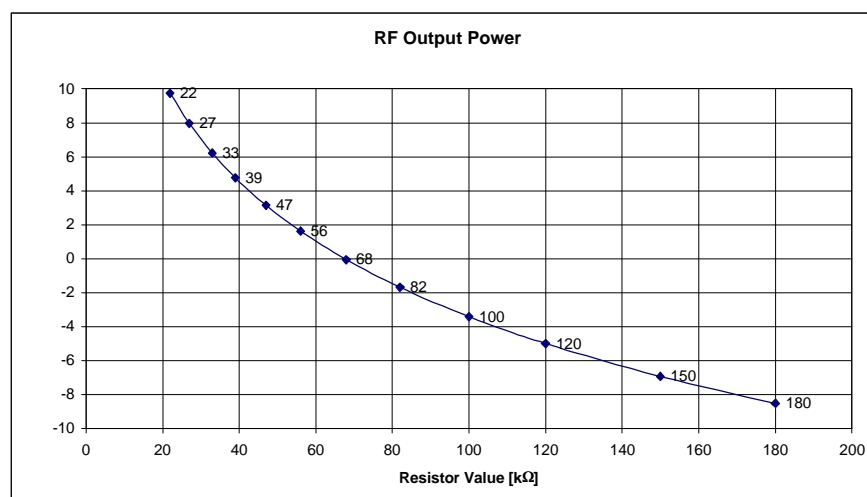


Figure 8. RF output power vs. external power setting resistor (R3) for nRF401.

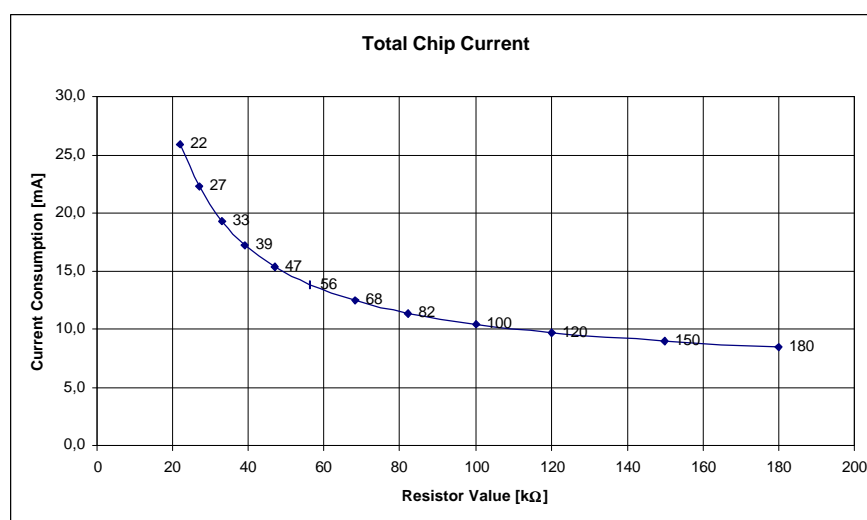


Figure 9. Total chip current consumption vs. external power setting resistor (R3) for nRF401.





**PLL loop filter**

The synthesiser loop filter is an external, single-ended second order lag-lead filter. The recommended filter component values are: C3 = 820 pF, C4 =15 nF, and R2 = 4.7 kΩ, see Figure 12.

**VCO inductor**

An external 22nH inductor connected between the VCO1 and VCO2 pins is required for the on-chip voltage controlled oscillator (VCO). This inductor should be a high quality chip inductor, Q > 45 @ 433 MHz, with a maximum tolerance of ± 2%. The following 22 nH inductors (0603) are suitable for use with nRF401.

Vendors	WWW address	Part. no., 22 nH inductors, 0603 size
Pulse	<a href="http://www.pulseeng.com">http://www.pulseeng.com</a>	PE-0603CD220GTT
Coilcraft	<a href="http://www.coilcraft.com">http://www.coilcraft.com</a>	0603CS-22NXGBC
muRata	<a href="http://www.murata.com">http://www.murata.com</a>	LQW1608A22NG00
Stetco	<a href="http://www.stetco.com">http://www.stetco.com</a>	0603G220GTE
KOA	<a href="http://www.koaspeer.com">http://www.koaspeer.com</a>	KQ0603TE22NG

Table 7. Vendors and part no. for suitable 22nH inductors.

See page 11 and 12 for PCB layout guidelines regarding placement of the inductor.

**Crystal specification**

To achieve an active crystal oscillator (XOSC) with low power consumption, certain requirements apply for crystal loss and capacitive load.

The crystal specification is:

- $f = 4.0000 \text{ MHz}$       Crystal parallel resonant frequency
- $C_o \leq 5 \text{ pF}$       Crystal parallel equivalent capacitance
- $ESR \leq 150 \text{ ohm}$  .      Crystal equivalent series resistance
- $C_L \leq 14 \text{ pF}$       Total crystal load capacitance, including capacitance in PCB layout.

For the crystal oscillator shown in Figure 10 the load capacitance becomes:

$$C_L = \frac{C1 \cdot C2'}{C1' + C2'} \cdot \text{Where } C1' = C1 + C_{PCB1} \text{ and } C2' = C2 + C_{PCB2}$$

C1 and C2 are 0603 SMD capacitors as shown in the application schematic, see Figure 12 and Table 9. C<sub>PCB1</sub> and C<sub>PCB2</sub> are the layout parasitic capacitance on the circuit board.

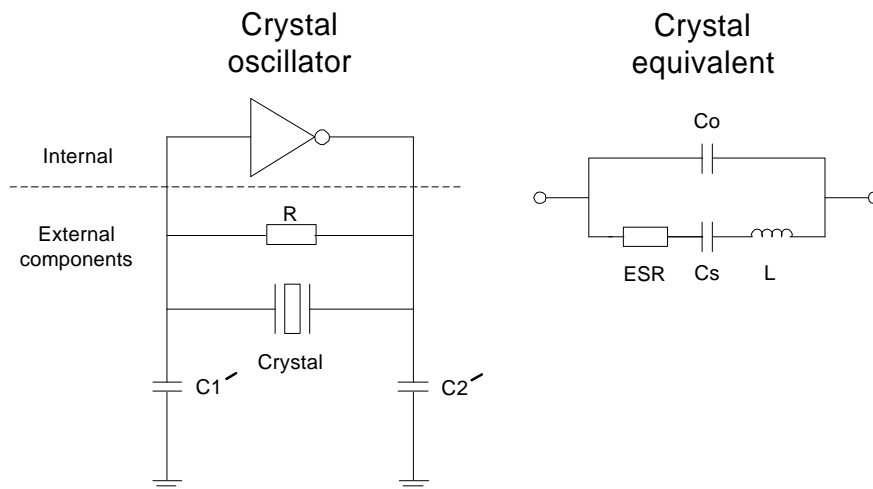


Figure 10. Crystal oscillator and crystal equivalent.

**Sharing a reference crystal with a micro-controller**

Figure 11 shows circuit diagram of a typical application where nRF401 and a micro controller share the reference crystal.

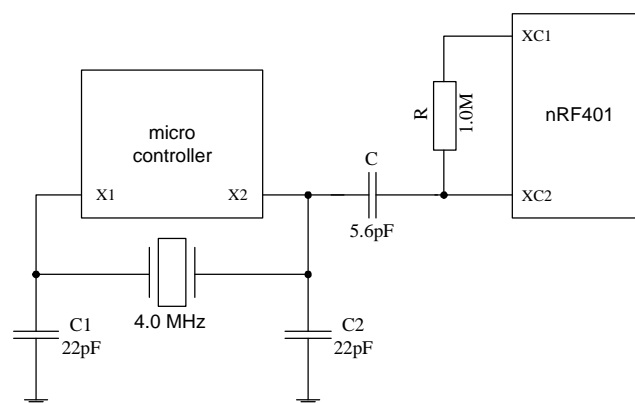


Figure 11. nRF401 and a micro-controller sharing the reference crystal.

The crystal reference line from the micro-controller should not be routed close to full swing digital data or control signals.

**Transmit/receive mode selection**

TXEN is a digital input for selection of transmit or receive mode.

TXEN = "1" selects transmit mode.

TXEN = "0" selects receive mode.

**Channel#1 / Channel#2 selection**

CS is a digital input for selection of either channel#1 ( $f_1=433.92\text{MHz}$ ) or channel#2 ( $f_2=434.33\text{MHz}$ ).

CS = "0" selects channel#1.

CS = "1" selects channel#2.



Input			Response	
TXEN	CS	PWR_UP	Channel #	Mode
0	0	1	1	RX
0	1	1	2	RX
1	0	1	1	TX
1	1	1	2	TX
X	X	0	--	Standby

Table 8. Required setting for standby and channel selection in RX and TX.

**D<sub>IN</sub> (data input) and D<sub>OUT</sub> (data output)**

The DIN pin is the input to the digital modulator of the transmitter. The input signal to this pin should be standard CMOS logic level at data rates up to 20 kbit/s. No coding of data is required.

$$DIN = "1" \rightarrow f = f_0 + \Delta f$$

$$DIN = "0" \rightarrow f = f_0 - \Delta f$$

The demodulated digital output data appear at the D<sub>OUT</sub> pin at standard CMOS logic levels.

$$f_0 + \Delta f \rightarrow DOUT="1",$$

$$f_0 - \Delta f \rightarrow DOUT="0".$$

**Power up**

PWR\_UP is a digital input for selection of normal operating mode or standby mode.

PWR\_UP = "1" selects normal operating mode.

PWR\_UP = "0" selects standby mode.

**Frequency difference between transmitter and receiver**

For optimum performance, the total frequency difference between transmitter and receiver should not exceed 70 ppm (30 kHz). This yields a crystal stability requirement of ±35 ppm for the transmitter and receiver. Frequency difference exceeding this will result in a -12dB/octave drop in receiver sensitivity. The functional frequency window of the transmission link is typically 450 ppm (200 kHz).

Example: A crystal with ±20 ppm frequency tolerance and ±25 ppm frequency stability over the operating temperature has a worst case frequency difference of ±45 ppm. If the transmitter and receiver operate in different temperature environments, the resulting worst-case frequency difference may be as high as 90 ppm. Resulting drop in sensitivity due to the extra 20 ppm, is then approx. 5dB.

**PCB layout and decoupling guidelines**

A well-designed PCB is necessary to achieve good RF performance. A PCB with a minimum of two layers including a ground plane is recommended for optimum performance.

The nRF401 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors, see Table 9. It is preferable to mount a



## **nRF401 Single Chip RF Transceiver**

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large surface mount capacitor (e.g. 2.2  $\mu$ F ceramic) in parallel with the smaller value capacitors. The nRF401 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF401 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes in or close to the VSS pads.

Full swing digital data or control signals should not be routed close to the PLL loop filter components or the external VCO inductor.

The VCO inductor placement is important. The optimum placement of the VCO inductor gives a PLL loop filter voltage of  $1.1 \pm 0.2$  V, which can be measured at FILT1 (pin4). For a 0603 size inductor the length between the centre of the VCO1/VCO2 pad and the centre of the inductor pad should be 5.4 mm, see Figure 13 (c) (layout, top view), for a 2 layer, 1.6 mm thick FR4 PCB.

### **PCB layout example**

Figure 13 shows a PCB layout example for the application schematic in Figure 12. A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a continuous ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane. There is no ground plane beneath the antenna.

For more layout information, please refer to application note nAN400-05, “nRF401 RF and antenna layout.



APPLICATION SCHEMATIC

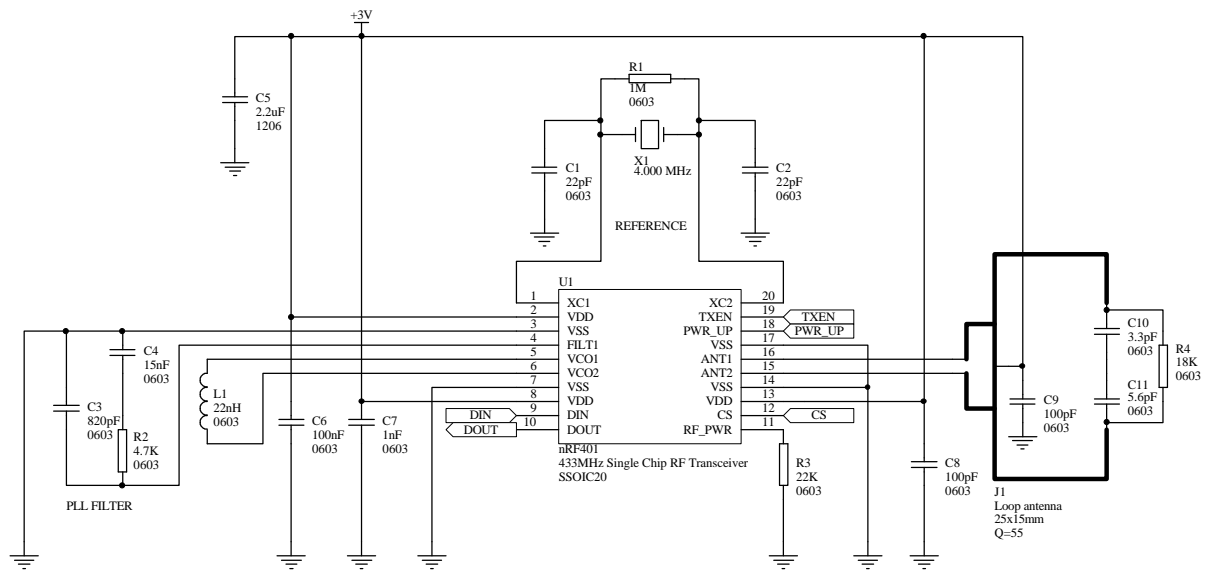


Figure 12. nRF401 application schematic.

Component	Description	Size	Value	Tolerance	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22		pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22		pF
C3	X7R ceramic chip capacitor, (PLL loop filter)	0603	820		pF
C4	X7R ceramic chip capacitor, (PLL loop filter)	0603	15		nF
C5	X7R ceramic chip capacitor, (Supply decoupling)	1206	2.2		μF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	100		nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	1		nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	100		pF
C9	NP0 ceramic chip capacitor, (Supply decoupling)	0603	100		pF
C10	NP0 ceramic chip capacitor, (Antenna tuning)	0603	3.3	±0.1	pF
C11	NP0 ceramic chip capacitor, (Antenna tuning)	0603	5.6	±0.25	pF
L1	VCO inductor, Q>45 @ 433 MHz	0603	22	±2%	nH
R1	0.1W chip resistor, (Crystal oscillator)	0603	1.0		MΩ
R2	0.1W chip resistor, (PLL loop filter)	0603	4.7		kΩ
R3	0.1W chip resistor, (Transmitter power setting)	0603	22		kΩ
R4	0.1W chip resistor, (Antenna Q reduction)	0603	18		kΩ
X1	Crystal	-	4.000		MHz

Table 9. Recommended External Components.

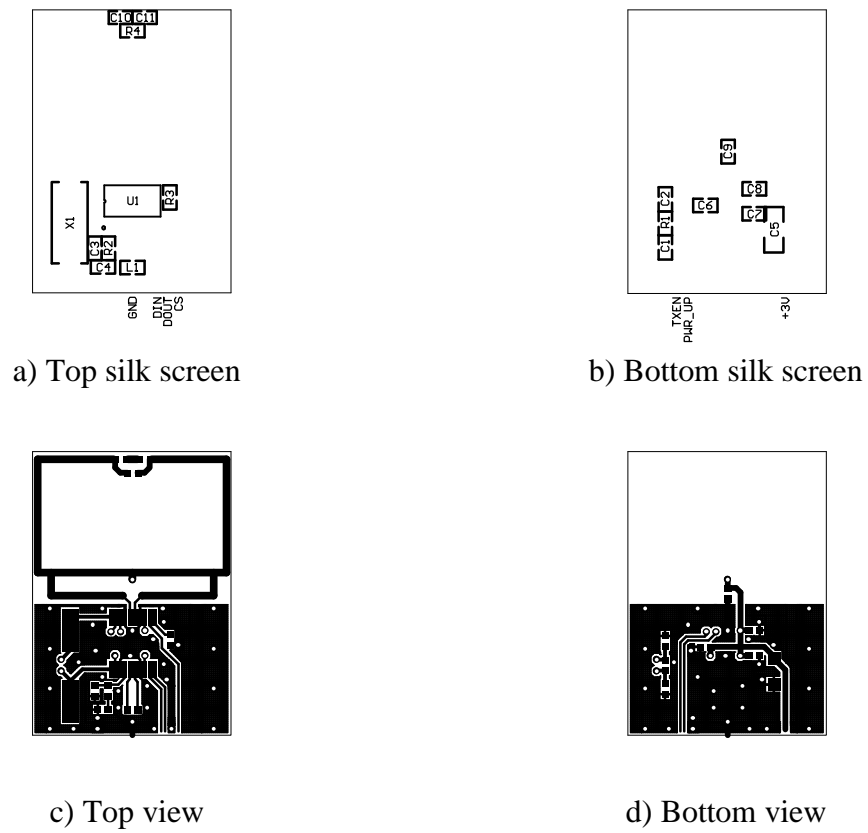


Figure 13. PCB layout (example) for nRF401 with loop antenna.



**DEFINITIONS**

<b>Data sheet status</b>	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<b>Limiting values</b>	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

Table 10. Definitions.

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

Product specification: Revision Date: 26.05.2000.

Datasheet order code: 260500nRF401

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**YOUR NOTES**





**YOUR NOTES**



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