10K ECL Logic Buffered Delay 16-Pin Modules
5-Tap: DECL • Single: FECL • Triple: MECL

Electrical Specifications at 25°C

Delay (ns)	Single 10K P/N	Triple 10K P/N
3 ± 0.5	FECL-3	MECL-3
4 ± 0.5	FECL-4	MECL-4
5 ± 0.5	FECL-5	MECL-5
6 ± 0.75	FECL-6	MECL-6
7 ± 0.75	FECL-7	MECL-7
8 ± 0.8	FECL-8	MECL-8
9 ± 1.0	FECL-9	MECL-9
10 ± 1.0	FECL-10	MECL-10
15 ± 1.5	FECL-15	MECL-15
20 ± 1.5	FECL-20	MECL-20
25 ± 1.5	FECL-25	MECL-25
50 ± 2.5	FECL-50	MECL-50
60 ± 3.0	FECL-60	----
75 ± 3.75	FECL-75	----
100 ± 5.0	FECL-100	----

Electrical Specifications at 25°C

10K ECL 5 Tap P/N	Tap Delay Tolerances +/- 5% or 1.5ns (+/- 0.8ns <10ns)					Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
DECL-6	2.0	3.0	4.0	5.0	6 ± 0.8	** 1 ± 0.4
DECL-10	2.0	4.0	6.0	8.0	10 ± 1.0	2 ± 0.6
DECL-15	3.0	6.0	9.0	12.0	15 ± 1.5	3 ± 0.8
DECL-20	4.0	8.0	12.0	16.0	20 ± 1.5	4 ± 1.0
DECL-25	5.0	10.0	15.0	20.0	25 ± 1.5	5 ± 1.0
DECL-30	6.0	12.0	18.0	24.0	30 ± 1.5	6 ± 1.5
DECL-40	8.0	16.0	24.0	32.0	40 ± 2.0	8 ± 2.0
DECL-45	9.0	18.0	27.0	36.0	45 ± 2.25	9 ± 2.0
DECL-50	10.0	20.0	30.0	40.0	50 ± 2.5	10 ± 2.0
DECL-75	15.0	30.0	45.0	60.0	75 ± 3.75	15 ± 2.5
DECL-100	20.0	40.0	60.0	80.0	100 ± 5.0	20 ± 3.0
DECL-125	25.0	50.0	75.0	100.0	125 ± 6.25	25 ± 3.0
DECL-150	30.0	60.0	90.0	120.0	150 ± 7.5	30 ± 3.0
DECL-200	40.0	80.0	120.0	160.0	200 ± 10.0	40 ± 4.0
DECL-250	50.0	100.0	150.0	200.0	250 ± 12.5	50 ± 5.0

** This part numbers does not have 5 equal taps.
Specified Tap-to-Tap Delays are referenced to Tap 1.

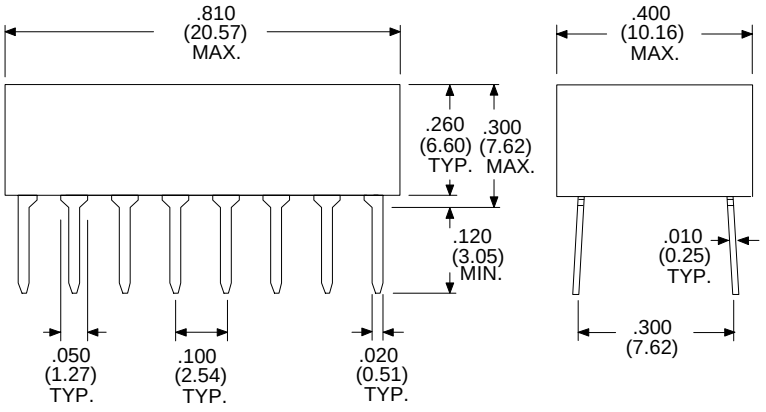
OPERATING SPECIFICATIONS (10K ECL)

V_{EE} Supply Voltage ..... -5.20 ± 0.25 VDC
Supply Current, I_{EE} , **DECL** ..... 60 mA typ., 75 mA max.
Supply Current, I_{EE} , **FECL** ..... 40 mA typ., 65 mA max.
Supply Current, I_{EE} , **MECL** ..... 85 mA typ., 105 mA max.
Logic "1" Input: V_{IH} ..... -0.98 V min.
I_{IH} ..... 265 µA max.
Logic "0" Input: V_{IL} ..... -1.63 V max.
I_{IL} ..... 0.5 mA max.
V_{OH} Logic "1" Voltage Out ..... -0.96 V min.
V_{OL} Logic "0" Voltage Out ..... -1.65V max.
T_{RO} Output Rise Time ..... < 3.00 ns typ.
Input Pulse Width, P_{WI} (**DECL,FECL**) ..... 40% of total delay, min.
Input Pulse Width, P_{WI} (**MECL**) ..... 100% of total delay, min.
Operating Temperature Range ..... -30° to +85°C
Storage Temperature Range ..... -65° to +150°C

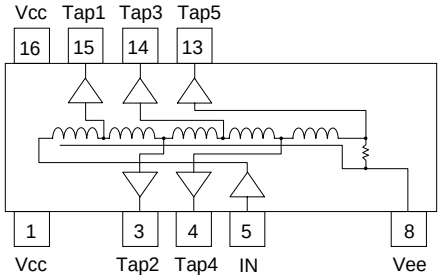
TEST CONDITIONS (Measurements made at 25°C)

V_{EE} Supply Voltage ..... -5.20VDC
Input Pulse Voltage ..... -.80V to -1.80V
Input Pulse Rise Time ..... 3.00ns max.
Input Pulse Period ..... 4.0 x Total Delay
Input Pulse Duty Cycle 50%
Outputs terminated through 100 Ω to -2.00 Vdc.

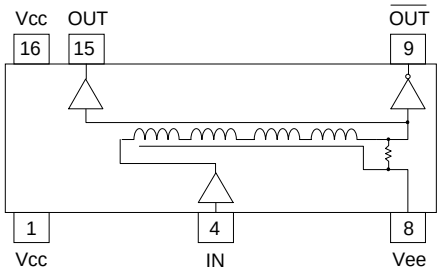
Dimensions in Inches (mm) -- Unused Leads Removed Per Schematic



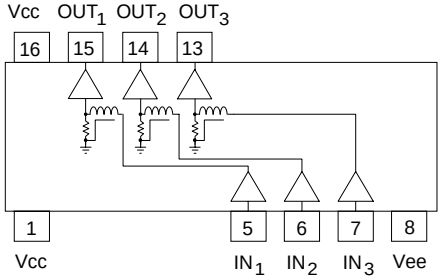
DECL Style Schematic



FECL Style Schematic



MECL Style Schematic



Also Available in 10KH ECL Versions: DECLH, FECLH & MECLH Series

Specifications subject to change without notice. **For other values & Custom Designs, contact factory.**