



# CEM9410

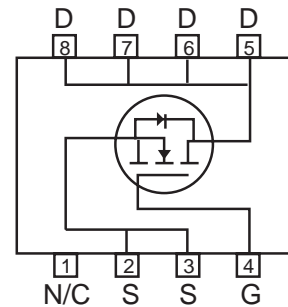
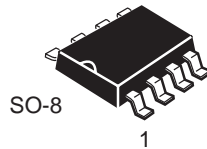
March 1998

## N-Channel Enhancement Mode Field Effect Transistor

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### FEATURES

- 30V , 7A ,  $R_{DS(ON)}=30m\Omega$  @  $V_{GS}=10V$ .  
 $R_{DS(ON)}=50m\Omega$  @  $V_{GS}=4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- Surface mount Package.



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>a</sup> @ $T_J=125^\circ C$ -Pulsed <sup>b</sup>	$I_D$	$\pm 7$	A
	$I_{DM}$	$\pm 20$	A
Drain-Source Diode Forward Current <sup>a</sup>	$I_S$	2.8	A
Maximum Power Dissipation <sup>a</sup>	PD	2.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	50	$^\circ C/W$
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## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.5	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> = 7A		25	30	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3.5A		38	50	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 5V	20			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 7A		14		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> = 0V f = 1.0MHz		500		pF
Output Capacitance	C <sub>OSS</sub>			270		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			95		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 15V, I <sub>D</sub> = 1A, V <sub>GEN</sub> = 10V, R <sub>GEN</sub> = 6Ω		9	15	ns
Rise Time	t <sub>r</sub>			9	20	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			25	50	ns
Fall Time	t <sub>f</sub>			20	35	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 7A, V <sub>GS</sub> = 10V		16	21	nC
Gate-Source Charge	Q <sub>gs</sub>			3		nC
Gate-Drain Charge	Q <sub>gd</sub>			5		nC

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## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2.0A		0.76	1.1	V

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Notes

- a. Surface Mounted on FR4 Board, t ≤ 10sec.
- b. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.

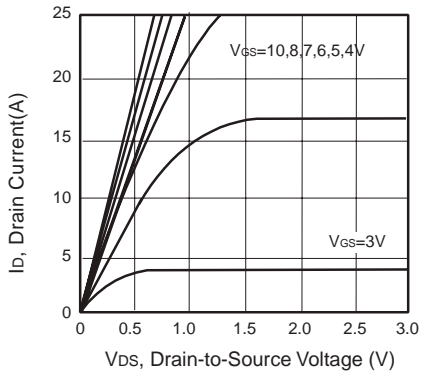


Figure 1. Output Characteristics

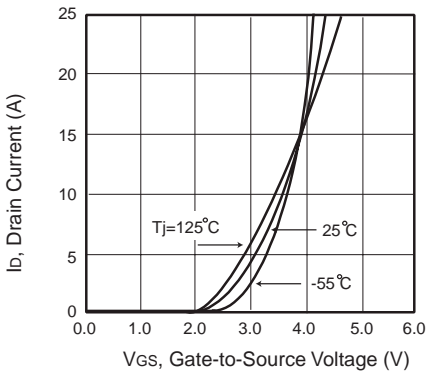


Figure 2. Transfer Characteristics

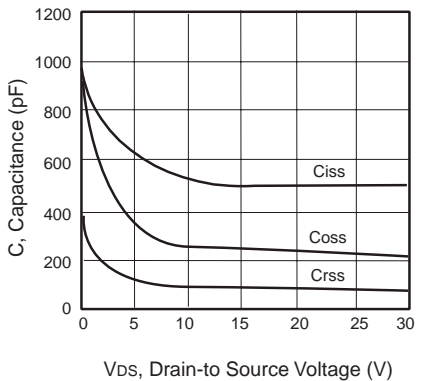


Figure 3. Capacitance

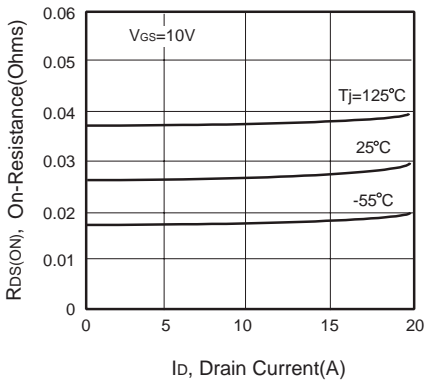
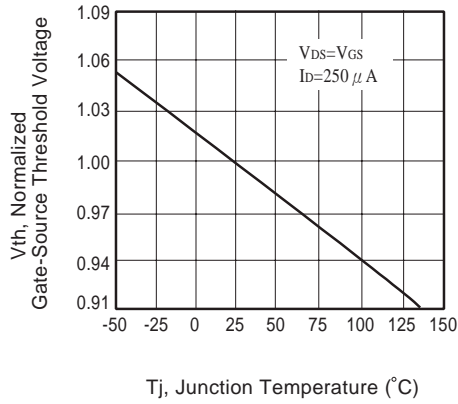


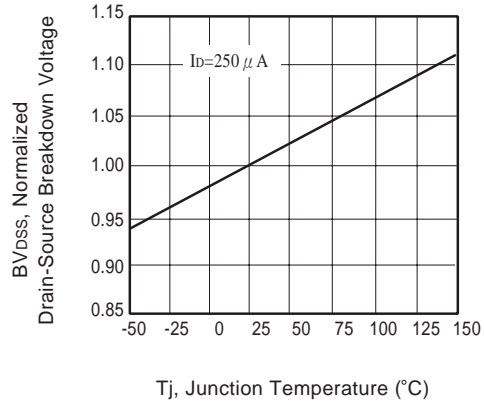
Figure 4. On-Resistance Variation with Drain Current and Temperature

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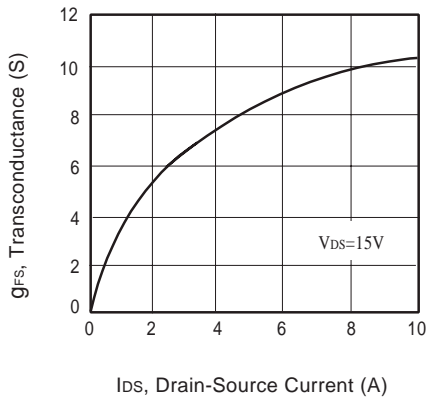
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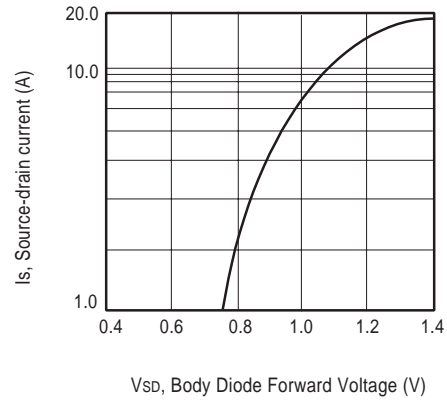
**Figure 5. Gate Threshold Variation with Temperature**



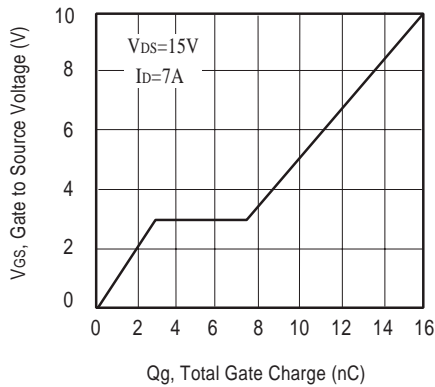
**Figure 6. Breakdown Voltage Variation with Temperature**



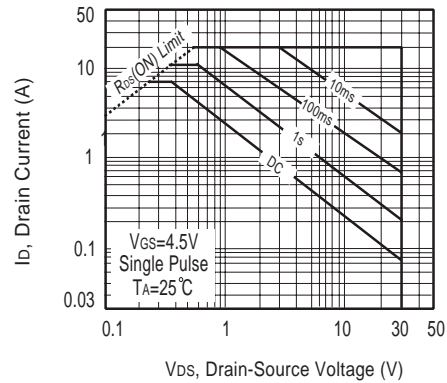
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

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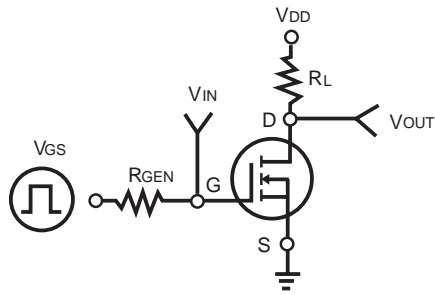


Figure 11. Switching Test Circuit

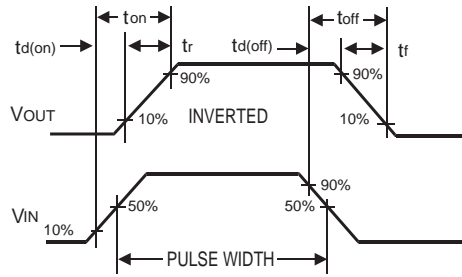


Figure 12. Switching Waveforms

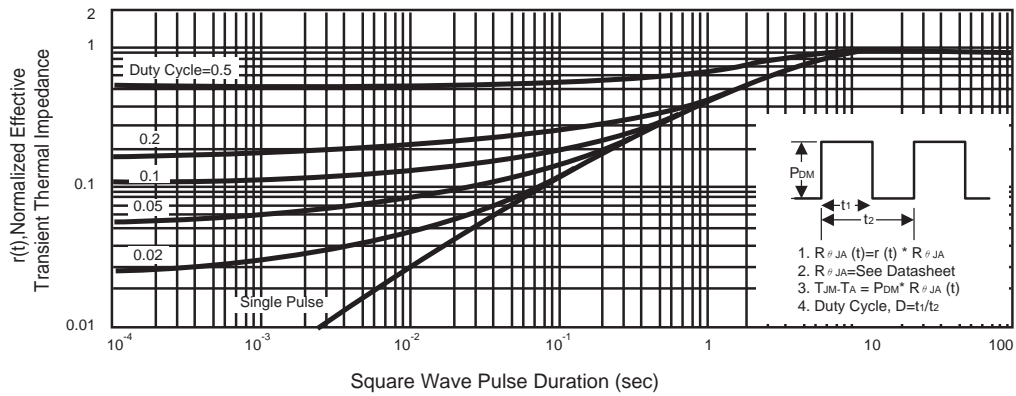


Figure 13. Normalized Thermal Transient Impedance Curve