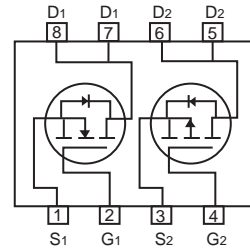
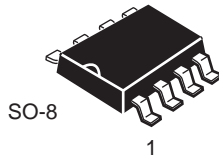


Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

- 40V, 6.1A, $R_{DS(ON)} = 32m\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 46m\Omega$ @ $V_{GS} = 4.5V$.
- -40V, -5.2A, $R_{DS(ON)} = 43m\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 65m\Omega$ @ $V_{GS} = 4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead free product is acquired.
- Surface mount Package.



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Channel 1	Channel 2	Units	
Drain-Source Voltage	V_{DS}	40	-40	V	
Gate-Source Voltage	V_{GS}	± 20	± 20	V	
Drain Current-Continuous	I_D	$T_A=25^\circ C$	6.1	-5.2	A
		$T_A=70^\circ C$	4.9	-4.2	
Drain Current-Pulsed ^a	I_{DM}	20	-20		
Maximum Power Dissipation	P_D	$T_A=25^\circ C$	2.0		W
		$T_A=70^\circ C$	1.28		
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$	

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient ^b	$R_{\theta JA}$	62.5	$^\circ C/W$



CEM4269

N-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6A$			32	$m\Omega$
		$V_{GS} = 4.5V, I_D = 5A$			46	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS} = 5V, I_D = 6A$		3		S
Dynamic Characteristics^d						
Input Capacitance	C_{iss}	$V_{DS} = 20V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1050		pF
Output Capacitance	C_{oss}			155		pF
Reverse Transfer Capacitance	C_{rss}			95		pF
Switching Characteristics^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20V, I_D = 6A, V_{GS} = 10V, R_{GEN} = 3\Omega$		14	30	ns
Turn-On Rise Time	t_r			10	20	ns
Turn-Off Delay Time	$t_{d(off)}$			17	35	ns
Turn-Off Fall Time	t_f			18	35	ns
Total Gate Charge	Q_g	$V_{DS} = 20V, I_D = 6A, V_{GS} = 10V$		20.5	27	nC
Gate-Source Charge	Q_{gs}			3.5		nC
Gate-Drain Charge	Q_{gd}			4.0		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				1.0	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = 1.0A$			1.0	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing.						



CEM4269

P-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40V, V_{GS} = 0V$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -5A$			43	$m\Omega$
		$V_{GS} = -4.5V, I_D = -2A$			65	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_D = -4.8A$		3		S
Dynamic Characteristics ^d						
Input Capacitance	C_{iss}	$V_{DS} = -20V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		1115		pF
Output Capacitance	C_{oss}			205		pF
Reverse Transfer Capacitance	C_{rss}			120		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20V, I_D = -5A,$ $V_{GS} = -10V, R_{GEN} = 3\Omega$		12	25	ns
Turn-On Rise Time	t_r			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			40	80	ns
Turn-Off Fall Time	t_f			10	20	ns
Total Gate Charge	Q_g	$V_{DS} = -20V, I_D = -5A,$ $V_{GS} = -10V$		20	26	nC
Gate-Source Charge	Q_{gs}			3.3		nC
Gate-Drain Charge	Q_{gd}			4.1		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				-1.0	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = -1.0A$			-1.0	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing.						



N-CHANNEL

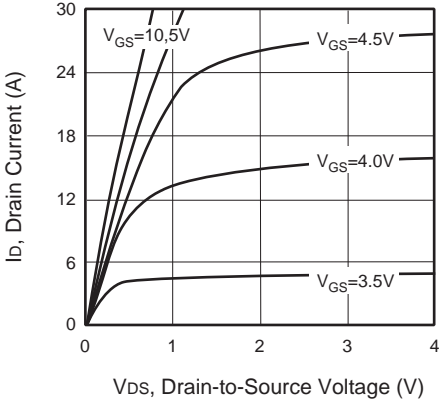


Figure 1. Output Characteristics

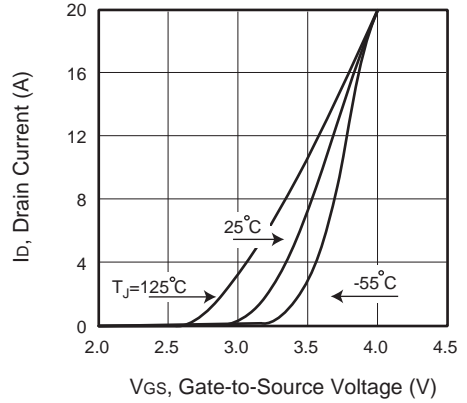


Figure 2. Transfer Characteristics

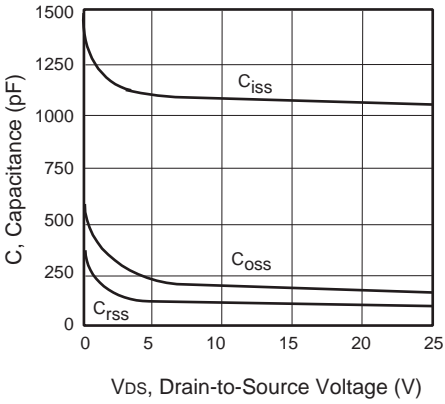


Figure 3. Capacitance

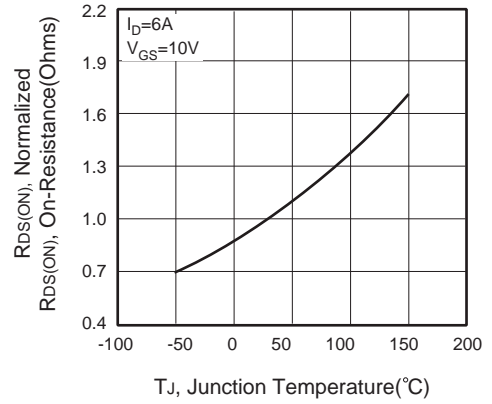


Figure 4. On-Resistance Variation with Temperature

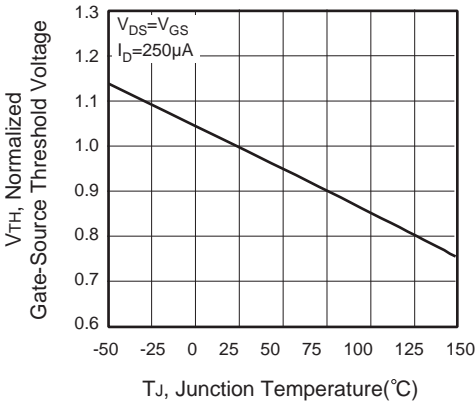


Figure 5. Gate Threshold Variation with Temperature

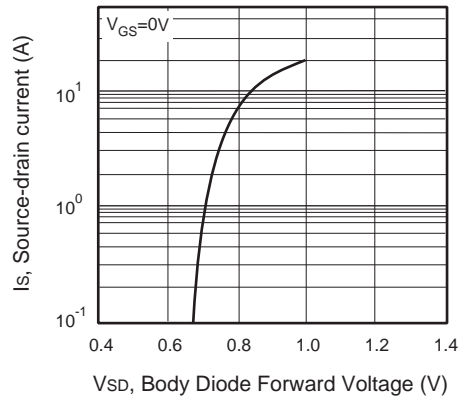


Figure 6. Body Diode Forward Voltage Variation with Source Current



P-CHANNEL

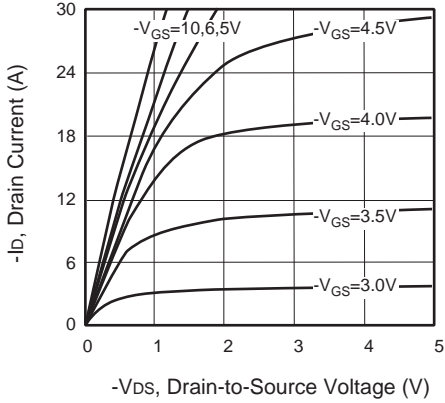


Figure 7. Output Characteristics

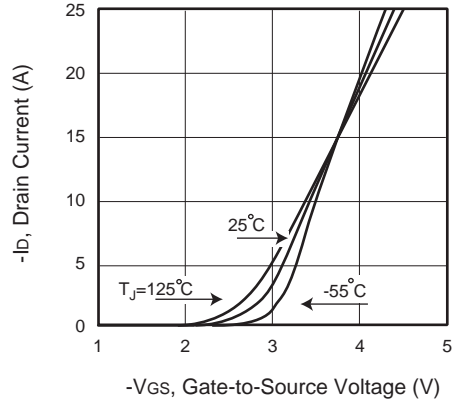


Figure 8. Transfer Characteristics

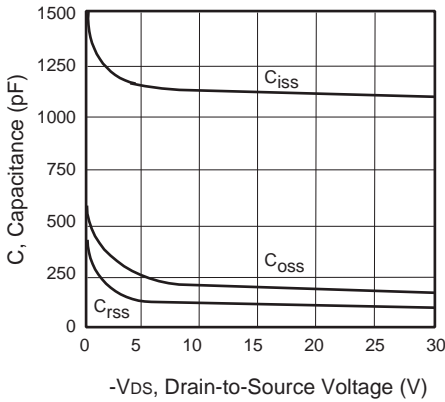


Figure 9. Capacitance

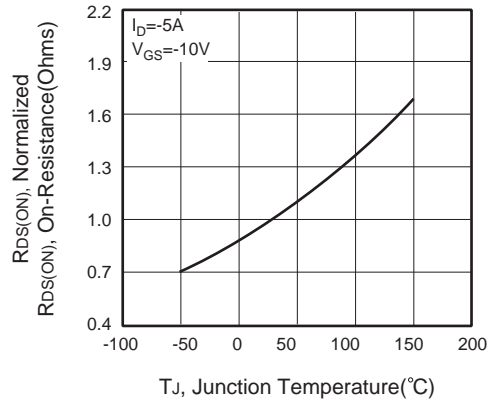


Figure 10. On-Resistance Variation with Temperature

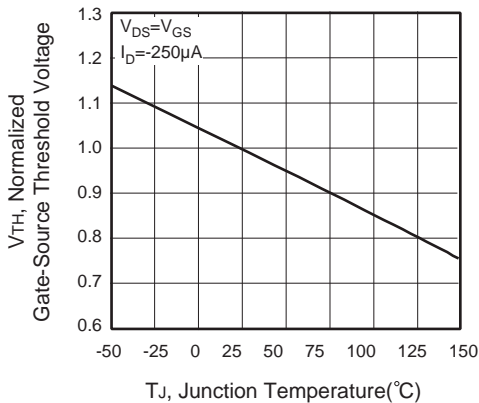


Figure 11. Gate Threshold Variation with Temperature

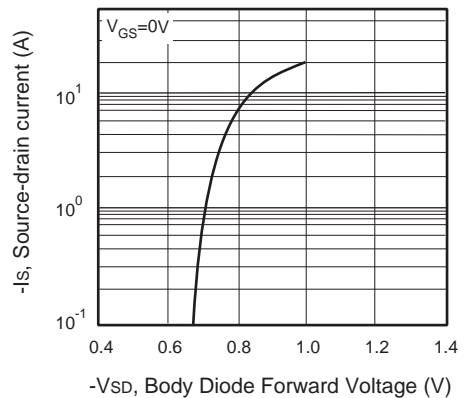


Figure 12. Body Diode Forward Voltage Variation with Source Current



N-CHANNEL

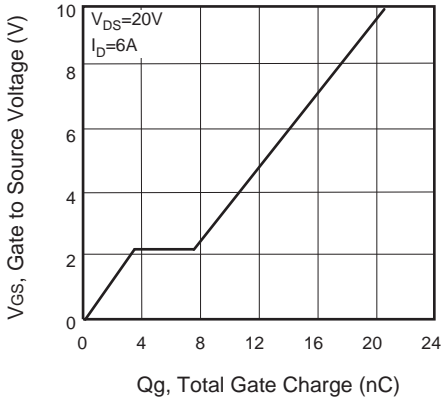


Figure 13. Gate Charge

P-CHANNEL

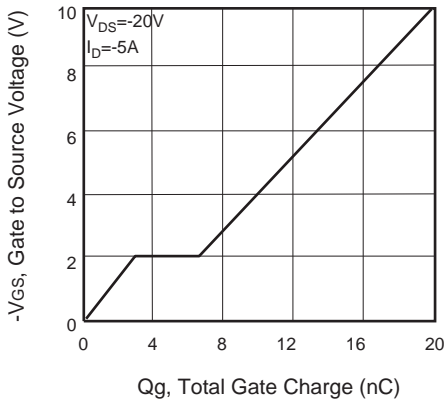


Figure 15. Gate Charge

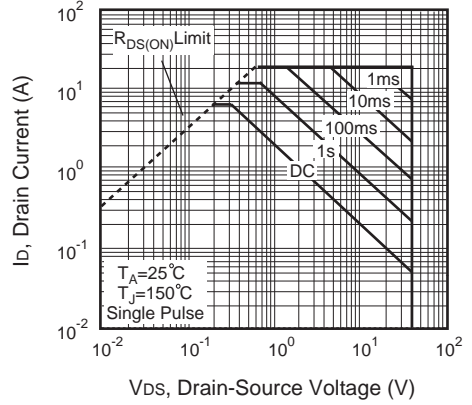


Figure 14. Maximum Safe Operating Area

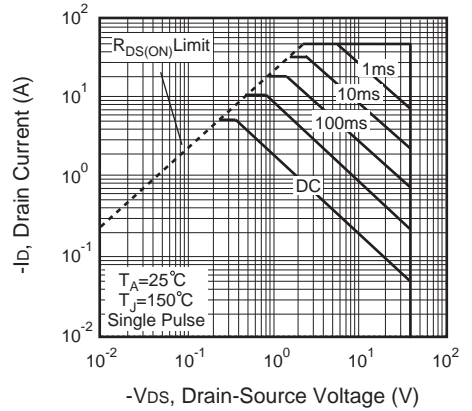


Figure 16. Maximum Safe Operating Area

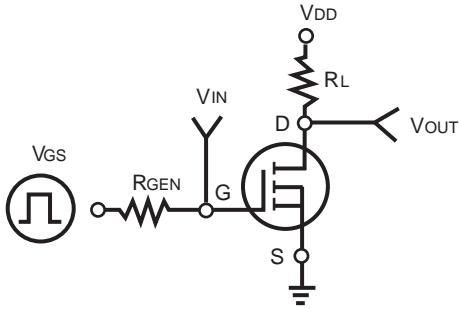


Figure 17. Switching Test Circuit

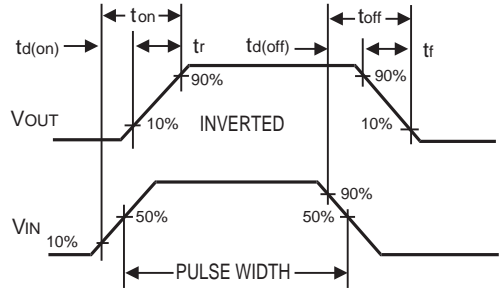


Figure 18. Switching Waveforms

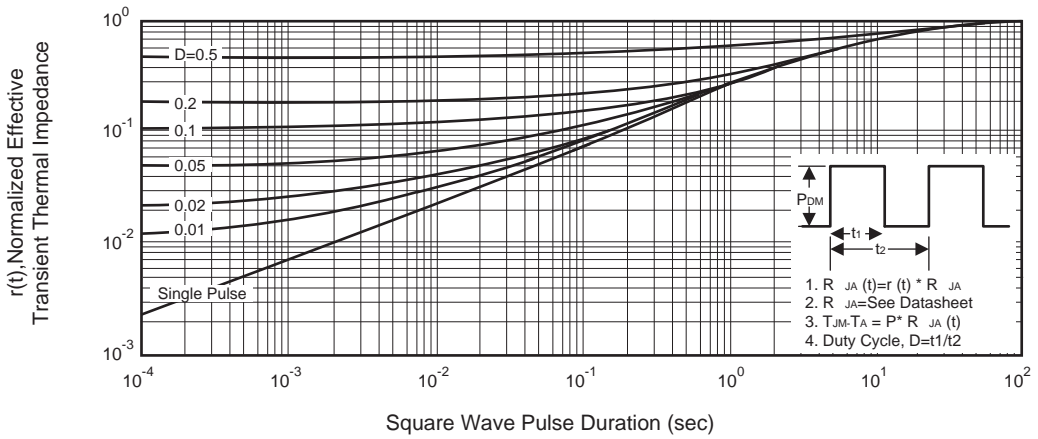


Figure 19. Normalized Thermal Transient Impedance Curve