CET

CEM4532

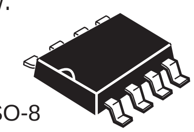
Jan. 2003

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

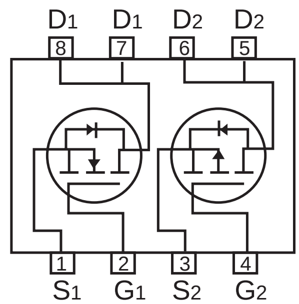
5

FEATURES

- 30V , 4.7A , $R_{DS(ON)}$=55mΩ @V_{GS}=10V.
  $R_{DS(ON)}$=85mΩ @V_{GS}=4.5V.
  -30V , -4.5A , $R_{DS(ON)}$=80mΩ @V_{GS}=-10V.
  $R_{DS(ON)}$=135mΩ @V_{GS}=-4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Surface Mount Package.


SO-8

1



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current-Continuous [a]	I_D	±4.7	±4.5	A
-Pulsed	I_{DM}	±20	±20	A
Drain-Source Diode Forward Current [a]	I_S	1.7	-1.7	A
Maximum Power Dissipation [a]	P_D	2.0		W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	62.5	°C/W

CEM4532

5

N-Channel ELECTRICAL CHARACTERISTICS (T_A=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	µA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	1		3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 4.7A		40	55	mΩ
		V_{GS} = 4.5V, I_D = 3.7A		70	85	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	15			A
Forward Transconductance	g_{FS}	V_{DS} = 15V, I_D = 4.7A		5		S
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{iss}	V_{DS} =15V, V_{GS} = 0V f =1.0MHz		357		pF
Output Capacitance	C_{oss}			190		pF
Reverse Transfer Capacitance	C_{rss}			60		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6 Ω		15	30	ns
Rise Time	t_r			18	40	ns
Turn-Off Delay Time	$t_{D(OFF)}$			30	60	ns
Fall Time	t_f			5	15	ns
Total Gate Charge	Q_g	V_{DS} =15V, I_D = 4.7A, V_{GS} =10V		10.4	15	nC
Gate-Source Charge	Q_{gs}			2.3		nC
Gate-Drain Charge	Q_{gd}			2.8		nC

5

P-Channel ELECTRICAL CHARACTERISTICS (T_A=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	µA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250µA	-1		-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -4.5A		60	80	mΩ
		V_{GS} = -4.5V, I_D = -3.6A		105	135	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-15			A
Forward Transconductance	g_{FS}	V_{DS} = -15V, I_D = -4.5A		5.8		S
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} =-15V, V_{GS} = 0V f =1.0MHz		448		pF
Output Capacitance	C_{OSS}			317		pF
Reverse Transfer Capacitance	C_{RSS}			308		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = -15V, I_D = -1A, V_{GEN} = -10V, R_{GEN} = 6 Ω		19	45	ns
Rise Time	t_r			19	45	ns
Turn-Off Delay Time	$t_{D(OFF)}$			38	75	ns
Fall Time	t_f			48	95	ns
Total Gate Charge	Q_g	V_{DS} =-15V, I_D = -4.5A, V_{GS} =-10V		18	23	nC
Gate-Source Charge	Q_{gs}			3		nC
Gate-Drain Charge	Q_{gd}			4.5		nC

CEM4532

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ[c]	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS [b]							
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, Is = 1.7A	N-Ch		0.8	1.2	V
		V_{GS} = 0V, Is =-1.7A	P-Ch		-0.8	-1.2	

Notes

a.Surface Mounted on FR4 Board, t ≤10sec.
b.Pulse Test:Pulse Width ≤300 μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

N-Channel

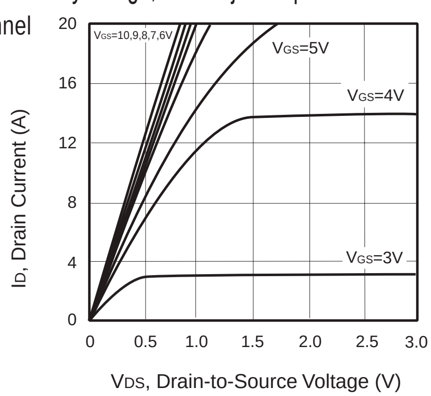


Figure 1. Output Characteristics

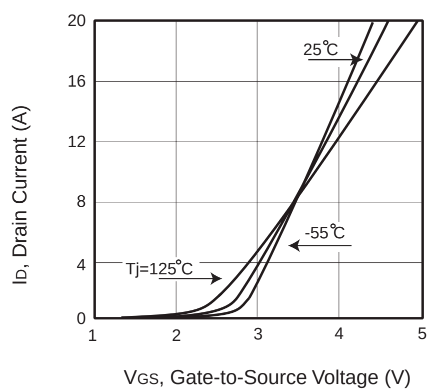


Figure 2. Transfer Characteristics

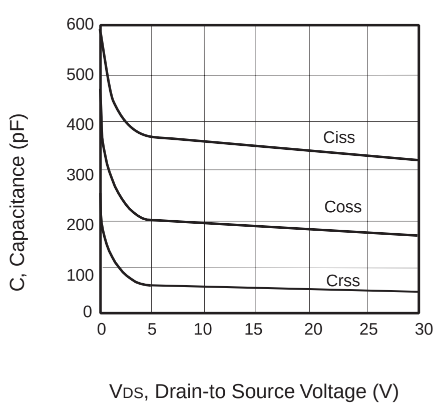


Figure 3. Capacitance

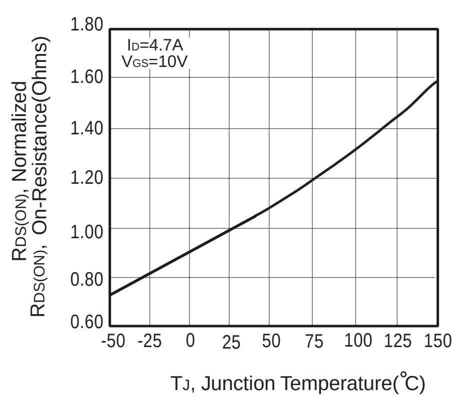


Figure 4. On-Resistance Variation with Temperature

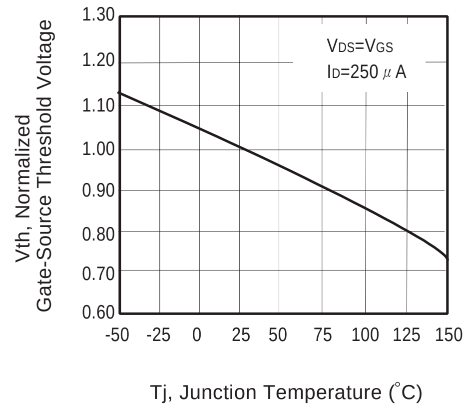


Figure 5. Gate Threshold Variation with Temperature

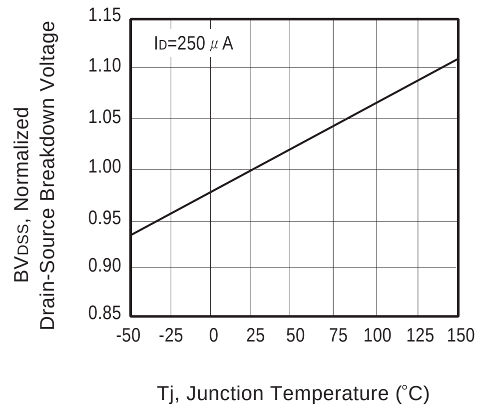


Figure 6. Breakdown Voltage Variation with Temperature

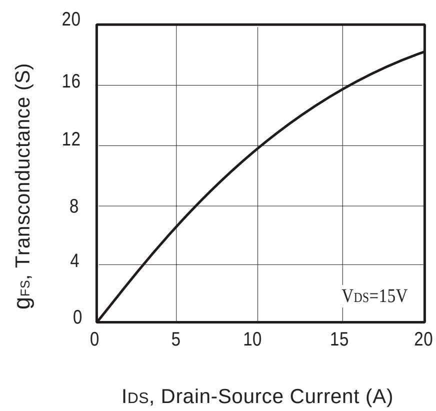


Figure 7. Transconductance Variation with Drain Current

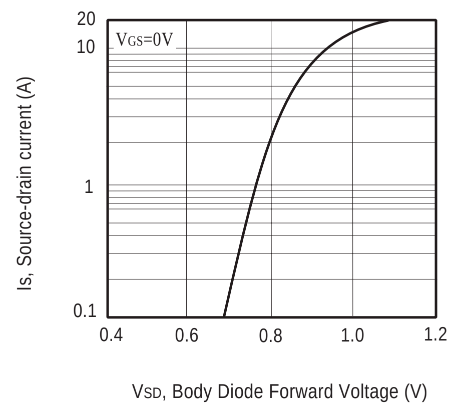


Figure 8. Body Diode Forward Voltage Variation with Source Current

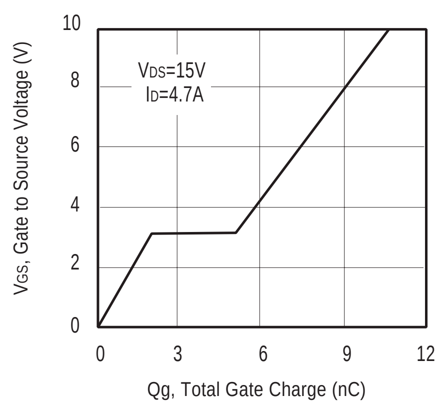


Figure 9. Gate Charge

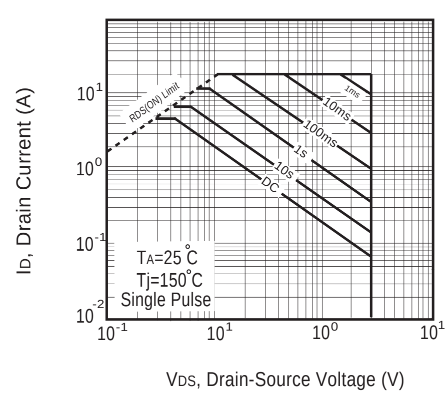


Figure 10. Maximum Safe Operating Area

CEM4532

P-Channel

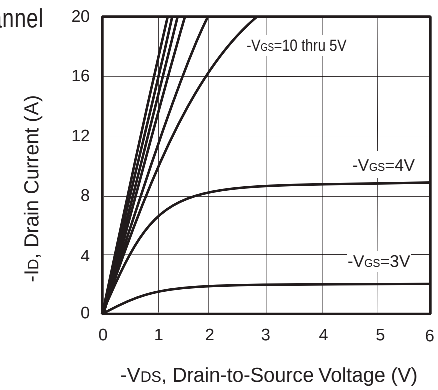


Figure 11. Output Characteristics

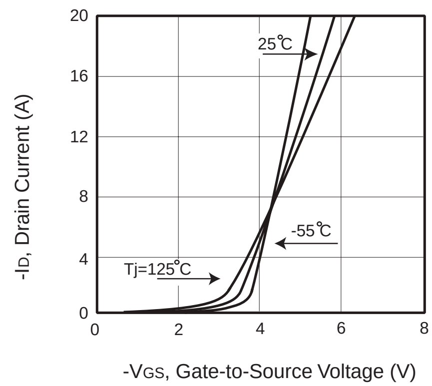


Figure 12. Transfer Characteristics

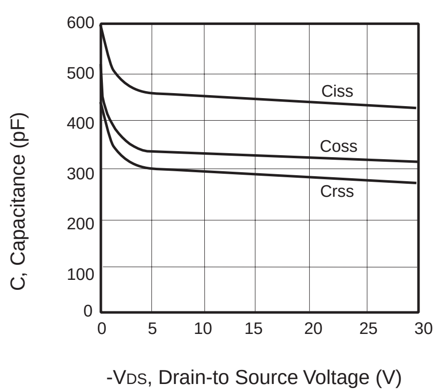


Figure 13. Capacitance

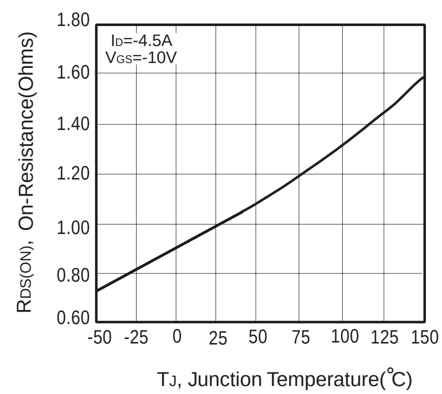


Figure 14. On-Resistance Variation with Temperature

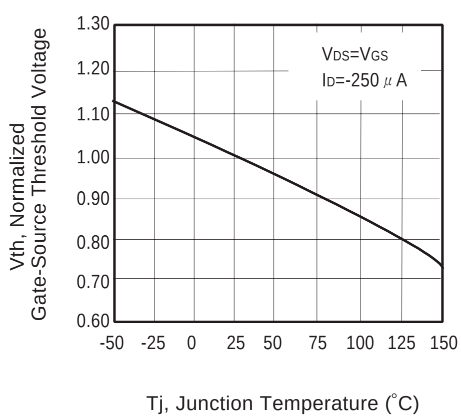


Figure 15. Gate Threshold Variation with Temperature

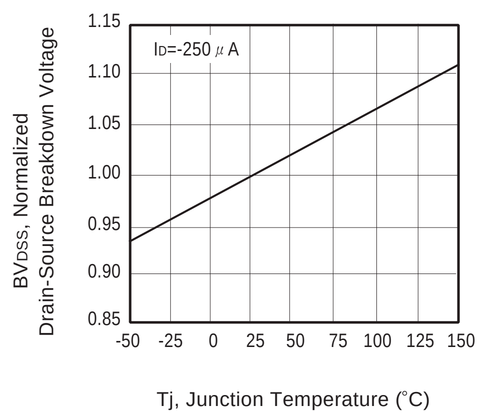


Figure 16. Breakdown Voltage Variation with Temperature

P-Channel

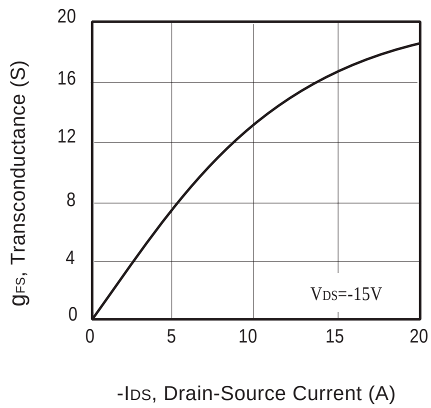


Figure 17. Transconductance Variation with Drain Current

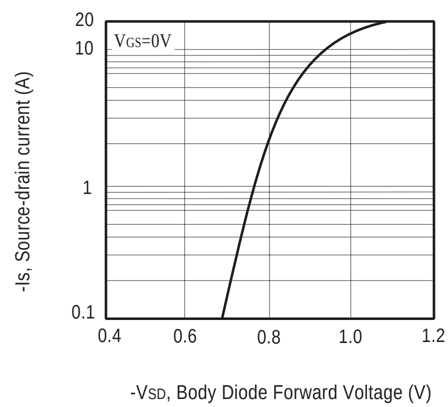


Figure 18. Body Diode Forward Voltage Variation with Source Current

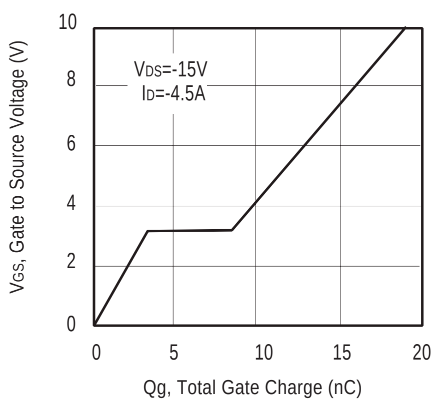


Figure 19. Gate Charge

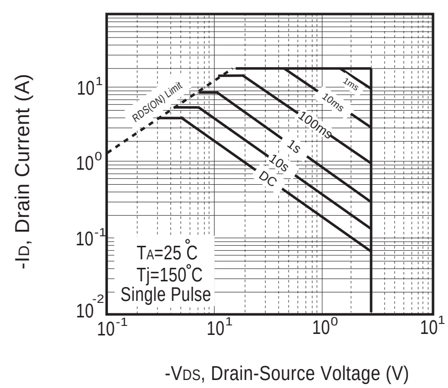


Figure 20. Maximum Safe Operating Area

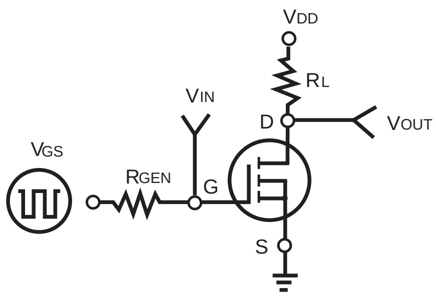


Figure 21. Switching Test Circuit

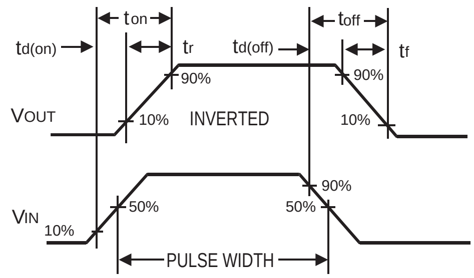


Figure 22. Switching Waveforms

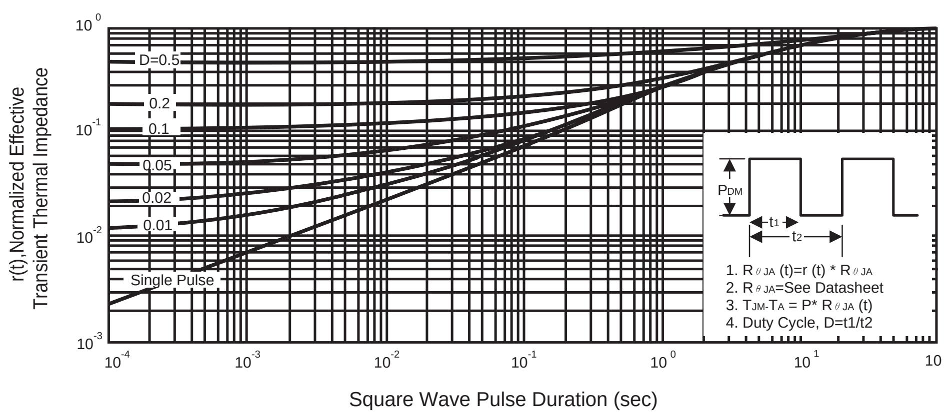


Figure 23. Normalized Thermal Transient Impedance Curve