CEM2005

PRELIMINARY

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

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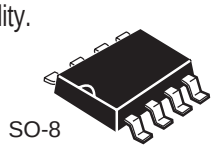
FEATURES

- 20V , 6.0A , $R_{DS(ON)}$=30mΩ @V_{GS}=4.5V.
  $R_{DS(ON)}$=40mΩ @V_{GS}=2.5V.
  -20V , -4.3A , $R_{DS(ON)}$=65mΩ @V_{GS}=-4.5V.
  $R_{DS(ON)}$=100mΩ @V_{GS}=-2.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Surface Mount Package.



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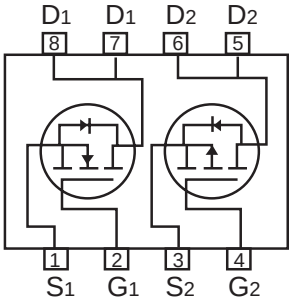

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	±8	±8	V
Drain Current-Continuous [a]	I_D	±6	±4.3	A
-Pulsed	I_{DM}	±24	±20	A
Drain-Source Diode Forward Current [a]	I_S	1.7	-1.7	A
Maximum Power Dissipation [a]	P_D	2.0		W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	62.5	°C/W

CEM2005

N-Channel ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±8V, V_{DS} = 0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.5		1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 5.0A		24	30	mΩ
		V_{GS} = 2.5V, I_D = 4.2A		32	40	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	20			A
Forward Transconductance	g_{FS}	V_{DS} = 15V, I_D = 5.0A		10		S
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} =8V, V_{GS} = 0V f =1.0MHz		500		pF
Output Capacitance	C_{OSS}			300		pF
Reverse Transfer Capacitance	C_{RSS}			140		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GEN} = 6Ω		20	40	ns
Rise Time	t_r			18	40	ns
Turn-Off Delay Time	$t_{D(OFF)}$			60	108	ns
Fall Time	t_f			28	56	ns
Total Gate Charge	Q_g	V_{DS} =10V, I_D = 4.7A, V_{GS} =4.5V		10	15	nC
Gate-Source Charge	Q_{gs}			2.3		nC
Gate-Drain Charge	Q_{gd}			2.9		nC

P-Channel ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	μA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±8V, V_{DS} = 0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.5		-1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -4.5A		50	65	mΩ
		V_{GS} = -4.5V, I_D = -3.6A		80	100	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-15			A
Forward Transconductance	g_{FS}	V_{DS} = -15V, I_D = -4.5A		5.8		S
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} =-8V, V_{GS} = 0V f =1.0MHz		1430		pF
Output Capacitance	C_{OSS}			800		pF
Reverse Transfer Capacitance	C_{RSS}			325		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = -10V, I_D = -1A, V_{GEN} = -4.5V, R_{GEN} = 6Ω		20	45	ns
Rise Time	t_r			21	45	ns
Turn-Off Delay Time	$t_{D(OFF)}$			76	135	ns
Fall Time	t_f			56	100	ns
Total Gate Charge	Q_g	V_{DS} =-10V, I_D = -4.3A, V_{GS} =-4.5V		19	25	nC
Gate-Source Charge	Q_{gs}			3		nC
Gate-Drain Charge	Q_{gd}			5		nC

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ[c]	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS [b]							
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, Is = 1.7A	N-Ch			1.2	V
		V_{GS} = 0V, Is =-1.7A	P-Ch			-1.2	

Notes

a.Surface Mounted on FR4 Board, t ≤10sec.
b.Pulse Test:Pulse Width ≤300 μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

N-Channel

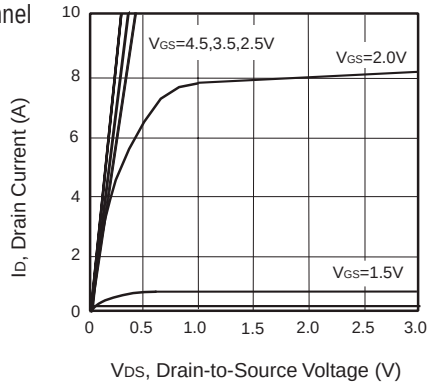

Figure 1. Output Characteristics

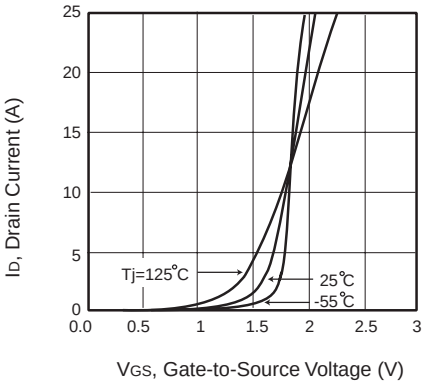

Figure 2. Transfer Characteristics

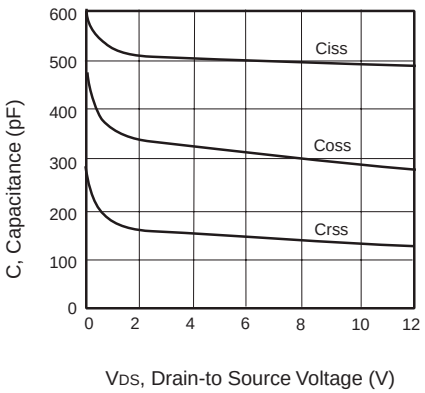

Figure 3. Capacitance

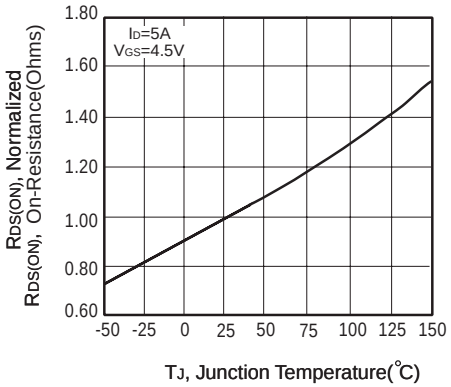

Figure 4. On-Resistance Variation with Temperature

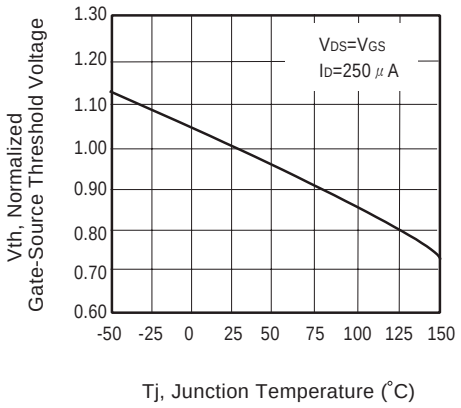

Figure 5. Gate Threshold Variation with Temperature

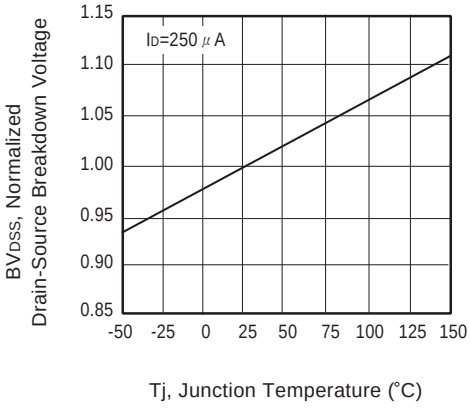

Figure 6. Breakdown Voltage Variation with Temperature

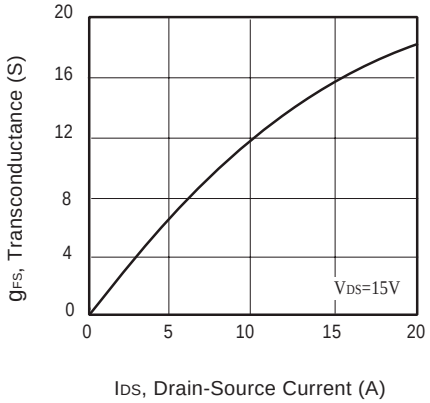

Figure 7. Transconductance Variation with Drain Current

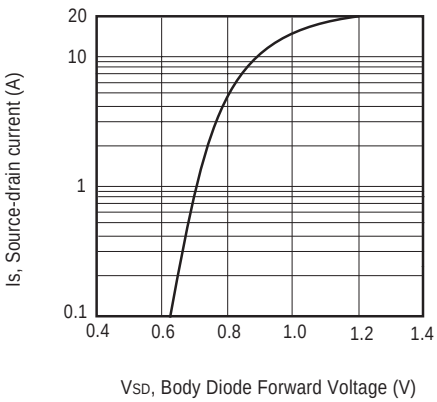

Figure 8. Body Diode Forward Voltage Variation with Source Current

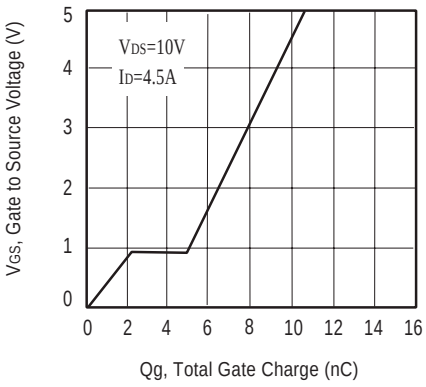

Figure 9. Gate Charge

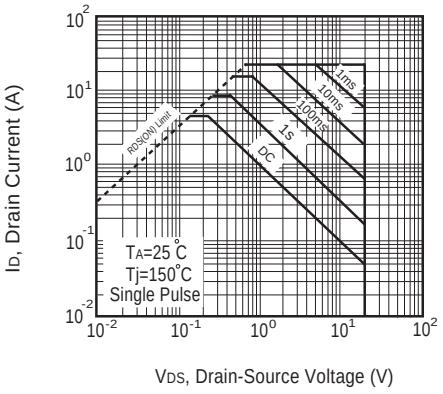

Figure 10. Maximum Safe Operating Area

P-Channel

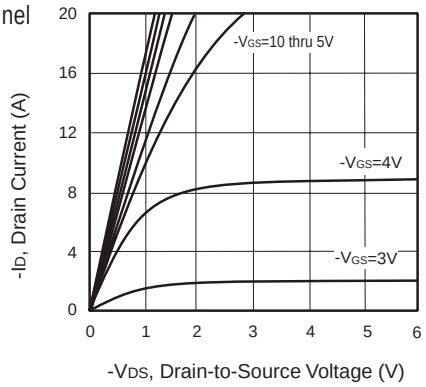

Figure 11. Output Characteristics

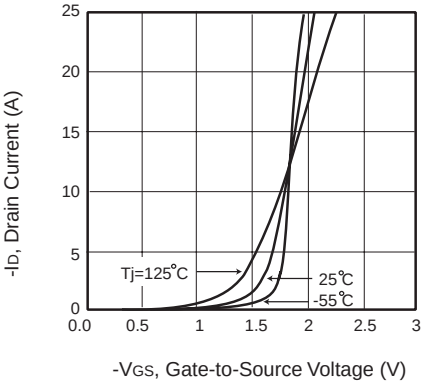

Figure 12. Transfer Characteristics

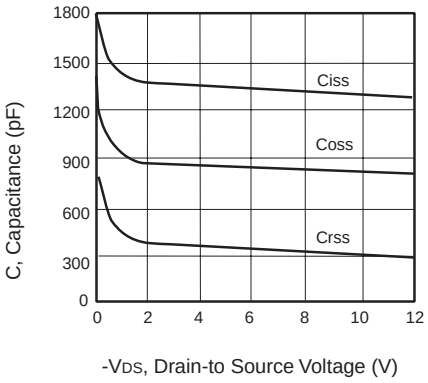

Figure 13. Capacitance

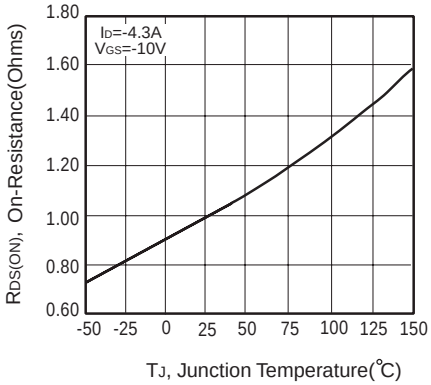

Figure 14. On-Resistance Variation with Temperature

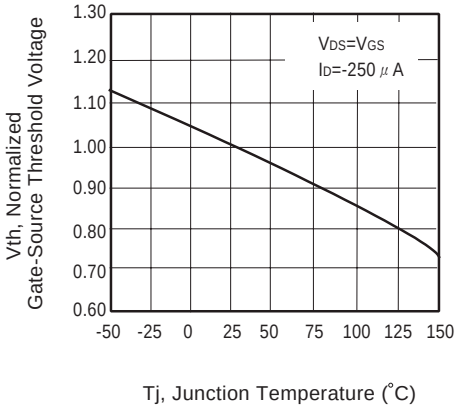

Figure 15. Gate Threshold Variation with Temperature

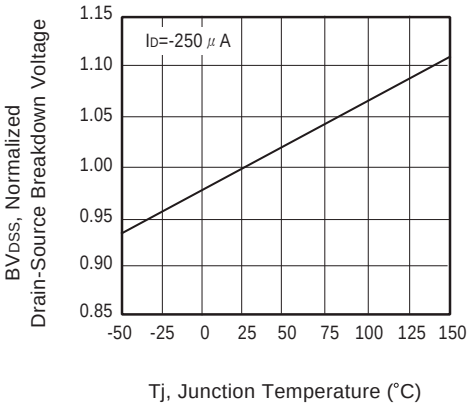

Figure 16. Breakdown Voltage Variation with Temperature

P-Channel

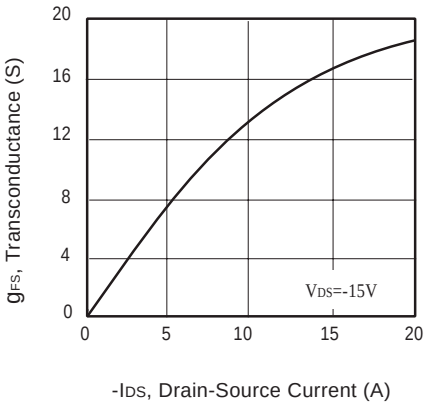

Figure 17. Transconductance Variation with Drain Current

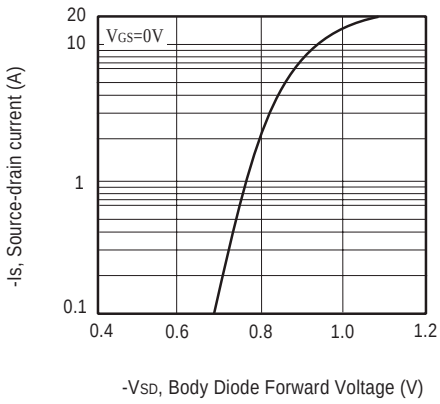

Figure 18. Body Diode Forward Voltage Variation with Source Current

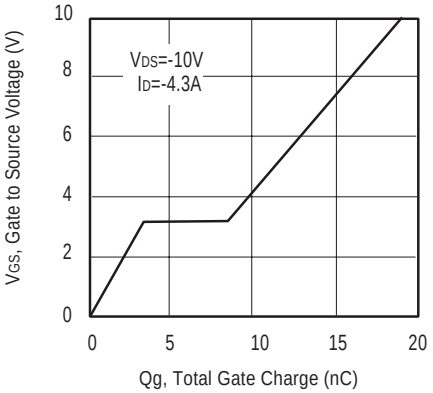

Figure 19. Gate Charge

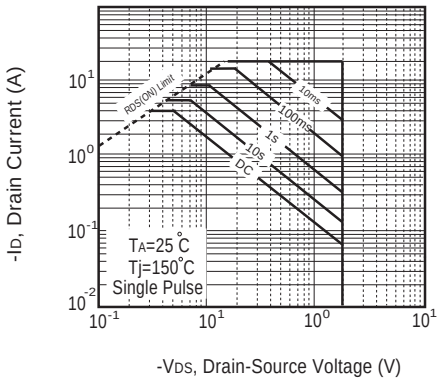

Figure 20. Maximum Safe Operating Area

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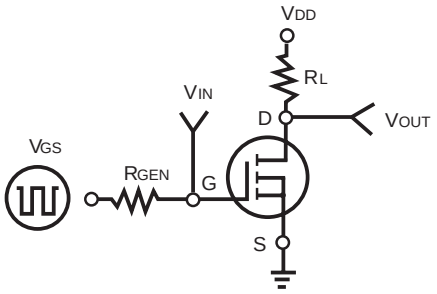

Figure 21. Switching Test Circuit

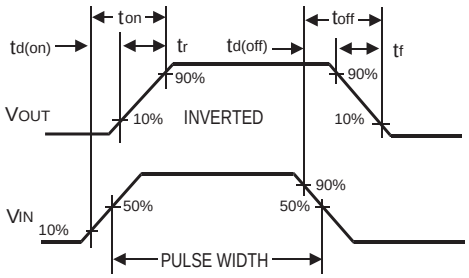

Figure 22. Switching Waveforms

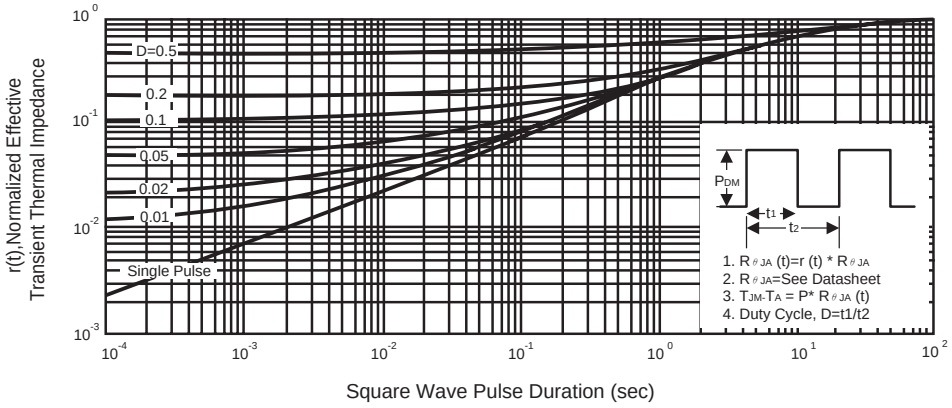

Figure 23. Normalized Thermal Transient Impedance Curve