LC4913

3003A Original CMOS Standard Logic LC4900B Series

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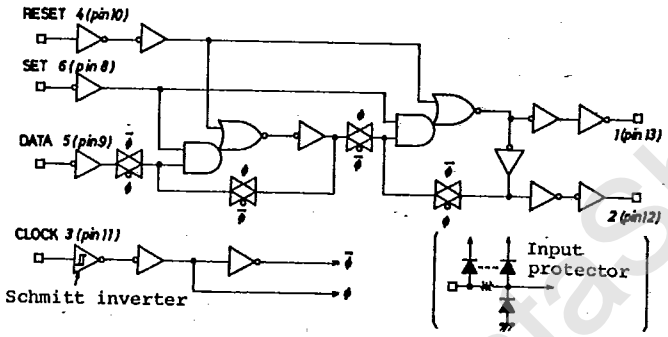
Dual D-Type Flip-Flop with Schmitt Clock Input

The LC4913 is a dual D-type flip-flop having such features as wide operating range, high noise margin, low power dissipation.

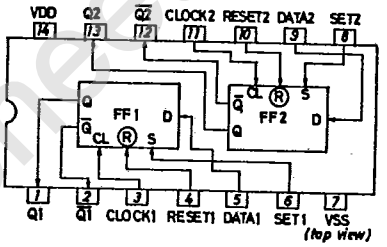
Absolute Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20.0	V
Maximum Input Voltage	$V_{IN}max$		V_{SS}-0.5 to V_{SS}+0.5	V
Maximum Output Voltage	$V_{OUT}max$		V_{SS}-0.5 to V_{SS}+0.5	V
Maximum Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	Pdmax	Ta≦85°C	300	mW
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C
Lead Temperature and Time	tsol		260°C,10sec	

Equivalent Circuit (1/2 LC4913)



Pin Assignment and Circuit Configuration

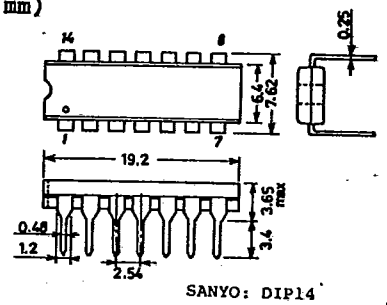


Truth Table

inputs				outputs	
CL△	D	S	R	Qn+1	$\overline{Qn+1}$
* *	*	H	L	H	L
*	*	L	H	L	H
*	*	H	H	L	H
↓	L	L	L	L	H
↓	H	L	L	H	L
↓	*	L	L	Qn^	$\overline{Qn}$^

*: don't care.
△: level change
^: no change

Case Outline 3003A-D14IC
(unit:mm)



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Allowable Operating Conditions at Ta=25±2°C, V_{SS}=0V

			V_{CC}		unit
Supply Voltage Range	V_{DD}	Ta=-40 to +85°C		3 to 18	V
Input Voltage Range	V_{IN}	Ta=-40 to +85°C		0 to V_{DD}	V
Data Setup Time	t_{SETUP}		5	150 min	ns
			10	100 min	ns
			15	80 min	ns
Data Hold Time	t_{HOLD}		5	150 min	ns
			10	100 min	ns
			15	80 min	ns
Clock Pulse Width	t_{WCLK}		5	200 min	ns
			10	100 min	ns
			15	80 min	ns
Clock Frequency	f_{CLK}		5	dc to 1.0	MHz
			10	dc to 2.0	MHz
			15	dc to 3.0	MHz
Clock Rise/Fall Time	t_{rCLK}, t_{fCLK}		5	to 50	ms
			10	to 25	ms
			15	to 10	ms
Set/Reset Pulse Width	t_{wS}, t_{wR}		5	300 min	ns
			10	200 min	ns
			15	160 min	ns

Electrical Characteristics at Ta=25°C±2°C, V_{SS}=0V

				V_{CC}	min	typ	max	unit
Output "H"-Level Voltage	V_{OH}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS},V_{DD}$		5	4.95	5.00		V
				10	9.95	10.00		V
				15	14.95	15.00		V
Output "L"-Level Voltage	V_{OL}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS},V_{DD}$		5		0.00	0.05	V
				10		0.00	0.05	V
				15		0.00	0.05	V
Output "H"-Level Current	I_{OH}	$V_{IN}=V_{SS}$, V_{DD}	Vo=4.6V	5	-0.16			mA
			Vo=9.5V	10	-0.40			mA
			Vo=13.5V	15	-1.2			mA
Output "L"-Level Current	I_{OL}	$V_{IN}=V_{SS}$, V_{DD}	Vo=0.4V	5	0.44			mA
			Vo=0.5V	10	1.1			mA
			Vo=1.5V	15	3.0			mA
Input "H"-Level Voltage (Inputs other than CLK)	V_{IH}	$\|I_{OUT}\|$<1uA	Vo=0.5;4.5V	5	3.5	2.75		V
			Vo=1.0;9.0V	10	7.0	5.5		V
			Vo=1.5;13.5V	15	11.0	8.25		V
Input "L"-Level Voltage (Inputs other than CLK)	V_{IL}	$\|I_{OUT}\|$<1uA	Vo=0.5;4.5V	5		2.25	1.5	V
			Vo=1.0;9.0V	10		4.5	3.0	V
			Vo=1.5;13.5V	15		6.75	4.0	V
"H"-Level Threshold Voltage	V_P	Same conditions as for V_{IH},V_{IL}, CLOCK input only.		5		3.0		
				10		6.0		
				15		9.0		
"L"-Level Threshold Voltage	V_N	"		5		2.0		
				10		4.0		
				15		5.0		
Hysteresis Width	V_H	"		5		1.0		
				10		2.0		
				15		4.0		
Input Leakage Current	I_{IH}	V_{IH}=18V		18		10	0.3	uA
	I_{IL}	V_{IL}=0V		18		-10	-0.3	uA
Quiescent Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$		5		0.01	4.0	uA
				10		0.01	8.0	uA
				15		0.01	16.0	uA

Current direction: + (no sign): Flowing into device
- : Flowing out of device

Electrical Characteristics at Ta=-40°C, V_{SS}=0V

				V_{CC}	min	typ	max	unit
Output "H"-Level Voltage	V_{OH}	($\|I_{OUT}\|$<1uA, V_{IN}=V_{SS},V_{DD})		5	4.95			V
				10	9.95			V
				15	14.95			V
Output "L"-Level Voltage	V_{OL}	($\|I_{OUT}\|$<1uA, V_{IN}=V_{SS},V_{DD})		5			0.05	V
				10			0.05	V
				15			0.05	V
Output "H"-Level Current	I_{OH}	(V_{IN}=V_{SS}, V_{DD})	Vo=4.6V	5	-0.2			mA
			Vo=9.5V	10	-0.5			mA
			Vo=13.5V	15	-1.4			mA
Output "L"-Level Current	I_{OL}	(V_{IN}=V_{SS}, V_{DD})	Vo=0.4V	5	0.52			mA
			Vo=0.5V	10	1.3			mA
			Vo=1.5V	15	3.6			mA
Input "H"-Level Voltage (Inputs other than CLK)	V_{IH}	($\|I_{OUT}\|$<1uA)	Vo=0.5;4.5V	5	3.5			V
			Vo=1.0;9.0V	10	7.0			V
			Vo=1.5;13.5V	15	11.0			V
Input "L"-Level Voltage (Inputs other than CLK)	V_{IL}	($\|I_{OUT}\|$<1uA)	Vo=0.5;4.5V	5			1.5	V
			Vo=1.0;9.0V	10			3.0	V
			Vo=1.5;13.5V	15			4.0	V
Input Leakage Current	I_{IH}	V_{IH}=18V		18			0.3	uA
	I_{IL}	V_{IL}=0V		18			-0.3	uA
Quiescent Current	I_{DD}	V_{IN}=V_{SS},V_{DD}		5			4.0	uA
				10			8.0	uA
				15			16.0	uA

Current direction: + (no sign): Flowing into device
- : Flowing out of device

Electrical Characteristics at Ta=+85°C, V_{SS}=0V

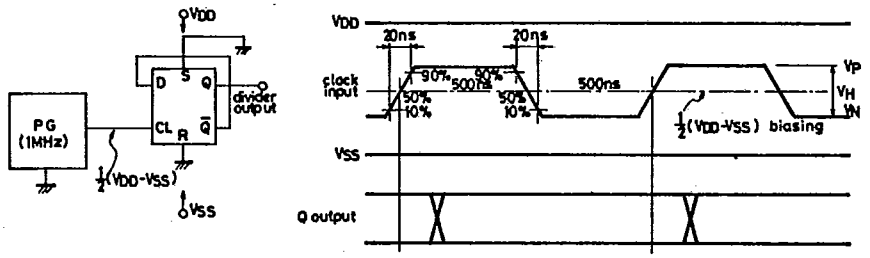
				V_{CC}	min	typ	max	unit
Output "H"-Level Voltage	V_{OH}	($\|I_{OUT}\|$<1uA, V_{IN}=V_{SS},V_{DD})		5	4.95			V
				10	9.95			V
				15	14.95			V
Output "L"-Level Voltage	V_{OL}	($\|I_{OUT}\|$<1uA, V_{IN}=V_{SS},V_{DD})		5			0.05	V
				10			0.05	V
				15			0.05	V
Output "H"-Level Current	I_{OH}	(V_{IN}=V_{SS}, V_{DD})	Vo=4.6V	5	-0.12			mA
			Vo=9.5V	10	-0.30			mA
			Vo=13.5V	15	-1.0			mA
Output "L"-Level Current	I_{OL}	(V_{IN}=V_{SS}, V_{DD})	Vo=0.4V	5	0.36			mA
			Vo=0.5V	10	0.90			mA
			Vo=1.5V	15	2.4			mA
Input "H"-Level Voltage (Inputs other than CLK)	V_{IH}	($\|I_{OUT}\|$<1uA)	Vo=0.5;4.5V	5	3.5			V
			Vo=1.0;9.0V	10	7.0			V
			Vo=1.5;13.5V	15	11.0			V
Input "L"-Level Voltage (Inputs other than CLK)	V_{IL}	($\|I_{OUT}\|$<1uA)	Vo=0.5;4.5V	5			1.5	V
			Vo=1.0;9.0V	10			3.0	V
			Vo=1.5;13.5V	15			4.0	V
Input Leakage Current	I_{IH}	V_{IH}=18V		18			1.0	uA
	I_{IL}	V_{IL}=0V		18			-1.0	uA
Quiescent Current	I_{DD}	Input V_{SS},V_{DD}		5			30	uA
				10			60	uA
				15			120	uA

Current direction: + (no sign): Flowing into device
- : Flowing out of device

Switching Characteristics at Ta=25°C±2°C, V_{SS}=0V, C_L=50pF

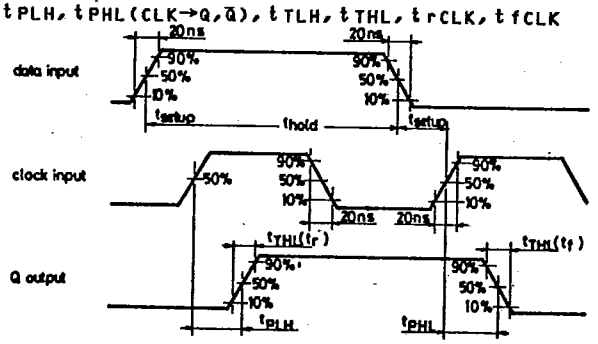
		V_{DD}	min	typ	max	unit
Output Rise Time	$t_{TLH(tr)}$	5		130	400	ns
		10		65	200	ns
		15		50	160	ns
Output Fall Time	$t_{THL(tf)}$	5		100	200	ns
		10		50	100	ns
		15		40	80	ns
Data Setup Time	t_{SETUP}	5		80	150	ns
		10		50	100	ns
		15		40	80	ns
Data Hold Time	t_{HOLD}	5		80	150	ns
		10		50	100	ns
		15		40	80	ns
Clock Rise/Fall Time	t_{rCLK}, t_{fCLK}	5			50	ms
		10			25	ms
		15			10	ms
Clock Frequency	f_{CLK}	5	1.0	2.0		MHz
		10	2.0	4.0		MHz
		15	3.0	6.0		MHz
"H"-Level Propagation Delay Time (CLK→Q,$\overline{Q}$)	t_{PLH}	5		350	700	ns
		10		150	300	ns
		15		100	200	ns
"L"-Level Propagation Delay Time (CLK→Q,$\overline{Q}$)	t_{PHL}	5		300	600	ns
		10		150	300	ns
		15		100	200	ns
"H"-Level Propagation Delay Time (RESET,SET→Q,$\overline{Q}$)	t_{PLH}	5		250	500	ns
		10		150	300	ns
		15		100	200	ns
"L"-Level Propagation Delay Time (RESET,SET→Q,$\overline{Q}$)	t_{PHL}	5		250	500	ns
		10		150	300	ns
		15		100	200	ns
Reset/Set Pulse Width	t_{WR}, t_{WS}	5		150	300	ns
		10		100	200	ns
		15		80	160	ns

Clock Input Hysteresis Test Circuit



Switching Time Test Waveforms

ⓐ f_{CLK}, t_{PLH}, t_{PHL} (CLK→Q, $\bar{Q}$), t_{TLH}, t_{THL}, t_{rCLK}, t_{fCLK}



ⓑ t_w, t_{PLH}, t_{PHL} (SET, RESET→Q, $\bar{Q}$)