DATA SHEET

TEA1206T
High efficiency DC/DC converter

Preliminary specification
Supersedes data of 1998 Mar 24
File under Integrated Circuits, IC03

1999 Sep 16

Philips Semiconductors

PHILIPS

High efficiency DC/DC converter TEA1206T

FEATURES

- Fully integrated DC/DC converter circuit
- Up-or-down conversion
- Start-up from 1.8 V input
- Adjustable output voltage
- High efficiency over large load range
- Power handling capability up to 1 A continuous average current
- 600 kHz switching frequency
- Low quiescent power consumption
- Synchronizes to external 9 to 20 MHz clock
- True current limit for Li-ion battery compatibility
- Up to 100% duty cycle in down mode
- Undervoltage lockout
- Shut-down function
- 8-pin SO package.

APPLICATIONS

- Cellular and cordless phones, PDAs and others
- Supply voltage source for low-voltage chip sets
- Portable computers
- Battery backup supplies
- Cameras.

GENERAL DESCRIPTION

The TEA1206T (see Fig.1) is a fully integrated DC/DC converter circuit. Efficient, compact and dynamic power conversion is achieved using a novel, digitally controlled Pulse Width and Frequency Modulation (PWFM) like control concept, integrated low R_{dsON} CMOS power switches with low parasitic capacitances, and fully synchronous rectification. The device operates at a high 590 kHz switching frequency which enables the use of minimum size external components. Deadlock is prevented by an on-chip undervoltage lockout circuit. Compatibility with Li-ion batteries is guaranteed by an accurate current limit function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1206T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage levels						
$V_{O(up)}$	output voltage range in up mode	$\overline{U}$/D = LOW	2.80	–	5.50	V
$V_{O(down)}$	output voltage range in down mode	$\overline{U}$/D = HIGH	1.25	–	5.50	V
$V_{i(up)}$	input voltage range in up mode	$\overline{U}$/D = LOW	V_{start}	–	5.50	V
$V_{i(down)}$	input voltage range in down mode	$\overline{U}$/D = HIGH	2.80	–	5.50	V
V_{start}	start-up voltage	up mode; I_L < 200 mA	1.40	1.60	1.85	V
V_{fb}	feedback voltage level		1.19	1.24	1.29	V
Current levels						
I_q	quiescent current at pin 3	down mode, V_i = 3.6 V	65	75	85	µA
I_{shdwn}	shut-down current		–	2	10	µA
I_{limN}	current limit NFET	up mode; note 1	0.5	–	5.0	A
I_{limP}	current limit PFET	down mode; note 1	0.5	–	5.0	A
I_{Lx}	maximum continuous current at pin 4		–	–	1.0	A
Power MOSFETS						
$R_{dsON(N)}$	pin-to-pin resistance NFET		0.08	0.14	0.20	Ω
$R_{dsON(P)}$	pin-to-pin resistance PFET		0.10	0.16	0.25	Ω
Efficiency; see Fig.5						
η	efficiency	V_i = 3.6 V; L = 10 µH	–	–	–	
	V_i = 3.6 up to 4.6 V	I_L = 1 mA	–	86	–	%
		I_L = 10 mA	–	93	–	%
		I_L = 50 mA	–	93	–	%
		I_L = 100 mA	–	93	–	%
		I_L = 500 mA	–	93	–	%
		I_L = 1000 mA; pulsed load current	–	87	–	%
	V_i = 3.6 down to 1.8 V	I_L = 1 mA	–	83	–	%
		I_L = 10 mA	–	90	–	%
		I_L = 50 mA	–	91	–	%
		I_L = 100 mA	–	87	–	%
		I_L = 500 mA	–	88	–	%
		I_L = 1000 mA; pulsed load current	–	82	–	%
Timing						
f_{sw}	switching frequency	PWM mode	475	560	645	kHz
f_{sync}	sync input frequency		9	13	20	MHz
t_{res}	response time from standby to P_{max}		–	25	–	µs

Note

1. Current limit is defined by an external resistor R_{lim}, having 1% accuracy. The typical value is presettable between 0.5 and 5.0 A with a spread of ±17.5%.

BLOCK DIAGRAM

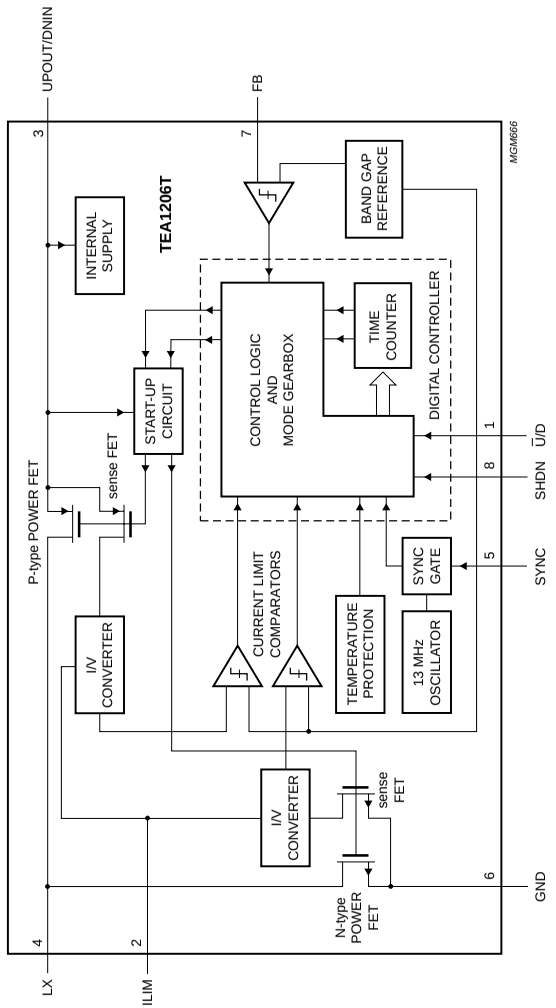


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{U}$/D	1	conversion mode selection input
ILIM	2	current limit resistor connection
UPOUT/DNIN	3	up mode; output voltage/ down mode; input voltage
LX	4	inductor connection
SYNC	5	synchronization clock input
GND	6	ground
FB	7	feedback input
SHDWN	8	shut-down input

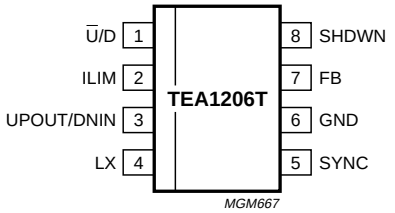


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Control mechanism

The TEA1206T DC/DC converter is able to operate in PFM (discontinuous conduction) or PWM (continuous conduction) operation. All switching actions are completely determined by a digital control circuit which uses the output voltage level as its control input. This novel digital approach enables the use of a new pulse width and frequency modulation scheme, which ensures optimum power efficiency over the complete range of operation of the converter. The scheme works as follows.

When high output power is requested, the device will operate in PWM (continuous conduction) mode. This results in minimum AC currents in the circuit components and hence optimum efficiency, cost and EMC. In this mode, the output voltage is allowed to vary between two predefined voltage levels. As long as the output voltage stays within this so-called window, switching continues in a fixed pattern. When the output voltage reaches one of the window borders, the digital controller immediately reacts by adjusting the pulse width and inserting a current step in such a way that the output voltage stays within the window with higher or lower current capability. This approach enables very fast reaction to load variations.

Figure 3 shows the converter's response to a sudden load increase. The upper trace shows the output voltage. The ripple on top of the DC level is a result of the current in the output capacitor, which changes in sign twice per cycle, times the capacitor's internal Equivalent Series Resistance (ESR). After each ramp-down of the inductor current, i.e. when the ESR effect increases the output voltage, the converter determines what to do in the next cycle. As soon as more load current is taken from the output the output voltage starts to decay. When the output voltage becomes lower than the low limit of the window, a corrective action is taken by a ramp-up of the inductor current during a much longer time. As a result, the DC current level is increased and normal PWM control can continue. The output voltage (including ESR effect) is again within the predefined window.

Figure 4 depicts the spread of the output voltage window. The absolute value is most dependent on spread, while the actual window size is not affected. For one specific device, the output voltage will not vary more than 2% typically.

In low output power situations, TEA1206T will switch over to PFM (discontinuous conduction) mode operation. In this mode, regulation information from earlier PWM mode operation is used. This results in optimum inductor peak current levels in PFM mode, which are slightly larger than the inductor ripple current in PWM mode. As a result, the transition between PFM and PWM mode is optimal under all circumstances. In PFM mode, TEA1206T regulates the output voltage to the high window limit shown in Fig.3.

Synchronous rectification

For optimal efficiency over the whole load range, synchronous rectifiers inside TEA1206T ensure that during the whole second switching phase, all inductor current will flow through the low-ohmic power MOSFETS. Special circuitry is included which detects that the inductor current reaches zero. Following this detection, the digital controller switches off the power MOSFET and proceeds regulation.

Start-up

Start-up from low input voltage in boost mode is realised by an independent start-up oscillator, which starts switching the N-type powerfet as soon as the voltage at pin 3 is measured to be sufficiently high. The switch actions of the start-up oscillator will increase the output voltage. As soon as the output voltage is high enough for normal regulation, the digital control system takes over the control over the power MOSFETS.

Undervoltage lockout

As a result of too high load or disconnection of the input power source, the output voltage can drop so low that normal regulation cannot be guaranteed. In that case, the device switches back to start-up mode. If the output voltage would drop down even further, switching is stopped completely.

Shut-down

When the shut-down pin is made HIGH, the converter disables both switches and power consumption is reduced to a few μA.

Power switches

The power switches in the IC are one N-type and one P-type MOSFET, having a typical pin-to-pin resistance of 0.14 Ω and 0.16 Ω respectively. The maximum average current in the switches is 1.0 A.

Temperature protection

When the device operates in PWM mode, and the device temperature gets too high (typically 175 °C), the converter stops operating. It resumes operation when the device temperature falls below 175 °C again. As a result, low-frequent cycling between on and off state will occur. It should be noted that in the event of device temperatures around the cut-off limit, the application differs strongly from maximum specifications.

Current limiters

If the current in one of the power switches exceeds its limit in PWM mode, current ramping is stopped immediately, and the next switching phase is entered. Current limitation is required to enable optimal use of energy in Lithium-Ion batteries, and to keep power conversion efficient during temporary high loads. Furthermore, current limitation protects the IC against overload conditions, inductor saturation, etc. The current limit level is set by an external resistor which must be connected to pin 2.

External synchronisation

If a high-frequency clock is applied to the external synchronisation pin, the switching frequency in PWM mode will be exactly that frequency divided by 22. In PFM mode, the switching frequency is always lower.
The quiescent current of the device increases when an external clock is applied. In case no external synchronisation is necessary, the sync pin must be tied to ground level.

Behaviour at regulation limits

In two cases, the output voltage will not stay in normal regulation because of excessive input voltage:

- Upconversion (see Fig.6): the output voltage will exceed the high window limit if the input voltage is higher than this limit plus the voltage drop over the diode. In that case, the converter will stop switching and the external schottky diode will take over all current. The output voltage will be equal to V_i minus the diode voltage drop. The input voltage must not exceed 5.5 V. The current limit function is not active since all current flows through the external diode in this situation.
- Downconversion (see Fig.7): the output voltage will get lower than the lower window limit when the input voltage is lower than this limit plus the voltage drop over the P-type FET. In that case, the P-type FET will stay conducting (100% duty cycle) resulting in V_o being equal to V_i minus some resistive voltage drop. The input voltage must not be lower than 2.8 V. The current limit function remains active.

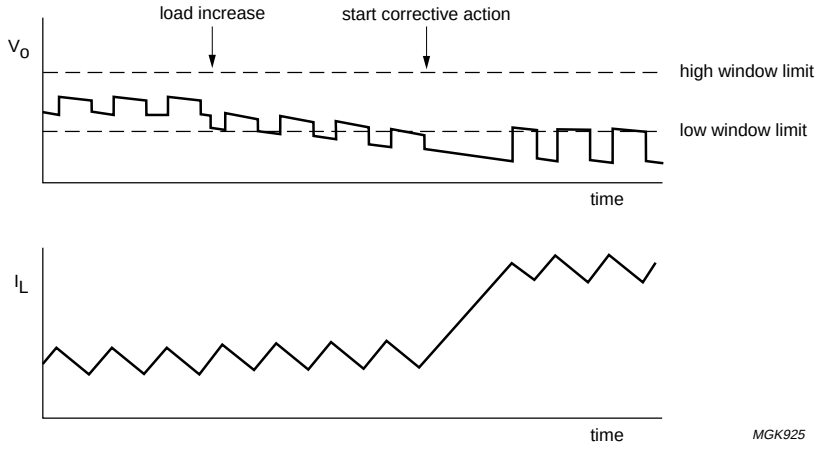


Fig.3 Response to load increase.

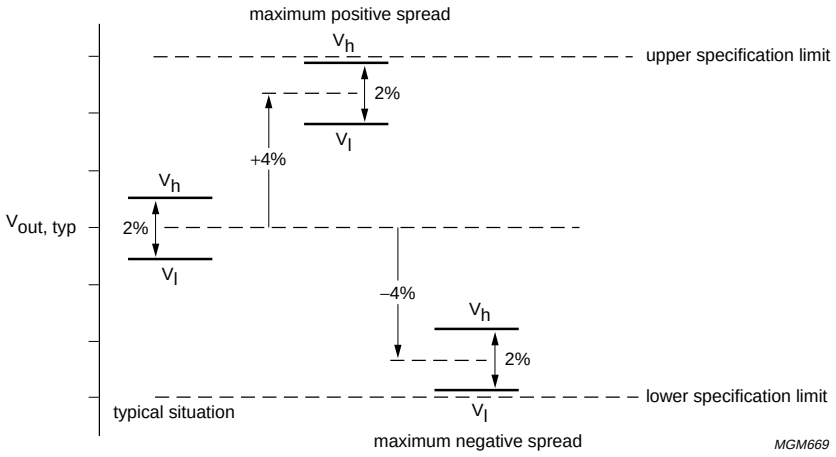


Fig.4 Output voltage window spread.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_n	voltage on any pin	shut-down mode	–0.2	+6.5	V
		operational mode	–0.2	+5.9	V
T_j	junction temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–40	+80	°C
T_{stg}	storage temperature		–40	+150	°C
V_{es}	electrostatic handling, pins 1,2,3,5,6,8	note 1	–3000	+3000	V
V_{es}	electrostatic handling, pins 4 and 7	note 1	–1000	+1000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	150	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611 part E”*.

CHARACTERISTICS

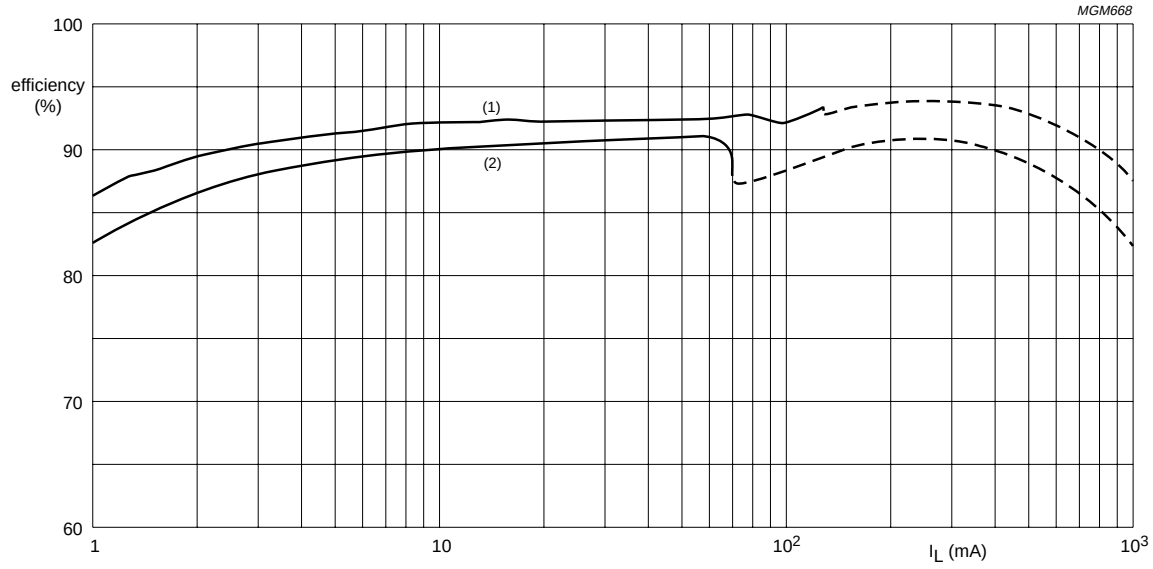
T_j = –40 to +80 °C; all voltages with respect to ground; positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage levels						
$V_{O(up)}$	output voltage range in up mode	$\overline{U}$/D = LOW	2.80	–	5.50	V
$V_{O(down)}$	output voltage range in down mode	$\overline{U}$/D = HIGH	1.25	–	5.50	V
$V_{i(up)}$	input voltage range in up mode	$\overline{U}$/D = LOW	V_{start}	–	5.50	V
$V_{i(down)}$	input voltage range in down mode	$\overline{U}$/D = HIGH; note 1	2.80	–	5.50	V
V_{start}	start-up voltage	up mode; I_L < 200 mA	1.40	1.60	1.85	V
V_{fb}	feedback voltage level		1.19	1.24	1.29	V
V_{wdw}	output voltage window spread	PWM mode; see Fig.4	1.5	2.0	3.0	%
V_{uvlo}	undervoltage lockout level	up mode; note 2	1.50	2.10	2.50	V
Current levels						
I_q	quiescent current at pin 3	V_3 = 3.6 V; note 3	65	75	85	µA
I_{shdwn}	shut-down current		–	2	10	µA
I_{limN}	current limit NFET	up mode; note 4	0.5	–	5.0	A
I_{limP}	current limit PFET	down mode; note 4	0.5	–	5.0	A
I_{Lx}	maximum continuous current at pin 4		–	–	1.0	A
Power MOSFETS						
$R_{dsON(N)}$	pin-to-pin resistance NFET		0.08	0.14	0.20	Ω
$R_{dsON(P)}$	pin-to-pin resistance PFET		0.10	0.16	0.25	Ω
Efficiency; see Fig.5						
η	efficiency	V_i = 3.6 V; note 5	–	–	–	
	V_i = 3.6 up to 4.6 V	I_L = 1 mA	–	86	–	%
		I_L = 10 mA	–	93	–	%
		I_L = 50 mA	–	93	–	%
		I_L = 100 mA	–	93	–	%
		I_L = 500 mA	–	93	–	%
		I_L = 1000 mA; pulsed load current	–	87	–	%
	V_i = 3.6 down to 1.8 V	I_L = 1 mA	–	83	–	%
		I_L = 10 mA	–	90	–	%
		I_L = 50 mA	–	91	–	%
		I_L = 100 mA	–	87	–	%
		I_L = 500 mA	–	88	–	%
		I_L = 1000 mA; pulsed load current	–	82	–	%
Timing						
f_{sw}	switching frequency	PWM mode	475	560	645	kHz
f_{sync}	sync input frequency		9	13	20	MHz
t_{res}	response time from standby to P_{max}		–	25	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Temperature						
T_{amb}	operating ambient temperature		–40	+25	+80	°C
T_{max}	internal cut-off temperature		150	175	200	°C
Digital levels						
V_{IL}	LOW-level input voltage pins 1, 5 and 8		0	–	0.5	V
V_{IH}	HIGH-level input voltage pin 1	note 6	$V_3 - 0.4$	–	$V_3 + 0.3$	V
V_{IH}	HIGH-level input voltage pins 5 and 8	note 6	$0.55V_3$	–	$V_3 + 0.3$	V

Notes

1. At V_i lower than the target output voltage, but higher than 2.8 V, the PFET will remain conducting (100% duty cycle), resulting in V_o following the input voltage.
2. The undervoltage lockout level shows wide specification limits since it decreases at increasing temperature. Since the minimum supply voltage of the digital control part also decreases when temperature goes up, correct operation of this function is guaranteed over the whole temperature range.
3. V_3 is the voltage at pin 3 (UPOUT/DNIN).
4. Current limit is defined by an external resistor R_{lim}, having 1% accuracy. The typical value is presettable between 0.5 and 5.0 A with a spread of ±17.5%.
5. The specified efficiency is valid when using an output capacitor having an ESR of 0.10 Ω and a Coilcraft DT1608C-103 10 µH small size inductor.
6. If the applied high level is less than $V_3 - 1$ V, the quiescent current level of the device will increase.



(1) Represents the curve for upconversion from 3.6 to 4.6 V. The solid line indicates PFM and the dashed line indicates PWM.
(2) Represents the curve for downconversion from 3.6 to 1,8 V. The solid line indicates PFM and the dashed line indicates PWM.
V_i = 3.6 V; L = 10 µH (DT1608-103); C_{out} = 330 µF (Sprague 595D) capacitor.

Fig.5 Efficiency as a function of load current I_L.

APPLICATION INFORMATION

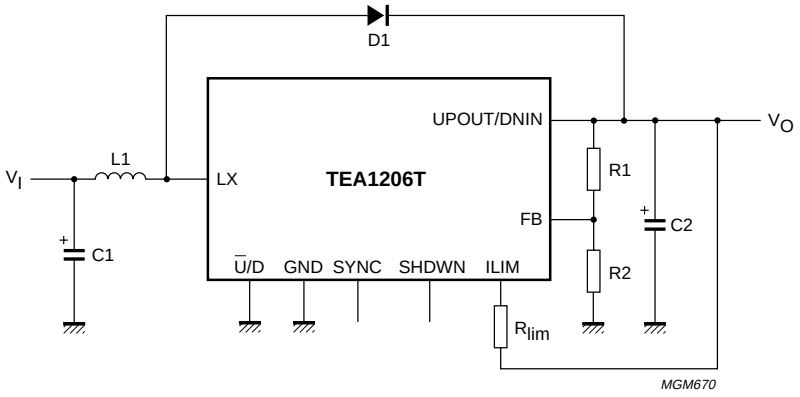


Fig.6 Complete application for upconversion.

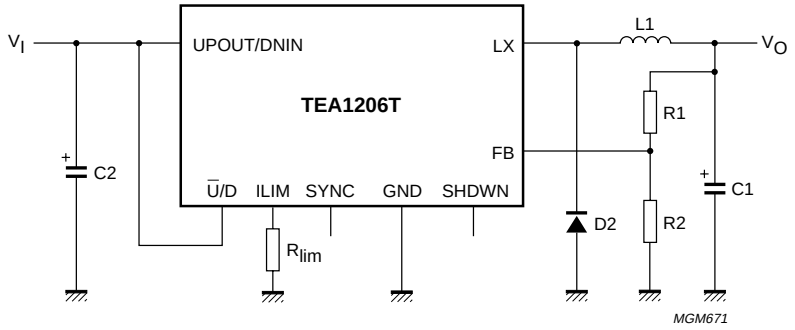


Fig.7 Complete application for downconversion.

External component selection

Inductor

The performance of the TEA1206 is not very sensitive to inductance value. Best efficiency performance over a wide load current range is achieved by using e.g. TDK SLF7032-6R8M1R6, having an inductance of 6.8 μH and a saturation current level of 1.6 A. In case the maximum output current is lower, other inductors are also suitable like the small sized Coilcraft DT1608 range.

Input capacitance

The value of C_{in} strongly depends on the type of input source. In general, a 100 μF tantalum capacitor will do, or a 10 μF ceramic capacitor featuring very low series resistance (ESR).

Output capacitor

The value and type of C_{out} depends on the maximum output current and the ripple voltage which is allowed in the application. Low-ESR tantalum as well as ceramic capacitors show good results. Most important specification of C_{out} is its ESR, which mainly determines output voltage ripple.

Diode

The schottky diode is only used during a small time during takeover from N-type powerfet and P-type powerfet and vice versa. Therefore, a medium-power diode like Philips PRLL5819 is sufficient.

Output voltage setting

The output voltage level is determined by the resistors R1 and R2. The following conditions apply:

- Use 1% accurate SMD type resistors only. In case larger body resistors are used, the capacitance on pin 7 (FB) will be too large, causing inaccurate operation.
- Resistors R1 and R2 shall have a maximum value of 50 kΩ when connected in parallel. A higher value will result in inaccurate operation.

Under these conditions, the output voltage can be set by the formula: $V_{out} = 1.24 \times (1 + R1/R2)$.

Current limit setting

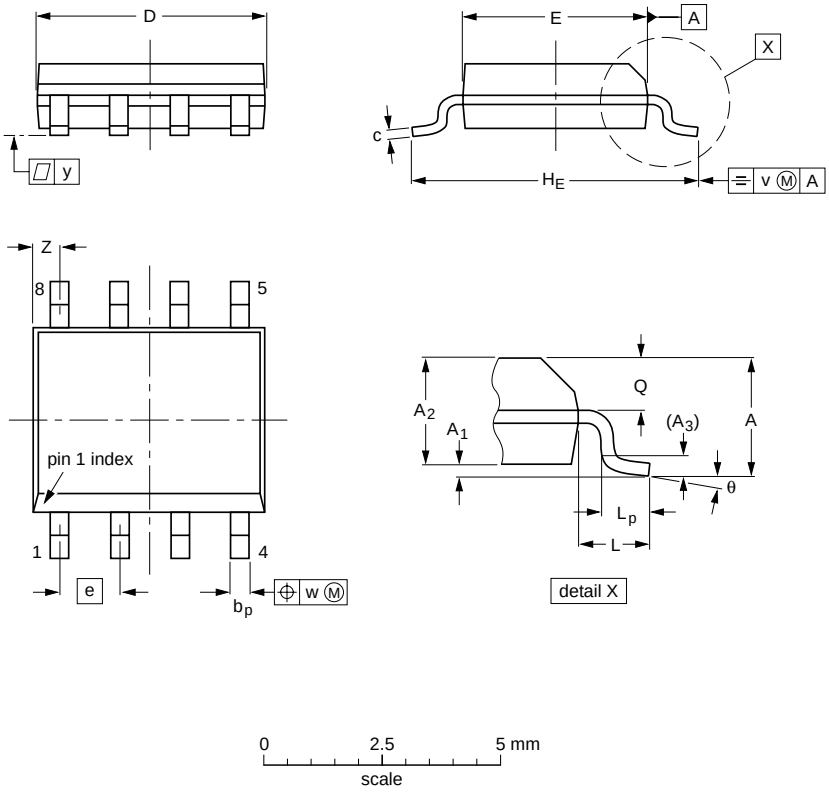
The maximum instantaneous current is set by the external resistor R_{lim}. Preferred type is SMD, 1% accurate.
The connection of R_{lim} differs per mode:

- In UP conversion mode, R_{lim} must be connected between pin 2 (ILIM) and pin 3 (UPOUT/DNIN).
  The current limit level is defined by: $I_{limN} = 440/ R_{lim}$.
- In DOWN conversion mode, R_{lim} must be connected between pin 2 (ILIM) and pin 6 (GND).
  The current limit level is defined by: $I_{limP} = 650/ R_{lim}$.

The average inductor current during current limit also depends on inductance value and resistive losses in all components in the power path. Ensure that $I_{lim} < I_{sat}$ of the inductor.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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