SC453

Portable, VID Programmed Single Phase Power Supply Controller

POWER MANAGEMENT

Description

The SC453 IC is a single chip high-performance Hysteretic PWM controller. With its integrated SmartDriver™, it powers advanced graphics and core processors. It provides sleep mode and boot voltage support. Automatic "power-save" is present to prevent negative current flow in the low-side FET during light loading conditions saving even more power. The high side driver initially turns on with a weak drive to reduce ringing, EMI, and capacitive turn-on of the low side.

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A 6-bit DAC, accurate to 0.85%, sets the output voltage reference, and implements the 0.700V to 1.708V range required by the processor. The hysteretic converter uses a comparator without an error amplifier, and therefore provides the fastest possible transient response, while avoiding the stability issues inherent to classical PWM controllers. The DAC is externally slew rate limited to minimize transient currents and audible noise.

The SC453 operates from 5VDC and also features soft-start, an open-drain PWRGD signal with power good blanking, and an enable input. Programmable current limiting shuts down the SC453 after 32 current limit pulses.

Features

- High Speed Hysteretic Controller
- Single Phase Operation
- Selectable Analog or VID Controlled Sleep Setting
- 6 Bit VID programmable Output
- Integrated Drivers with Soft-High Side Turn-On
- Programmable Soft-Start
- Programmable Boot Voltage
- Programmable Sleep Voltage with Sleep Mode
- Under-Voltage Lockout on VCCA
- Over-voltage Protection on CORE
- Current Limit Protection on CORE
- Thermal Protection
- Power Good Flag with Blanking During V_{CORE} Changes
- Automatic Power Save at Light Load
- TSSOP-28 Package

Applications

- Low Power Notebook and Laptop Computers
- Embedded Applications

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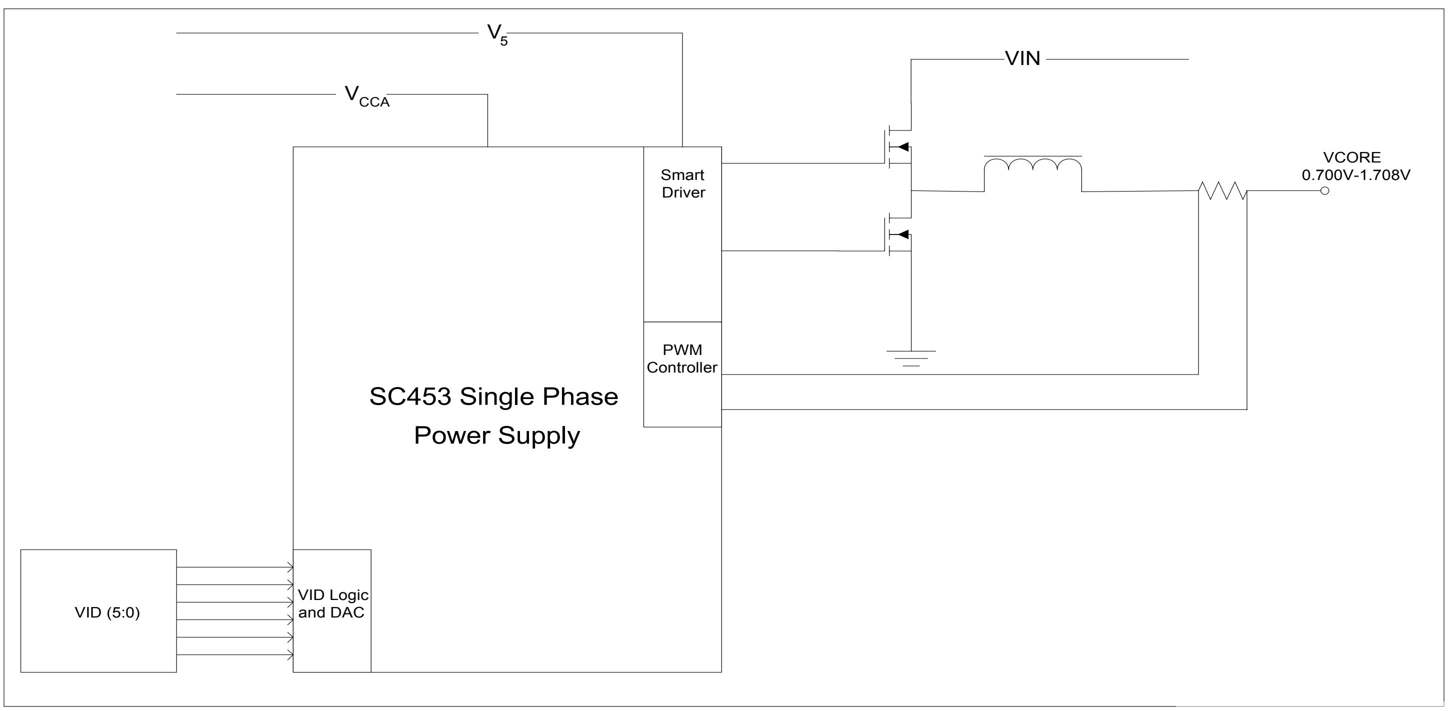
Typical Application Circuit



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Reference Design

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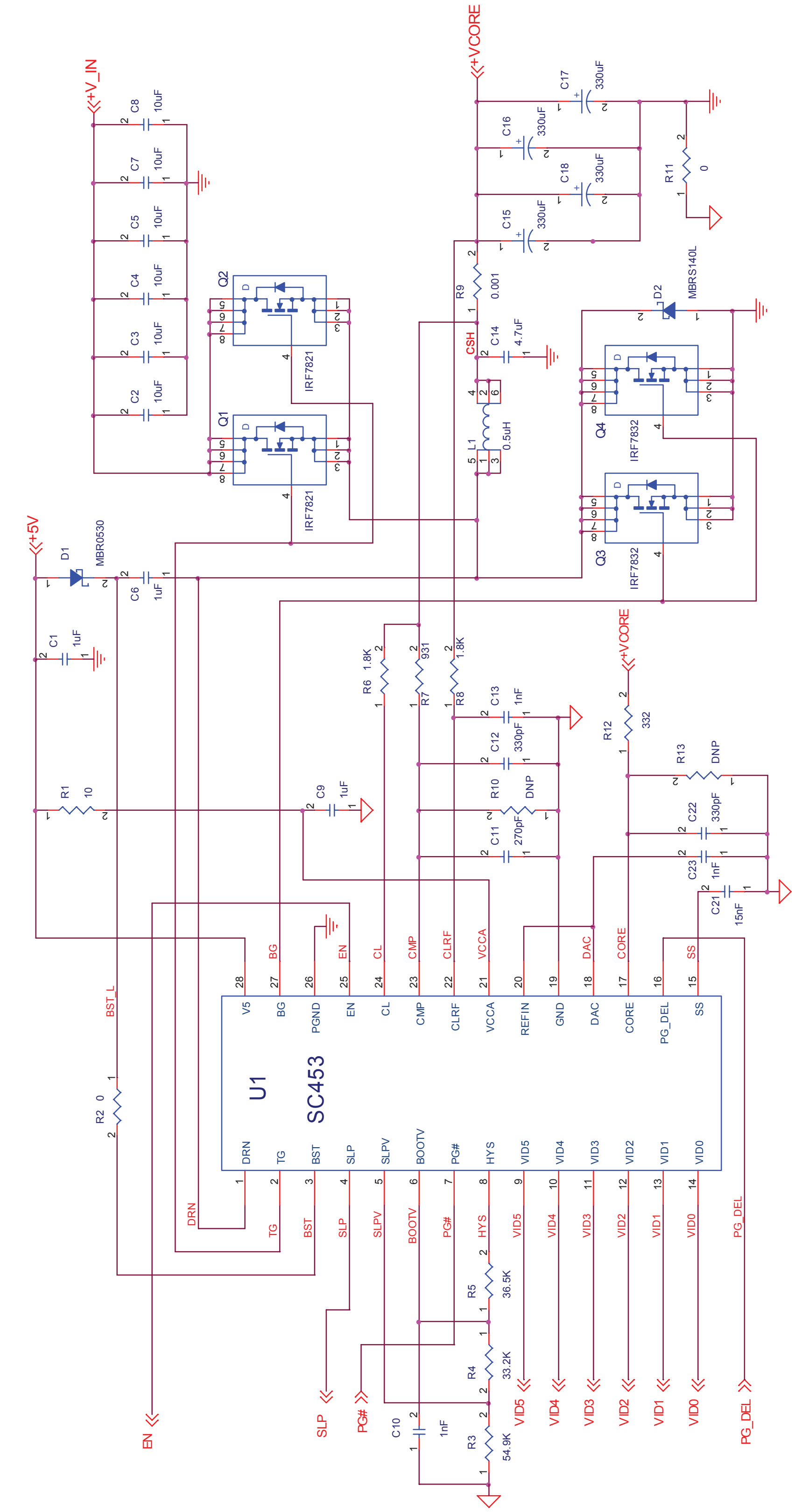

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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Min	Max	Units
Supply Voltages	V_{CCA}, V_5		-0.3	7	V
Input and Output Voltages	VSLPV, V SLP, V VID [0.5], V DAC, V REFIN, V CMP, V HYS, V CORE, V CL, V CLRF, V PG#, V BOOTV, V SS, V GND, V BG, V CLSET		-0.3	V_{CCA} +0.3	V
EN	V_{EN}			7	V
BST to PGND		Static	-0.3	36	V
BST to PGND		Transient < 100ns		40	V
BST to DRN			-0.3	7	V
DRN to PGND		Static	-2	30	V
DRN to PGND		Transient < 100ns	-5	34	V
TG	T_{STG}		-2	BST +0.3	V
PGND to AGND			-0.3	0.3	V
Thermal Resistance Junction to Ambient	θ_{JA}	TSSOP-28		70	°C/W
Thermal Resistance Junction to Case	θ_{JC}	TSSOP-28		20	°C/W
Lead Temperature (Soldering) 10s	T_{LEAD}	TSSOP-28		300	°C
Peak IR Reflow Temperature 10 - 40s	T_{PKG}	TSSOP-28		260	°C

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NOTES:
(1) Calculated from package in still air, mounted to 3” x 4.5”, 4 layer FR4 PCB.
(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless otherwise specified: V_{IN} = 15V, V_{CCA} = 5V, and V5 = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply (V_{IN}, V_{CCA}, V_5)						
V_{IN} Supply Voltage Range	V_{IN}		3.0		25	V
V_5 Supply Voltage Range	V_5		4.3	5.0	6.0	V
V_{CCA} Voltage Range	V_{CCA}		4.5	5.0	6.0	V
V_{CCA} Quiescent Current	I_{CCQ}	EN is low			10	μA
		EN is high in UVLO		400		μA

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Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{CCA} Operating Current	I_{CC}			5		mA
Under-Voltage Lockout Circuits (V_{CCA}, V_5)						
Threshold (V_{CCA} falling)	V_{HCCA}		3.47	3.70	3.93	V
V_{CCA} Hysteresis	$V_{HYST\ CCA}$			190		mV
Threshold (V_5 falling)	V_{HV5}		3.85	4.00	4.25	V
V_5 Hysteresis	$V_{HYST\ V5}$			210		mV
Fixed Over-Voltage Protection (CORE)						
Threshold (CORE Rising)	$V_{TH\ CORE\ FIXED}$		1.95	2.00	2.05	V
Enable Input (EN)						
Input High	$V_{iH\ (EN)}$		2			V
Input Low	$V_{iL\ (EN)}$				0.8	V
V_{CORE} Power Good Generator (PG_DEL, PG#)						
Core Input Threshold	$V_{TH\ CORE}$	V_{DAC} = 0.6 - 1.75V; Note: during UVLO, the output level of this signal is undefined — Upper Threshold	1.1× V_{DAC}		1.15× V_{DAC}	V
		Lower Threshold	0.86× V_{DAC}		0.9× V_{DAC}	V
		Hysteresis		1		%
PG# Output Voltage	$V_{PG\#}$	Pulled up with external 680Ω resistor to $V_{PULL-UP}$ — $V_{CORE} = V_{DAC}$			0.4	V
		Either $V_{CORE} < 0.88*V_{DAC}$, or, $V_{CORE} > 1.12*V_{DAC}$	0.95× $V_{PULL-UP}$			V
		EN is low or EN is high but UVLO condition	0.95× $V_{PULL-UP}$			V
PG_DEL Output Voltage	V_{PG_DEL}	$V_{CORE} = V_{DAC}$ pulled-up with external 680Ω resistor to $V_{PULL-UP}$ 1.2V	0.95× $V_{PULL-UP}$			V
		Either $V_{CORE} < 0.88*V_{DAC}$, or, $V_{CORE} > 1.12*V_{DAC}$			0.4	V
		EN is low or EN is high but UVLO condition			0.8	V
PG_DEL Delay (at start-up)		Measured from PG# assertion		1007		Clocks

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Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Soft-Start & DAC Slew (SS)						
Soft-Start/DAC Slew Current Note: SS cap is not discharged until EN goes low or UVLO cuts in. To enable the converter, SS has to drop below V_{SS_EN}.	I_{SS}	Discharge (sink) Current	5	10		mA
		Soft-Start transition $0 < T_A < 85°C$, $-40 < T_A < 85°C$	7.5	10.5	16	µA
		Sleep Exit, $0 < T_A < 85°C$	204	256	310	
		Sleep Exit, $-40 < T_A < 85°C$	180	240	320	
		VID Transition, $0 < T_A < 85°C$	102	128	155	
		VID Transition, $-40 < T_A < 85°C$	90	120	160	
Soft-Start Enable Threshold	V_{SS_EN}			40	100	mV
DAC (VID [5:0])						
VID Input Threshold	V_{iH_VID}		0.55			V
	V_{iL_VID}				0.45	
DAC Output Voltage Accuracy	V_{DAC_ERR}	$0° < T_A < 85°C$, VID [5:0] = 000000 "111111(1.708V" 0.812V)	-0.85		+0.85	%
		$-25°C < T_A < 85°C$, VID [5:0] = 000000 "111111 (1.708V" 0.700V)	-2.0		+2.0	%
Boot Voltage (BOOTV)						
Input Voltage Offset	V_{BOOTV}-V_{DAC}	BOOTV = 1.2V			|±3|	%
BOOT Delay Time[1]	TBOOT		10	35		µs
Sleep (SLP, SLPV)						
Input Voltage Offset	V_{SLPV}-V_{DAC}	SLPV = 0.8V			|±3|	%
SLP Logic Threshold	V_{iH_SLP}		2			V
	V_{iL_SLP}				0.8	
CORE Comparator (CMP, REFIN, HYS)						
Input Bias Current	I_{REFIN}	V_{REFIN} = 1.3V			|±2|	µA
Input Voltage Offset	V_{CMP} - V_{REFIN}			|±1.5|	|±3|	mV

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Electrical Characteristics (Cont.)

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Parameter	Symbol	Conditions		Min	Typ	Max	Units
CORE Comparator (CMP, REFIN, HYS) (Cont.)							
Hysteresis Setting Current SLP = low	I_{CMP}	R_{HYS} = 17K	$V_{CMP} < V_{REFIN}$	-110	-100	-90	µA
			$V_{CMP} > V_{REFIN}$	90	100	110	
		R_{HYS} = 170K	$V_{CMP} < V_{REFIN}$	-7	-10	-13	
			$V_{CMP} > V_{REFIN}$	7	10	13	
Hysteresis Setting Current SLP = high	$I_{SLP\_}I_{CMP}$	R_{HYS} = 17K	$V_{CMP} < V_{REFIN}$	-83	-73	-63	µA
			$V_{CMP} > V_{REFIN}$	63	73	83	
Current Limit Comparator (CL, CLRF, HYS)							
Input Bias Current	I_{CL}	$V_{CL1,2}$ = 1.3V				|±2|	µA
Input Voltage Offset	$V_{CL}-V_{CLRF}$				|±3|	|±5|	mV
Current Limit Setting Current SLP = low	I_{CLRF}	R_{HYS} = 17K	$V_{CL} < V_{CLRF}$	150	200	250	µA
			$V_{CL} > V_{CLRF}$	250	300	350	
		R_{HYS} = 170K	$V_{CL} < V_{CLRF}$	15	20	25	
			$V_{CL} > V_{CLRF}$	25	30	35	
Current Limit Setting Current SLP = high	I_{SLP_CLRF}	R_{HYS} = 17K	$V_{CL} < V_{CLRF}$	120	150	180	µA
			$V_{CL} > V_{CLRF}$	195	230	265	
Zero-Crossing (Powersave) Comparators (CL, CORE)							
Offset	$V_{CL}-V_{CORE}$					|±5|	mV
High Side Driver (TG)							
Peak Output Current(1)	I_{pkh}				1.5		A
Output Resistance	R_{SRC_TG}	I = 100mA, $V_{BST}-V_{DRN}$ = 5V	V_{DRN} < 1V		4.2		Ω
			V_{DRN} > 1V		1	4	
	R_{SINK_TG}	I = 100mA, $V_{BST}-V_{DRN}$ = 5V			0.7	1.4	Ω
Rise Time(1)	tr_{TG}	C_{TG} = 3nF, $V_{BST}-V_{DRN}$ = 5V			60		ns
Fall Time(1)	tf_{TG}	C_{TG} = 3nF, $V_{BST}-V_{DRN}$ = 5V			36		ns

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Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High Side Driver (Cont.)						
Propagation Delay TG Going High[(1)]	$tpdh_{TG}$	CMP crossing REFIN to 10% point of TG, C_{TG} = 3nF, BG = 0V		45		ns
Propagation Delay TG Going Low[(1)]	$tpdl_{TG}$	CMP crossing REFIN to 90% point of TG, C_{TG} = 3nF		45		ns
Shoot-thru Protection Delay Time[(1)]	tspd		21	30	39	ns
Low Side Driver (BG)						
Peak Output Current[(1)]	I_{pkl}			3		A
Output Resistance	R_{SRC_BG}	I = 100mA, V5 = 5V		1.0	2.6	Ω
	R_{SINK_BG}			0.5	1.2	
Rise Time[(1)]	tr_{BG}	C_{BG} = 3nF, V5 = 5V		25		ns
Fall Time[(1)]	tf_{BG}	C_{TG} = 3nF, V = 5V		15		ns
Propagation Delay TG Going High[(1)]	$tpdh_{BG}$	CMP crossing REFIN to 10% point of BG, C_{BG} = 3nF, DRN = 0V		35		ns
Propagation Delay TG Going Low[(1)]	$tpdl_{BG}$	CMP crossing REFIN to 90% point of TG, C_{TG} = 3nF, DRN = 0V		35		ns

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Notes:
1) Guaranteed by design.

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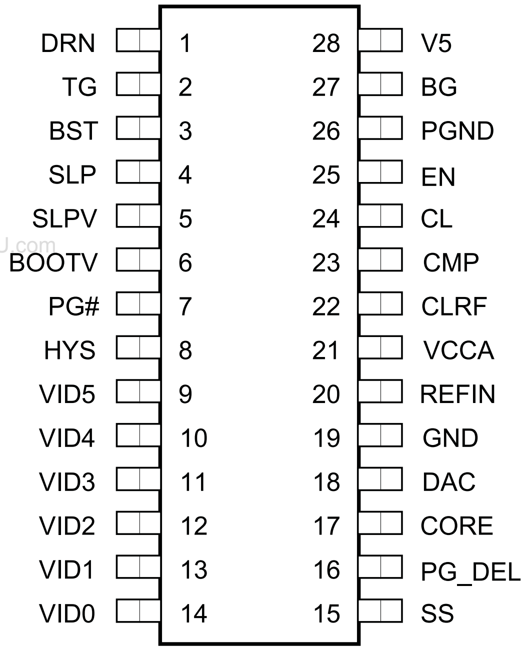
Pin Configuration

TOP VIEW



(28 Pin TSSOP)

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Ordering Information

Device	Package	Temp Range(T_J)
SC453TSTRT	TSSOP-28	-40°C to + 125°C
SC453EVB	EVALUATION BOARD	

Notes:

1. Only available in tape and reel packaging. A reel contains 2500 devices.
2. Lead-free package compliant with J-STD-020B. Qualified to support maximum IR reflow temperature of 260°C for 30 seconds.
3. This device is ESD sensitive. Use of standard ESD handling precautions is required.
4. All parameters subject to change without notice.
5. Lead-free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin#	Pin Name	Pin Function
1	DRN	This pin connects to the junction of the switching and synchronous MOSFETs.
2	TG	Output gate drive for the switching (high-side) MOSFET.
3	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET.
4	SLP	Sleep logic input signal.
5	SLPV	Connect this pin to V_{CCA} to select "VID Sleep Mode". Otherwise, "SLPV Sleep Mode" is selected and the voltage on this pin sets the DAC output during sleep.
6	BOOTV	The voltage on this pin sets the BOOT-Up voltage.
7	PG#	Start clock indicator - open drain output. Active low.
8	HYS	Core Comparator Hysteresis. Connect to ground thru an external resistor called R_{HYS}. Hysteresis current is established by an internal V_{REF} voltage, 1.7V, divided by R_{HYS}.
9	VID5	VID most significant bit main controller voltage programming DAC input.
10	VID4	VID input.

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Pin Descriptions (Cont.)

Pin#	Pin Name	Pin Function
11	VID3	VID input.
12	VID2	VID input.
13	VID1	VID input.
14	VID0	VID least significant bit main controller voltage programming DAC input.
15	SS	Soft-start. An external cap defines the soft-start ramp.
16	PG_DEL	Delayed power good - open drain output. When the Main Converter Output approaches and stays within ± 14% of the VID_DAC setting, and the t_{CPU_PWRGD} period has terminated. This signal is pulled high by an external resistor.
17	CORE	Main CORE converter output feedback to the power good generator. A small RC filter should be used to filter out any HF component to prevent faulty trip condition.
18	DAC	Main controller digital-to-analog output.
19	GND	Analog ground.
20	REFIN	Core Comparator reference input pin. Connect to DAC.
21	VCCA	5V supply for precision analog circuitry.
22	CLRF	Current limit reference input pin
23	CMP	Core Comparator input pin.
24	CL	Current limit input pin.
25	EN	Enable - active high. This is capable of accepting a 5.0V signal level.
26	PGND	Power ground. Connect to the synchronous FET power ground.
27	BG	Output drive for the synchronous (low-side) FET.
28	V5	5VDC supply for the driver. A capacitor should be connected from V5 to GND.

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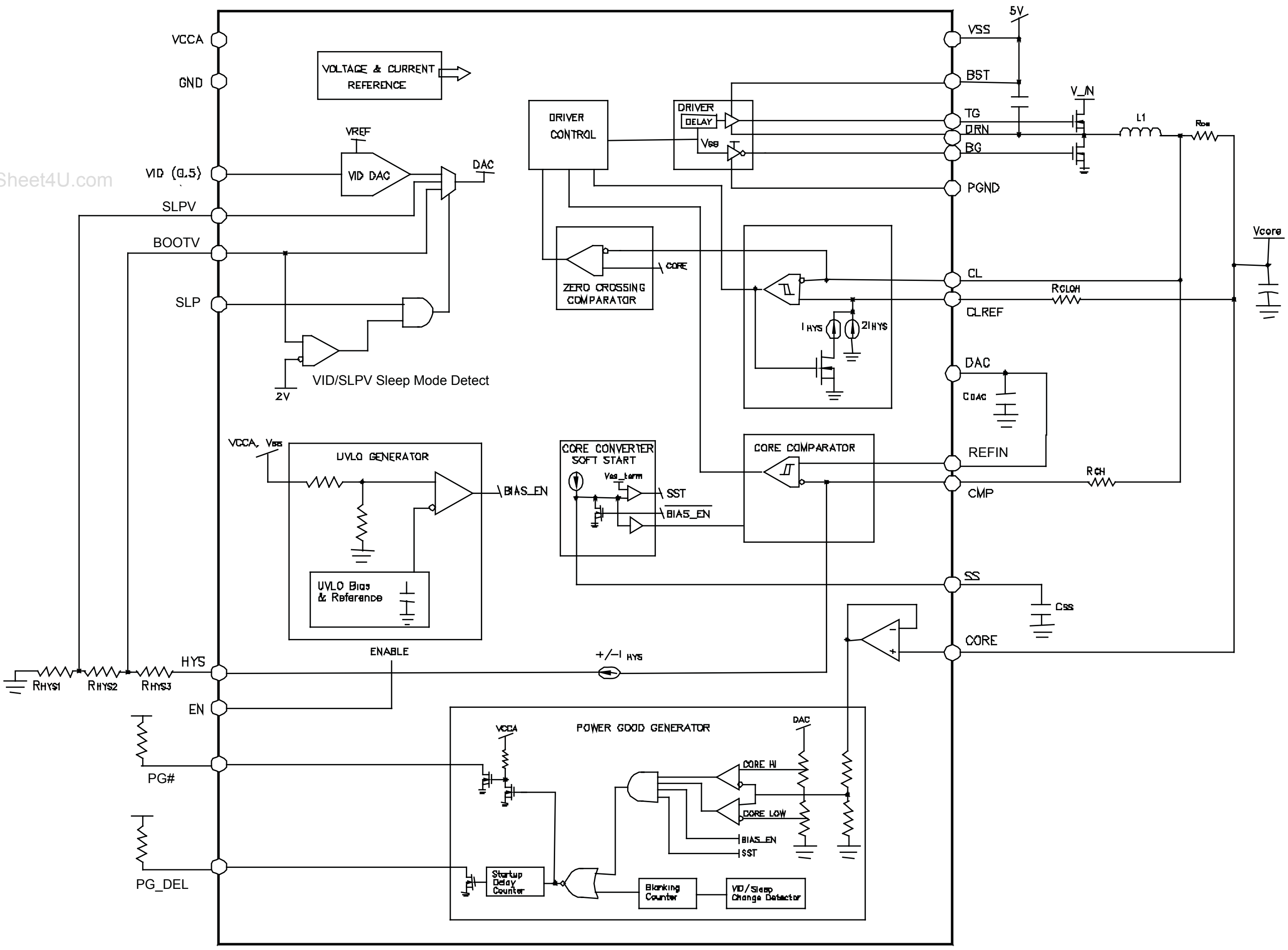
Block Diagram



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Applications Information (Cont.)

SUPPLY, BIAS, UVLO, POWER GOOD GENERATOR

Supply
The chip is optimized to operate from a 5V ± 5% rail but also designed to work up to 6V maximum supply voltage.

Under-Voltage Lock-Out Circuit
The Under-Voltage Lock-Out Circuit consists of comparators which monitor the VCCA and V5 voltage levels. The SC453 is in UVLO mode while either supply has not ramped above the upper threshold or has dropped below the lower threshold. During UVLO, the external FETs are held off, tri-stating the output (DRN).

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Over-Voltage Protection
If the CORE voltage is greater than +14% of the DAC (i.e., out of the power good window), the SC453 will latch off and hold the low-side driver on permanently. Either the power or EN must be recycled to clear the latch. The latch is disabled during soft-start and VID/Sleep transitions. For safety, the latch is enabled if the CORE voltage exceeds 2V even during VID/Sleep transitions.

Thermal Shutdown
The device will be disabled and latched off when the internal junction temperature reaches approximately 160°C. Either the power or EN must be recycled to clear the latch.

Band Gap Reference
A ± 0.85% precision Band Gap reference acts as the internal reference voltage standard of the chip, which all critical biasing voltages and currents are derived from. All references to VREF in the equations to follow will assume VREF = 1.7V.

Precision DAC
This 6-bit digital-to-analog converter (DAC) serves as the programmable reference source of the Core Comparator. Programming is accomplished by logic voltage levels applied to the DAC inputs. The VID code vs. the DAC output is shown in the following table. The accuracy of the VID /DAC is maintained on the same level as the Band Gap reference.

VID						V_{DAC}	VID						V_{DAC}
5	4	3	2	1	0	V	5	4	3	2	1	0	V
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

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CORE CONVERTER CONTROLLER

Core Comparator

This is an ultra-fast hysteretic comparator with a typical propagation delay of about 20ns at a 20mV overdrive. Hysteresis is generated by the current set at the HYS pin impressed upon an external resistor connected to the CMP pin.

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Current Limit Comparator

The Current Limit Comparator monitors the core converter output current and turns off the high side FETs when the current exceeds the upper current limit threshold, VHCL and is re-enabled only if the phase current drops below the lower current limit threshold, VLCL. The current is sensed by monitoring the voltage drop across the current sense resistor, RCS connected in series with the core converter inductor. VHCL and VLCL are fixed by the current set at the HYS pin impressed upon an external resistor connected to the CLRF pin.

Current Limit Latch

If the CORE voltage goes lower than 14% below the VID (i.e., out of the power good window), then sustained current limiting (32 current limit pulses) will cause the part to permanently latch off. The latch is inhibited during soft-start.

Core Converter Soft-Start Timer

This block controls the start-up ramp time of the CORE voltage up to the boot voltage. The primary purpose is to reduce the initial in-rush current on the core input voltage (battery) rail.

Cycle-by-Cycle Power-Save

A zero crossing comparator detects when the currents through the external sense resistor reduces to zero. When the current in the external sense resistor reaches zero, the bottom FET is latched off. The latch is reset when the controller decides to switch on the top FET. This prevents excessive switching at light loads and hence saves switching power losses.

DAC Slew Control

The output of the DAC will slew at a rate defined by the current in the SS pin and the capacitor applied externally to the SS pin. The slew rate (charge current) applied depends on which mode (soft-start, VID or sleep transition) is in effect. The SS capacitor together with the DAC capacitor will determine the stability of the DAC, a 1nF capacitor is recommended for the DAC pin.

Blanking During VID Changes

On any VID change or Sleep change, the PG# and PG_DEL signals are blanked for 62 switching cycles to prevent glitching during the transition.

Sleep Function

In sleep mode, the DAC output is set by the voltage on the SLPV pin when the SLP pin is held high. In "VID Sleep" mode, the DAC output is set by the VID bits when SLP is held high. During sleep, the hysteresis and current limit hysteresis currents are reduced to 70% of their nominal values.

SLPV/VID Sleep Mode

By default, the controller is in "SLPV controlled Sleep" mode. In this mode, the voltage applied to the SLPV pin appears at the DAC output when SLP is asserted.

By holding the SLPV pin at VCCA during start-up, "VID controlled sleep" mode is engaged. In this mode, the DAC output continues to be set by the VID inputs even when SLP is asserted.

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Applications Information (Cont.)

PG# Output

This is an open-drain output and should be pulled up externally. This signal is asserted (pulled low) by the SC453 whenever the core voltage is within ±14% of the VID programmed value. If the chip is disabled or enabled in UVLO, then PG# is de-asserted. During start-up PG# remains de-asserted until the core voltage has reached the defined boot voltage and remains there for the BOOT period (10µS minimum). This signal is forced low (asserted) during VID and sleep transitions.

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PG_DEL Output

This signal is delayed a minimum of 3mS from first assertion of the PG# signal. This is an open drain output and should be pulled up externally. This signal is asserted (open drain) by the SC453 whenever the core is within ±14% of the VID programmed value. If the chip is disabled or enabled in UVLO, then PG_DEL is de-asserted. The signal is forced high (open drain) during VID and sleep transitions.

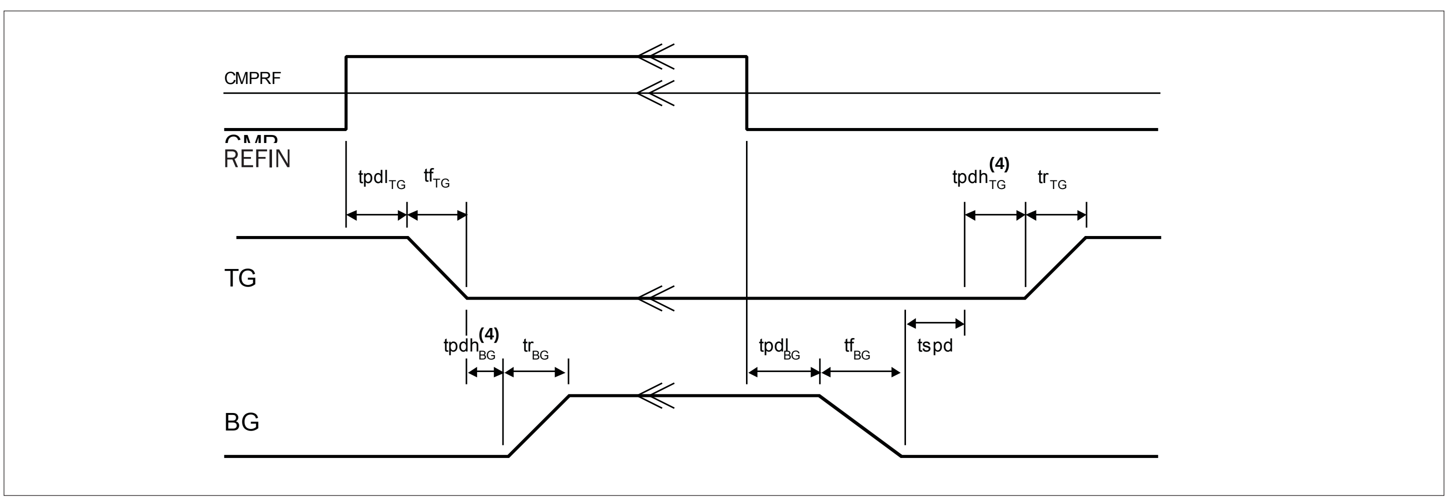
Start-Up and Sequencing

On start-up, V_{CORE} ramps to the boot voltage set by the BOOTV pin irrespective of the status of the VID pins. After a minimum of 10µs, PG# asserts, and V_{CORE} responds to the VID inputs. The controller will then count 1007 switching cycles before asserting PG_DEL.

Summary of Fault Conditions

Protection Mode	Latched?	When Active	Driver Status	SS Pin Status
Supply UVLO (VCCA, V5)	No	Always	All low	Low
32 Cycle Current Limit	Yes	SS has terminated and PGDEL is low	TG low	Sawtooth
114% V_{CORE} OVP	Yes	SS has terminated and PGDEL is low	BG high	High
2.0V_{CORE} OVP	Yes	Always	BG high	High
Thermal Shutdown	Yes	Always	BG, TG low	High

Driver Timing Diagram



Note (4): subtract a typical value of 17ns for the core comparator delay since this parameter is specified from a CMP edge.

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DESIGN PROCEDURE

Step 1: Define Constants

$V_{INMAX} := 20V$	Maximum input voltage
$V_{INMIN} := 8V$	Minimum input voltage
$I_{MAX\_FL} := 20A$	Maximum load current, highest output voltage
$I_{LKGMAX} := 5A$	Leakage current, highest output voltage
$V_{MAX\_NL} := 1.212V$	The highest V_{CORE} voltage
$V_{MIN\_NL} := 0.956 \cdot V$	The lowest V_{CORE} voltage
$V_{REF} := 1.7V$	SC453 Internal reference voltage
$C_{OUT} := 330 \cdot \mu F$	Output capacitance per cap
$R_{ESR} := 6m \cdot \Omega$	ESR per cap
$R_{CS} := 1m \cdot \Omega$	Current sense resistor
$R_{CU} := 0.5m \cdot \Omega$	Parasitic resistance from the current sense resistor to the processor
$V_{POS\_TRANS} := 50mV$	Voltage droop allowed for a low current to high current transient
$V_{NEG\_TRANS} := 50mV$	Voltage rise allowed for a high current to low current transient
$V_{RIPPLE} := 20m\,V$	Desired maximum output ripple

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Step 2: Output Inductor and Capacitor Selection

The SC453 has "passive" droop. The voltage at full load is less than the DAC voltage by the voltage drop across the current sense resistor and any PCB copper losses from the sense resistor to the processor socket. The steady-state voltage at full load is:

$$V_{MAX\_FL} := V_{MAX\_NL} - \left(R_{CS} + R_{CU}\right) \cdot I_{MAX\_FL}$$

$$V_{MAX\_FL} = 1.182\ V$$

Output capacitance and ESR values are a function of transient requirements and output inductor value. Figure 1 illustrates the response of a hysteretic converter to a positive transient. In a hysteretic converter with passive droop, like the SC453, two conditions determine if you meet the positive transient requirements.

A. $$ESR \le \frac{V_{POS\_TRANS}}{\left(I_{MAX\_FL} - I_{LKGMAX}\right)}$$

B. $$V_{NEG\_TRANS} \ge \text{deltaV}\left(C_{OUT}\right)$$

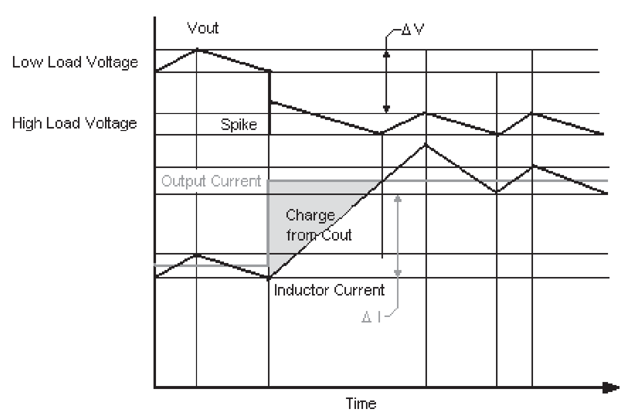

Figure 1 - Hysteretic Converter Response to a Positive Transient

The first condition is easy to see; if the ESR is too high, the transient response will fail.

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Applications Information (Cont.)

In the second condition, because the hysteretic converter responds in < 100ns, the capacitor does not droop very far before the inductor current starts ramping up. (This is not true of control schemes where time constants in the error amplifier cause delays.) Once the inductor current starts to rise, the increasing ΔV of the capacitor is offset by reduced ΔV from the ESR, so ΔV is constant. If the ΔV due to the charge taken from the capacitor before the inductor current reaches the load current (note the shaded area on the graph) is less than VPOS_TRANS, then the transient response passes.

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Since the highest output voltage has the most severe requirements, any other modes are satisfied by a design optimized for the highest output voltage.

C.

$$ESR_{MAX} := \frac{V_{POS\_TRANS}}{\left(I_{MAX\_FL} - I_{LKGMAX}\right)}$$

$$ESR_{MAX} = 3.333 \times 10^{-3}\,\Omega$$

For the second condition, we need to know the inductor value, which is a function of the highest desired switching frequency. The maximum frequency occurs at the highest input voltage. As a reasonable compromise between efficiency and component size, a maximum switching frequency of 350kHz is desired.

D.

$$F_S := 350\,K\cdot Hz$$

E.

$$d_{MIN} := \frac{V_{MAX\_NL}}{V_{INMAX}}$$

F.

$$L_{MIN} := d_{MIN}\cdot\frac{\left(V_{INMAX} - V_{MAX\_NL}\right)\cdot\left(ESR_{MAX} + R_{CS}\right)}{F_S\cdot V_{RIPPLE}\cdot\left(\frac{ESR_{MAX} + R_{CS}}{ESR_{MAX}}\right)}$$

$$L_{MIN} = 5.422 \times 10^{-7}\,H$$

Based on the following four factors: 1) minimum inductance requirement; 2) device availability at the time we designed the evaluation board; 3) low DCR ; 4) height and package size consideration. Keep in mind, the choice you make should be based upon the requirement of the converter design, including minimum inductance, minimum saturation current, efficiency, foot area, maximum allowable height, and of course, device availability. In the current demo board design,

G.

$$L_1 := 0.60\cdot\mu H$$

This value of inductance is required up to maximum load. Inductors with a "swinging choke" characteristic, where the zero current value of inductance is much less than the full load current inductance can be used, as long as the above restriction is met. Then, the worst-case (low input voltage) response time (the time for the current to reach the new transient value) is:

H.

$$dT := \frac{L_1\cdot\left(I_{MAX\_FL} - I_{LKGMAX}\right)}{V_{INMIN} - V_{MAX\_NL}}$$

$$dT = 1.326 \times 10^{-6}\,s$$

Add ~100ns for the propagation delay from a change at the output to the MOSFET switch turning on in reaction. Since the shaded area is triangular, the total charge taken out of the capacitor = (dI / dt) / 2. Q = C / dV = (dI / dt) / 2, therefore;

I.

$$C_{MINP} := \frac{\left(I_{MAX\_FL} - I_{LKGMAX}\right)\cdot\left(dT + 1\cdot 10^{-7}\cdot sec\right)}{V_{POS\_TRANS}}$$

$$C_{MINP} = 4.278 \times 10^{-4}\,F$$

This condition applies only to the positive transient.

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Applications Information (Cont.)

LOAD RELEASE

The worst-case for the transient load release to happen is when the hysteresis has just reached the maximum, (i.e., the high-side switch has just turned of); at this time the inductor has reached its peak current.

$$I_{RIPPLE} := \frac{\left(V_{INMAX} - V_{MAX\_FL}\right) \cdot d_{MIN}}{L_1 \cdot F_S} \cdot \frac{L_1}{L_{MIN}}$$

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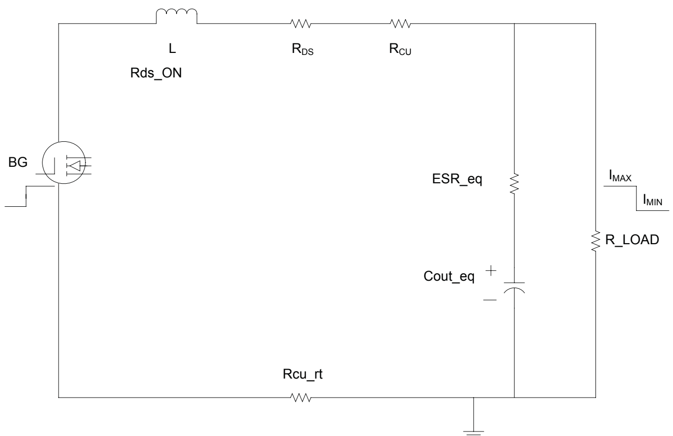
$$I_{RIPPLE} = 6.01\ A$$

$$I_{t0} := I_{MAX\_FL} + \frac{I_{RIPPLE}}{2}$$

$$I_{t0} = 23.005\ A$$

Load is stepping from high to low.



Immediately after the load steps down from I_{MAX} to I_{MIN}, the high side FET is turned off, and the bottom FET is turned on after the dead time. We assume for the worst-case condition, at t = 0, the output inductor is sitting at its maximum; after t = 0, the inductor discharges at a rate equal to V_{FL} / L. (without the consideration of the secondary order effect, such as, Rds_on drop, current sense resistor and copper losses). The energy released from the output inductor during load step-down, charges the output capacitors and is dissipated through the following means: Rds_on, Rcs, Rcu, Rcu_rt, ESR of the output capacitors and load.

$$t := 0, 10n \cdot s .. 10\mu \cdot s$$

$$I_L(t) := \left(I_{t0} - \frac{V_{MAX\_FL} \cdot t}{L_1}\right)$$

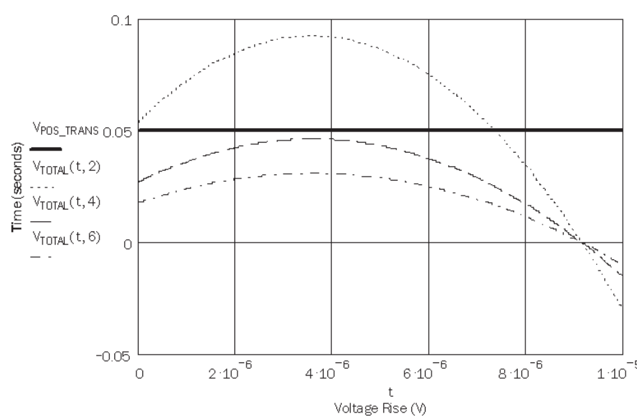
$$I_{CAP}(t) := I_L(t) - I_{LKGMAX}$$

Since the output inductor is discharging at a fixed rate, there are two terms contributing to the increase of the voltage on the output capacitors: 1) is due to the ESR of the output capacitor; 2) is due to the added charge contributed by the inductor current.

J. $$V_{ESR}\left(t, N_{CAP}\right) := I_{CAP}(t) \cdot \frac{R_{ESR}}{N_{CAP}}$$

K. $$dV_{CAP}\left(t, N_{CAP}\right) := \frac{I_{CAP}(t) \cdot t}{C_{OUT} \cdot N_{CAP}}$$

L. $$V_{TOTAL}\left(t, N_{CAP}\right) := V_{ESR}\left(t, N_{CAP}\right) + dV_{CAP}\left(t, N_{CAP}\right)$$



The chart above shows the system response for the capacitors defined in Step 1 and the chart to follow shows the details of the response for the chosen number of output capacitors.

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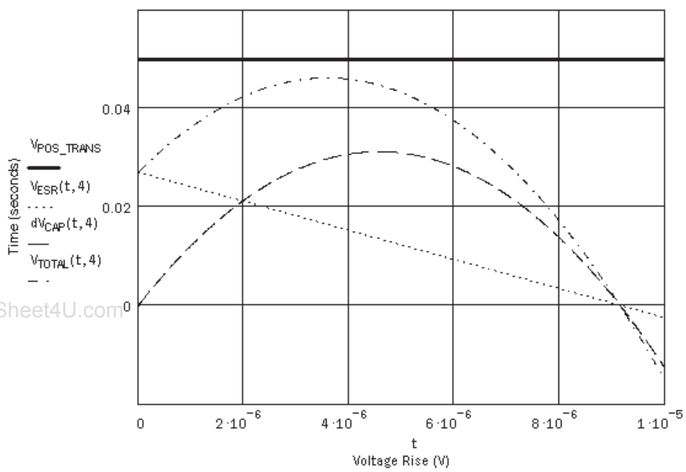

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Step 3: Setting RHYS

The next step is to calculate R_{HYS}. Since the SC453 is a hysteretic controller, it regulates the amount of output ripple according to a hysteresis value set by R_{HYS}. The designer must therefore decide upon the amount of desired output ripple, and then set R_{HYS} accordingly.

The hysteresis controls the amount of ripple at the point of regulation, which is the point between the inductor and the current sense resistor. The amount of ripple at the output is defined by the current sense resistor and the output cap, ESR. This factor is taken into account in the equation shown below relating V_{RIPPLE} to V_{HYS}.

To achieve tight accuracy, it is recommended that the output ripple be set to 20mV peak-to-peak.

$$ESR := \frac{R_{ESR}}{N_{CAP}} \qquad ESR = 1.5 \times 10^{-3}\,\Omega$$

$$V_{RIPPLE} = 0.02\text{ V}$$

M. $$V_{HYS} := V_{RIPPLE}\cdot\frac{(R_{CS} + ESR)}{ESR}$$

$$V_{HYS} = 0.033\text{ V}$$

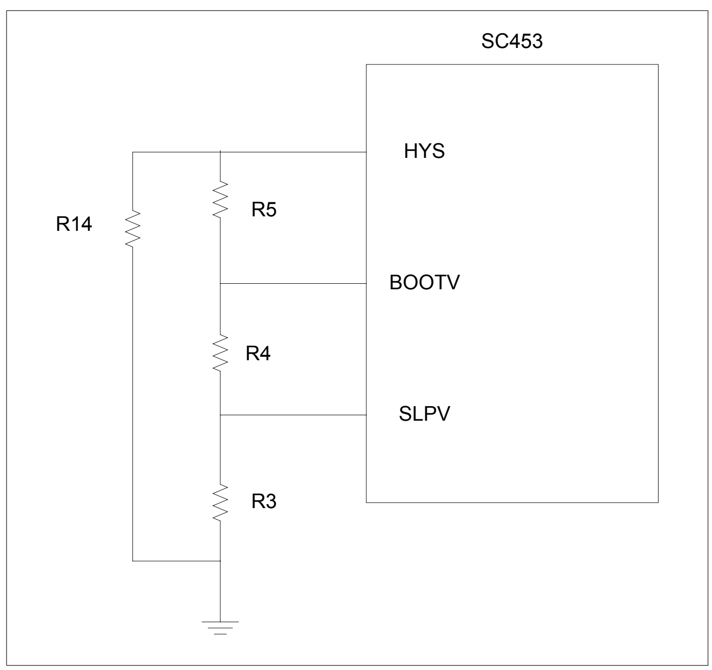
V_{HYS} is created by a current source, I_{HYS}, through R9 (see the diagram below). The current source value is controlled via R_{HYS}. For simplicity it is easier to select a value for R7 (the resistor in series with the CMP pin) first, and then calculate R_{HYS}, as follows:

N. $$R_7 := 1K\cdot\Omega$$

$$R_{HYS} := \frac{2\cdot V_{REF}}{\left(\frac{V_{HYS}}{R_7}\right)} \qquad R_{HYS} = 102.0\text{ K}\Omega$$

.

In the SC453 application circuit, R_{HYS} consists of three resistors (R3, R4 and R5). These resistors also form the dividers for BOOTV and SLPV. Note also that depending on circuit layout and parasitics, R_{HYS} may have to be adjusted slightly to obtain optimum performance. (We will come back to calculate the above resistors after we set the PBOOT and Deeper Sleep voltages). To increase hysteresis without having to change the divider resistors, a fourth resistor (R14), can be added. Additional hysteresis is needed when inductances in the current sense paths cause additional signal that add to the resistive signal, limiting the accuracy of the calculations.



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Applications Information (Cont.)

Step 4: BOOTV Design

The boot-up voltage for V_{CORE} is set at 1.2V. For the SC453 typical application circuit, R3, R4, and R5 form a voltage divider off V_{REF} and are used to set the boot voltage. For simplicity, we define R_{BOOT} : = R3 + R4.

O.

$$V_{BOOT} := 1.2V$$

$$R_{HYS} := \frac{1}{\frac{1}{R_{25}} + \frac{1}{R_{BOOT} + R_5}}$$

P.

$$R_{BOOT} := \frac{V_{BOOT} \cdot R_5}{V_{REF} - V_{BOOT}}$$

Step 5: Sleep Voltage Design

The sleep voltage is set at 0.750V nominally using the R3 - R4 - R5 divider.

Q.

$$V_{SLP} := 0.750V$$

$$R_3 := V_{SLP} \cdot \frac{(R_4 + R_5)}{V_{REF} - V_{SLP}}$$

R3, R4 and R5 are calculated using a matrix to solve the simultaneous equations. R14 is set at 1MΩ as a place-holder:

$$R_{14} := 1000\,K\Omega$$

$$M_x := \begin{pmatrix} 1 & 1 & 1 \\ 1 & 1 & -\frac{V_{BOOT}}{V_{REF} - V_{BOOT}} \\ 1 & V_{SLP} \cdot \frac{-1}{V_{REF} - V_{SLP}} & V_{SLP} \cdot \frac{-1}{V_{REF} - V_{SLP}} \end{pmatrix}$$

$$v := \begin{pmatrix} \frac{R_{14} \cdot R_{HYS}}{R_{14} - R_{HYS}} \\ 0 \\ 0 \end{pmatrix}$$

$$soln := lsolve(M_x, v) \qquad soln = \begin{pmatrix} 5.011 \times 10^4 \\ 3.007 \times 10^4 \\ 3.341 \times 10^4 \end{pmatrix} \Omega$$

$$R_3 := (1\ \ 0\ \ 0) \cdot soln \qquad R_3 = 5.011 \times 10^4\,\Omega$$

$$R_4 := (0\ \ 1\ \ 0) \cdot soln \qquad R_4 = 3.007 \times 10^4\,\Omega$$

$$R_5 := (0\ \ 0\ \ 1) \cdot soln \qquad R_5 = 3.341 \times 10^4\,\Omega$$

From the standard 1% resistor value table, we choose the following values according to the calculation results:

R5 = 33.2KΩ.
R4 = 30.1KΩ
R3 = 49.9KΩ

Step 6: Current Limit Calculation

Setting the threshold for current limit is a relatively straightforward process. To do this we must calculate the peak current based on the maximum DC value plus the worst-case ripple current. The following calculations apply for a single phase. Worst-case ripple occurs at the highest input voltage. Since ripple is also inversely proportional to inductance, it is recommended that the minimum inductance value be used based on the manufacturer's specified tolerance:

$$L_{LOW} := L_1 \cdot (1 - 20\%) \qquad L_{LOW} = 4.8 \times 10^{-7}\,H$$

R.

$$I_{RIPPLE\_MAX} := \frac{(V_{INMAX} - V_{MAX\_NL}) d_{MIN}}{L_{LOW} \cdot F_S}$$

$$I_{RIPPLE\_MAX} = 6.777\,A$$

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Applications Information (Cont.)

To calculate the maximum DC value of current we must add the maximum DC current and the maximum ripple value to obtain peak current:

S. $$I_{PEAK} := I_{MAX\_FL} + \frac{I_{RIPPLE\_MAX}}{2}$$

$$I_{PEAK} = 23.389\ A$$

It is recommended that the current limit be set at 120% of the peak value to allow for inductor current overshoot during load transients:

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T. $$I_{CLIM} := 120\% \cdot I_{PEAK}$$

$$I_{CLIM} = 28.066\ A$$

The Current Limit Comparator internal to the SC453 monitors the output current and turns the high side switch off when the current exceeds the upper current limit threshold, I_{CLMAX} and re-enables only if the load current drops below the lower current limit threshold, I_{CLMIN}. The current is sensed by monitoring the voltage drop across the current sense resistor R_{CS}.

Current limiting will cycle from I_{CLMAX} to I_{CLMIN} for 32 switching cycles to allow for short term transients, then the converter is latched off. I_{CLMAX} and I_{CLMIN} are set according to the following equations:

U. $$I_{CLMAX} := 3 \cdot V_{REF} \cdot \frac{R_{CL}}{R_{HYS} \cdot R_{CS}}$$

$$I_{CLMIN} := 2 \cdot V_{REF} \cdot \frac{R_{CL}}{R_{HYS} \cdot R_{CS}}$$

We set the current limit at I_{CLIM} = ICLMAX, and then solve for R_{CL}, which is R6 in the typical applications circuit. For balance, R8, in series with the CLRF pin is kept the same value as R6.

V. $$R_{CL} := \frac{I_{CLIM} \cdot R_{HYS} \cdot R_{CS}}{2.5 \cdot V_{REF}}$$

$$R_{CL} = 673.59\ \Omega \qquad R_6 := 681\Omega$$

$$R_8 := R_6 \qquad R_8 = 681\ \Omega$$

Step 7: Small Capacitors/Resistor Selection

Several small capacitors are required for signal filtering. Use SMT ceramic capacitors with an X7R or better temperature coefficient. COG is preferred.

C11, which filters the output voltage feedback, is sized to provide filtering beyond the 5th harmonic of the fundamental.

W. $$C11 := \frac{1}{2 \cdot \Pi \cdot R_7 \cdot F_S \cdot 5}$$

$$C11 = 9.095 \times 10^{-11} F$$

In the evaluation board design, we use 100pF, 603, X7R ceramic caps for C11. The DAC output requires a 1nF, X7R or COG capacitor (C23) for high frequency noise filtering. The values for C12 and C13 are calculated in a similar manner, though they are returned to the CORE pin because that is the reference point for the current limit comparator.

X. $$C_{12} := \frac{1}{2 \cdot \Pi \cdot R_6 \cdot F_S \cdot 5} \qquad C_{13} := C_{12}$$

$$C_{12} = 1.335 \times 10^{-10} F \qquad C_{13} = 1.335 \times 10^{-10} F$$

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Step 8: Calculate Input RMS Current

In order to calculate the worst-case input RMS current, we need to assume the efficiency at V_{IN_MIN} and full load. From the measurement result, we are safe to assume 80%, (this number is very conservative, actual efficiency should be much higher). The actual converter efficiency depends on component selection, layout, airflow, etc.

$$P_{OUT} := I_{MAX\_FL} \cdot V_{MAX\_FL} \qquad P_{OUT} = 23.64\ W$$

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$$P_{IN} := \frac{P_{OUT}}{85\%}$$

$$I_{IN\_DC} := \frac{P_{IN}}{V_{INMIN}} \qquad D := \frac{V_{MAX\_FL}}{V_{INMIN}} \qquad I_{IN\_DC} = 3.476\ A$$

$$I_{RMS} := \sqrt{\left[\left(I_{MAX\_FL}\right) - I_{IN\_DC}\right]^2 \cdot D + \left[I_{IN\_DC}{}^2 \cdot (1 - D)\right]}$$

$$I_{RMS} = 7.116\ A$$

$$C_{I\_RMS} := 2A$$

10µF@25V, MLCC cap from Panasonic is rated 2A RMS.

$$C_{I\_NUM} := \mathrm{ceil}\left(\frac{I_{RMS}}{C_{I\_RMS}}\right) \qquad C_{I\_NUM} = 4$$

The calculation indicates four of these MLCC caps satisfy the worst-case RMS current requirement.

Input Capacitance Calculation:
(based on ripple voltage)

dVin is the allowable input ripple voltage contributed by the amount of input capacitance. For this exercise, we use 250mV as the allowable input ripple voltage. The maximum value occurs at D = 0.5

$$dVin := 250\,mV$$

$$D_{MAX} := 0.5$$

$$T_{in} := \frac{1}{F_S}$$

$$C_{IN\_MIN} := \frac{I_{PEAK}}{2} \cdot \left(D_{MAX} - D_{MAX}{}^2\right) \cdot \frac{T_{in}}{dVin}$$

$$C_{IN\_MIN} = 3.341 \times 10^{-5}\ F$$

$$C_{IN} := 10\,\mu F$$

$$N_{IN\_MIN\_RIPPLE} := \mathrm{ceil}\left(\frac{C_{IN\_MIN}}{C_{IN}}\right)$$

$$N_{IN\_MIN\_RIPPLE} = 4$$

Based on the above calculations, we choose N = 4 for the input capacitor.

Step 9: OVP

No calculations are necessary for Over-Voltage Protection. If V_{CORE} is greater than +14% of the DAC (i.e., out of the power good window), the SC453 will latch off and hold the low-side driver on permanently (for each phase). Either the power or EN must be recycled to clear the latch. The latch is disabled during soft-start and VID/DeeperSleep transitions. The latch is enabled if V_{CORE} exceeds 2V even during VID/DeeperSleep transitions to ensure that the processor maximum is not exceeded. The table on Page 13 is a summary of fault conditions using SC453.

Step 10: Soft-Start/DAC Slew Control

The soft-start cap C21 in the SC453 design serves three conditions: 1) to define the soft-start ramp; 2) to define the DAC slew rate during sleep and VID transitions (during VID transitions the SS current is nominally +/- 120µA. During sleep transitions the SS current increases to +/- 240µA); 3) during start-up, the SS current is normally +/- 6.5µA.

We will be doing three soft-start exercises based on the above three conditions for SC453 application:

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Applications Information (Cont.)

1. Start-Up:

$$I_{SS} := 6.5\ \mu A$$

$$dt_{SU} := 3\ ms$$

$$dV_{dacSU} := V_{MAX\_NL}$$

$$C_{SS\_max\_startup} := \frac{I_{SS} \cdot dt_{SU}}{dV_{dacSU}}$$

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$$C_{SS\_max\_startup} = 1.609 \times 10^{-8}\ F$$

2. VID Change:

$$I_{SSV} := 120\ \mu A$$

$$dt_{V} := 100\ \mu s$$

$$dV_{dacV} := V_{MAX\_NL} - V_{MIN\_NL}$$

$$C_{SS\_max\_VID} := \frac{I_{SSV} \cdot dt_{V}}{dV_{dacV}}$$

$$C_{SS\_max\_VID} = 4.687 \times 10^{-8}\ F$$

3. Sleep Entry/Exit:

$$I_{SSS} := 240\ \mu A$$

$$dt_{S} := 33\ \mu s$$

$$dV_{dacS} := V_{MAX\_NL} - V_{SLP}$$

$$C_{SS\_max\_drs} := \frac{I_{SSS} \cdot dt_{S}}{dV_{dacS}}$$

$$C_{SS\_max\_drs} = 1.714 \times 10^{-8}\ F$$

Exercise #1 predicts the max capacitance allowed. In order to allow tolerance, we choose C22 = 15nF.

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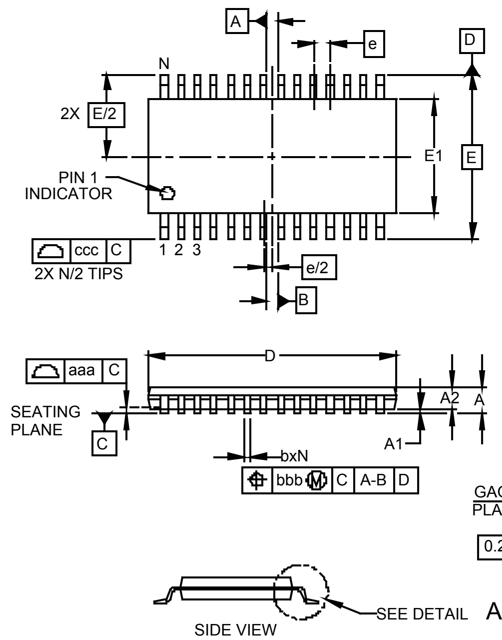
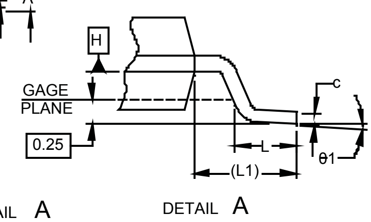
Outline Drawing - TSSOP-28



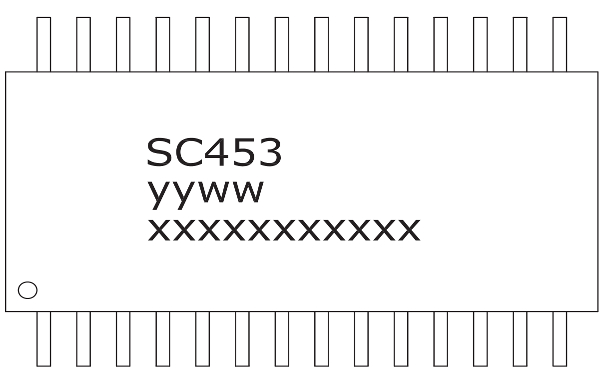
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.378	.382	.386	9.60	9.70	9.80
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	28			28		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AE.

Marking Information



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Land Pattern - TSSOP-28

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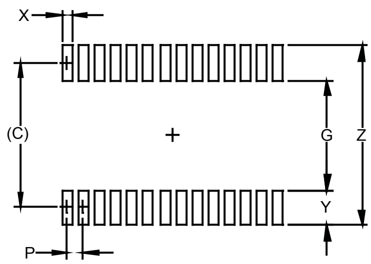

DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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