Device Features

- Fully Qualified Bluetooth v2.0 + EDR System
- Enhanced Data Rate (EDR) compliant with v2.0 of specification for both 2Mbits/s and 3Mbits/s modulation modes
- Full-speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- 1.8V core, 1.7 to 3.6V I/O Split Rails
- Ultra Low Power Consumption
- Excellent Compatibility with Cellular Telephones
- Minimum External Components Required
- Integrated 1.8V Linear Regulator
- USB and UART Port to 3MBits/s
- Support for 802.11 Co-existence
- RoHS Compliant

BlueCore™4-ROM CSP EDR

Single Chip Bluetooth® v2.0 + EDR System

Product Data Sheet for

BC41B143A

September 2005

BlueCore™4-ROM CSP EDR Product Data Sheet

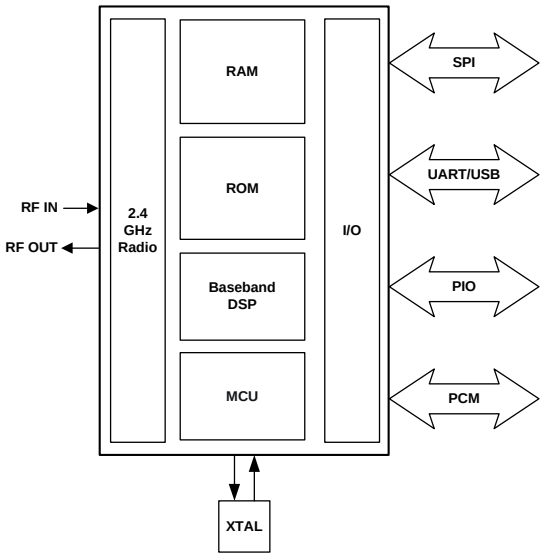
General Description

BlueCore4-ROM CSP is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including EDR to 3Mbits/s.

With the on-chip CSR Bluetooth software stack it provides a fully compliant Bluetooth system to v2.0 + EDR of the specification for data and voice communications.

Applications

- Cellular Handsets
- Personal Digital Assistants (PDAs)
- Digital cameras and other high-volume consumer products
- Space critical applications



BlueCore4-ROM CSP System Architecture

BlueCore4-ROM CSP is designed to reduce the number of external components required. This ensures that production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.0 + EDR Specification (all mandatory and optional features).

To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of co-existence features are available including a variety of hardware signalling: basic activity signalling and Intel WCS activity and channel signalling.

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1 Status Information

The status of this Data Sheet is **Advance Information.**

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications. Production Data Sheets supersede all previous document versions.

RoHS Compliance

BlueCore4-ROM devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

CSR's products are not authorised for use in life-support or safety-critical applications

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2 Key Features

Radio

- Common TX/RX terminals simplify external matching and eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs are available
- Bluetooth v2.0 + EDR Specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class 1 support using external power amplifier, with RF power controlled by an internal 8-bit DAC
- Supports DQPSK (2Mbps) and 8DPSK (3Mbps) modulation

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Supports DQPSK and 8DPSK modulation
- Channel classification

Synthesiser

- Fully integrated synthesizer requires no external VCO varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 40MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands with an integrated low-power oscillator for ultra-low Park/Sniff/Hold mode
- Clock Request output to control an external clock source

Auxiliary Features (continued)

- Device can run in low power modes from an external 32KHz clock signal
- Auto Baud Rate setting for different TCXO frequencies
- On-chip linear regulator, producing 1.8V output from 2.2-4.2V input
- Power-on-reset cell detects low supply voltage

Baseband and Software

- Internal 48-KByte RAM, allows full-speed data transfer, mixed voice and data, and full piconet operation, including all medium rate preset types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth v2.0 + EDR features including eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable baud rate up to 3Mbits/s with an optional bypass mode
- Full-speed USB v2.0 interface supports OHCI and UHCI host interfaces
- Synchronous bi-directional serial programmable audio interface
- Optional I^2C™ compatible interfaces
- Optional 802.11 co-existence interfaces

Bluetooth Stack

CSR's Bluetooth protocol stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI (UART or USB)
- Customised builds with embedded application code

Package Options

- 47-ball CSP 3.8 x 4.0 x 0.7mm

3 CSP Package Information

3.1 BlueCore4-ROM CSP Pinout Diagram

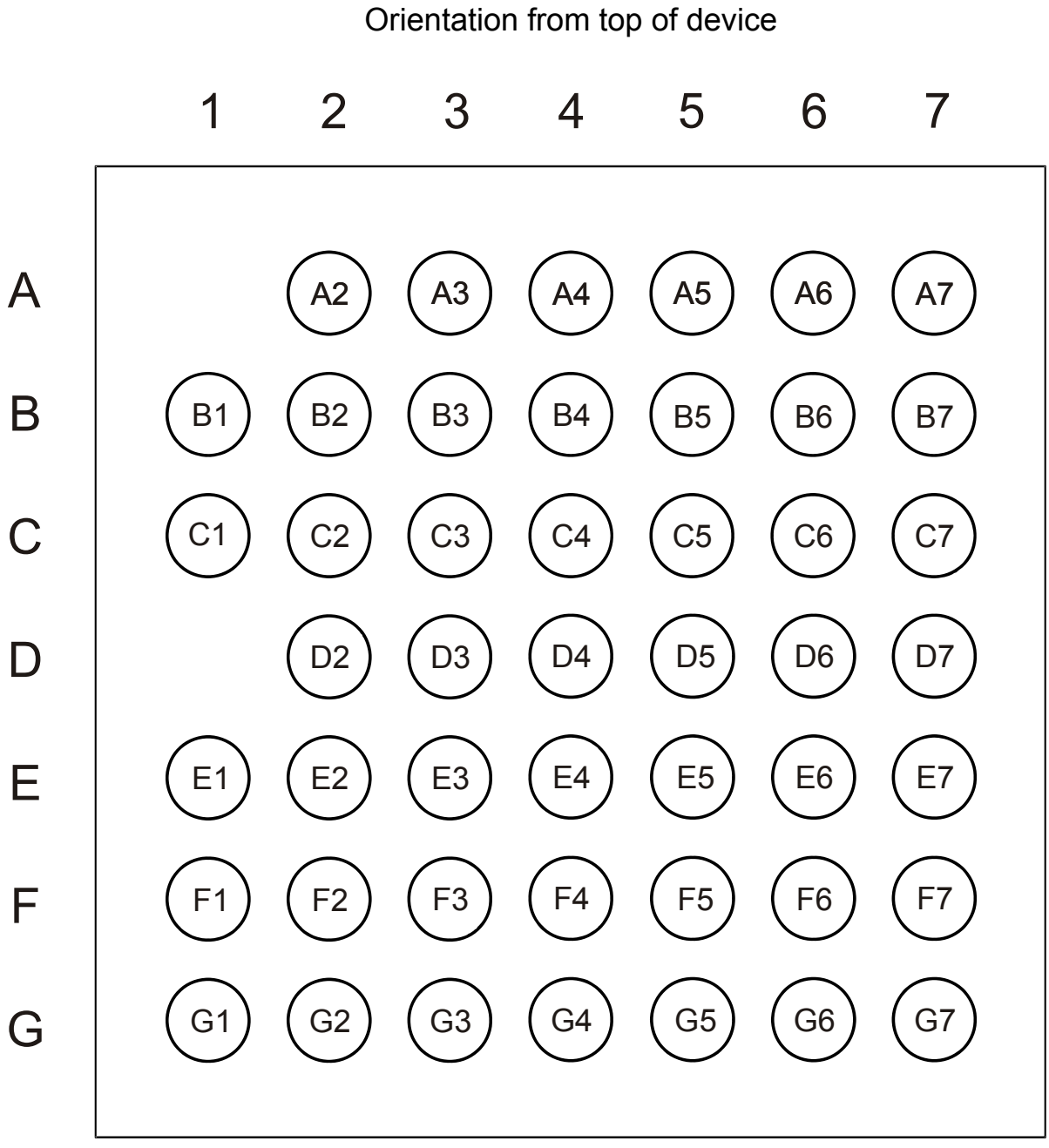


Figure 3.1: BlueCore4-ROM CSP Package

3.2 BC41B143AXX-IXF Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_A	E2	Analogue	Transmitter output/switched receiver input
RF_B	E1	Analogue	Complement of RF_A
AUX_DAC	D2	Analogue	Voltage DAC

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	A3	Analogue	For crystal or external clock input
XTAL_OUT	B3	Analogue	Drive for crystal

PCM Interface	Ball	Pad Type	Description
PCM_OUT	E4	CMOS output, tri-statable with weak internal pull-down	Synchronous data output
PCM_IN	B7	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	D5	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	B6	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	C5	CMOS output, tri-statable with weak internal pull-up	UART data output active high
UART_RX	D4	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	A7	CMOS output, tri-statable with weak internal pull-up	UART request to send active low
UART_CTS	C4	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	B5	Bi-directional	USB data plus with selectable internal 1.5kΩ Pull-up resistor
USB_DN	A6	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESETB	E7	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	G6	CMOS input with weak internal pull-up	Chip select for Serial Peripheral Interface (SPI), active low
SPI_CLK	G5	CMOS input with weak internal pull-down	SPI clock
SPI_MOSI	F6	CMOS input with weak internal pull-down	SPI data input into BlueCore
SPI_MISO	F7	CMOS output, tri-state with weak internal pull-down	SPI data output from BlueCore
TEST_EN	G7	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port	Ball	Pad Type	Description
PIO[0]	F3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[1]	F4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[2]	G1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	G2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	F5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	D7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	E5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	F1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	F2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	D3	Bi-directional	Programmable input/output line
AIO[2]	C3	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	A2	Regulator input	Regulator input
VDD_USB	A5	VDD	Positive supply for UART ports and AIOs
VDD_PIO	G4	VDD	Positive supply for PIO [3:0] and [10:8]
VDD_PADS	D6	VDD	Positive supply for all other digital input/output ports, and PIO [7:4]
VDD_CORE	C6	VDD	Positive supply for internal digital circuitry
VDD_LO	B2	VDD	Positive supply for VCO and synthesiser circuitry
VDD_RADIO	C2	VDD	Positive supply for RF circuitry
VDD_ANA	A4	VDD/Regulator output	Positive supply for analogue circuitry and internal 1.8V regulator output
VSS_DIG	C7	VSS	Ground connection for internal digital circuitry and digital ports
VSS_PADS	G3	VSS	Ground connection for digital ports
VSS_RADIO	C1	VSS	Ground connections for RF circuitry
VSS_ANA	B4	VSS	Ground connections for analogue circuitry
VSS_LO	B1	VSS	Ground connection for VCO and synthesiser circuitry

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Minimum**	**Maximum**
Storage temperature	-40°C	150°C
Supply voltage: VDD_RADIO, VDD_LO, VDD_ANA, and VDD_CORE	-0.4V	2.2V
Supply voltage: VDD_PADS, VDD_PIO and VDD_USB	-0.4V	3.7V
Supply voltage: VREG_IN	-0.4V	5.6V
Other terminal voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Minimum**	**Maximum**
Operating temperature range	-40°C	105°C
Guaranteed RF performance range(1)	-40°C	105°C
Supply voltage: VDD_RADIO, VDD_LO, VDD_ANA, and VDD_CORE	1.7V	1.9V
Supply voltage: VDD_PADS, VDD_PIO and VDD_USB	1.7V	3.6V
Supply voltage: VREG_IN	2.2V	4.2V(2)

Note:

(1) Typical figures are given for RF performance between -40°C and +105°C.

(2) The device will operate without damage with VREG_IN as high as 5.6V. However the RF performance is not guaranteed above 4.2V.

Input/Output Terminal Characteristics					
Linear Regulator		**Minimum**	**Typical**	**Maximum**	**Unit**
Normal Operation					
Output voltage (I_{load} = 70mA / VREG_IN = 3.0V)		1.70	1.78	1.85	V
Temperature coefficient		-250	-	250	ppm/°C
Output noise(1)		-	-	1	mV rms
Load regulation (I_{load} < 70mA)		-	-	50	mV/A
Settling time(2)		-	-	50	µs
Output current:	Maximum output current	70	-	-	mA
	Minimum load current	5	-	-	µA
Input voltage		-	-	4.2(3)	V
Dropout voltage (I_{load} = 70mA)		-	-	350	mV
Quiescent current (excluding load, I_{load} < 1mA)		25	35	50	µA
Low Power Mode(4)					
Quiescent current (excluding load, I_{load} < 100µA)		4	7	10	µA
Disabled Mode(5)					
Quiescent current		1.5	2.5	3.5	µA

Notes:

(1) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors. Frequency range 100Hz to 100kHz

(2) 1mA to 70mA pulsed load

(3) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore4-ROM CSP, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V

(4) Low power mode is entered and exited automatically when the IC enters/leaves Deep Sleep mode

(5) Regulator is disabled when VREG_EN is pulled low. It can also be disabled by VREG_IN when it is either open circuit or driven to the same voltage as VDD_ANA

Input/Output Terminal Characteristics (Continued)					
Digital Terminals		**Minimum**	**Typical**	**Maximum**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_o = 4.0mA) (1), 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
V_{OL} output logic level low, (I_o = 4.0mA) (1), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA) (2), 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_o = -4.0mA) (2), 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-State Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		10	40	100	µA
Weak pull-up		-5	-1	-0.2	µA
Weak pull-down		0.2	1	5.0	µA
I/O pad leakage current		-1	0	1	µA
C_I input capacitance		1.0	-	5.0	pF

Notes:

(1) Current sunk into terminal

(2) Current sourced out of terminal

Input/Output Terminal Characteristics (Continued)				
USB Terminals	**Minimum**	**Typical**	**Maximum**	**Unit**
VDD_USB for correct USB operation	3.1		3.6	V
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.7VDD_USB	-	-	V
Input leakage current				
VSS_USB< V_{IN}< VDD_USB[1]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage levels **To correctly terminated USB Cable**				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

Notes:

(1) Internal USB pull-up disabled

Input/Output Terminal Characteristics (Continued)				
Power-on reset	**Minimum**	**Typical**	**Maximum**	**Unit**
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Input/Output Terminal Characteristics (Continued)					
Auxiliary ADC		**Minimum**	**Typical**	**Maximum**	**Unit**
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate		-	-	700	Samples/s

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC	**Minimum**	**Typical**	**Maximum**	**Unit**
Resolution	-	-	8	Bits
Average output step size(1)	12.5	14.5	17.0	mV
Output Voltage		monotonic		
Voltage range (IO=0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (IO=100µA)	0.0	-	0.2	V
Maximum output voltage (IO=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	+1	µA
Offset	-220	-	+120	mV
Integral non-linearity(1)	-2	-	+2	LSB
Settling time (50pF load)	-	-	10	µs

Note:

(1) Specified for an output voltage between 0.2V and VDD_PIO -0.2V. Output is high impedance when chip is in Deep Sleep mode."

Input/Output Terminal Characteristics (Continued)				
Crystal Oscillator	**Minimum**	**Typical**	**Maximum**	**Unit**
Crystal frequency (1)	8.0	-	40.0	MHz
Digital trim range (2)	5.0	6.2	8.0	pF
Trim step size (2)	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance(3)	870	1500	2400	Ω
External Clock				
Input frequency(4)	8.0	-	40.0	MHz
Clock input level(5)	0.4	-	VDD_ANA	V pk-pk
Allowable jitter	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

Notes:

VDD_CORE, VDD_RADIO, VDD_LO and VDD_ANA are at 1.8V unless shown otherwise.

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise.

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

(1) Integer multiple of 250kHz.

(2) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

(3) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF.

(4) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz and also covers the CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

(5) Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN.

4.1 Power Consumption

Operation Mode	Connection Type	UART Rate (Kbits/s)	Average	Unit
Page scan, time interval 1.28s	-	115.2	0.41	mA
Inquiry & page scan	-	115.2	0.77	mA
ACL data transfer no traffic	Master	115.2	6.4	mA
ACL data transfer with file transfer	Master	115.2	11	mA
ACL data transfer no traffic	Slave	115.2	14	mA
ACL data transfer with file transfer	Slave	115.2	17	mA
ACL data transfer 40ms sniff	Master	38.4	1.5	mA
ACL data transfer 1.28s sniff	Master	38.4	0.19	mA
SCO connection HV1	Master	38.4	34	mA
SCO connection HV3	Master	38.4	17	mA
SCO connection HV3 30ms sniff	Master	38.4	17	mA
ACL data transfer 40ms sniff	Slave	38.4	1.5	mA
ACL data transfer 1.28s sniff	Slave	38.4	0.24	mA
SCO connection HV1	Slave	38.4	34	mA
SCO connection HV3	Slave	38.4	21	mA
SCO connection HV3 30ms sniff	Slave	38.4	17	mA
Parked 1.28s beacon	Slave	38.4	0.18	mA
Standby Host connection	-	38.4	0.03	mA
Reset (RESETB low)	-	-	40	µA

Note:

Conditions: 20°C, 1.80V supply

5 Radio Characteristics – Basic Data Rate

5.1 Temperature +20°C

5.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)(2)	-	5.5	-	-6 to +4(3)	dBm
Variation in RF power over temperature range with compensation enabled (±)(4)	-	1.5	-	-	dB
Variation in RF power over temperature range with compensation disabled (±)(4)	-	2.5	-	-	dB
RF power control range	-	35	-	≥16	dB
RF power range control resolution (5)	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	-	≤1000	kHz
Adjacent channel transmit power F=F_0 ±2MHz(6)(7)	-	-40	-	≤-20	dBm
Adjacent channel transmit power F=F_0 ±3MHz(6)(7)	-	-45	-	≤-40	dBm
Adjacent channel transmit power F=F_0>±3MHz(6)(7)	-	-55	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	165	-	140<$\Delta f1_{avg}$<175	kHz
Δf2max “Minimum Modulation”	-	155	-	≥115	kHz
Δf2avg / Δf1avg	-	0.99	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50µs
Drift (single slot packet)	-	9	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz
2nd Harmonic content	-	-40	-	≤-30	dBm
3rd Harmonic content	-	-50	-	≤-30	dBm

Note

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v2.0+EDR limits.

(2) Measurement made using a PSKEY_LC_MAX_TX_POWER setting corresponds to a PSKEY_LC_POWER_TABLE power table entry of 63.

(3) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR.

(4) To some extent these parameters are dependent on the matching circuit used, and its behaviour over temperature. Therefore these parameters may be beyond CSR’s direct control.

(5) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level >20.

(6) Measured at F_0 = 2441MHz.

(7) Up to three exceptions are allowed in v2.0+EDR of the Bluetooth specification. BlueCore4-ROM CSP is guaranteed to meet the ACP performance as specified by the Bluetooth specification v2.0+EDR.

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Emitted power in cellular bands measured at the unbalanced port of the balun. Output power ≤5dBm	0.869 – 0.894[1]	-	-130	-	GSM 850	dBm /Hz
	0.869 – 0.894[2]	-	-134	-	CDMA 850	
	0.925 – 0.960[1]	-	-133	-	GSM 900	
	1.570 – 1.580[3]	-	-137	-	GPS	
	1.805 – 1.880[1]	-	-141	-	GSM 1800 / DCS 1800	
	1.930 – 1.990[4]	-	-142	-	PCS 1900	
	1.930 – 1.990[1]	-	-140	-	GSM 1900	
	1.930 – 1.990[2]	-	-140	-	CDMA 1900	
	2.110 – 2.170[2]	-	-140	-	W-CDMA 2000	
	2.110 – 2.170[5]	-	-140	-	W-CDMA 2000	

Notes:

(1) Integrated in 200kHz bandwidth and then normalised to a 1Hz bandwidth.

(2) Integrated in 1.2MHz bandwidth and then normalised to a 1Hz bandwidth.

(3) Integrated in 1MHz bandwidth and then normalised to a 1Hz bandwidth.

(4) Integrated in 30kHz bandwidth and then normalised to a 1Hz bandwidth.

(5) Integrated in 5MHz bandwidth and then normalised to a 1Hz bandwidth.

5.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-84	-	≤-70	dBm
	2.441	-	-84	-		
	2.480	-	-84	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm
	Frequency (MHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Continuous power required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	30 – 2000	-	>0	-	-10	dBm
	2000 – 2400	-	>-10	-	-27	
	2500 – 3000	-	>0	-	-27	
	3000 – 3300	-	>3	-	-10	
C/I co-channel		-	8	-	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$ (1) (2)		-	-5	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ (1) (2)		-	-4	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$ (1) (2)		-	-45	-	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$ (1) (2)		-	-22	-	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$ (1) (2)		-	-48	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$ (1) (2)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F=F_{Image}$ (1) (2)		-	-23	-	≤-9	dB
Maximum level of intermodulation interferers (3)		-	-30	-	≥-39	dBm
Spurious output level (4)		-	-160	-	-	dBm/Hz

Notes:

(1) Up to five exceptions are allowed in v2.0+EDR of the Bluetooth specification. BlueCore4-ROM CSP is guaranteed to meet the C/I performance as specified by the Bluetooth specification v2.0+EDR.

(2) Measured at F_0 = 2441MHz.

(3) Measured at f1-f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c. i.e. wanted signal at -64dBm.

(4) Measured at the unbalanced port of the balun. Integrated in 100kHz bandwidth and then normalized to 1Hz. Actual figure is typically below -160dBm/Hz except for peaks of -60dBm at 1.6GHz, -45dBm inband at 2.4GHz and -60dBm at 3.2GHz.

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	4(1)	-	GSM 850	dBm
	0.824 – 0.849	-	-10	-	CDMA	
	0.880 – 0.915	-	10	-	GSM 900	
	1.710 – 1.785	-	>4	-	GSM 1800 / DCS 1800	
	1.850 – 1.910	-	>3	-	GSM 1900 / PCS 1900	
	1.850 – 1.910	-	-10	-	CDMA 1900	
	1.920 – 1.980	-	-19	-	W-CDMA 2000	
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -72dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	3	-	GSM 850	dBm
	0.824 – 0.849	-	-15	-	CDMA	
	0.880 – 0.915	-	0	-	GSM 900	
	1.710 – 1.785	-	>4	-	GSM 1800 / DCS 1800	
	1.850 – 1.910	-	>3	-	GSM 1900 / PCS 1900	
	1.850 – 1.910	-	-15	-	CDMA 1900	
	1.920 – 1.980	-	-15	-	W-CDMA 2000	

Note:

(1) 0dBm if $f_{BLOCKING}$ <0.831GHz

5.2 Temperature -40°C

5.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	6.0	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-43	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	165	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	150	-	115	kHz
Δf2avg / Δf1avg	-	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v2.0+EDR limits

(2) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v2.0+EDR of the Bluetooth specification

5.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-84.5	-	≤-70	dBm
	2.441	-	-86	-		
	2.480	-	-85	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

5.3 Temperature -25°C

5.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	5.5	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	165	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	150	-	115	kHz
Δf2avg / Δf1avg	-	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v2.0+EDR limits

(2) Class 2 RF transmit power range, Bluetooth specification v2.0 + EDR

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v2.0 + EDR of the Bluetooth specification

5.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-84.5	-	≤-70	dBm
	2.441	-	-85.5	-		
	2.480	-	-85	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

5.4 Temperature +85°C

5.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	3.5	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	165	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	150	-	≥115	kHz
Δf2avg / Δf1avg	-	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	10	-	≤25	kHz
Drift (five slot packet)	-	10	-	≤40	kHz

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v2.0+EDR limits

(2) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v2.0+EDR of the Bluetooth specification

5.4.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-81.0	-	≤-70	dBm
	2.441	-	-81.5	-		
	2.480	-	-82.0	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

5.5 Temperature +105°C

5.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	2.0	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	165	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	145	-	115	kHz
Δf2avg / Δf1avg	-	0.96	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	9	-	≤25	kHz
Drift (five slot packet)	-	10	-	≤40	kHz

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v2.0+EDR limits

(2) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v2.0+EDR of the Bluetooth specification

5.5.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-80	-	≤-70	dBm
	2.441	-	-80.5	-		
	2.480	-	-82.5	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

6 Radio Characteristics – Enhanced Data Rate

6.1 Temperature +20°C

6.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20C						
		Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)		-	1.5	-	-6 to +4(2)	dBm
Relative transmit power(3)		-	-1.2	-	-4 to +1	dB
π/4 DQPSK Max carrier frequency stability(3) w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK Max carrier frequency stability(3) w_i		-	6	-	≤±75 for all packets	kHz
π/4 DQPSK Max carrier frequency stability(3) $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
8DPSK Max carrier frequency stability(3) w_0		-	2	-	≤±10 for all blocks	kHz
8DPSK Max carrier frequency stability(3) w_i		-	6	-	≤±75 for all packets	kHz
8DPSK Max carrier frequency stability(3) $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy(3)(4)	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	19	-	≤35	%
8DPSK Modulation Accuracy(3)(4)	RMS DEVM	-	7	-	≤13	%
	99% DEVM	-	13	-	≤20	%
	Peak DEVM	-	17	-	≤25	%
In-band spurious emissions(5)	F > F_o +3MHz	-	<-50	-	≤-40	dBm
	F < F_o -3MHz	-	<-50	-	≤-40	dBm
	F = F_o - 3MHz	-	-46	-	≤-40	dBm
	F = F_o - 2MHz	-	-34	-	≤-20	dBm
	F = F_o – 1MHz	-	-35	-	≤-26	dB
	F = F_o + 1MHz	-	-35	-	≤-26	dB
	F = F_o + 2MHz	-	-31	-	≤-20	dBm
	F = F_o + 3MHz(5)	-	-33	-	≤-40	dBm
EDR Differential Phase Encoding		-	No errors	-	-	%

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.

(2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.

(3) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification.

(4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.

(5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

6.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(1)	π/4 DQPSK	-	-87	-	≤-70	dBm
	8DPSK	-	-78	-	≤-70	dBm
Maximum received signal at 0.1% BER(1)	π/4 DQPSK	-	-8	-	≥-20	dBm
	8DPSK	-	-10	-	≥-20	dBm
C/I co-channel at 0.1% BER(1)	π/4 DQPSK	-	10	-	≤+13	dB
	8DPSK	-	19	-	≤+21	dB
Adjacent channel selectivity C/I $F=F_0$ +1MHz(1)(2)(3)	π/4 DQPSK	-	-10	-	≤0	dB
	8DPSK	-	-5	-	≤+5	dB
Adjacent channel selectivity C/I $F=F_0$ -1MHz(1)(2)(3)	π/4 DQPSK	-	-11	-	≤0	dB
	8DPSK	-	-5	-	≤+5	dB
Adjacent channel selectivity C/I $F=F_0$ +2MHz(1)(2)(3)	π/4 DQPSK	-	-40	-	≤-30	dB
	8DPSK	-	-40	-	≤-25	dB
Adjacent channel selectivity C/I $F=F_0$ -2MHz(1)(2)(3)	π/4 DQPSK	-	-23	-	≤-20	dB
	8DPSK	-	-20	-	≤-13	dB
Adjacent channel selectivity C/I $F\geq F_0$ +3MHz(1)(2)(3)	π/4 DQPSK	-	-45	-	≤-40	dB
	8DPSK	-	-45	-	≤-33	dB
Adjacent channel selectivity C/I $F\leq F_0$ –5MHz(1)(2)(3)	π/4 DQPSK	-	-45	-	≤-40	dB
	8DPSK	-	-45	-	≤-33	dB
Adjacent channel selectivity C/I $F=F_{Image}$(1)(2)(3)	π/4 DQPSK	-	-20	-	≤-7	dB
	8DPSK	-	-15	-	≤0	dB

Notes:

(1) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification

(2) Up to five exceptions are allowed in Bluetooth v2.0 + EDR specification. BlueCore4-ROM is guaranteed to meet the C/I performance as specified by the Bluetooth v2.0 + EDR specification.

(3) Measured at F_0 = 2405MHz, 2441MHz, 2477MHz

6.2 Temperature -40°C

6.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C						
		Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)		-	4	-	-6 to +4(2)	dBm
Relative transmit power(3)		-	-1.2	-	-4 to +1	dB
π/4 DQPSK Max carrier frequency stability(3) w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK Max carrier frequency stability(3) w_i		-	7	-	≤±75 for all packets	kHz
π/4 DQPSK Max carrier frequency stability(3) $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
8DPSK Max carrier frequency stability(3) w_0		-	3	-	≤±10 for all blocks	kHz
8DPSK Max carrier frequency stability(3) w_i		-	7	-	≤±75 for all packets	kHz
8DPSK Max carrier frequency stability(3) $\lvert w_0 + w_i \rvert$		-	9	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy(3)(4)	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	14	-	≤30	%
	Peak DEVM	-	19	-	≤35	%
8DPSK Modulation Accuracy(3)(4)	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	12	-	≤20	%
	Peak DEVM	-	18	-	≤25	%
In-band spurious emissions(5)	$F > F_o$ +3MHz	-	<-50	-	≤-40	dBm
	$F < F_o$ -3MHz	-	<-50	-	≤-40	dBm
	$F = F_o$ - 3MHz	-	-42	-	≤-40	dBm
	$F = F_o$ - 2MHz	-	-25	-	≤-20	dBm
	$F = F_o$ – 1MHz	-	-32	-	≤-26	dB
	$F = F_o$ + 1MHz	-	-33	-	≤-26	dB
	$F = F_o$ + 2MHz	-	-25	-	≤-20	dBm
	$F = F_o$ + 3MHz(5)	-	-30	-	≤-40	dBm
EDR Differential Phase Encoding		-	No errors	-	-	%

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.

(2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.

(3) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification.

(4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.

(5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

6.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(1)	π/4 DQPSK	-	-89	-	≤-70	dBm
	8DPSK	-	-79	-	≤-70	dBm
Maximum received signal at 0.1% BER(1)	π/4 DQPSK	-	-12	-	≥-20	dBm
	8DPSK	-	-15	-	≥-20	dBm

Notes:

(1) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification

6.3 Temperature -25°C

6.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power(1)		-	3	-	-6 to +4(2)	dBm
Relative transmit power(3)		-	-1.2	-	-4 to +1	dB
π/4 DQPSK Max carrier frequency stability(3) w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK Max carrier frequency stability(3) w_i		-	6	-	≤±75 for all packets	kHz
π/4 DQPSK Max carrier frequency stability(3) $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
8DPSK Max carrier frequency stability(3) w_0		-	2	-	≤±10 for all blocks	kHz
8DPSK Max carrier frequency stability(3) w_i		-	6	-	≤±75 for all packets	kHz
8DPSK Max carrier frequency stability(3) $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy(3)(4)	RMS DEVM	-	6	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy(3)(4)	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	11	-	≤20	%
	Peak DEVM	-	16	-	≤25	%
In-band spurious emissions(5)	$F > F_o + 3MHz$	-	<-50	-	≤-40	dBm
	$F < F_o - 3MHz$	-	<-50	-	≤-40	dBm
	$F = F_o - 3MHz$	-	-43	-	≤-40	dBm
	$F = F_o - 2MHz$	-	-29	-	≤-20	dBm
	$F = F_o – 1MHz$	-	-32	-	≤-26	dB
	$F = F_o + 1MHz$	-	-33	-	≤-26	dB
	$F = F_o + 2MHz$	-	-27	-	≤-20	dBm
	$F = F_o + 3MHz$(5)	-	-31	-	≤-40	dBm
EDR Differential Phase Encoding		-	No errors	-	-	%

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.

(2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.

(3) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification.

(4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.

(5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

6.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(1)	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-79	-	≤-70	dBm
Maximum received signal at 0.1% BER(1)	π/4 DQPSK	-	-12	-	≥-20	dBm
	8DPSK	-	-15	-	≥-20	dBm

Notes:

(1) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification

6.4 Temperature +85°C

6.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C						
		Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power[1]		-	-3	-	-6 to +4[2]	dBm
Relative transmit power[3]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK Max carrier frequency stability[3] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK Max carrier frequency stability[3] w_i		-	7	-	≤±75 for all packets	kHz
π/4 DQPSK Max carrier frequency stability[3] $\lvert w_0 + w_i \rvert$		-	9	-	≤±75 for all blocks	kHz
8DPSK Max carrier frequency stability[3] w_0		-	2	-	≤±10 for all blocks	kHz
8DPSK Max carrier frequency stability[3] w_i		-	7	-	≤±75 for all packets	kHz
8DPSK Max carrier frequency stability[3] $\lvert w_0 + w_i \rvert$		-	9	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[3][4]	RMS DEVM	-	6	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy[3][4]	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	11	-	≤20	%
	Peak DEVM	-	16	-	≤25	%
In-band spurious emissions[5]	$F > F_o + 3MHz$	-	<-50	-	≤-40	dBm
	$F < F_o - 3MHz$	-	<-50	-	≤-40	dBm
	$F = F_o - 3MHz$	-	-43	-	≤-40	dBm
	$F = F_o - 2MHz$	-	-29	-	≤-20	dBm
	$F = F_o – 1MHz$	-	-32	-	≤-26	dB
	$F = F_o + 1MHz$	-	-33	-	≤-26	dB
	$F = F_o + 2MHz$	-	-27	-	≤-20	dBm
	$F = F_o + 3MHz$[5]	-	-31	-	≤-40	dBm
EDR Differential Phase Encoding		-	No errors	-	-	%

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.

(2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.

(3) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification.

(4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.

(5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

6.4.2 Receiver

Radio Characteristics	**VDD = 1.8V**	**Temperature = +85°C**				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(1)	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-74	-	≤-70	dBm
Maximum received signal at 0.1% BER(1)	π/4 DQPSK	-	-5	-	≥-20	dBm
	8DPSK	-	-5	-	≥-20	dBm

Notes:

(1) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification

6.5 Temperature +105°C

6.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power(1)		-	-4	-	-6 to +4(2)	dBm
Relative transmit power(3)		-	-1.3	-	-4 to +1	dB
π/4 DQPSK Max carrier frequency stability(3) w_0		-	1	-	≤±10 for all blocks	kHz
π/4 DQPSK Max carrier frequency stability(3) w_i		-	7	-	≤±75 for all packets	kHz
π/4 DQPSK Max carrier frequency stability(3) $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
8DPSK Max carrier frequency stability(3) w_0		-	1	-	≤±10 for all blocks	kHz
8DPSK Max carrier frequency stability(3) w_i		-	7	-	≤±75 for all packets	kHz
8DPSK Max carrier frequency stability(3) $\lvert w_0 + w_i \rvert$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy(3)(4)	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	12	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy(3)(4)	RMS DEVM	-	7	-	≤13	%
	99% DEVM	-	12	-	≤20	%
	Peak DEVM	-	15	-	≤25	%
In-band spurious emissions(5)	$F > F_o + 3MHz$	-	<-50	-	≤-40	dBm
	$F < F_o - 3MHz$	-	<-50	-	≤-40	dBm
	$F = F_o - 3MHz$	-	-51	-	≤-40	dBm
	$F = F_o - 2MHz$	-	-45	-	≤-20	dBm
	$F = F_o – 1MHz$	-	-37	-	≤-26	dB
	$F = F_o + 1MHz$	-	-32	-	≤-26	dB
	$F = F_o + 2MHz$	-	-37	-	≤-20	dBm
	$F = F_o + 3MHz$(5)	-	-38	-	≤-40	dBm
EDR Differential Phase Encoding		-	No errors	-	-	%

Notes:

(1) BlueCore4-ROM CSP firmware maintains the transmit power to be within the Bluetooth v2.0 + EDR specification limits.

(2) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification.

(3) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification.

(4) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.

(5) The Bluetooth specification values are for 8DPSK modulation. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.0 + EDR specification.

6.5.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(1)	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-73	-	≤-70	dBm
Maximum received signal at 0.1% BER(1)	π/4 DQPSK	-	-5	-	≥-20	dBm
	8DPSK	-	-5	-	≥-20	dBm

Notes:

(1) Measurement methods are in accordance with the Bluetooth v2.0 + EDR specification

7 Device Diagram

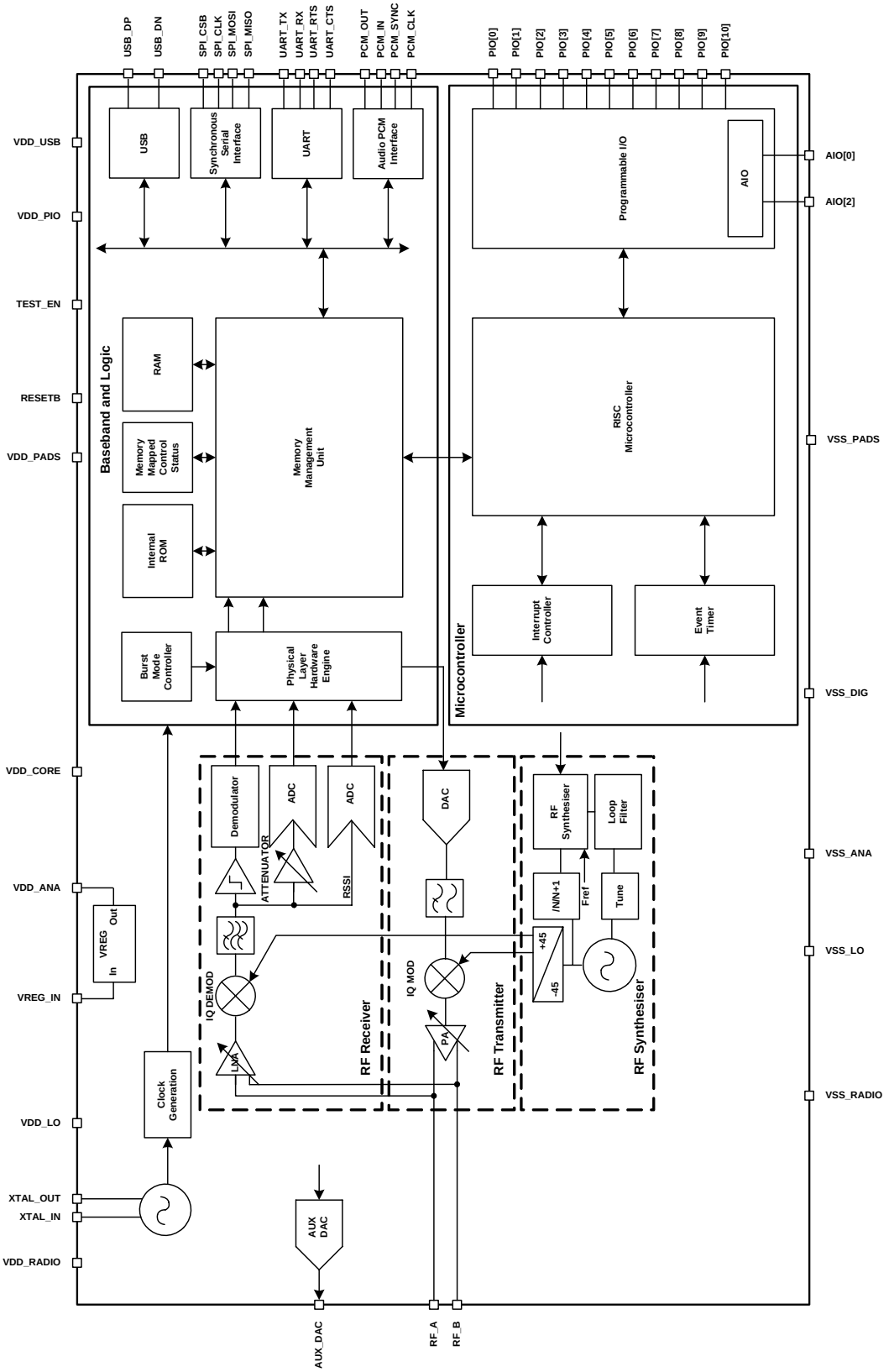


Figure 7.1: BlueCore4-ROM CSP Device Diagram for CSP Package

8 Description of Functional Blocks

8.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-ROM CSP to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, an Analogue to Digital Converter (ADC) is used to digitise the IF received signal.

8.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation. Differential mode is used for Class 2 operation.

8.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

8.2 RF Transmitter

8.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

8.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore4-ROM CSP to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

8.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation or for any other customer specific application.

8.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth Specification v2.0 + EDR.

8.4 Power Control and Regulation

BlueCore4-ROM CSP contains one linear 1.8V regulator which may be used to power the 1.8V supplies of the device.

8.5 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8MHz and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

8.6 Baseband and Logic

8.6.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

8.6.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

8.6.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v2.0 + EDR including AFH and eSCO.

8.6.4 RAM

48Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

8.6.5 ROM

4Mbits of metal programmable ROM is provided for system firmware implementation.

8.6.6 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore4-ROM CSP acts as a USB peripheral, responding to requests from a master host controller such as a PC.

8.6.7 Synchronous Serial Interface

This is a serial peripheral interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging.

8.6.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

8.6.9 Audio PCM Interface

The Audio Pulse Code Modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

8.7 Microcontroller

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit Reduced Instruction Set Computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

8.7.1 Programmable I/O

BlueCore4-ROM CSP has a total of 13 (11 digital and 2 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

8.7.2 802.11 Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware. Since the details of some methods are proprietary (for example Intel WCS) please contact CSR for details.

9 CSR Bluetooth Software Stacks

BlueCore4-ROM CSP is supplied with Bluetooth v2.0 + EDR compliant stack firmware which runs on the internal RISC microcontroller.

The BlueCore4-ROM CSP software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

9.1 BlueCore HCI Stack

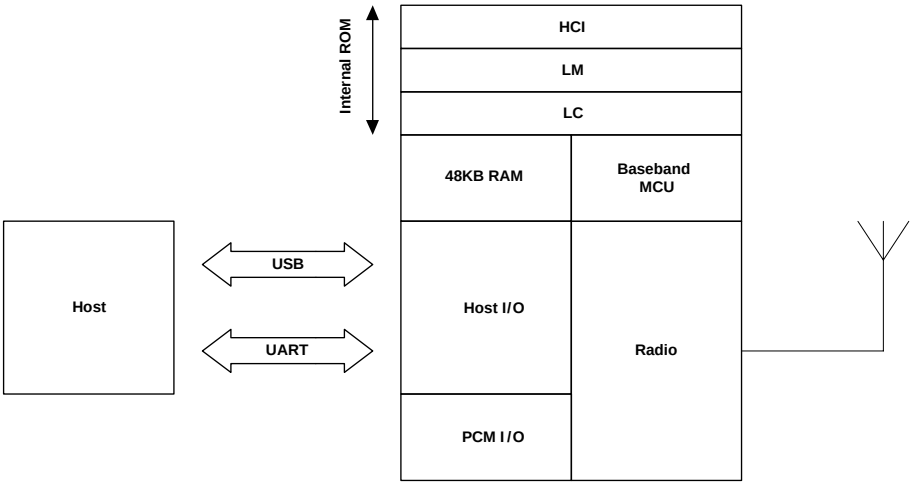


Figure 9.1: BlueCore HCI Stack

In the implementation shown in Figure 9.1 the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

9.1.1 Key Features of the HCI Stack – Standard Bluetooth Functionality

Bluetooth v2.0 + EDR mandatory functionality

- EDR, 2Mbps payload data rate
- EDR, 3Mbps payload data rate
- Support 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3 and 3-DH5 packet types
- Support 2-EV3, 2-EV5, 3-EV3 and 3-EV5 packet types

Bluetooth v1.2 mandatory functionality:

- Adaptive Frequency Hopping (AFH), including classifier
- Faster connection – enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges
- Support of AUX1 packet type

Optional v2.0 + EDR functionality supported:

- AFH as Master and automatic channel classification
- Fast connect – interlaced inquiry and page scan plus RSSI during inquiry
- Extended SCO (eSCO), eV3 + CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware has been written against the Bluetooth Core Specification v2.0 + EDR:

- Bluetooth components: Baseband (including LC), LM and HCI
- Standard USB v2.0 (full speed) and UART HCI transport layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2Kbits/s asymmetric(1)
- Operation with up to seven active slaves(1)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus “transparent SCO”
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power-saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes

The firmware’s supported Bluetooth features are described in the standard Protocol Implementation Conformance Statement (PICS) documents, available from http://www.csr.com.

Note:

(1) Maximum allowed by Bluetooth Specification v2.0 + EDR

(2) BlueCore4-ROM CSP supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth Specification v2.0 + EDR

9.1.2 Key Features of the HCI Stack - Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – "BlueCore Command") provides:
  - Access to the IC's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers – these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable – a simple command connects to a dedicated hardware switch that determines whether the radio can transmit
  - The firmware can read the voltage on pins AIO[2] and AIO[0]. This is normally used to build a battery monitor
  - A block of BCCMD commands provides access to the persistent store (PS) configuration database. The database sets the Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM and USB constants, etc.
  - A UART "break" condition can be used as follows:
    - Presenting a UART break condition to the IC can force the IC to perform a hardware reboot
    - Presenting a break condition at boot time can hold the IC in a low power state, preventing normal initialisation while the condition exists
    - When using BCSP host transport, the firmware can be configured to send a break to the host before sending data. This is normally used to wake the host from a deep sleep state
  - A block of "radio test" or BIST commands allows direct control of the IC's radio. This can be used during support Bluetooth qualification and factory testing.
- Hardware low-power modes: shallow sleep and deep sleep. The IC drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the single PCM port (at the same time as routing any remaining SCO channels over HCI).
- Co-operative existence with 802.11b/g chipsets. The device can be optionally configured to support a number of different co-existence schemes including:
  - TDMA – Bluetooth and WLAN avoid transmitting at the same time.
  - FDMA – Bluetooth avoids transmitting within the WLAN channel
  - Combination TDMA and FDMA – Bluetooth avoids transmitting in the WLAN channel only when WLAN is active.
  - Refer to separate documentation for full details of the co-existence schemes that CSR supports.

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

9.2 BCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to integrate Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore ICs. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application, for example a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP and Service Discovery Protocol, SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains three elements:

- Example drivers (BCSP and proxies)
- Bluetooth profile managers
- Example applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). Example applications in ANSI C are included with BCHS, which makes the process of writing the application easier.

9.3 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore4-ROM CSP, a UART software driver is supplied that presents the L2CAP and SDP APIs to higher Bluetooth stack layers running on the host. The code is provided as ‘C’ source or object code.

9.4 CSR Development Systems

CSR’s BlueLab and Casira development kits are available to allow the evaluation of the BlueCore4-ROM CSP hardware and software, and as toolkits for developing on-chip and host software.

10 Enhanced Data Rate

Enhanced Data Rate (EDR) has been introduced to provide 2x and 3x[(1)] data rates with minimal disruption to higher layers of the Bluetooth stack. BlueCore4-ROM supports both of the new data rates and is compliant with the Bluetooth v2.0 + EDR specification.

Note:

(1) The inclusion of 3x data rates is optional.

10.1 Enhanced Data Rate Baseband

At the baseband level EDR utilises the same 1.6kHz slot rate and 1MHz symbol rate as the basic data rate. Where EDR differs is that each symbol in the payload portion of a packet represents 2 or 3-bits. This is achieved using two new distinct modulation schemes. These are summarised in Table 10.1 and in Figure 10.1.

Link establishment and management are unchanged and still use GFSK for both the header and payload portions of these packets.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Data Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 10.1: Data Rate Schemes

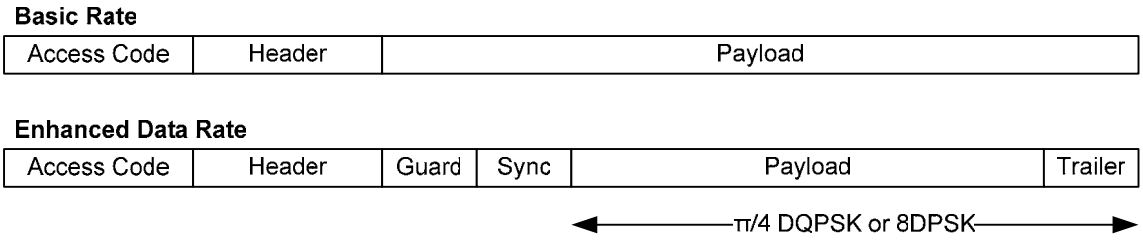


Figure 10.1: Basic Data Rate and Enhanced Data Rate Packet Types

10.2 Enhanced Data Rate π/4 DQPSK

The 2x rate for EDR uses a π/4 DQPSK. Each symbol represents two bits of information. The constellation is shown in Figure 10.2. It is described as having two places, each with four points. Although there appear to be eight possible phase states, the encoding ensures that the trajectory of the modulation between symbols is restricted to the four states in the other plane.

For a given starting point, each phase change between symbols is restricted to +3π/4, +π/4, -π/4 or -3π/4 radians (+135°, +45°, -135° or -45°). For example, the arrows shown in Figure 10.2 represents trajectory to the four possible states in the other plane. The phase shift encoding of symbols is shown in Table 10.2.

There are two primary advantages in using π/4-DQPSK modulation:

- The scheme avoids crossing the origin (a +π or –π phase shift) and therefore minimises amplitude variations in the envelope of the transmitted signal. This is in turn allows the RF power amplifiers of the transmitter to be operated closer to their compression point without introducing spectral distortions. Consequently, the DC to RF efficiency is maximised.
- The differential encoding also allows for demodulation without the knowledge of an absolute value for the phase of the RF carrier.

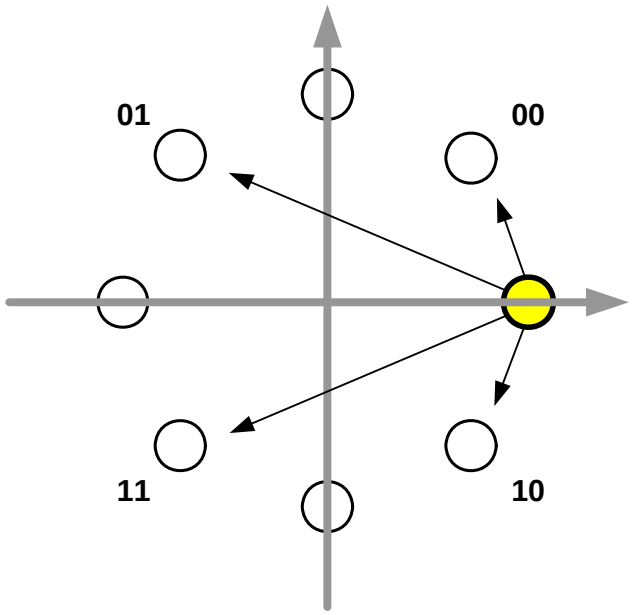


Figure 10.2: π/4 DQPSK Constellation Pattern

Bit Pattern	Phase Shift
00	π/4
01	3π/4
11	-3π/4
10	-π/4

Table 10.2: 2-Bits Determine Phase Shift Between Consecutive Symbols

10.3 Enhanced Data Rate 8DPSK

3x data rate modulation uses eight phase differential phase shift keying (8DPSK). Each symbol in the payload portion of the packet represents three baseband bits. Although 8DPSK appears to be similar to π/4 DQPSK, the differential phase shifts between symbols are now permissible between any of the eight possible phase states. This reduces the separation between adjacent symbols on the constellation to π/4 (45°C) and thereby reduces the noise and interference immunity of the modulation scheme. Nevertheless, since each symbol now represents 3 baseband bits, the actual throughput of the data is 3x when compared with the basic data rate packet.

Figure 10.3 illustrates the 8DPSK constellation and Table 10.3 defines the phase encoding.

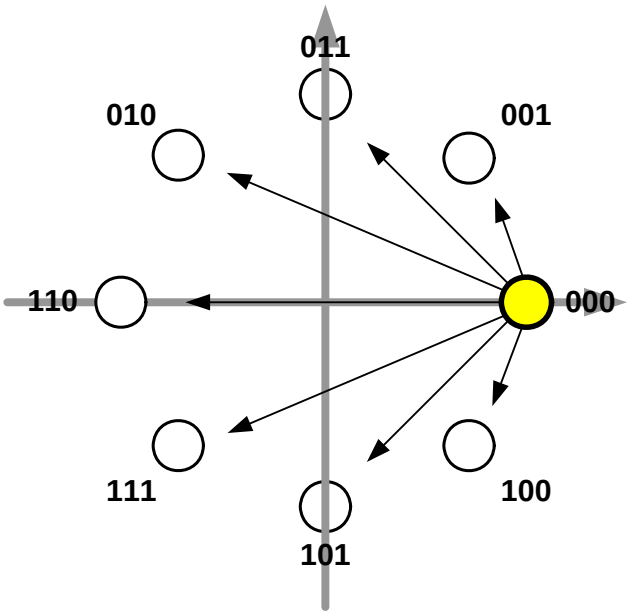


Figure 10.3: 8DPSK Constellation Pattern

Bit Pattern	Phase Shift
000	0
001	π/4
011	π/2
010	3π/4
110	π
111	-3π/4
101	-π/2
100	-π/4

Table 10.3: 3-Bits Determine Phase Shift Between Consecutive Symbols

11 Device Terminal Descriptions

11.1 RF_A and RF_B

RF_A and RF_B form a complementary balanced pair. On transmit, their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip side), the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The bond wire can be represented as series inductance.

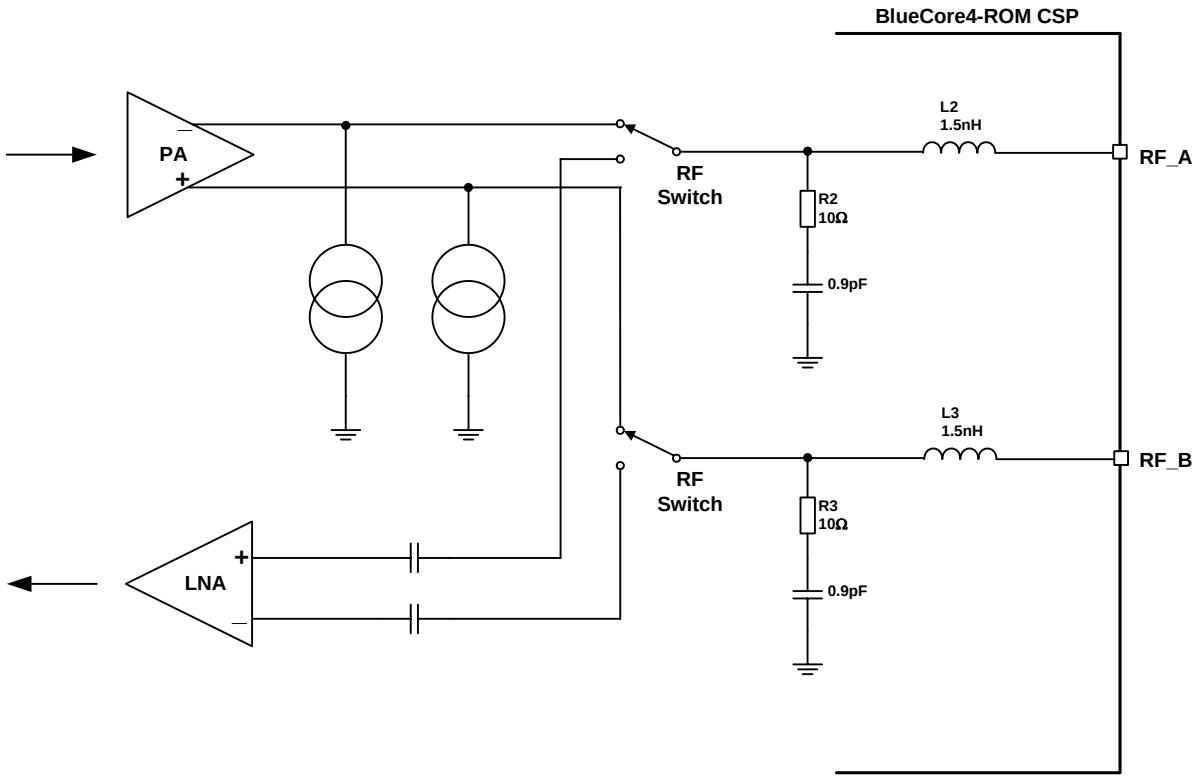


Figure 11.1: Circuit RF_A and RF_B

11.1.1 Transmit RF Power Control for Class 1 Applications

An 8-bit voltage DAC (AUX_DAC) can be used to control the amplification level of an external PA for Class 1 operation. The DAC output is derived from the on-chip band gap voltage reference and is virtually independent of temperature and supply voltage. The output voltage is given by either:

$$V_{AUX\_DAC} = MIN\left(\left(3.3V \times \frac{CNTRL\_WORD}{255}\right), (VDD\_PIO - 0.3V)\right)$$

Equation 11.1: Output Voltage with Load Current ≤ 10mA

for a load current ≤10mA (sourced from the device) or:

$$V_{AUX\_DAC} = MIN\left(\left(3.3V \times \frac{CNTRL\_WORD}{255}\right), VDD\_PIO\right)$$

Equation 11.2: Output Voltage with No Load Current

for no load current.

BlueCore4-ROM CSP enables the external PA only when transmitting. Before transmitting, the IC normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the gain pin on the PA from AUX_DAC.

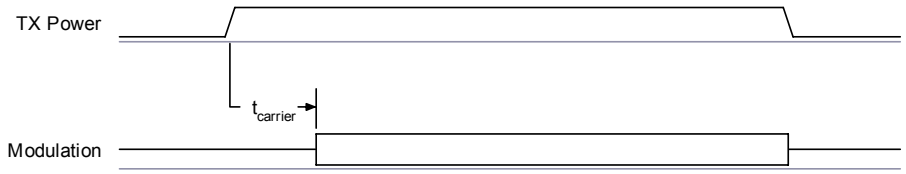


Figure 11.2: Internal Power Ramping

The PS Key PSKEY_TX_GAINRAMP controls the delay (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which gives the transmit circuitry time to fully settle to the correct frequency.

Bits [15:8] define a delay, $t_{carrier}$, (in units of μs), between the end of the transmit power ramp and the start of modulation. In this period an unmodulated carrier is transmitted, which aids interoperability with some other vendor equipment which is not strictly Bluetooth compliant.

11.1.2 Control of External RF Components

A PS Key, PSKEY_TXRX_PIO_CONTROL, controls external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this, as described in Table 11.1.

PSKEY_TXRX_PIO_CONTROL Value	Effect
0	PIO[0], PIO[1] and AUX_DAC are not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX and PIO[1] is high during TX. AUX_DAC is not used. Power ramping is internal.
2	PIO[0] is high during RX and PIO[1] is high during TX. AUX_DAC is used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX and PIO[1] is low during TX. AUX_DAC is used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX and PIO[1] is high during TX. AUX_DAC is used to set gain of external PA. Power ramping is internal.

Table 11.1: PSKEY_TXRX_PIO_CONTROL Values

11.2 External Reference Clock Input (XTAL_IN)

The BlueCore4-ROM CSP RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore4-ROM CSP XTAL_IN input. This reference can be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal connection is described in Section 11.3.

11.2.1 External Mode

BlueCore4-ROM CSP can be configured to accept an external reference clock (from another device, such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. This will cause XTAL_OUT to shut off, and it will not drive to ground. The external clock can either be a digital level square wave or sinusoidal and this can be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (~33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 11.2.

	Min	Typ	Max
Frequency(1)	7.5MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA(2)(3)

Table 11.2: External Clock Specifications

Notes:

(1) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(2) VDD_ANA is 1.8V nominal

(3) If the external clock is driven through a DC blocking capacitor then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk

11.2.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically only 10fF. When transitioning from deep sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input is used to prevent other devices that share the clock signal from being disrupted.

11.2.3 Clock Timing Accuracy

As Figure 11.3 shows, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.0 + EDR Specification. Radio activity may occur after 11ms. Therefore, at this point the timing accuracy of the external clock source must be within 20ppm. The CLK_REQ signal can be output from a GPIO under the control of PSKEY_CLOCK_REQUEST_ENABLE.

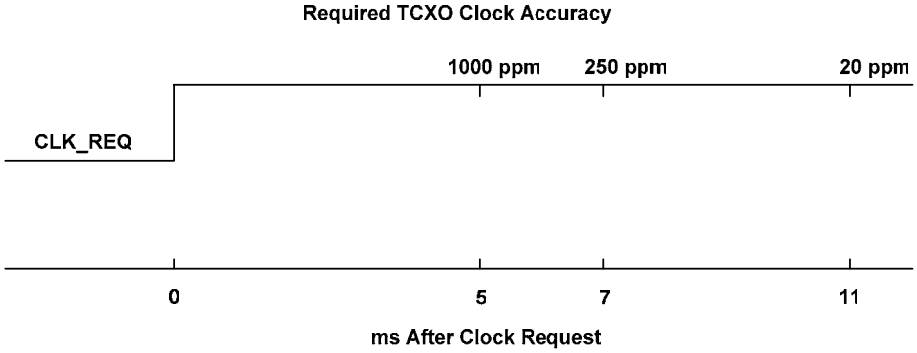


Figure 11.3: TCXO Clock Accuracy

11.2.4 Clock Start-Up Delay

BlueCore4-ROM CSP hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore4-ROM CSP firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in units of milliseconds from 5-31ms.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore4-ROM CSP as low as possible. BlueCore4-ROM CSP consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

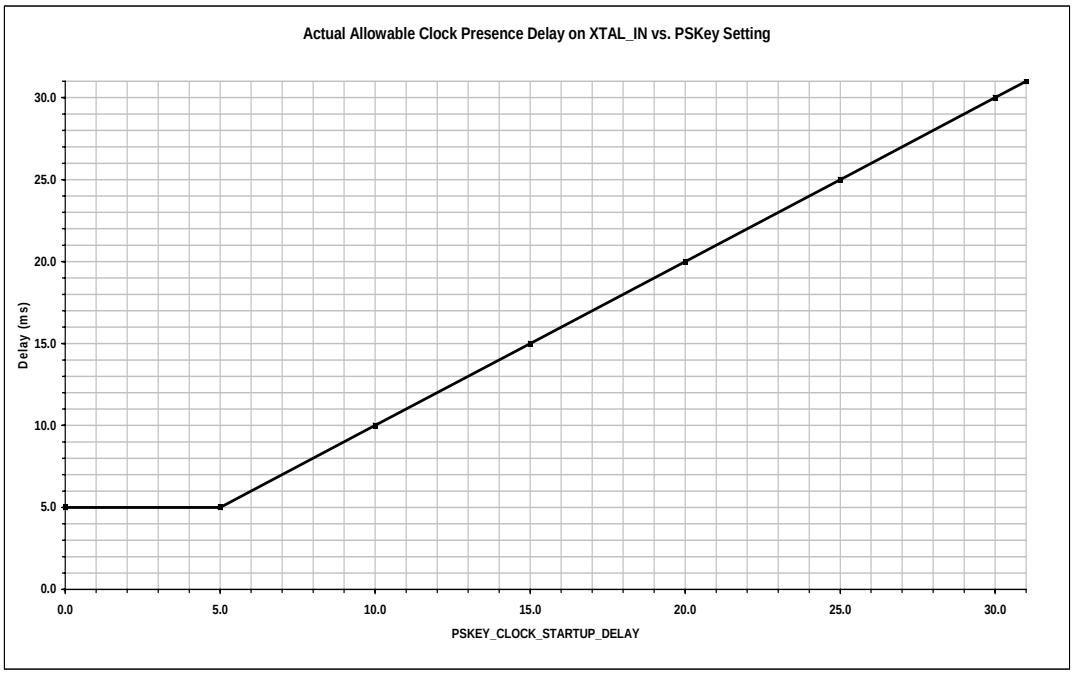


Figure 11.4: Actual Allowable Clock Presence Delay on XTAL_IN vs. PS Key Setting

11.2.5 Input Frequencies and PS Key Settings

BlueCore4-ROM CSP should be configured to operate with the chosen reference (XTAL_IN) frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ. The input frequency default setting in BlueCore4-ROM CSP is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (Units of 1kHz)
7.68	7680
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 11.3: PS Key Values for CDMA/3G Phone TCXO Frequencies

11.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

The BlueCore4-ROM CSP RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore4-ROM CSP XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The external reference clock mode is described in Section 11.2.

11.3.1 XTAL Mode

BlueCore4-ROM CSP contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

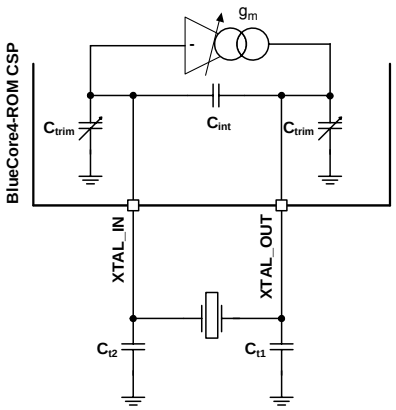


Figure 11.5: Crystal Driver Circuit

Figure 11.6 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

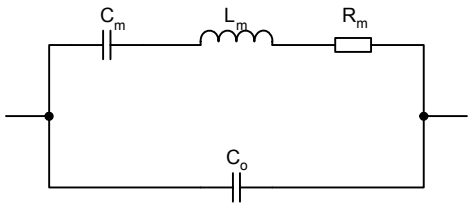


Figure 11.6: Crystal Equivalent Circuit

The resonant frequency can be trimmed with the crystal load capacitance. BlueCore4-ROM CSP contains variable internal capacitors to provide a fine trim.

	Min	Typ	Max
Frequency	8MHz	16MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 11.4: Crystal Specification

The BlueCore4-ROM CSP driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

11.3.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore4-ROM CSP provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN, to which all on-chip clocks are referred. Crystal load capacitance, C_l is calculated with the following equation:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \cdot C_{t2}}{C_{t1} + C_{t2}}$$

Equation 11.3: Load Capacitance

Where:

C_{trim} = 3.4pF nominal (Mid range setting)

C_{int} = 1.5pF

Note:

C_{int} does not include the crystal internal self capacitance. It is the driver self capacitance.

11.3.3 Frequency Trim

BlueCore4-ROM CSP enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the PS Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated as:

$$C_{trim} = 110\ \text{fF} \times \text{PSKEY\_ANA\_FTRIM}$$

Equation 11.4: Trim Capacitance

There are two C_{trim} capacitors which are both connected to ground. When viewed from the crystal terminals they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 11.5.

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 55 \times 10^{-3} (\text{ppm/LSB})$$

Equation 11.5: Frequency Trim

Where F_x is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal can be calculated from its motional capacitance with Equation 11.6.

$$\frac{\partial(F_x)}{\partial(C)} = F_x \cdot \frac{C_m}{4(C_l + C_0)^2}$$

Equation 11.6: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 11.6.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

11.3.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore4-ROM CSP uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than 3. The transconductance required for oscillation is defined by the following relationship:

$$g_m > \frac{3(C_{t1} + C_{trim})(C_{t2} + C_{trim})}{(2\pi F_x)^2 R_m((C_0 + C_{int})(C_{t1} + C_{t2} + 2C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}$$

Equation 11.7: Transconductance Required for Oscillation

BlueCore4-ROM CSP guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger Rm) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance, by setting the PS Key KEY_XTAL_LVL (0x241).

11.3.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore4-ROM CSP crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance can be calculated for it with the following formula in Equation 11.8.

$$R_{neg} > \frac{3(C_{t1} + C_{trim})(C_{t2} + C_{trim})}{g_m(2\pi F_x)^2(C_0 + C_{int})((C_{t1} + C_{t2} + 2C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}$$

Equation 11.8: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore4-ROM CSP driver as a function of its drive strength.

The value of the driver negative resistance can be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

11.3.6 Crystal PS Key Settings

See tables in Section 11.2.5.

11.3.7 Crystal Oscillator Characteristics

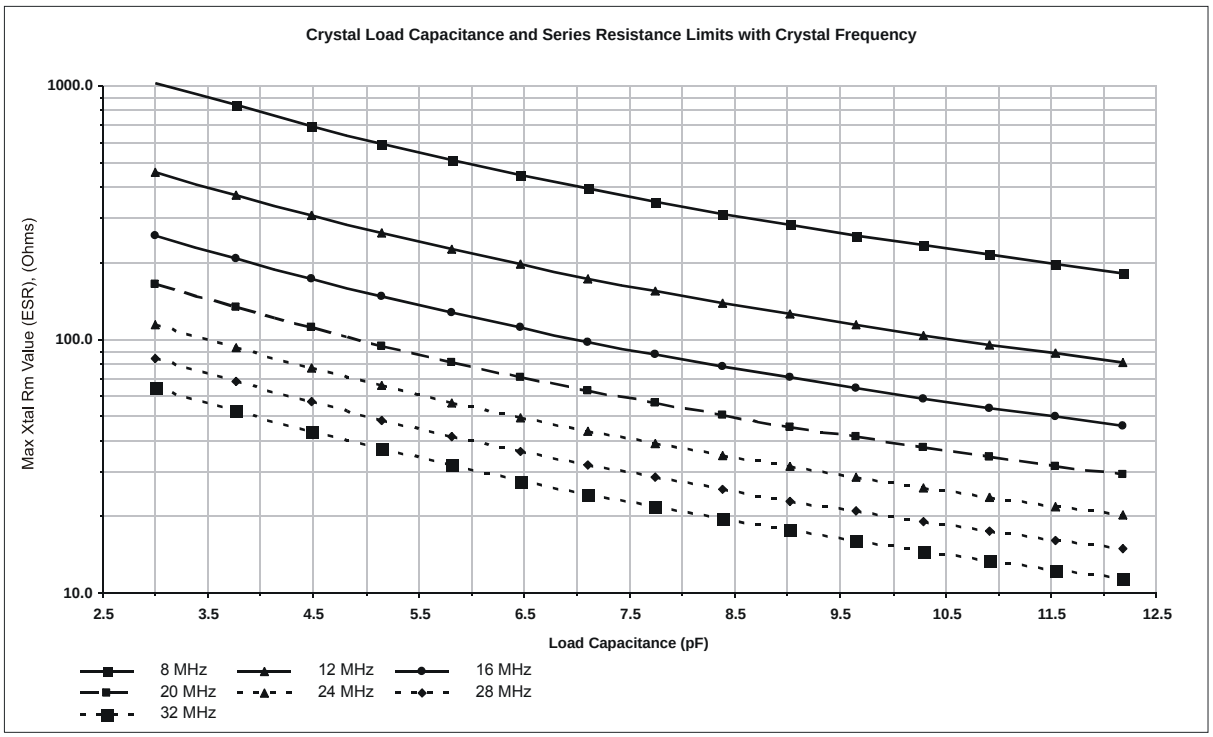


Figure 11.7: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Figure 11.7 shows results for BlueCore4-ROM CSP crystal driver at maximum drive level.

Conditions:

C_{trim} = 3.4pF centre value

Crystal C_o = 2pF

Transconductance setting = 2mA/V

Loop gain = 3

C_{t1}/C_{t2} = 3

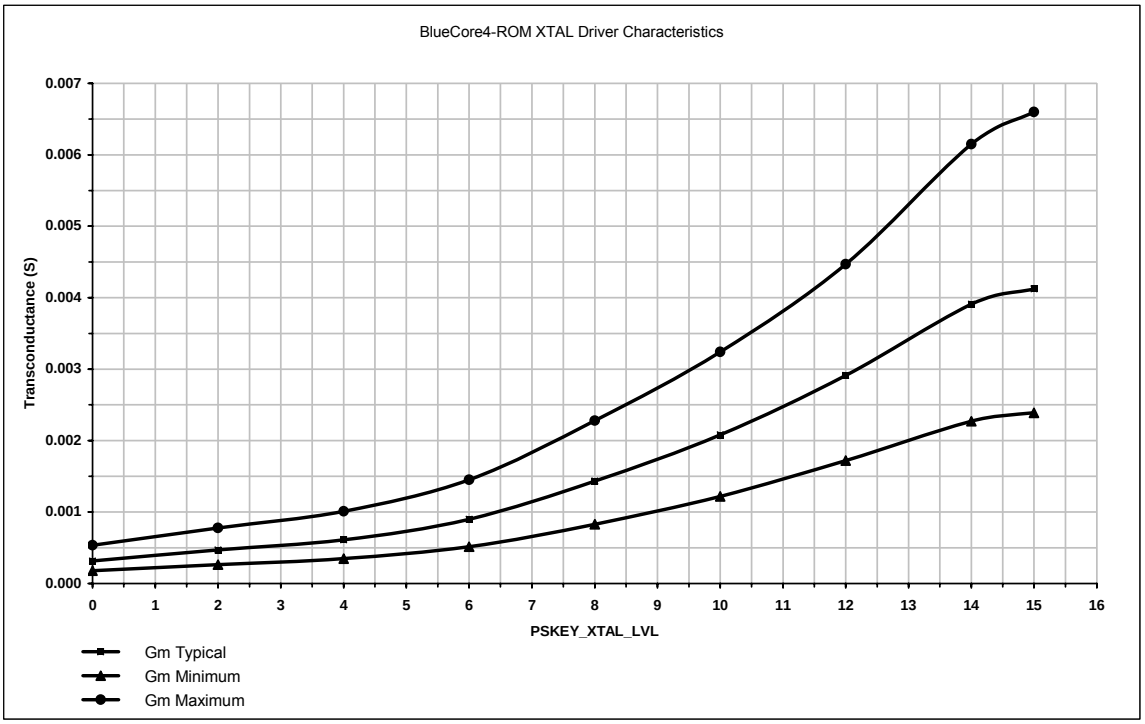


Figure 11.8: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by PS Key PSKEY_XTAL_LVL.

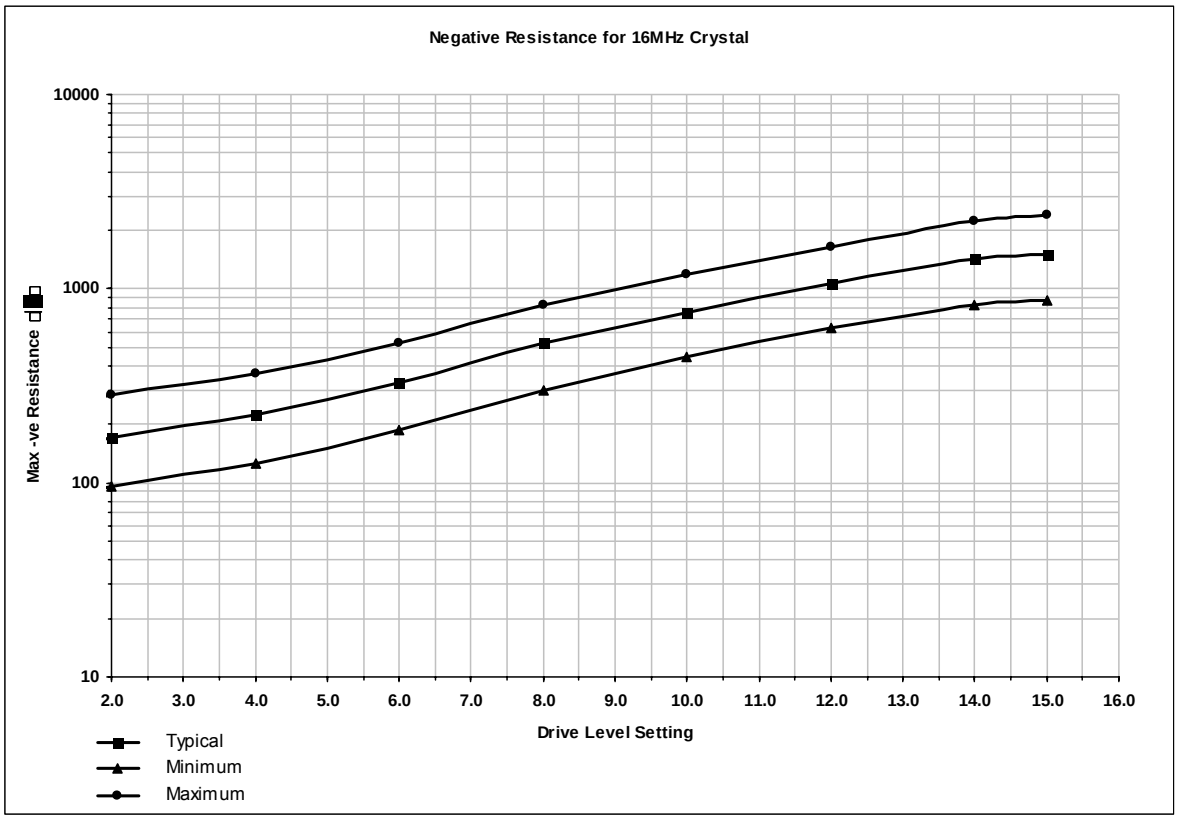


Figure 11.9: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (Refer to your software build release note for frequencies supported)

Crystal C_0 = 0.75pF

Circuit parameters:

C_{trim} = 8pF, maximum value

C_{t1},C_{t2} = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

11.4 UART Interface

BlueCore4-ROM CSP UART interface provides a simple mechanism for communicating with other serial devices using the RS232 standard (1).

Four signals are used to implement the UART function:

- UART_TX
- UART_RX
- UART_RTS
- UART_CTS

When BlueCore4-ROM CSP is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. That is, low means data can be sent. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.

UART configuration parameters, such as Baud rate and packet format, are set using BlueCore4-ROM CSP PS keys.

Notes:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

(1) Uses RS232 protocol but voltage levels are 0V to VDD_USB (requires external RS232 transceiver chip)

Parameter		Possible Values
Baud Rate	Minimum	1200 Baud (≤2%Error)
		9600 Baud (≤1%Error)
	Maximum	3MBaud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Table 11.5: Possible UART Settings

The UART interface is capable of resetting BlueCore4-ROM CSP upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 11.10. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset occurs. This allows a host to initialise the system to a known state. Also, BlueCore4-ROM CSP can emit a break character that can be used to wake the Host.

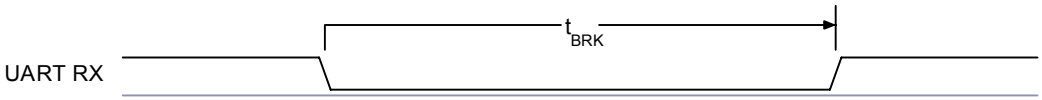


Figure 11.10: Break Signal

Table 11.6 shows a list of commonly used Baud rates and their associated values for the PS Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any Baud rate within the supported range can be set in the PS Key according to the formula in Equation 11.9.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Equation 11.9: Baud Rate

Baud Rate	PSKEY_UART_BAUD_RATE Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 11.6: Standard Baud Rates

11.4.1 UART Bypass

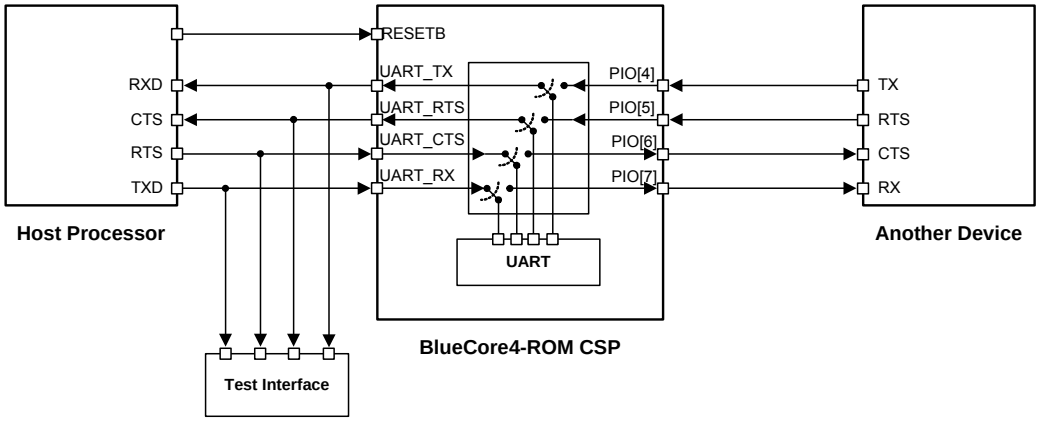


Figure 11.11: UART Bypass Architecture

11.4.2 UART Configuration while RESETB is Active

The UART interface for BlueCore4-ROM CSP while the IC is being held in reset is tri-stated. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore4-ROM CSP RESETB pin is de-asserted and the firmware begins to run.

11.4.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore4-ROM CSP can be used. The default state of BlueCore4-ROM CSP after reset is de-asserted is for the host UART bus to be connected to the BlueCore4-ROM CSP UART, thereby allowing communication to BlueCore4-ROM CSP via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS(1).

To apply the UART bypass mode, a BCCMD command is issued to BlueCore4-ROM CSP. At this command it will switch the bypass to PIO[7:4] as shown in Figure 11.11. When the bypass mode has been invoked, BlueCore4-ROM CSP enters the deep sleep state indefinitely.

To re-establish communication with BlueCore4-ROM CSP, the IC must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

Note:

(1) The range of the signalling level for the standard UART described in section 11.4 and the UART bypass may differ between CSR BlueCore devices, as the power supply configurations are chip dependent. For BlueCore4-ROM CSP the standard UART is supplied by VDD_USB so has signalling levels of 0V and VDD_USB, whereas in the UART bypass mode the signals appear on the PIO[4:7] which are supplied by VDD_PADS. Therefore the signalling levels are 0V and VDD_PADS.

11.5 USB Interface

BlueCore4-ROM CSP devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth Specification v2.0 + EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as a set of USB speakers.

USB is a master/slave oriented system (in common with other USB peripherals). BlueCore4-ROM CSP only supports USB slave operation.

11.5.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore4-ROM CSP and therefore have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP / USB_DN and the cable. Typically these resistors are between 22Ω and 27Ω.

11.5.2 USB Pull-Up Resistor

BlueCore4-ROM CSP features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore4-ROM CSP is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

11.5.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

11.5.4 Self-powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode to design for because the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS is connected to BlueCore4-ROM CSP via a resistor network (R_{vb1} and R_{vb2}), so BlueCore4-ROM CSP can detect when VBUS is powered up. BlueCore4-ROM CSP will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5kΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in BlueCore-4 ROM CSP is only suitable for bus-powered USB devices (dongles, for example).

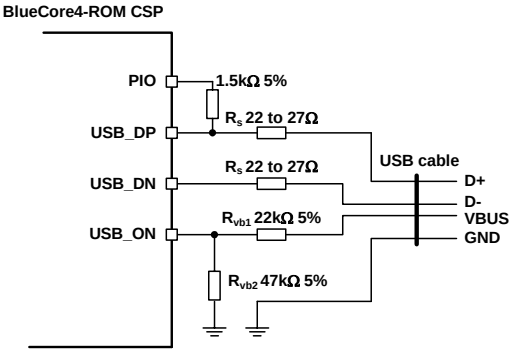


Figure 11.12: USB Connections for Self Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding PIO number.

11.5.5 Bus-powered Mode

In bus-powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore4-ROM CSP negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, BlueCore4-ROM CSP requests 100mA during enumeration.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than 10µF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore4-ROM CSP will result in reduced receive sensitivity and a distorted RF transmit signal.

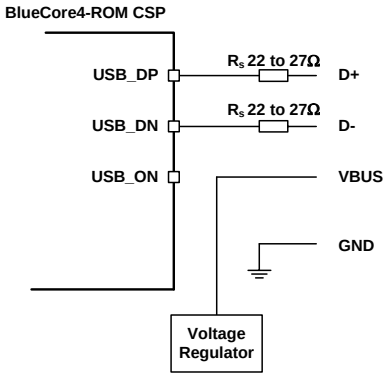


Figure 11.13: USB Connections for Bus-Powered Mode

Note:

USB_ON is shared with BlueCore4-ROM CSP PIO terminals.

Identifier	Value	Function
R_s	22 to 27Ω	Impedance matching to USB cable

Table 11.7: USB Interface Component Values

11.5.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB Suspend mode. While in USB Suspend, bus-powered devices must not draw more than 0.5mA from USB VBUS (self-powered devices can draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or RF power amplifiers can be turned off by BlueCore4-ROM CSP. The entire circuit must be able to enter the suspend mode. (For more details on USB Suspend, see BlueCore Power Saving Modes).

11.5.7 Detach and Wake-Up Signalling

BlueCore4-ROM CSP can provide out-of-band signalling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore4-ROM CSP into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore4-ROM CSP to put USB_DN and USB_DP in a high impedance state and turn off the USB pull-up resistor. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore4-ROM CSP will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB_WAKE_UP message (which runs over the USB cable and cannot be sent while BlueCore4-ROM CSP is effectively disconnected from the bus).

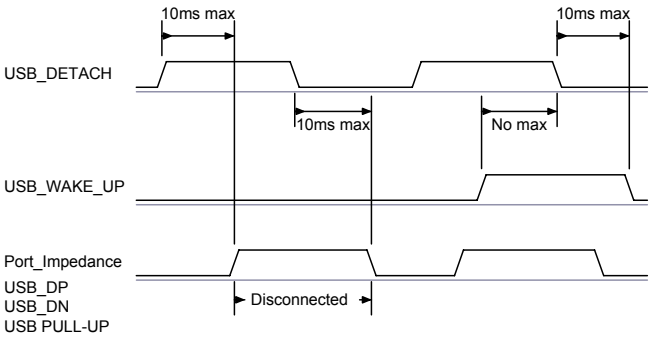


Figure 11.14: USB_DETACH and USB_WAKE_UP Signalling

11.5.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore4-ROM CSP and Bluetooth software running on the host computer. Suitable drivers are available from www.csrsupport.com.

11.5.9 USB Compliance

BlueCore4-ROM CSP is designed to be compatible with and adhere to the USB specification v1.1, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore4-ROM CSP meets the USB specification, CSR cannot guarantee that an application circuit designed around the IC is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification (Chapter 7) electrical requirements.

11.5.10 USB 2.0 Compatibility

BlueCore4-ROM CSP is compatible with USB 2.0 host controllers. Under these circumstances the two ends default to 12Mbits/s and do not enter high-speed mode.

11.6 Serial Peripheral Interface

BlueCore4-ROM CSP uses a 16-bit data and 16-bit address serial peripheral interface. Transactions may occur when the internal processor is running or is stopped. This section describes the considerations required when interfacing to BlueCore4-ROM CSP via the four dedicated serial peripheral interface terminals. Data can be written or read one word at a time or the auto increment feature can be used to access blocks of data.

11.6.1 Instruction Cycle

The BlueCore4-ROM CSP is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. The instruction cycle for an SPI transaction is shown in Table 11.8.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 11.8: Instruction Cycle for an SPI Transaction

Except when resetting the SPI interface, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4-ROM CSP on the rising edge of SPI_CLK. When reading, BlueCore4-ROM CSP replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CSB high.

It is a significant overhead to send a command word and the address of a register every time the register is to be read or written, especially when large amounts of data are transferred. To overcome this BlueCore4-ROM CSP offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low after a word of data is written or read, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

11.6.2 Writing to BlueCore4-ROM CSP

To write to BlueCore4-ROM CSP, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16 bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address A[15:0]. Thereafter for each subsequent 16 bits clocked in, the address A[15:0] is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

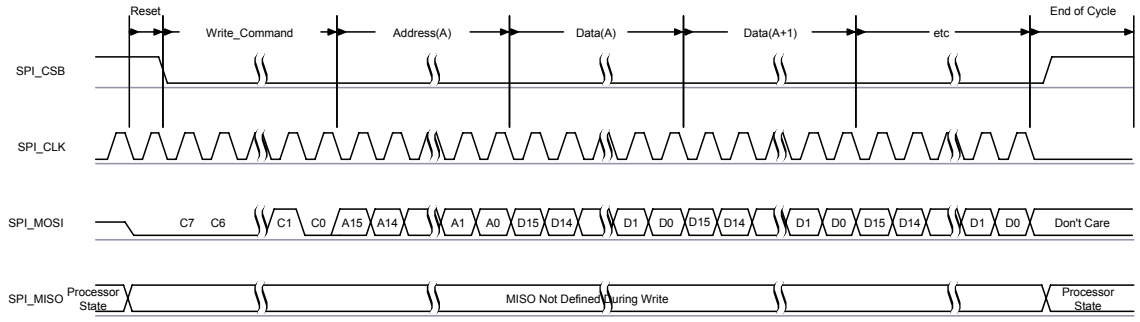


Figure 11.15: Write Operation

11.6.3 Reading from BlueCore4-ROM CSP

Reading from BlueCore4-ROM CSP is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore4-ROM CSP then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of C[7:0], A[15:8]. The check word can be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, where it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

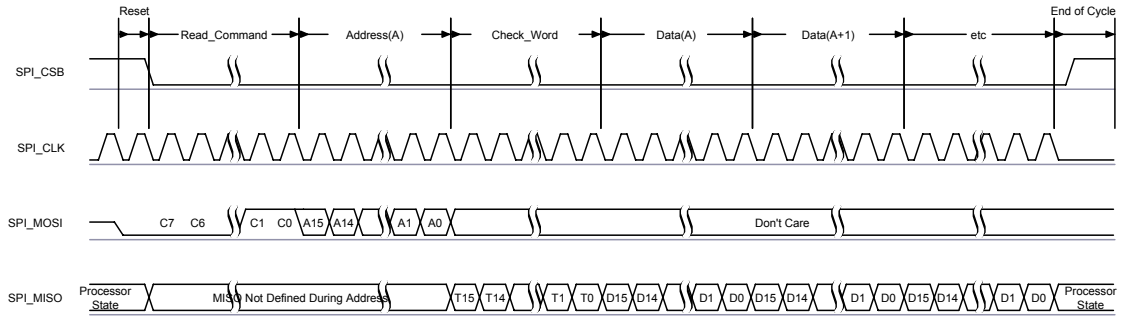


Figure 11.16: Read Operation

11.6.4 Multi-Slave Operation

BlueCore4-ROM CSP should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4-ROM CSP is deselected (SPI_CSB = 1), the SPI_MISO line does not float. Instead, BlueCore4-ROM CSP outputs 0 if the processor is running or 1 if it is stopped.

11.7 Audio PCM Interface

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, BlueCore4-ROM CSP has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. BlueCore4-ROM CSP offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore4-ROM CSP allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time(1).

BlueCore4-ROM CSP can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. BlueCore4-ROM CSP is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s, and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG.

BlueCore4-ROM CSP interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore4-ROM CSP is also compatible with the Motorola SSI™ interface

Note:

(1) Subject to firmware support. Contact CSR for current status.

11.7.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, BlueCore4-ROM CSP generates PCM_CLK and PCM_SYNC.

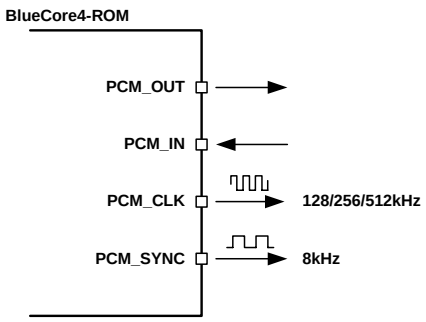


Figure 11.17: BlueCore4-ROM CSP as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore4-ROM accepts PCM_CLK rates up to 2048kHz.

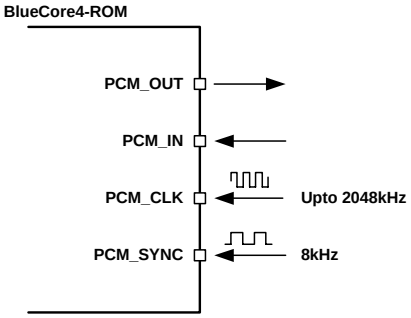


Figure 11.18: BlueCore4-ROM CSP as PCM Interface Slave

11.7.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-ROM CSP is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When BlueCore4-ROM CSP is configured as PCM Slave, PCM_SYNC can be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, that is 62.5µs long.

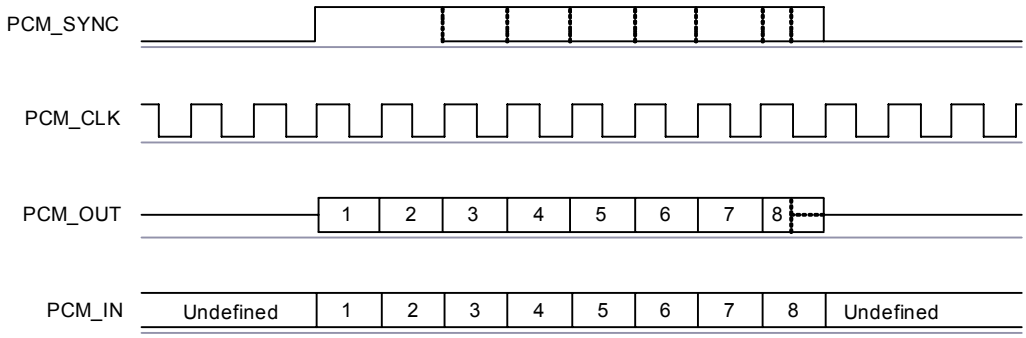


Figure 11.19: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4-ROM CSP samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

11.7.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

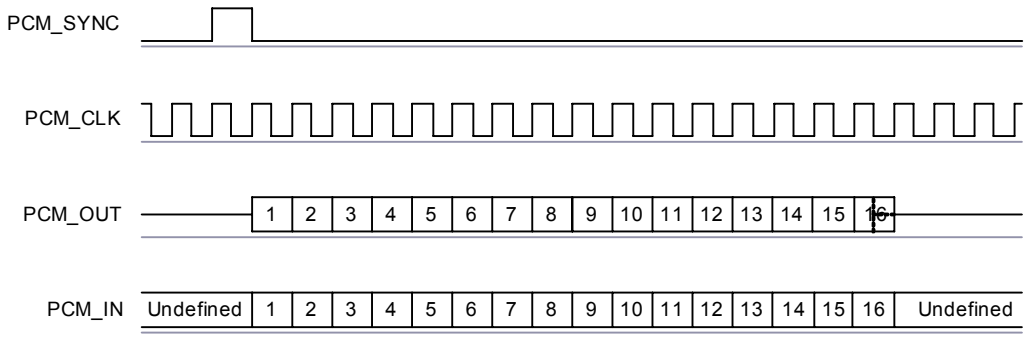


Figure 11.20: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4-ROM CSP samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT can be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

11.7.4 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

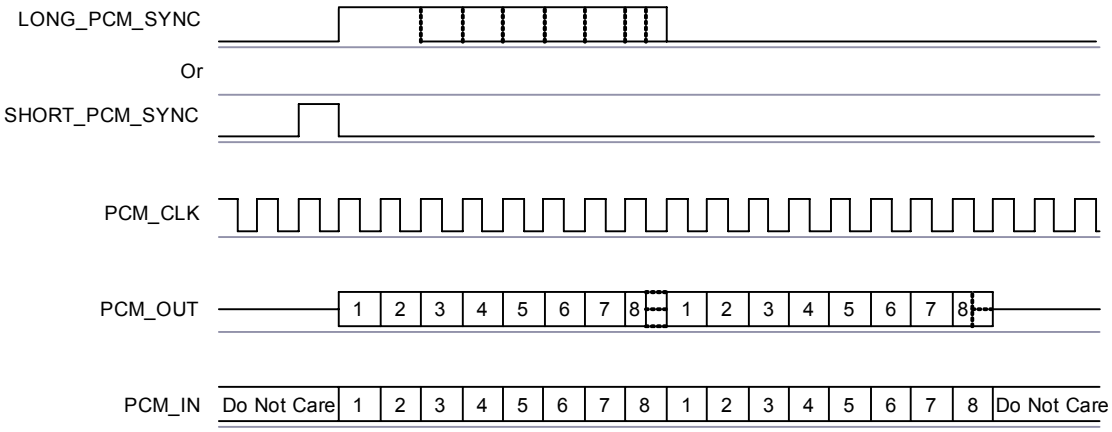


Figure 11.21: Multi Slot Operation with Two Slots and 8-bit Companded Samples

11.7.5 GCI Interface

BlueCore4-ROM CSP is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbits/s B channels can be accessed when this mode is configured.

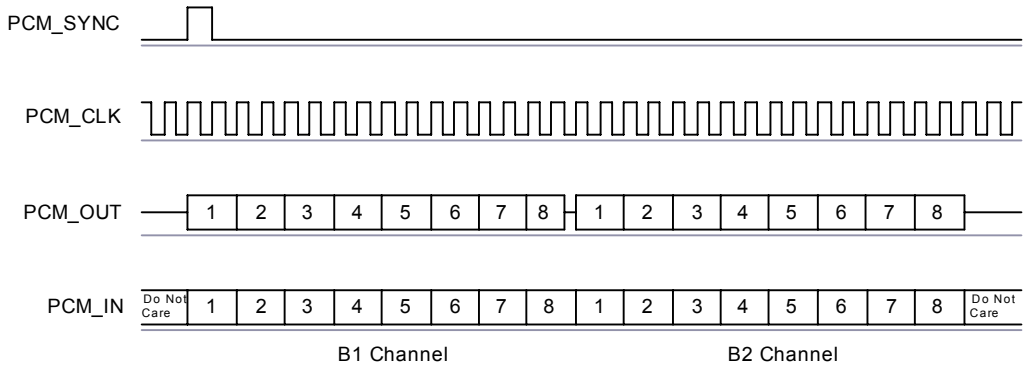


Figure 11.22: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore4-ROM CSP in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

11.7.6 Slots and Sample Formats

BlueCore4-ROM CSP can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles can only be used with 8-bit sample formats. Durations of 16 clocks can be used with 8, 13 or 16-bit sample formats.

BlueCore4-ROM CSP supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order can be little or big-endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot can be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

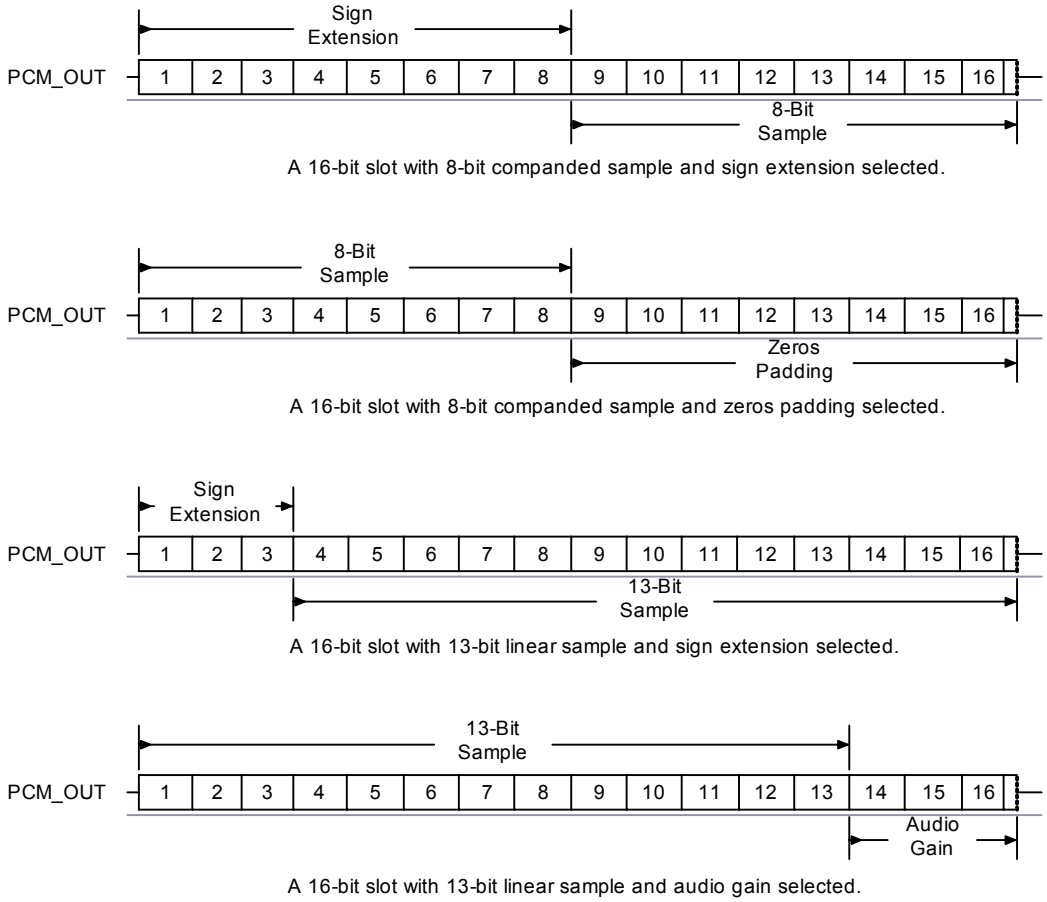


Figure 11.23: 16-Bit Slot Length and Sample Formats

11.7.7 Additional Features

BlueCore4-ROM CSP has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

11.7.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable, see Table 11.11	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable, see Table 11.12 and Section 11.7.10	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh} (1)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} (1)	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 11.9: PCM Master Timing

Note:

(1) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

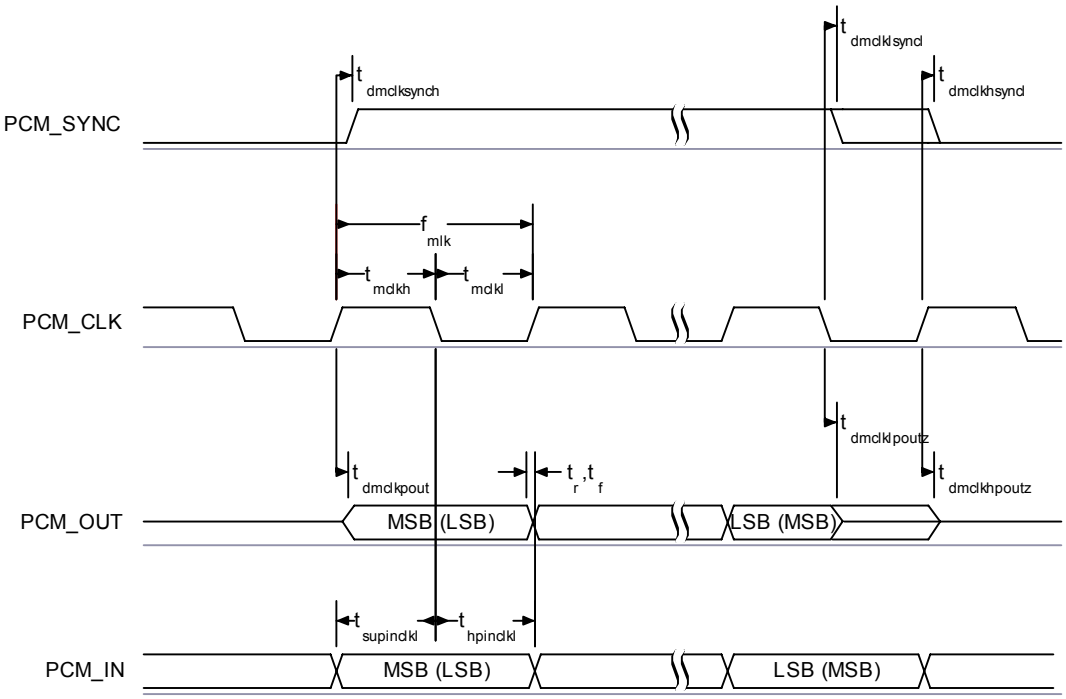


Figure 11.24: PCM Master Timing Long Frame Sync

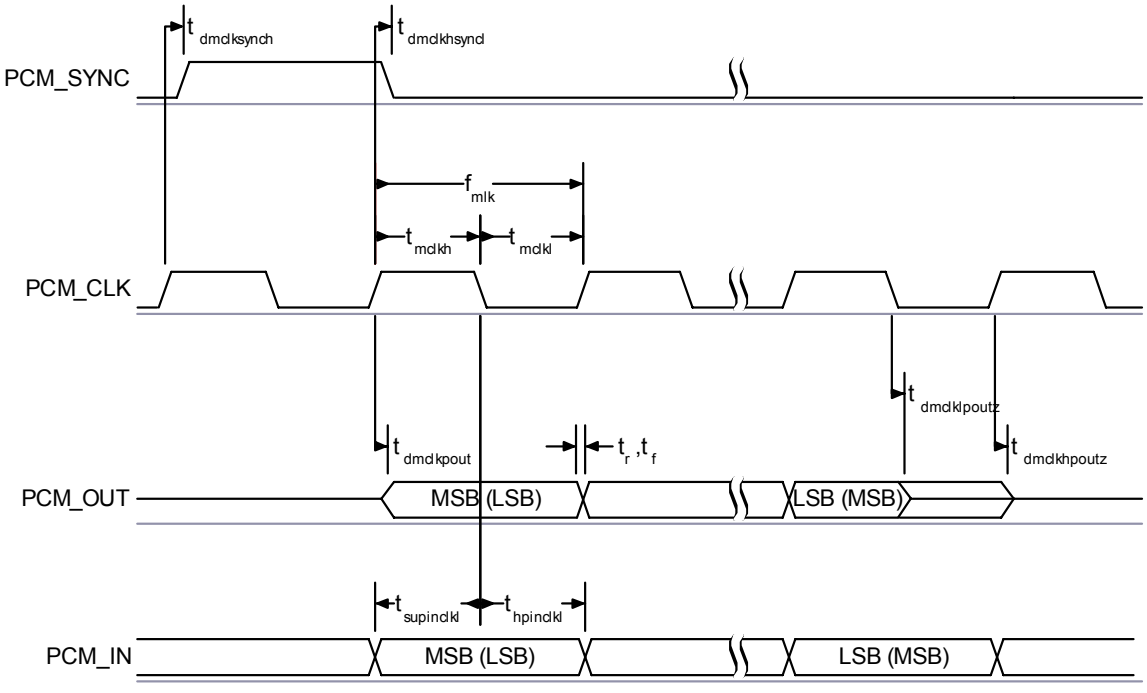


Figure 11.25: PCM Master Timing Short Frame Sync

11.7.9 PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-		ns

Table 11.10: PCM Slave Timing

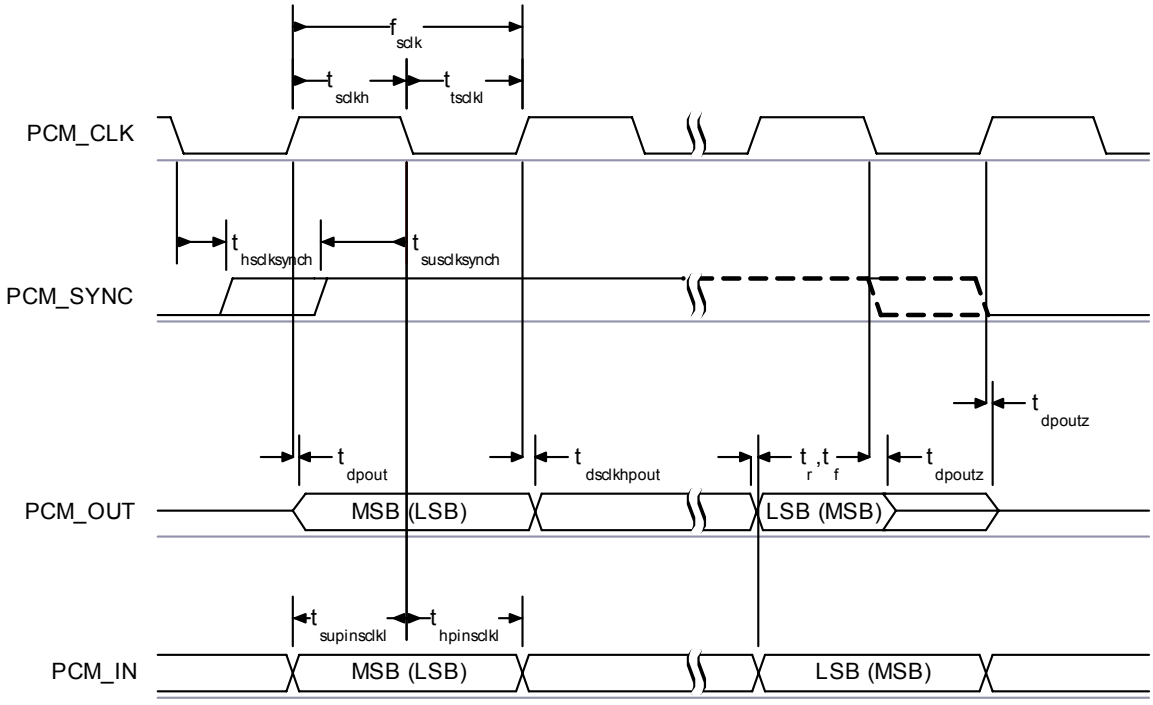


Figure 11.26: PCM Slave Timing Long Frame Sync

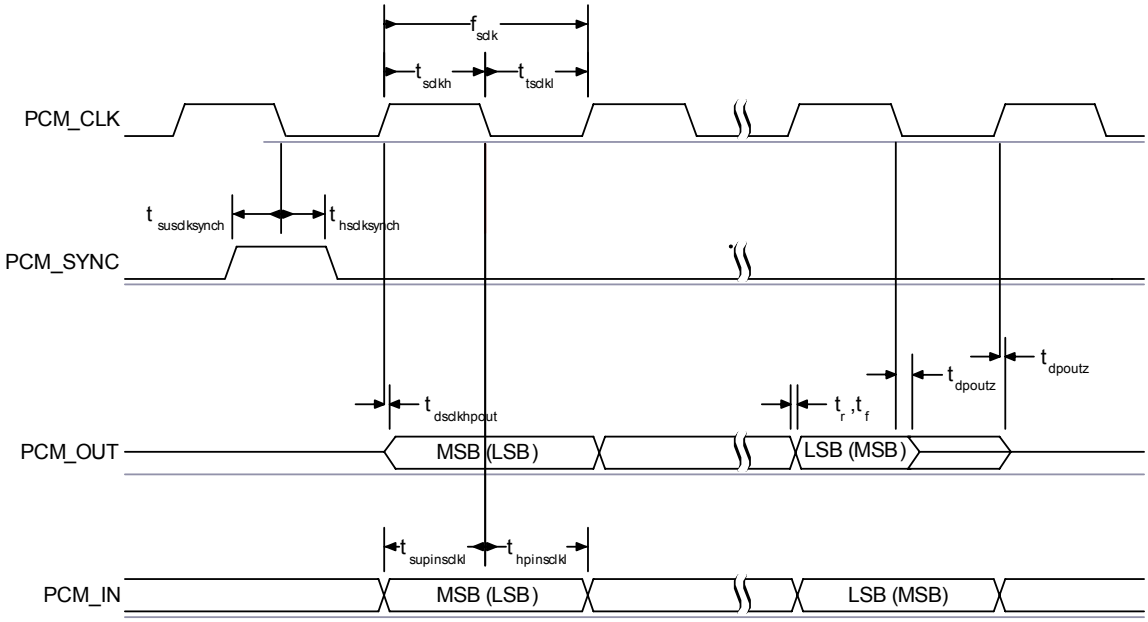


Figure 11.27: PCM Slave Timing Short Frame Sync

11.7.10 PCM_CLK and PCM_SYNC Generation

BlueCore4-ROM CSP has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore4-ROM CSP internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock which allows a greater range of frequencies to be generated with low jitter but consumes more power. This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by the LONG_LENGTH_SYNC_EN bit in PSKEY_PCM_CONFIG32.

Equation 11.10 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 11.10: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using following equation:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 11.11: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to `0x08080177`.

11.7.11 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The following tables describe these PS Keys. The default for PSKEY_PCM_CONFIG32 is 0x00800000. That is, first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristating of PCM_OUT. Table 11.12 describes PSKEY_PCM_LOW_JITTER_CONFIG.

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set.
SHORT_SYNC_EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 selects padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. 1 selects sign extension. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting. With 8-bit samples the 8 padding bits are zeroes.
LSB_FIRST_EN	5	0 transmits and receives voice samples MSB first. 1 uses LSB first.
TX_TRISTATE_EN	6	0 drives PCM_OUT continuously. 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 enables PCM_SYNC output when master. 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 enables GCI mode.
MUTE_EN	10	1 forces PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles. 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 11.11: PSKEY_PCM_LOW_JITTER_CONFIG Description

Name (Continued)	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit.
CNT_RATE	[23:16]	Sets PCM_CLK count rate.
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

Table 11.12: PSKEY_PCM_LOW_JITTER_CONFIG Description

11.8 I/O Parallel Ports

Thirteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[10:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO[0] and AIO[2] are powered from VDD_USB.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset. See section 3 CSP Package Information for details.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore4-ROM CSP is provided from a system application specific integrated circuit (ASIC).

BlueCore4-ROM CSP has two general-purpose analogue interface pins, AIO[0] and AIO[2]. These access internal circuitry and control signals. One pin, typically AIO[2], is allocated to decoupling for the on-chip band gap reference voltage. The other can be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals, 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_USB (1.8V).

11.8.1 PIO Defaults for BlueCore4-ROM CSP

CSR cannot guarantee that these terminal functions remain the same. Refer to the software release note for the implementation of these PIO lines because they are firmware build specific.

11.9 I²C Master

PIO[8:6] can be used to form an interface. The interface is driven by “bit banging” these PIO pins using software. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

Note:

PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM cannot support UART bypass mode.

PIO lines need to be pulled-up through 2.2kΩ resistors.

For connection to EEPROMs, refer to CSR documentation on I²C EEPROMS for use with BlueCore. This provides information on the type of devices that are currently supported.

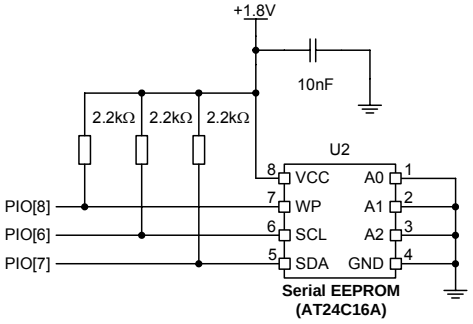


Figure 11.28: Example EEPROM Connection

11.10 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4-ROM CSP where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the Host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4-ROM CSP.

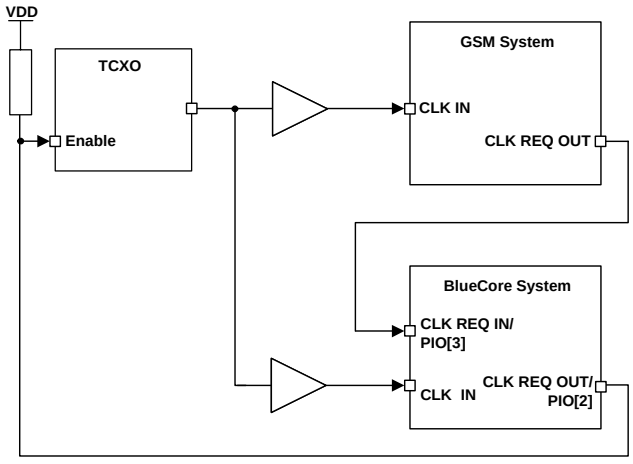


Figure 11.29: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] is tri-stated. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

11.11 Resetting BlueCore4-ROM CSP

BlueCore4-ROM CSP can be reset from several sources:

- the RESETB pin
- power on reset
- a UART break condition
- via a software configured watchdog timer

The RESETB pin is an active low reset and is internally filtered to prevent short glitches from causing a reset. A reset is performed between 1.5 and 4.0ms following RESETB being active. CSR recommends that RESETB is applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-stated. The PIOs have weak pull-downs.

Following a reset, BlueCore4-ROM CSP assumes that XTAL_IN is 40MHz, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-ROM CSP is configured for the actual XTAL_IN frequency. If there is no clock present at XTAL_IN, the oscillator in BlueCore4-ROM CSP free runs, again at a safe frequency though RF operation will not be possible until a clock is provided at XTAL_IN.

11.11.1 Pin States during Reset

Table 11.13 shows the pin states of BlueCore4-ROM CSP during reset.

Pin name	State: BlueCore4-ROM CSP
PIO[10:0]	Input with weak pull-down
PCM_OUT	Tri-stated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Tri-stated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Tri-stated with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Tri-stated with weak pull-down
AIO[2], AIO[0]	Connected to VSS
RESETB	Input with weak pull-up
TX_A	High impedance
TX_B	High impedance
XTAL_IN	High impedance, 250kΩ to XTAL_OUT
XTAL_OUT	High impedance, 250kΩ to XTAL_IN

Table 11.13: Pin States of BlueCore4-ROM CSP on Reset

11.11.2 Status after Reset

The state of the IC after a reset is as follows:

- Warm Reset(1): Baud rate and RAM data typically remain available, depending on firmware configuration
- Cold Reset(2): Baud rate and RAM data not available

Note:

(1) Warm Reset preserves persistent store in RAM but otherwise does a full system reset. All of memory (except the PS RAM) is erased. The memory manager is reinitialised. All the hardware is reset, all Bluetooth links are lost, and the USB bus is detached from and reattached to.

(2) Cold Reset is one of the following:

- Power cycle
- System reset (firmware fault code)
- Reset signal, see Section 11.11.

11.12 Power Supply

11.12.1 Voltage Regulator

An on-chip linear voltage regulator can be used to power the 1.8V dependent supplies. It is advised that a smoothing circuit using a 2.2µF low ESR capacitor in series with a 2.2Ω resistor is placed on the output VDD_ANA.

The regulator is switched into a low power mode when the device is sent into deep sleep mode. When the on-chip regulator is not required VDD_ANA is used as a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

11.12.2 Sequencing

It is recommended that VDD_CORE, VDD_RADIO and VDD_VCO are powered at the same time. This is true when these supplies are powered from the internal regulator in BlueCore4-ROM CSP. The order of powering supplies for VDD_PIO, VDD_PADS and VDD_USB is not important. However, if VDD_CORE is not present all inputs have a weak pull-down irrespective of the reset state.

11.12.3 Sensitivity to Disturbances

It is recommended that if BlueCore4-ROM CSP is supplied from an external voltage source VDD_VCO, VDD_ANA and VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided. A simple RC filter is recommended for VDD_CORE as this reduces transients put back onto the power supply rails.

The transient response of the regulator is also important as at the start of a packet power consumption will jump to the levels defined in peak current consumption section. It is essential that the power rail recovers quickly, so the regulator should have a response time of 20µs or less.

See Figure 12.1, the application schematic.

12 Application Schematic

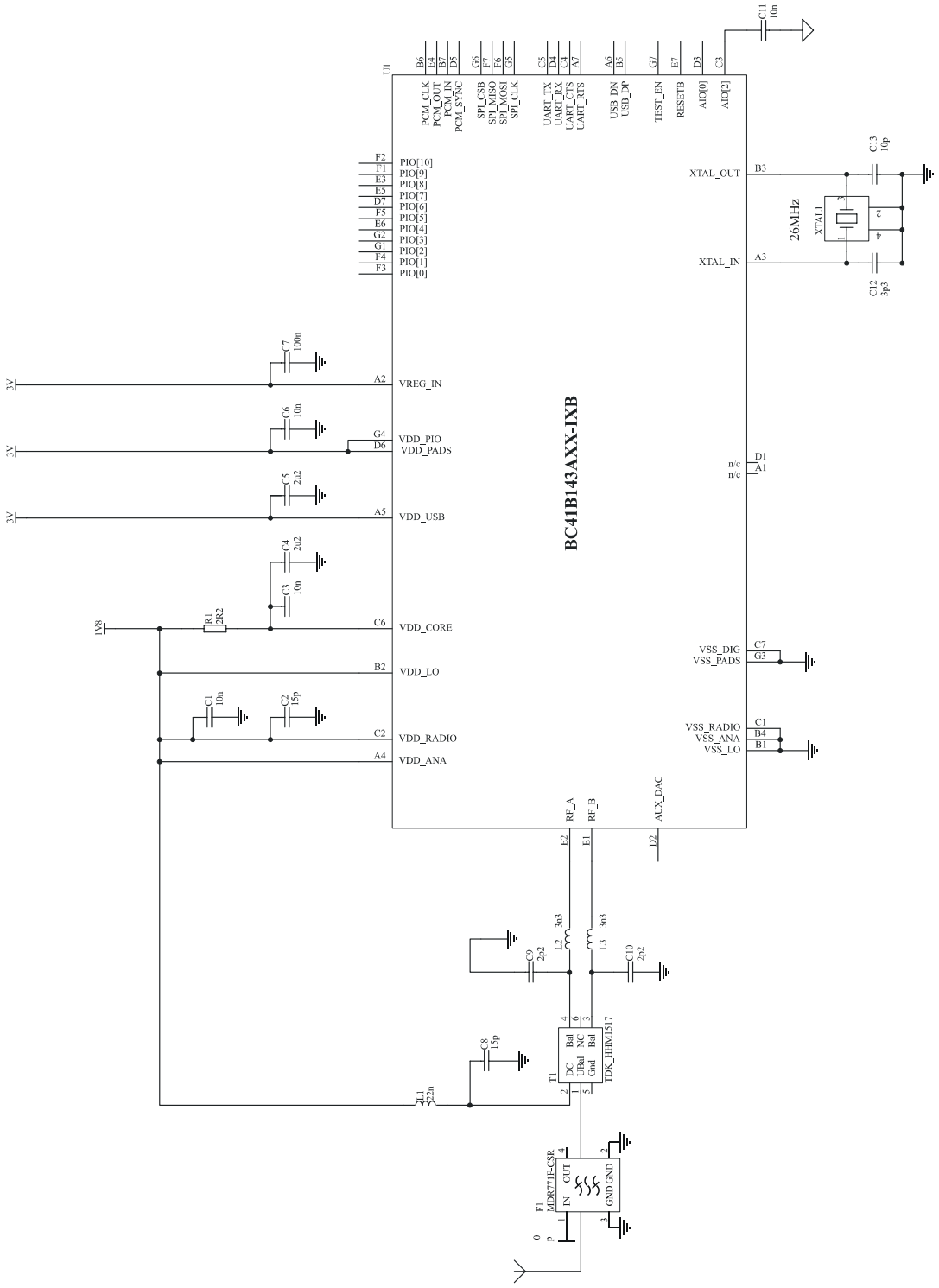
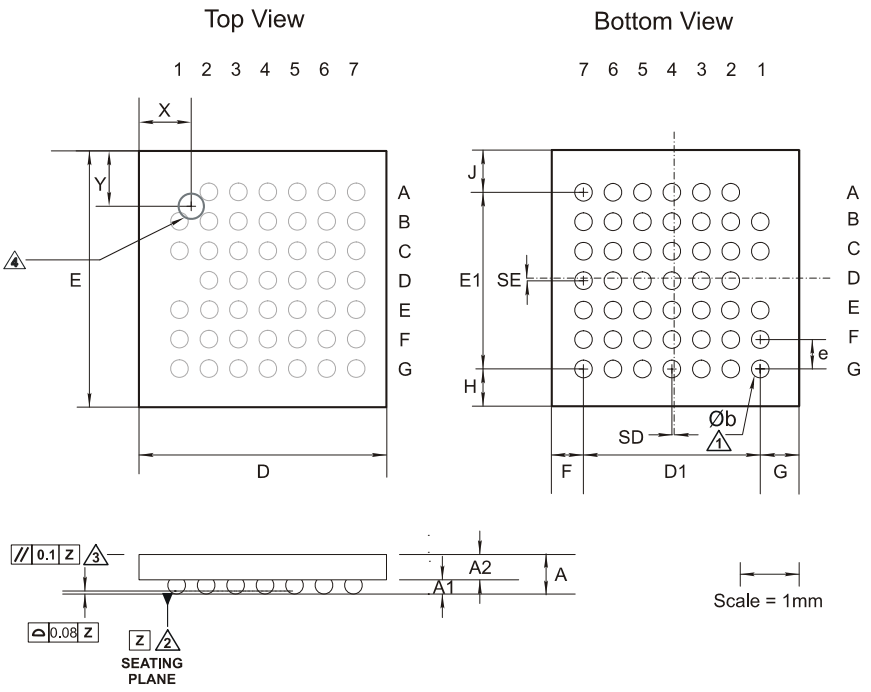


Figure 12.1: Application Circuit for CSP Package

13 Package Dimensions



Description	47-Ball Chip Scale Package (CSP)			
Size	3.8 x 4.0 x 0.7mm			
Pitch	0.5mm			
Package Ball Land	Non solder mask defined. Land aperture 300µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A	0.61	0.67	0.70	1 Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.21	0.24	0.27	
A2		0.43		
b	0.25	0.30	0.35	2 Datum Z is defined by the spherical crowns of the solder balls
D	3.65	3.75	3.85	
E	3.85	3.95	4.05	
e		0.50		3 Parallelism measurement shall exclude any effect of mark on top surface of package
D1		3.00		
E1		3.00		
F	0.285	0.335	0.385	4 Polarity mark. The dimension of the polarity mark is 0.3mm diameter
G	0.365	0.415	0.465	
H	0.375	0.425	0.475	
J	0.475	0.525	0.575	
SD		0.04		
SE		0.05		
X		1		
Y		1		
JEDEC	MO-211			
Unit	mm			

Figure 13.1: BlueCore4-ROM CSP Package Dimensions

14 Ordering Information

14.1 BlueCore4-ROM CSP

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	47-Ball CSP (Pb free)	3.8 x 4.0 x 0.7mm	Tape and reel	BC41B143AXX-IXB-E4

Note:

XX denotes firmware type and firmware version status. These are determined on a customer and project basis.

Minimum Order Quantity

2kpcs taped and reeled

15 Contact Information

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To contact a CSR representative, go to http://www.csr.com/contacts.htm

16 Document References

Document	Reference
Specification of the Bluetooth system	v2.0 + EDR, 04 November 2004
Universal Serial Bus Specification	v2.0, 27 April 2000
Selection of I^2C EEPROMS for Use with BlueCore	bcore-an-008Pb, 30 September 2003
EDR RF Test Specification	v2.0.e.2, D07r22, 16 March 2004
RF Prototyping Specification for Enhanced Data Rate IP	v.90, r29, 2004
BlueCore Power Saving Modes	bcore-me-008Pa

Terms and Definitions

π/4 DQPSK	pi/4 rotated Differential Quaternary Phase Shift Keying
8DPSK	8-phase Differential Phase Shift Keying
AC	Alternating Current
ACL	Asynchronous ConnectionLess, a Bluetooth data packet type
ADC	Analogue to Digital Converter
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
A-law	Audio encoding standard
BCCMD	BlueCore Command
BCHS	BlueCore Host Software
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BGA	Ball Grid Array
BIST	Built-In Self-Test
BlueCore™	Group term for CSR's range of Bluetooth chips
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
C/I	Carrier Over Interferer
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CSB	Chip Select (Active Low)
CSP	Chip Scale Package
CSR	Cambridge Silicon Radio
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DEVM	Differential Error Vector Magnitude
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended Synchronous Connection-Oriented
ESR	Equivalent Series Resistance
FDMA	Frequency Division Multiple Access
FSK	Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
HV	Header Value
I/O	Input Output
IF	Intermediate Frequency
IQ Modulation	In-Phase and Quadrature Modulation

ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksamples/s	kilosamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LED	Light Emitting Diode
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LSB	Least-Significant Bit
MCU	Modem Controller
MISO	Master In Slave Out
MOSI	Master Out Slave In
μ-law	Audio Encoding Standard
OHCI	Open Host Controller Interface
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PDA	Personal Digital Assistant
PICS	Protocol Implementation Conformance Statement
PIO	Parallel Input Output
ppm	parts per million
PS Key	Persistent Store Key, a non-volatile setting held in flash memory or downloaded at boot time
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
rms	root mean squared
RoHS	Restrictions of Hazardous Substances
ROM	Read Only Memory
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SPI	Serial Peripheral Interface
SSI	Signal Strength Indication
TCXO	Temperature Controlled Crystal Oscillator
TDMA	Time Division Multiple Access

TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHCI	Universal Host Control Interface
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
W-CDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Document History

Date	Revision	Reason for Change
FEB 05	a	Original publication of Advance Information Product Data Sheet (CSR reference BC41B143A-ds-001Pa).
MAR 05	b	Change to section 2 Key Features and 3.2 UART_RX and UART_CTS (CSR reference BC41B143A-ds-002Pb).
AUG 05	c	Updated Auxiliary DAC in Description of Functional Blocks Amendment to note concerning specified output voltage in the Auxiliary DAC table (Input/Output Terminal Characteristics) in Electrical Characteristics Amendment to note concerning VREG_EN and VREG_IN in Linear Regulator table of Electrical Characteristics section. Power Consumption moved from Radio Characteristics - Basic Data Rate to Electrical Characteristics section; added Enhanced Data Rate section Changed title of Record of Changes to Document History; changed title of Acronyms and Abbreviations to Terms and Definitions Changed copyright information on Status Information page; updated Contact Information
SEPT 05	d	Data Sheet raised to Production Status Major changes include: ▪ Addition of Typical Radio Performance – Basic Data Rate section to Data Book ▪ Updated Radio Characteristics – Basic Data Rate and Radio Characteristics – EDR ▪ Updated Power Consumption, Electrical Characteristics

BlueCore™4-ROM CSP EDR

Product Data Sheet

BC41B143A-ds-002Pd

September 2005