sames

AN1500A
APPLICATION NOTE

SINGLE CHIP TELEPHONE DEMO BOARD
SA2532K

1 Scope

This application note describes the use of the SA2532K Single Chip Telephone IC developed specifically to meet with India's Department of Telecommunication (DOT) Specification for the Electronic Telephone Instruments. This application note is based on the use of the multi-purpose demo board DB1500I with the SA2532K IC

2 Key Features

- High performance telephone with speech circuit, DTMF/Pulse dialer and tone ringer
- Very few external low cost components
- CMOS technology, far less sensitive to EMC
- EMC proof single sided layout, provision for EMC blocking capacitors installed
- Internally set real AC impedance to reduce external components
- Sidetone programmable by two resistors and one capacitor
- Ring frequency discrimination
- Line loss compensation selectable by jumper
- 2 different flash timings selectable by 2 flash keys
- 31 digit last number redial
- Sliding cursor protocol and pause key
- One-touch repeat dialing
- 1 direct memory
- Tone / Pulse switch
- Modular connectors for handset and line cord, line connector a/b- terminals selectable by jumper
- Layout prepared for 16kHz blocking filters
- 19-key SPST Keyboard on board
- Tone LED output Indicator
- Several hook transistor configurations
- Over-voltage and over-current circuit options

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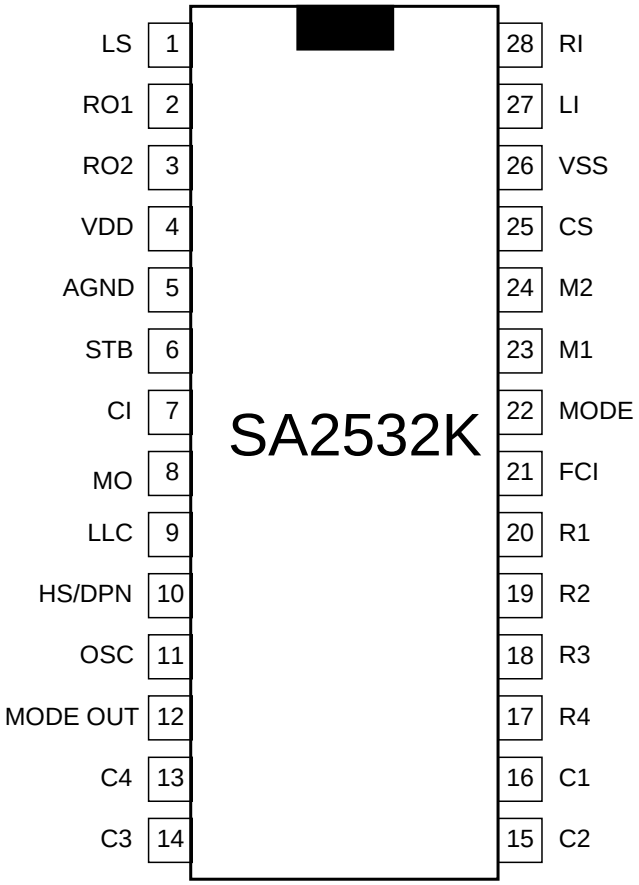
6. Application note for using Dynamic Mic : Application Note SAN3021

4 Revision status

AN1500 Application Note (this document):	
AN1500 Demo Board Schematic	Rev.: B
DB1500I Demo Board Layout	Rev.: 1.0

5 SA2532K Pin Layout .



6 General Description

The SA2532K device was developed to provide “plug & play” solution for the Indian DOT, emphasizing high performance voice transmission and reception. In spite of the fact that voice transmission and reception are the most vital features in telephony, they are very often ignored or given lower priority compared with some more or less useless non-voice features. No compromises were accepted during the design phase of the SA2532K, which is based on the SA2531/2 speech circuit and which supersedes even the hardest PTT requirements worldwide.

The dialler part is based on a long history of producing a wide range of dialer circuits with user-friendly features in compliance with various national PTT regulations. This knowledge enabled us to develop a specific product to meet with DOT type approval.

The last piece in the puzzle to complete the full picture of the first CMOS single chip POT was the tone ringer. A ring frequency discrimination circuit was implemented to avoid false “bell-tinkle” during pulse dialing from a parallel telephone. The 3-tone melody generator provides the ringing signal.

Note: all the subsequent component numbering is referenced to the AN1500 schematic, shown in pt.22

7 Demo board configuration

The SA2532K is the rare combination of advanced technology and down-to-earth simplicity providing easy and uncomplicated design effort for the telephone manufacturer. No fussing around: Simply go by the straight forward guidelines supplied by a highly experienced application group. No technology stress but appealing functionality. See Fig. 1 for configuration locations:

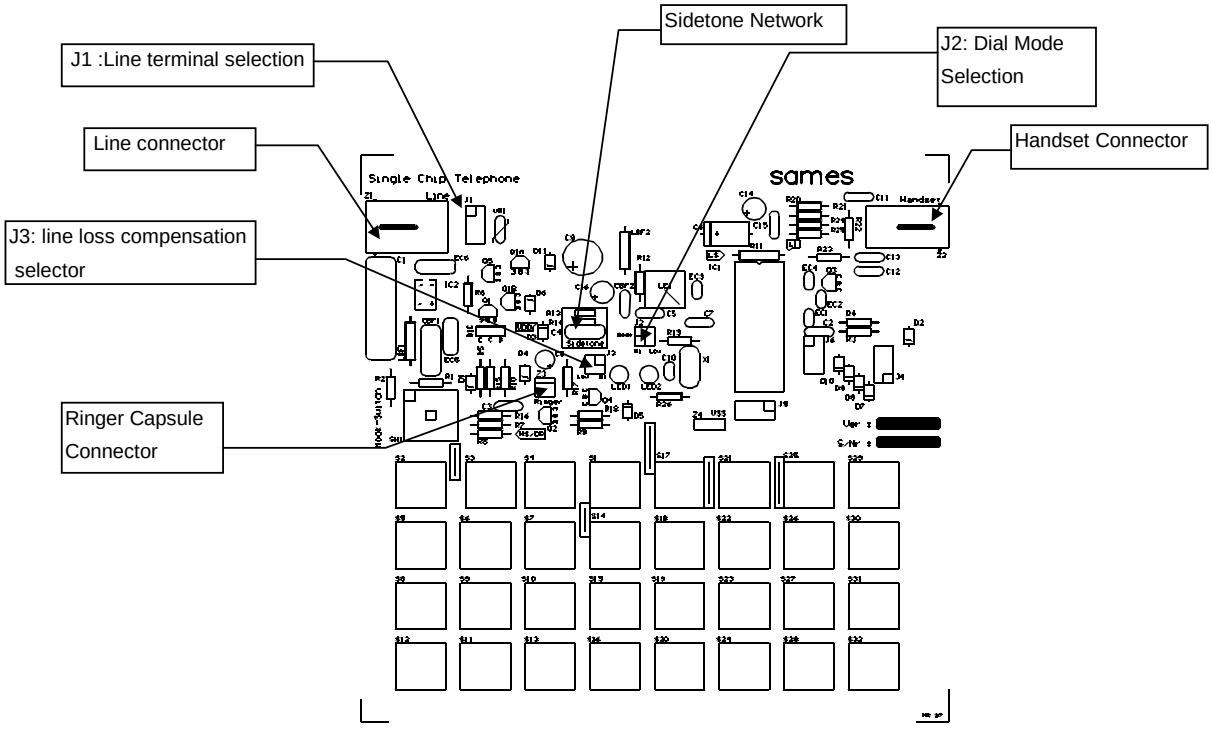
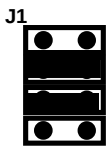
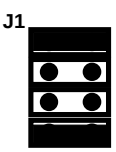


Fig. 1: Demo board configuration

7.1 Setting a/b line connection

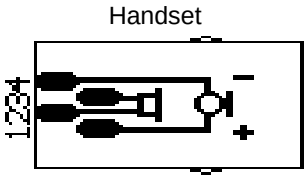
J1 allows selection of a/b line terminals to easily adapt the demo board to various PTT line connections:

inner two pins (default)	outer two pins (optional)
	

7.2 Connecting a handset

A handset connected at Z2 should have the following connections:

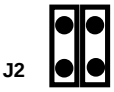
remark: observe polarity of the electret microphone



7.3 Setting dialing mode

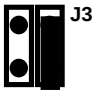
By J2, a selection of 3 different dialing modes can be made, 2 pulse (=LD) dialing modes and a DTMF dialing mode.

If LD Mode is selected then it is possible to switch into MF mode by pressing the ★ key but the mode will return to LD after a hookswitch operation or after a Recall (flash). In LD mode pulsing is at 10 pulses per second.

LD Mode make/break ratio 1:2	LD Mode make/break ratio 2:3	MF Mode
		

7.4 Setting line loss compensation (AGC)

Line loss compensation = line current dependent gain setting of Tx and Rx amplifiers can be set by jumper setting to 3 different modes : high, low and no LLC (=default).

LLC 45 to 75mA	LLC 20 to 50mA	no LLC
		

7.5 AC impedance

The Characteristic or output impedance of the SA2532K is set internally to 600Ω. No further components are required. For a complex impedance refer to pt 11.

8 Description of keyboard functions

The user-friendly operating procedures comply with different PSTN and PABX systems worldwide. By choosing between the total of 19 keys it is possible to fit the SA2532K into most telephone designs.

The keyboard is connected to 8 pins of the SA2532K (C1...C4, R1...R4) by a n*m SPST keyboard matrix. To extend two of the rows, a diode (D9 and D10) are added. This arrangement allows detection of 19 keys on a 4*4 matrix.

8.1 Numeric keys

The numeric keys (1..0,★,#) are standard number dial keys for both DTMF and pulse dialing (★and # only DTMF). Additionally the ★key can be used for temporary MF switching.

8.2 Flash keys (R,R2)

Selection of flash timing can be made by selecting one of the 2 flash keys :R1= 100ms and R2= 270ms.

8.3 Last number redial key (LNR)

The last number redial facility allows redialing of the last manually entered number by one keystroke. LNR is repeatable after each off-hook. The LNR key also supports the sliding cursor protocol (see pt. 10) to allow convenient redialing with PABX systems.

8.4 Pause key (PAUSE)

This key is to insert a pause in a digit string. Each pause is 2 seconds if inserted within the first 5 digits otherwise a wait function will halt dialling until a PS or LNR key is depressed.

8.5 Tone / Pulse switching

When any of the LD dialing modes is selected (see pt. 7.3), a switch to temporary MF can be performed by pressing the ★ key to get into DTMF mode and one of the flash (R)-keys to get back to pulse dialing. Once in MF mode the mode output LED is active.

Remark: temporary MF can only be activated, when the initial dialing mode selected by J2 (see pt. 7.3) is in one of the pulse dialing modes.

8.6 Enter/M5

The ENTER key is used to program the memory (M5). Pressing ENTER followed by the key M5 opens the memory location for storing the number.

9 Using the SA2532K

The DB1500I demo board is delivered with an SA2532K installed and the key functions are according to the chip are illustrated below.

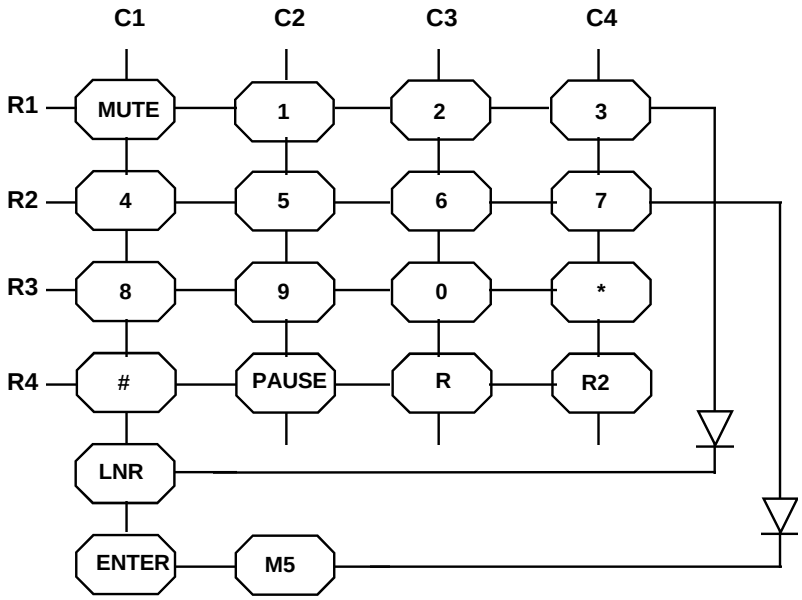


Fig. 2: SA2532K keyboard labels

10 Sliding cursor protocol and pause insertion

To accommodate easy and uncomplicated redialing behind a PABX, a **sliding cursor** protocol is implemented: if a manually entered digit string matches the contents of the LNR memory, pressing LNR will only dial out the remaining digits :

example: desired number 0123456 (where 01 is the access code)

off-hook, manual entry = **01**	-wait for dial tone	-**23456**	- line is busy	-on-hook
	(LNR contents is 0123456)			
off-hook, manual entry = **01**	-wait for dial tone	- press **LNR** key:		
	LNR dials out the remaining digits: 23456			

11 AC impedance of the SA2532K

The SA2532K is designed for applications requiring a characteristic impedance of 600 Ohms, no connection should be made to CI (pin 7) if a real impedance is required. Should a complex impedance be required a capacitor of approximately 1/10 of the complex part of the impedance should be connected to CI. Every complex impedance consists of a real and complex part. The ac impedance of the SA2532K is calculated by

$$Z_{AC} = Z_{SYN} + Z1$$

Where :

Z1 = the external resistor connected between pin 1(LS) and pin 27 (LI) . This resistor is also used by the device for current monitoring and sets the DC resistance. To maintain correct operation the value of this resistor should be set to 30 Ohm.

Z_{SYN} = the internally synthezised impedance.

For real impedances

$$Z_{SYN} = 19 * Z1$$
$$Z_{AC} = (19*Z_{SYN}) + Z1$$
$$Z_{AC} = 20 * Z1 = 600\ Ohm$$

If a impedance lower than Z_{AC} is required, then a external parallel impedance should be added between LS and V_{SS}. To calculate the resulting AC impedance, any parallel impedance path between LS and V_{SS} should be considered. For example, if a bipolar line transistor is used, the resistance from the transistors base to VSS (Z_P) is in the order of 10K (R10). If a MOSFET is used then Z_P is in the order of 100K which is negligible.

$$Z_{AC} = 600//Z_P$$

Care must be taken when selecting the value of ZP since the value chosen should be such that the line transistor is driven into full saturation.

11.1 Demo board measurements:

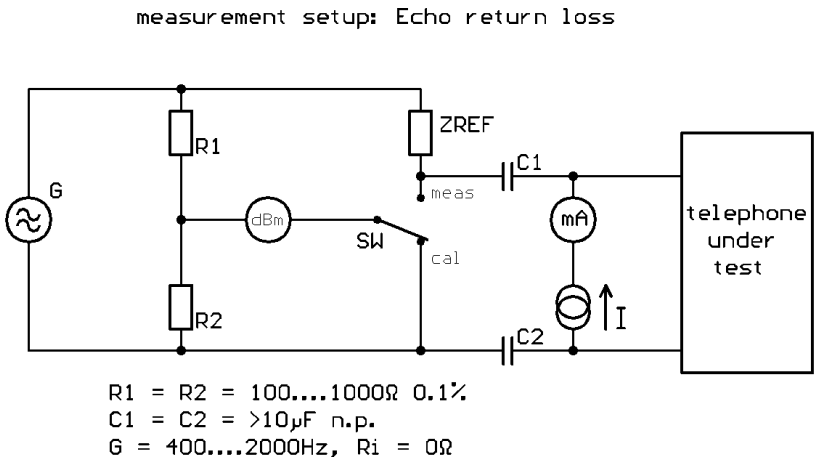
11.1.1 Definition:

return loss is defined as:

$$returnloss = 20 * \log\left|\frac{Zref + Zx}{Zref - Zx}\right|$$

where: Zref = the reference AC impedance (= the line termination)
Zx = the AC impedance of the telephone under test

11.1.2 Measurement:



Echo return loss (according to BAPT223 ZV5) is measured by bridge balance measurement as shown in Fig.3:
R1 and R2 must be matched to 0.1%, the measuring equipment must be isolated from earth and should have an input resistance of >25kΩ.
Capacitors C1 and C2 must be >10µF.
The Telephone under test is supplied by a (high ohmic) current source and measurements are taken in speech mode with a connected handset.

Fig. 3: Return loss measurement setup

Calculation of results:

The sending level, measured in “cal”-position of switch SW is tuned to ps=-10dB$_{950mV}$= 300mV$_{rms}$,thus the sinewave generator’s level is -4dB$_{950mV}$ = 600mV$_{rms}$.The receive level (=pe) is measured in “meas”-position of switch SW.

The echo return loss is then calculated by: **ar_{dB} = ps - pe** (ps, pe levels in dB$_{950mV}$)
or **ar_{dB} = 20* log (ps / pe)** (ps, pe levels in mV$_{rms}$)

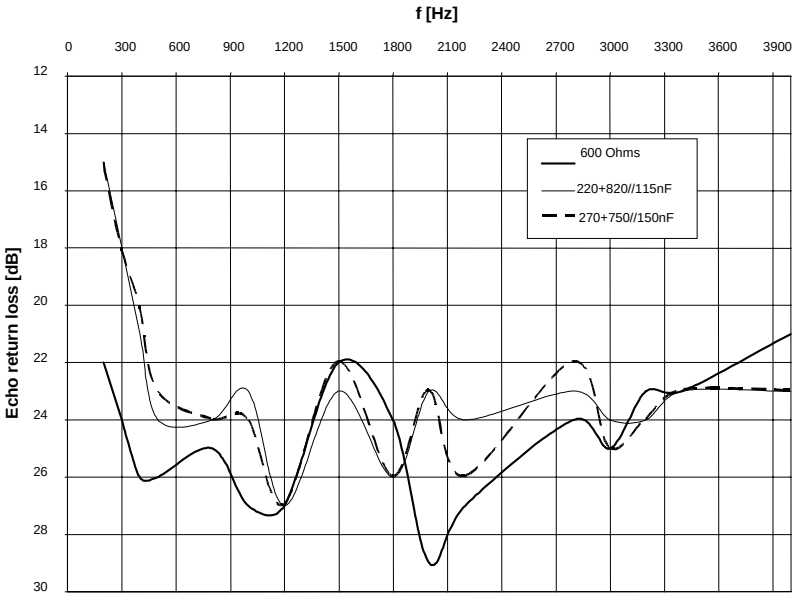


Fig.4 shows some typical results, measured with the DB1500I demo board with Z_{ref}= 600Ω, Z_{ref}= 220Ω + 820Ω//115nF and Z_{ref}= 270Ω + 750Ω//150nF.
The board was configured as shown in the schematic, using a single bipolar (2SA1210) line transistor.

Fig. 4: typ. return loss measurement results with the DB1500I demo board

12 Sidetone cancellation

The side tone is probably one of the most important parameters, if not *the* most important parameter. It determines very much the overall instinctive performance of a telephone since it has direct influence on other parameters. In a subjective test the two most inherent parameters are distortion and side tone, or other parameters directly influenced by those two, e.g. echo, acoustic stability, clearness, etc.

During the design of the SA2532K family considerable effort was put into the system definition of the side tone cancellation. It was clear that even the highest side tone cancellation could give an unpleasant harsh distortion at very large signal levels if no efficient limiter was provided. This led to the designing of what turned out to be the best “soft clipping” circuit yet developed, surpassing any solution used in a telephone so far.

The encounter is a side tone which is easy to calculate and which gives a well defined cancellation virtually independent of other parameters like return loss (ac impedance) and dynamic range (absolute input signal levels).

12.1 Dual Soft clipping:

The dual soft clipping circuit prevents harsh distortion and acoustic shock in both directions by limiting the maximum output of the Tx/Rx amplifiers at a level which still maintains a non-distorted signal (see V_{AGC} levels in data sheet).
If the output of the amplifier is already at the soft clip level and the input level is further increased, then the amplifier’s gain is reduced, so that the output level remains non-distorted at the soft clip level. Even fast input signal peaks are detected because of the fast attack time (see t_{ATTACK}) of the soft clip circuit. Instabilities are prevented by using a long decay time (see t_{DECAY} in data sheet).

12.2 Side tone balance network:

The side tone balance network is simply calculated as:

$Z_{BAL} = Z_{LINE} \times 10$

12.3 Example:

For a line termination of	270Ω+750Ω//150nF
the resulting sidetone balance network would be:	2k7 + 7k5//15nF
Within the AN2201 application, this would apply to	R13= 2k7 R14= 7k5 C4 = 15nF

13 The Double Wheatstone principle

The family of SA2532K single chip telephones are using a double Wheatstone bridge for return loss and side tone cancellation. This unique configuration makes it very easy and uncomplicated to set the side tone network.
Fig. 5 explains the principle of the Double Wheatstone bridge: For easier understanding the block diagram is split into two separate diagrams, which only show the relevant components.
The components shown in the block diagram represent the following components in the DB1500I schematic:

Z_{Line}:	the PTT´s AC impedance (external)
Z_1:	R11 = 30Ω
Z_2:	R12 = 300Ω
Z_{syn}:	Q3
Z_{bal}:	the sidetone network
R_{ref},Z_{ref}:	internal resistors

13.1 Sidetone cancellation

Perfect sidetone cancellation is achieved, when the sidetone balance network is matched to the line impedance by a factor of 10, which is equal to the matching of the resistors Z2 and Z1.
With ideal matching, no differential potential of the transmitted signal occurs at nodes RI and STB and the output of the RX amplifier is 0.

13.2 AC impedance

An internal amplifier controls the impedance of Zsyn by matching LI to an internal reference. Part of this internal reference is accessible by pin CI. When no external component is connected at that pin, the AC impedance of the circuit is synthesized to 600Ω.
When a capacitor is connected at CI, the AC impedance of the chip becomes complex. For correct adaption, the capacitance of CCI should be 1/10 of the line's complex part.

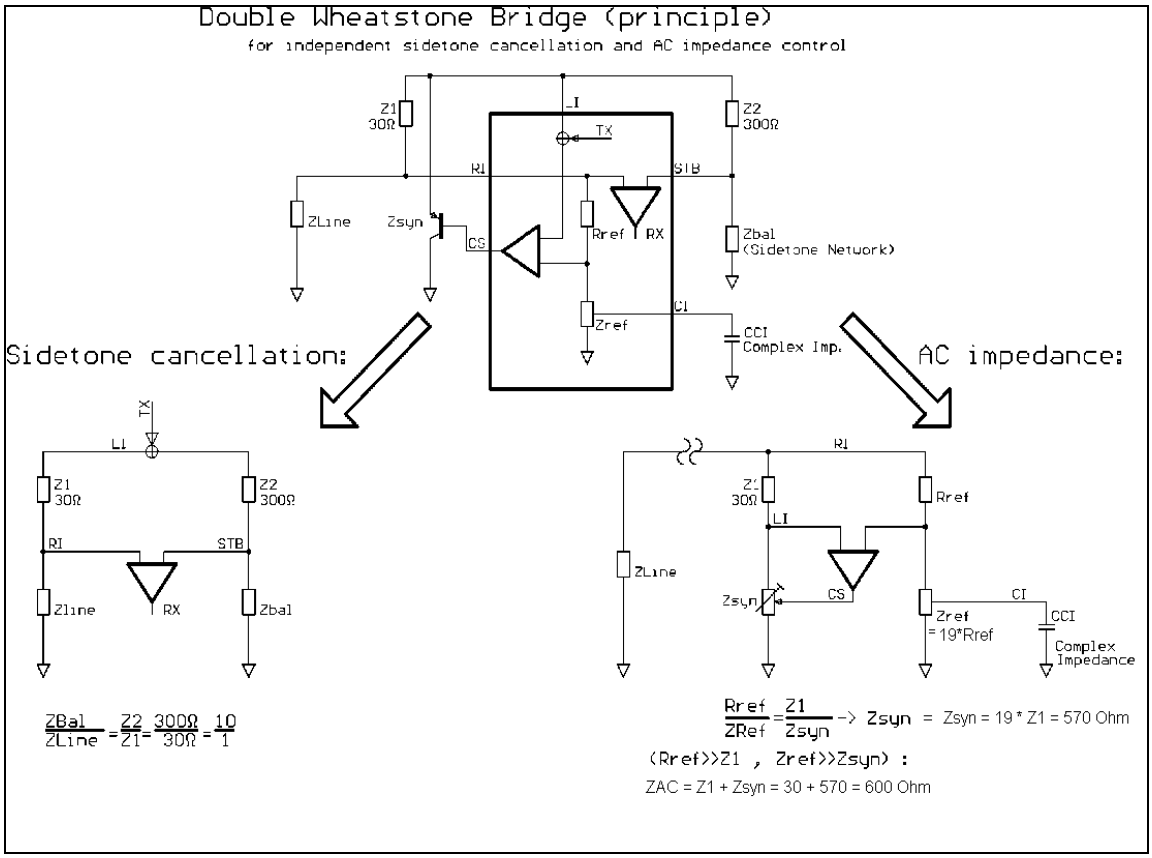


Fig. 5: Double Wheatstone bridge principle

14 Further Adjustments

14.1 Frequency response shaping: Transmit

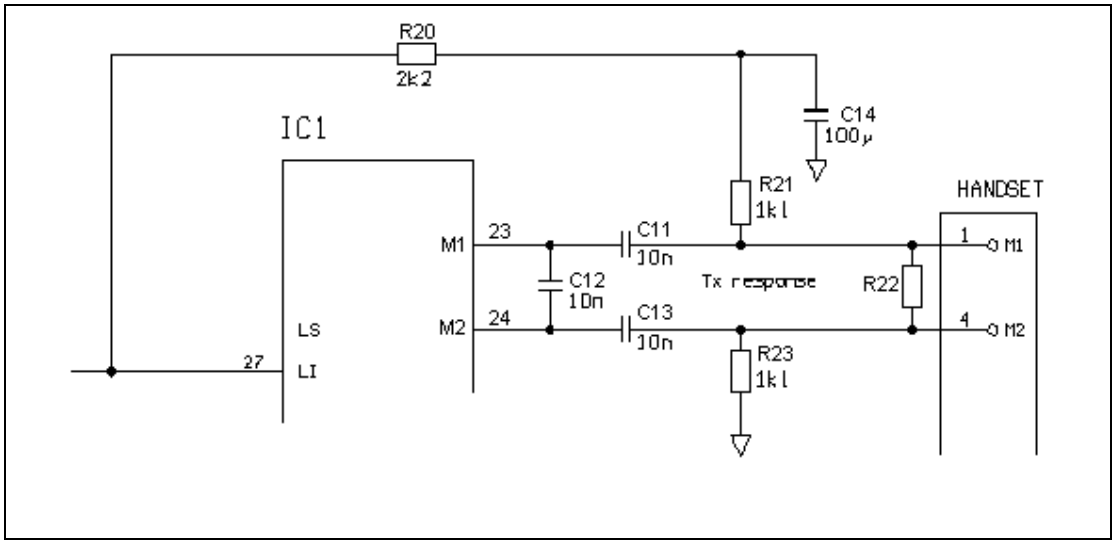


Fig. 6: Tx signal path

Transmit frequency response shaping is performed by 3 resistors for gain setting and 3..4 capacitors for frequency shaping:

14.1.1 Microphone gain setting

The electret handset microphone is supplied from the constant voltage at LI (#27), filtered by R20 and C14 (see fig 6). R21 and R23 are the bias resistors of the electret microphone. Transmit gain is set by both selecting the proper microphone type (sensitivity) and by varying R21 & R23. Reasonable values for these resistors are in the range of 1...2.5kΩ (each), which results in a gain adjustment range in the order of 6..8dB.

14.1.2 Tx frequency shaping:

Transmit frequency shaping can be done by C11,C13 (high pass) and C12(low pass). R22 can be installed to attenuate the microphone signal without affecting the frequeny response curve,

M1(#23) and M2 (#24)are differential inputs of the microphone amplifier. Please note the proper connection of the M1 and M2 inputs in respect to the positive and negative side of the microphone.

To find the correct values, a SLR (sending loudness ratings) measurement with the specific handset used in the customer's application must be made.

14.2 Frequency response shaping: Receive

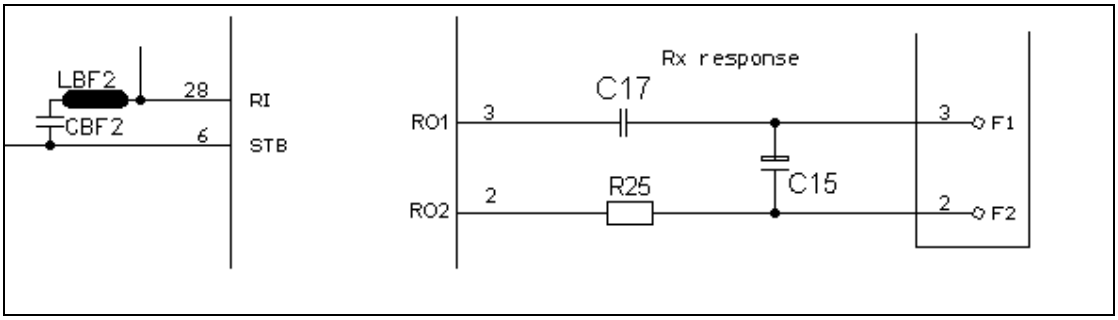


Fig. 7: Rx signal path

The receive signal is applied at the Rx amplifier input, RI (#28) and STB (#6) and is available at the differential outputs RO1 and RO2.

14.2.1 Receive gain setting:

Rx gain can be set by both the sensitivity of the earpiece and the value of R25.

14.2.2 Rx frequency shaping

Receive frequency shaping is done by C15 (low pass) at the Rx amplifier output. C17 impedes the DC path through RO1, RO2.

To find the correct values, a RLR (receive loudness ratings) measurement with the specific handset used in the customer's application must be made.

14.2.3 Metering pulses filtering

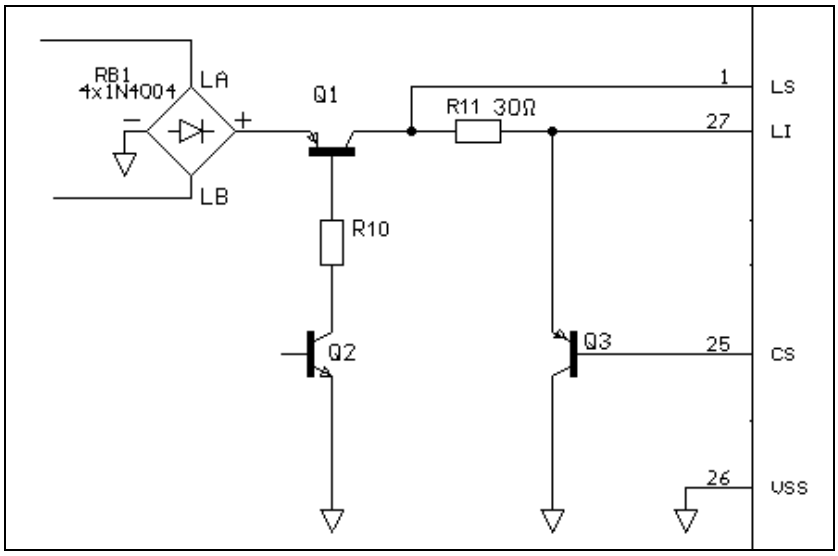
If filtering of metering pulses (typ. 12 or 16kHz) is required (for example in Germany) two blocking filters can be installed:
LBF1 , CBF1 as notch filter at the line input and
LBF2 ,CBF2 as notch filter at the Rx amplifier input

Note:
since CBF1 is connected at the line side, it must be a .../250V capacitor and LBF1 must be able to drive the maximum line current (≈100mA) without saturation.
LBF2 and CBF2 however, can be low voltage, low current components .

The application AN1500, shown with two resonators, gives adequate attenuation of the metering pulses signal. The benefit of this application is, that only one filter (LBF1,CBF1) is used on the high voltage/high current side, while the second notch filter (LBF2,CBF2) is connected at a low voltage/low current node, enabling use of low cost components.

15 Off-Hook conditions & DC mask

15.1 Line current path



When going off-hook, SW1/1 short circuits the leakage supply resistor R1 and enables a low-ohmic path from line into the telephone. At the same time SW1/2 supplies the base of Q2 via R7 and R8 and signals a "off-hook" state to the IC´s HS/DP-pin (#10). The base/gate of Q1 is pulled down by Q2 and the SA2532K is started up. V_{LI} (pin #27) is regulated to the specified voltage by shunt regulation from Q3.
Line current flows through the following path:

La -- RB1 -- Q1 -- R11 -- Q3 -- V_{SS} -- RB1 -- Lb

Fig. 8: DC mask & line current path

15.2 DC mask path

The DC characteristics (DC loop resistance) of the application is determined by the following conditions:

$$\mathbf{Va,b = V_{LI} + V_{R11} + V_{CE,Q1} + 2x(V_{f,RB1})}$$

- **V_{LI} :** The voltage at LI (#27) is shunt-regulated to 4.5V by Q3.
- **V_{R11}:** **$V_{R11} = I_{line} * R11$**, where: R11=30Ω
  changing the value of R11 is not recommended, since it affects the following parameters:
  AC impedance
  Tx and Rx gains
  DTMF level
  AGC switching positions
- **$V_{CE,Q1}$**: This parameter is mostly affected by the type of hook transistor configuration used, see pt.16 for details
- **$2x(V_{f,RB1})$**: Generally, the rectifier bridge must be installed to meet the specification for independence of polarity. **V_f** is typ. 0,7....0,8V (20...100mA). If lower forward voltages are required, an active (MOSFET) bridge must be used.

15.2.1 Setting for low DC mask:

The standard application regulates the voltage at LI to ≈4.5V_{DC} for line currents >10mA, determining the absolute level of the DC mask. Lower line currents cause a slope-down of V_{LI}, enabling operation down to 5mA . The resulting DC mask fits into most countries´ DC mask specs. Some countries however, like Denmark or Norway require a very low DC mask at line currents below ≈20mA line current. The constant voltage level at LI can be lowered to about 4.3V by connecting a 16kΩ-resistor from CI (#7) to Vss (#26). With this adaption, the DC mask is

lowered by only ≈0.2V for line currents >17mA. At lower line currents however, as required for these countries, the DC mask is lowered significantly, since slope-down of LI occurs already at line currents <17mA..

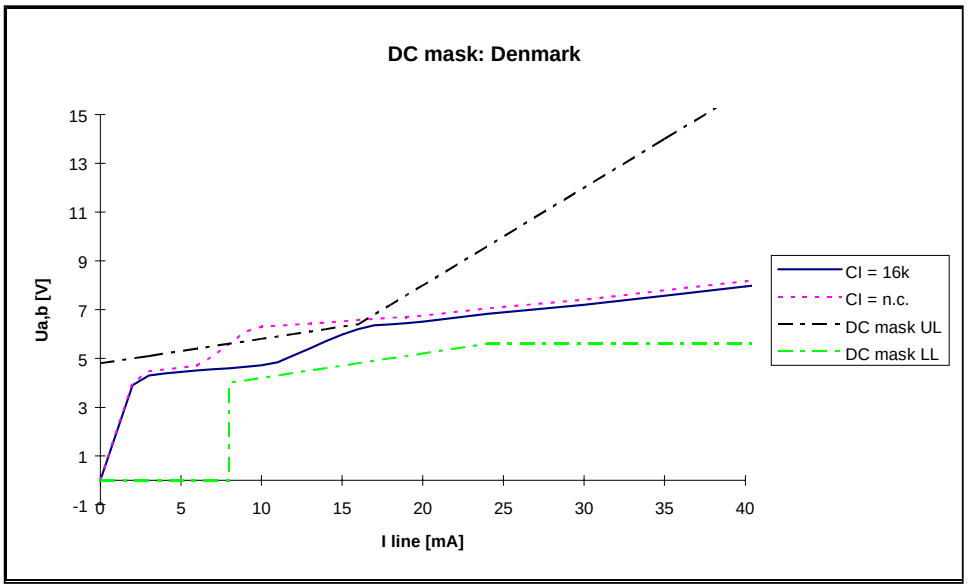


Fig. 9 : Example for low DC mask: Denmark

Fig.10 shows a typical example for a low DC mask setting compared with the DC-mask specs for Denmark (ETS 300 001: March 1996) : the solid line indicates the DC mask with a 16kΩ resistor connected at CI, while the dotted line shows the DC mask of the original AN1500 A0 version with a single PNP hook transistor (ref. pt.16).
Note: When connecting a resistor at CI, AC impedance, DTMF level, Tx/Rx gains and LLC gain curves are slightly changed. Therefore, after installing a resistor at CI, the above parameters must be readjusted.

15.3 Speech mode

In speech mode, shunt regulation (by Q3) is active and line current flows as described in pt 15.1. At the same time, both Tx and Rx amplifiers and 2 wire-4 wire conversion circuits are active.

15.4 DTMF dialing

During DTMF dialing the same line conditions as in Speech mode apply, except that speech is muted in both directions and a confidence tone is sent to the Rx amplifier.
The DTMF signal is modulated to the line by controlling the shunt transistor, Q3. During inter-digit pauses speech is also muted.

15.5 Pulse dialing

With pulse dialing, the line has to be interrupted during “break” periods and short circuited during “make” periods.
For example, “LD 60/40 10pps” means: break/make ratio is 60:40 with 10 pulses per second =
The dialing pulse is a **60ms break** (line interrupt) followed by a **40ms make** (line short circuit).
Dialing number “1” will result in one dialing pulse, total time = 100ms.
Dialing number “0” will result in 10 dialing pulses, total time = 10*100ms = 1sec.

Line break pulses are performed by Q1 being switched off. The on-off control signal is output from the HS/DP pin (#10) switching Q2 (and in turn Q1) on and off.

Make pulses are performed by Q3 with Q1 being switched on. The base of Q3 (=pin CS, #25) is pulled to V_{SS}, resulting in $V_{LI} = V_{BE} \approx 0.7V$.
CS is pulled low during the complete dialing period of one digit, which means in worst case (dialing number "0") the circuit cannot be supplied from line and must be buffered by the V_{DD}-cap, C9. Therefore C9 must be big enough to supply the active circuit for 1 second.

15.6 Pre-digit, Inter-digit ,inter-tone and access pauses

During pulse and DTMF dialing, several pauses must be added (see also: data sheet):

- pre-digit pause (PDP): Pause between CS=low and first break (pulse dialing only)
- inter-digit pause (IDP): Pause between pulse dialed out numbers, from last "make" to next PDP
- inter-tone pause (ITP): Pause between DTMF dialed out numbers
- access pause (AP): manually inserted pause in a digit string (see pt. 7.8)

16 Hook Transistor options

The following tables give an overview of the advantages and disadvantages of 3 different types of hook transistor arrangements: single bipolar PNP, PNP darlington and MOSFET. Any of these configurations can be installed on the demo board. Just check for corresponding part name on the PCB layout.

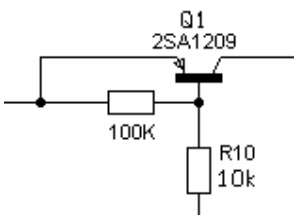
16.1 electrical requirements

Both hook transistor (Q1) and driver transistor (Q2) must be >=200V types, Q1 must have an IC >100mA. If single PNP configuration is used, the transistor must have a gain $\frac{IC}{IB} \geq 100$ at I_C=100mA. The driver transistor (Q2) must have enough gain to be in full saturation at high line currents (if driving a bipolar hook transistor).

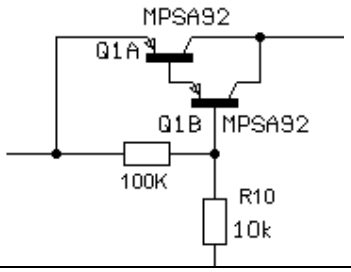
recommended types:

Q1	Q2
2SA1210, MPSA92,BSS92 (depending on configuration) BSP92 (SMD) KSA1156Y	2N5551 MPSA43 BF820 (SMD)

16.2 Single bipolar transistor

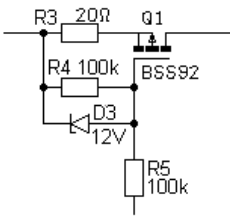
Schematic	+	-
	• lowest DC mask at low currents • just one transistor	• Transistor type must have a gain $\frac{IC}{IB} \geq 100$ at I_C=100mA • high on-resistance at high currents slightly affects gains and DTMF level • 10kΩ base resistor (R4) affects AC impedance

16.3 Bipolar darlington transistor

Schematic	+	-
	• low cost	• high DC mask at low currents may be tight to spec limits for some PTTs • 2 transistors • 10kΩ base resistor (R4) affects AC impedance

16.4 VMOS-FET with surge protection

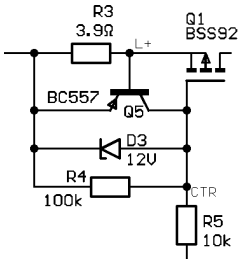
(surge protection = R3 =20Ω may also be used with bipolar hook transistor options)

Schematic	+	-
	• powerless switching • low on-resistance • low DC-mask • excellent surge protection • gate resistor (R5) does not affect AC impedance	• MOS handling required • higher cost than bipolars • few vendors

Principle: the source voltage is limited to ≈10V (D6; see schematic) in off-hook state . High voltage peaks induced at line will generate a high positive voltage drop across R3, lifting the gate voltage over the source voltage and thus cause the (P-channel) Transistor to shut off.

16.5 VMOS-FET with overcurrent protection

(overcurrent protection =R3,Q5 may also be used with bipolar hook transistor options)

Schematic	+	-
	• powerless switching • low on-resistance • lowest DC-mask • adjustable overcurrent protection • gate resistor (R5) does not affect AC impedance	• MOS handling required • higher cost than bipolars • few vendors • extra (low cost) transistor required

Principle: the line current generates a voltage drop across R3. If this voltage drop is >0.7V, C-E of Q5 is on and shuts Q1 off by short circuiting its Gate/Source voltage.
The shutoff current is calculated by $I_{shutoff}$ = 0.7V / R3 ; installed = 0.7V/3.9 Ω= 180mA

16.6 Current Limiting

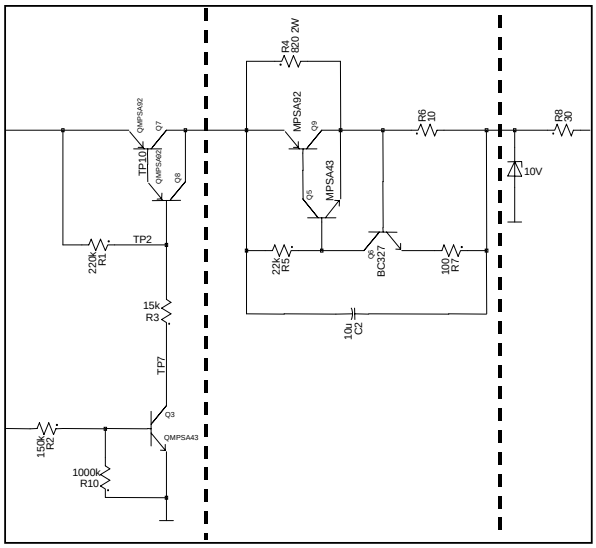


Fig. 9 : Example of current limiting circuit

Principle: the line current generates a voltage drop across R6. If this voltage drop is >0.7V the Q6 switches on effectively shutting off Q9. The 2W resistor R4 is used to dissipate the power generated as a result of the current through and voltage across C-E of Q9. $I_{shutoff} = 0.7V / R6$

16.7 Overvoltage protection of the PCB:

Additionally to the protection measures described in pt. 16.4 and 16.5 it is highly advised to install an additional surge protection device directly at the a- and b- terminals.
The maximum C-E breakdown voltages of the line and driver transistors are:

transistor type (line)	V_{CEO} ,$V_{(BR)DSS}$	transistor type (driver)	V_{CEO}
BSS 92,BSP92	200V	MPS-A42, KSP42	300V
MPS-A 92	300V	MPS-A43,KSP43	200V
2 SA 1209	160V	2N5551	160V
2 SA 1210	200V		

The clamping voltage of a 150V-varistor can be up to 400V at 5 Amp. clamping current. In other words, it may not be able to protect the line transistor at very high surge spikes.

16.8 DC-mask for various hook transistor arrangements

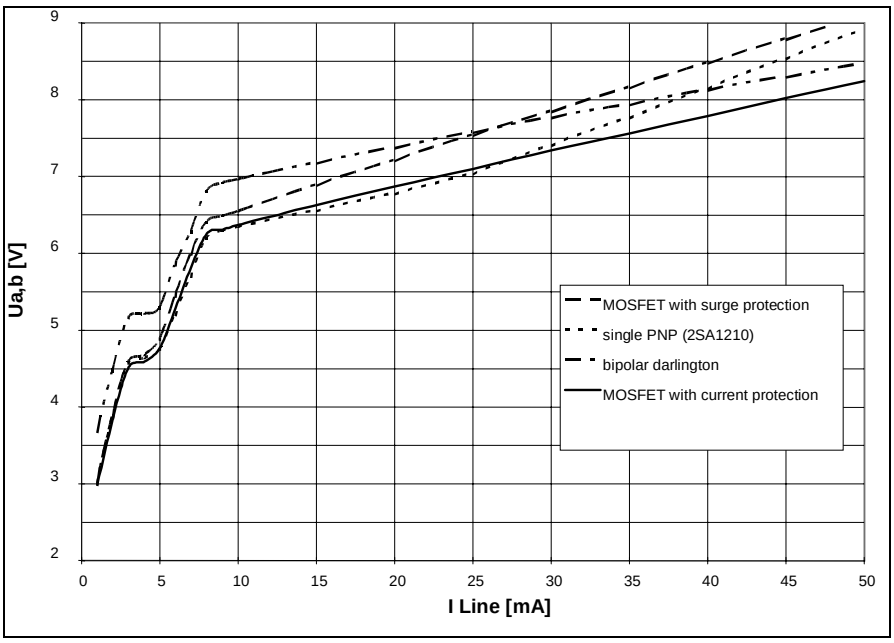


Fig. 9 shows a typical DC mask graph for the optional hook transistor arrangements: MOSFET with overcurrent pro-tection, MOSFET with surge protection, single PNP and PNP darlington .
The X-scale shows line current in mA and the Y-scale shows the voltage across the a- and b-terminals.
Check with your application's PTT require- ments to find the arrangement that fits best into the specification.

(see also: pt 15.2.1: setting for low DC mask)

Fig. 11: DC mask for various hook transistor options

17 Shunt- and Ringer Transistors

Q3 is used to shunt excess line current to V_{SS} to maintain a constant voltage on LI (#27). It is also used for DTMF line modulation and short circuits the speech part during pulse dialing *(ref. Fig.8)*.
The transistor must be capable of driving >100mA and have a typ. gain B >=100.

Q4 is used to switch the piezo ringer on and off, it can be any NPN single or darlington transistor capable of driving 100mA at 25V U_{CE}.

recommended types:

Q3	Q4
BC327-16 BCX 51-16 (SMD)	BC547 BC517 (Darlington) BCV27 (SMD- Darlington)

18 On-hook conditions

In on-hook state the circuit is supplied by a very small current to maintain retention of stored numbers and ringing melody. The hook transistor is off and the HS pin (#10) is forced to zero by R8 and R9//$Q2_{B,E}$. The IC is powered down, only a very small current flows from line to maintain V_{DD} and thus retention of stored memories and ringing melody. The DC resistance of the application in this state is >5MΩ (= the value of R1).

18.1 Quiescent current path

La -- R1 (determines on hook DC resistance) -- RB1 -- R15 -- V_{DD} (C9 // D1)
V_{SS} -- RB1 -- Lb

If the telephone is disconnected from line memories are not lost since C9 keeps charging V_{DD} for a limited period of time. The absolute time span depends on the quality (internal discharge) of C9 and the leakage resistance of D1.

19 Ringing mode

In on-hook state the circuit is supplied by a very small current to maintain the retention of stored numbers and the ringing melody
Frequency discrimination assures that the tone ringer is activated only when a valid ring signal is applied and not when pulse dialing from a parallel telephone (false “bell-tinkle”).

19.1 Ringing frequency comparator

The ring signal is checked at pin FCI (#21) for a valid ringing frequency. As soon as a signal is applied to the line the internal “ring frequency detector” will start, provided that the signal level at FCI is above the trigger threshold (≈ 2/3 V_{DD}) . If the frequency is within the specified range the melody generator will send a bitstream out of MO (#8), charging the piezo ringer via Q4 and discharging it via D5 and an internal high voltage transistor. As soon as a non-valid or missing ring signal is detected, the bitstream is stopped and the circuit returns to standby.

Ringing signal path
La -- C1 -- R2 -- RB1 -- C8//D4 (charges piezo ringer supply) -- C8//D4 (charges V_{DD})
V_{SS} -- RB1 -- Lb

another path exists from C1 -- D2 -- R3 to FCI // C2 // R4 for the ringing frequency detector input.

20 Oscillator input

A 3.58MHz ceramic resonator (recommended type MuRata CSA 3.58MHz) must be connected at OSC (#11). The parallel capacitor C10 is to trim the oscillation frequency (not required with the recommended resonator type).

The exact resonant frequency should not be measured at the OSC input directly, because the capacitive load of the Oscilloscope probe will shift the oscillation frequency.
DTMF frequencies are derived from the resonant frequency, if these frequencies (see DTMF frequency standards or data sheet) are not centered, the oscillator must be trimmed.

21 EMC & RFI issues

EMC (electromagnetic compatibility) and **RFI** (radio frequency interference) is a major concern in most PTT approvals. And due to the upcoming digital networks (GSM, CDMA, DECT) also a feature which can be “heard” by the user. Therefore it is a major headache for telephone designers, since EMC testing is generally done with finished designs and failing EMC tests may result in adding expensive components, like coils, chokes etc.
Much can be done by considering EMC from the very beginning ! The most important factors are IC technology, layout and placement of EMC blocking components:

21.1 Technology:

Due to SAMES unique CMOS technology the circuits show far less sensitivity to RFI than bipolar circuits which makes EMC a much easier task.

21.2 Layout hints:

As a common rule, V_{SS} ground planes should be as large as possible. “Bottlenecks” and long distances in the ground path should be avoided.

Additionally, long distances between LI (#27) and the Emitter of the shunt transistor (Q3) should be avoided. Therefore, Q3 should be placed near the IC pins :
collector = pin #26 =Vss,
base = pin #25 = CS,
emitter = pin #27 = LI.

21.3 EMC blocking parts:

Connections for blocking components, preferably ceramic capacitors (far less cost than coils) should be already considered in the layout design. These capacitors should be connected as close to the IC (or line/handset connector) pins as possible with a low-ohmic connection to V_{SS} . SMD caps have best performance for EMC blocking because of short leads and they can be placed directly underneath the IC at the solder junction.
If the use of SMD components is not possible, leaded ceramic capacitors can be connected at top PCB side as shown in the demo board’s layout. Refer to EC1..EC7 on both schematic and layout.
The actual number of required EMC blocking components in the customer’s design cannot be predicted, since EMC performance is influenced by many other factors, like telephone assembly, wire lengths etc.

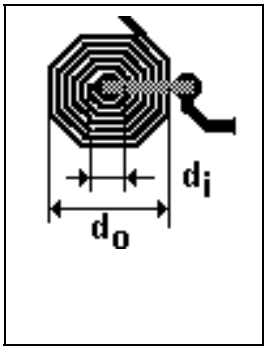
21.4 Blocking of AGND:

For SA2532K EMC designs, it is very effective to block the AGND-pin (#5) with an inductor of ≈150nH or higher. This small inductance can be installed without extra cost by a printed coil with ≈8..10mm diameter and ≥5 turns (see PCB layout).

How to calculate the inductance of a printed spiral coil:

$$L_{[nH]} \approx \frac{10.75 \bullet n^2 (d_o + d_i)}{1 + 2.72\left(\frac{d_o - d_i}{d_o + d_i}\right)}$$

where:
n = number of turns
d_o = outer diameter in cm
d_i = inner diameter in cm



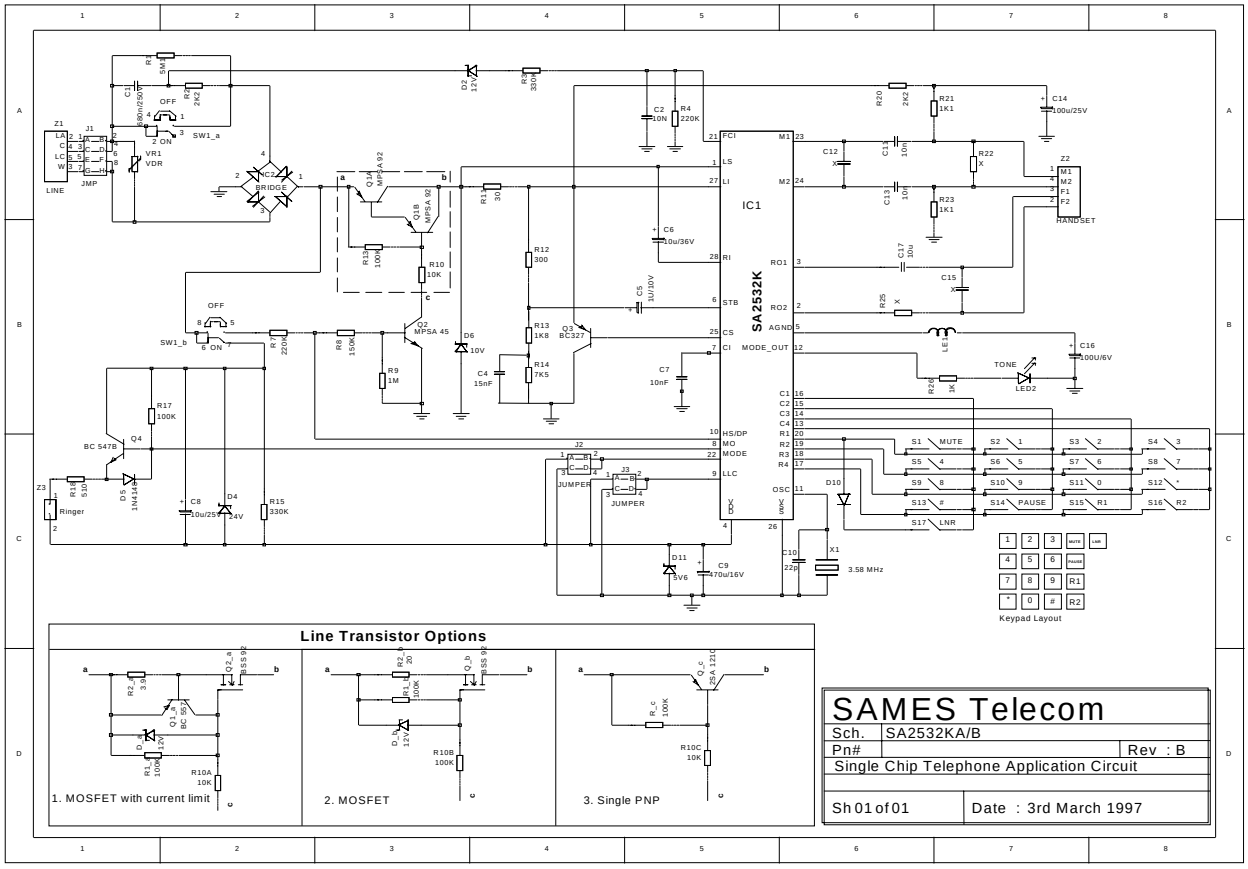
Example:
The printed coil used in the DB1500I layout has the following dimensions (see Fig.12):
d_o= 8.2 mm
d_i = 2.6 mm
n = 5.5

$$L_{[nH]} \approx \frac{10.75 \bullet 5.5^2 (0.82 + 0.26)}{1 + 2.72\left(\frac{0.82 - 0.26}{0.82 + 0.26}\right)} = \underline{\underline{146nH}}$$

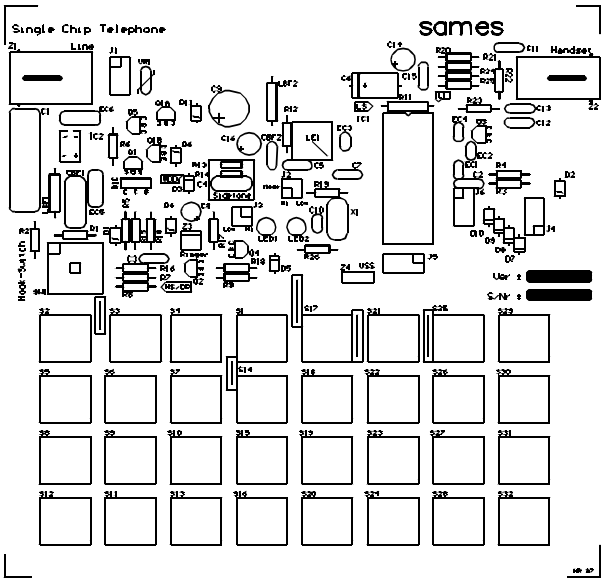
Fig. 10:printed coil on DB1500I PCB for EMC protection

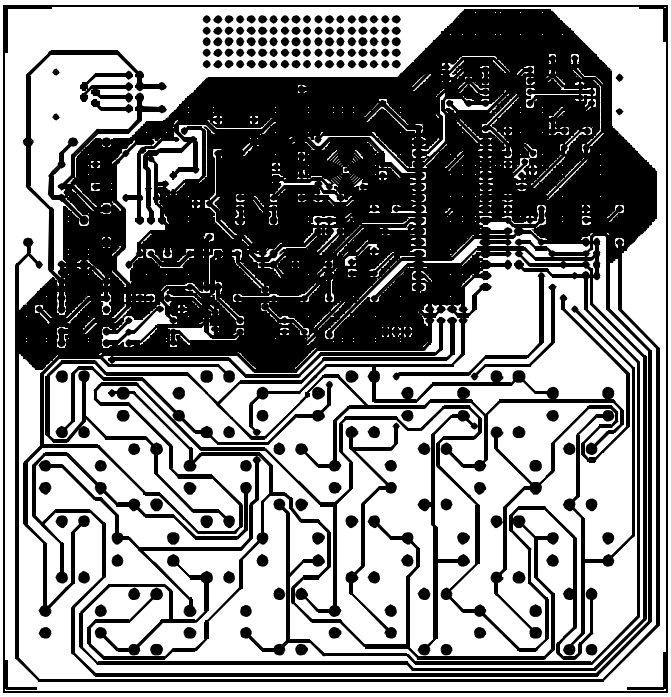
Note: Instead of a printed coil, a helical air-coil (7mm diameter, 7..9mm length, 5..7 turns) made by a piece of copper wire may also be used.

22 Board Schematic



23 Board Layout





24 Part list

Designator	Part Type	Description
C1	680n/250v	Ringer Capacitor
C2	10n	Anti aliasing filter, ring frequency detector
C3		*not fitted (hookswitch filter)*
C4		*not fitted (sidetone network)*
C5	1u	DC-AC separation, RX amplifier
C6	10u/35v	DC-AC separation, RX amplifier
C7		*not fitted*
C8	10u/30V	Filter and buffer for ringer supply
C9	470u/16v	Vdd supply capacitor
C10		Oscillator fine tuning
C11	10n	TX response shaping, DC-AC separation
C12		*TX response shaping (low pass) (not fitted)*
C13	10n	TX response shaping, DC-AC separation
C14	100u/25v	Electret handset microphone supply filter
C15	*10n*	*RX Response shaping (not fitted)*
C16	100u/25v	Analogue ground filter
C17	10u	DC-AC separation RX Output
CBF1	*.../250V*	*Metering pulses blocking filter (not fitted)*
CBF2	*..../10V*	*Metering pulses blocking filter (not fitted)*
D1	*12V*	*Gate voltage protection for MOSFET transistor (not fitted)*
D2	12V	Ringer voltage clamping, FCI input protection
D3		*not fitted*
D4	24V	Ringer voltage limitation
D5	1N4148 (or LED)	Piezo ringer discharge (LED for ring indicator)
D6	10V	Surge protection
D7-D9	*1N4148*	*not fitted*
D10	1N4148	Keyboard
D11	5v6	Vdd limitation
EC1-EC6	*1n*	*EMC blocking capacitors (not fitted)*
IC1	SA252K	Single Chip Telephone
IC2	DF06	Rectifier bridge
J1	Line	Line connector pin selection
J2	Mode	Dialling mode selector
J3	LLC	Line Loss compensation selector
J4		*not fitted*
J5, J6	(short circuited)	Simulate on-resistance of keypad
LBF1	*not fitted*	*Metering pulses blocking filter, must not be in saturation at Iline max*
LBF2	*not fitted*	*Metering pulses blocking filter*
LE1		EMC filter (printed on PCB)
LED1	*not fitted*	*n/a*
LED2		LED Tone Indicator (SA2532K)
Q1	*BSS92*	*Hook transistor for Mosfet option (not fitted)*
Q1A,B	MPSA92	Hook transistor for PNP Darlington option
Q1C	*2SA1210*	*Hook transistor for single PNP option (not fitted)*
Q2	MPSA45	Driver transistor for Q1
Q3	BC327	Line current shunt transistor
Q4	BC547B	Ringer driver transistor
Q5	*BC557*	*Current limiter transistor (not fitted)*
R1	5.1M	Leakage current limitation
R2	2K2	Ringing impedance
R3	330k	FCI input protection and voltage divider
R4	220k	Voltage divider

Designator	Part Type	Description
R5	*not fitted*	
R6	*not fitted*	*Line Current sensing resistor for Q5*
R7	220k	Pull-up resistor, HS input current limitation
R8	150k	Base resistor for Q2
R9	1M	Base shunt resistor for Q2
R10	10k	Base/gate series resistor for Q1
R11	30	Sensing resistor for DC-mask and Line current
R12	300	Side tone balance bridge resistor
R13	2k7	Side tine network
R14	3k3	Side tone network
R15	330k	Leakage current supply during On-Hook
R16	*not fitted*	*Ringing impedance*
R17	100k	Pull-up resistor for Q4
R18	510R	Low pass filter for ringer capacitance
R19	*not fitted*	*Series resistor for LED1*
R20	2K2	Filter for electret hanset microphone supply
R21, R23	1K1	Supply for electret microphone
R22	*not fitted*	*TX Frequency response shaping*
R24	*short circuited*	*RX Frequency response shaping*
R25	*short circuited*	*RX Frequency response shaping*
R26	1K	Series resistor for LED2
S1-S17	SPST	Keypad Switches
SW1	SW-HOOK	Telephone Hook switch
VR1	150V	Varistor, surge protection
X1	3.58MHz	Ceramic resonator
Z1	LINE	AMP modular connector
Z2	Handset	AMP modular connector
Z3	Ringer	Piezo ringer connector

25 Applications

Applications based on the SA2531/2 are continuously updated. Ask your local distributor or SAMES sales office for available papers.

26 Liability and Copyright Statement

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