AN10E40
Field Programmable Analog Array

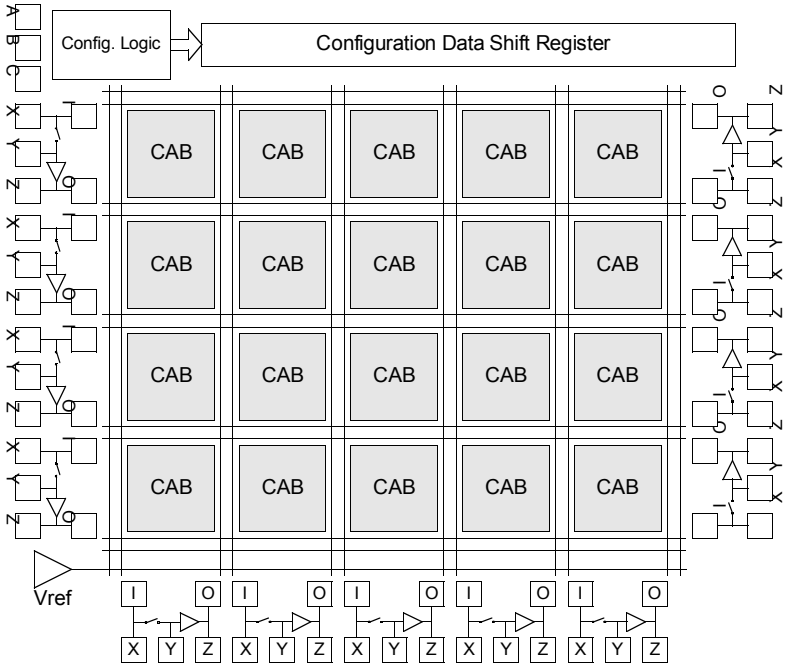
The AN10E40 brings to analog what FPGAs brought to digital; extremely rapid production and prototype circuit realization with field re-programmability. The AN10E40 consists of a 4 x 5 matrix of fully configurable switched capacitor cells, enmeshed in a fabric of programmable interconnect resources. These programmable features are directed by an on-chip SRAM configuration memory. The SRAM configuration memory is initialized on power up via an off chip serial PROM or through the AN10E40's standard microprocessor peripheral interface.

A configuration memory image is easily constructed using the companion AnadigmDesigner® software which includes an extensive library of adjustable, proven, pre-built functions. The configurable analog blocks are often consumed one at a time, though some of the more complex library functions may consume two or more blocks. Specialized IO cells surround the core to bring your analog signals in and out of the array.

The AN10E40 coupled with the intuitive AnadigmDesigner® software gives both digital and analog designers a competitive advantage in designing analog circuits that can't really be compared to any other design system in existence. Quickly constructed, accurate, drift free, temperature compensated and *programmable* analog circuits are now yours. Imagine the power of programmable with the versatility of analog.

Benefits

- Extremely Rapid Analog Design – Minutes not weeks to re-spin a new design idea
- In Circuit Programmable – Behavior can be changed as fast as 125 microseconds
- Re-Configurable Using Conventional Logic, Serial PROMs or Microcontrollers
- Extremely Stable over Voltage and Temperature
- No Component Aging
- Reliable and Repeatable Performance
- Flexible Internal Clock and Routing Resources
- No More Trimming Components
- No More Tuning Components



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Features of AN10E40

- 20 Programmable Analog Cells
- 13 Analog IO Cells
- 2 Spare Op-Amps
- 8 Bit Programmable Internal Vref Source
- 4 Programmable Internal Clock Sources
- Easy Power-On-Reset Self Boot Using Serial PROM
- Microprocessor Boot Option
- Intuitive Design Software
- Drift Free Designs
- Rapidly Configurable

Available IPmodule Functions

- Gain Stages
- Summing Amplifiers
- Sample and Hold
- Track and Hold
- High, Low and Band Pass/Stop Filters
- High Q, Low Q Filters
- Cosine Filters
- Full and Half Non/Inverting Rectifiers
- Non/Inverting Comparators
- 1 and 2 Input Comparators
- DC Reference Voltage Sources
- Limiters
- Schmitt Triggers
- Non/Inverting Integrators
- Differentiators
- New IP Modules Continuously Available

How It Works

On power up, the AN10E40's reset circuitry initializes the configuration engine. The configuration engine takes over and first examines the state of the Mode port. The pin settings of the Mode port determine which of the boot methods should be exercised. One popular option is to boot from an off chip Serial PROM. The configuration engine takes care of taking data out of the Serial PROM and loading it into on-chip configuration SRAM. The whole boot process takes just a few milliseconds. Once the configuration SRAM has been loaded, the analog circuitry is automatically enabled and the configuration engine idled. The chip now performs the analog functions according to the configuration bit stream just loaded.

Creating a configuration bit stream is no more complicated than using the device itself. The AnadigmDesigner® design tool provides the user an intuitive drag and drop GUI in which you simply select several of the IPmodule functions from the extensive library, drop them onto a graphical representation of the chip, fill in some parametric information about the IPmodule, wire up the internal and I/O connections, and hit a button to generate the bit stream (or download it directly to the device on your bench).

The device internals are more complicated than the easy to use device may lead you to believe. The AN10E40 array is based on programmable switched capacitor op-amp cells with very flexible internal and external connection and clocking resources. The AnadigmDesigner® and the associated IPmodule library shields the user from these complexities.

Switched capacitor circuits are remarkably stable over voltage, temperature and device aging. Using the AN10E40 for your analog circuit realization allows you to rest assured knowing that once a circuit has been designed, it will continue perform as expected. Say goodbye to trim pots.

Another advantage of this technology is the tremendous decrease in design time. Along with the elimination of trim pots, you'll also be able to clear your bench of all the normal discrete R and C components. "Prototyping" is now a drag and drop computer exercise. A simple push of a button and your design is downloaded into the AN10E40 nearly instantaneously.

The kicker to all of this is that it is infinitely re-programmable. If a single set of analog functions is not sufficient for your system, then you can load new configuration files into the AN10E40 with only a very small interruption to the analog signal stream. Consider how filter parameters can be changed to adapt to varying input signal conditions. Consider how a single physical circuit can be used in all of your different system designs. Consider all the advantages that programmable analog will bring to your designs.

AN10E40 Architecture

The AN10E40 is comprised of a 4x5 array of Configurable Analog Blocks (CABs), enmeshed in clocking, switching, local and global routing resources. Nearly every element of the AN10E40 is programmable giving the user tremendous flexibility in the sorts of processing circuits that can be realized.

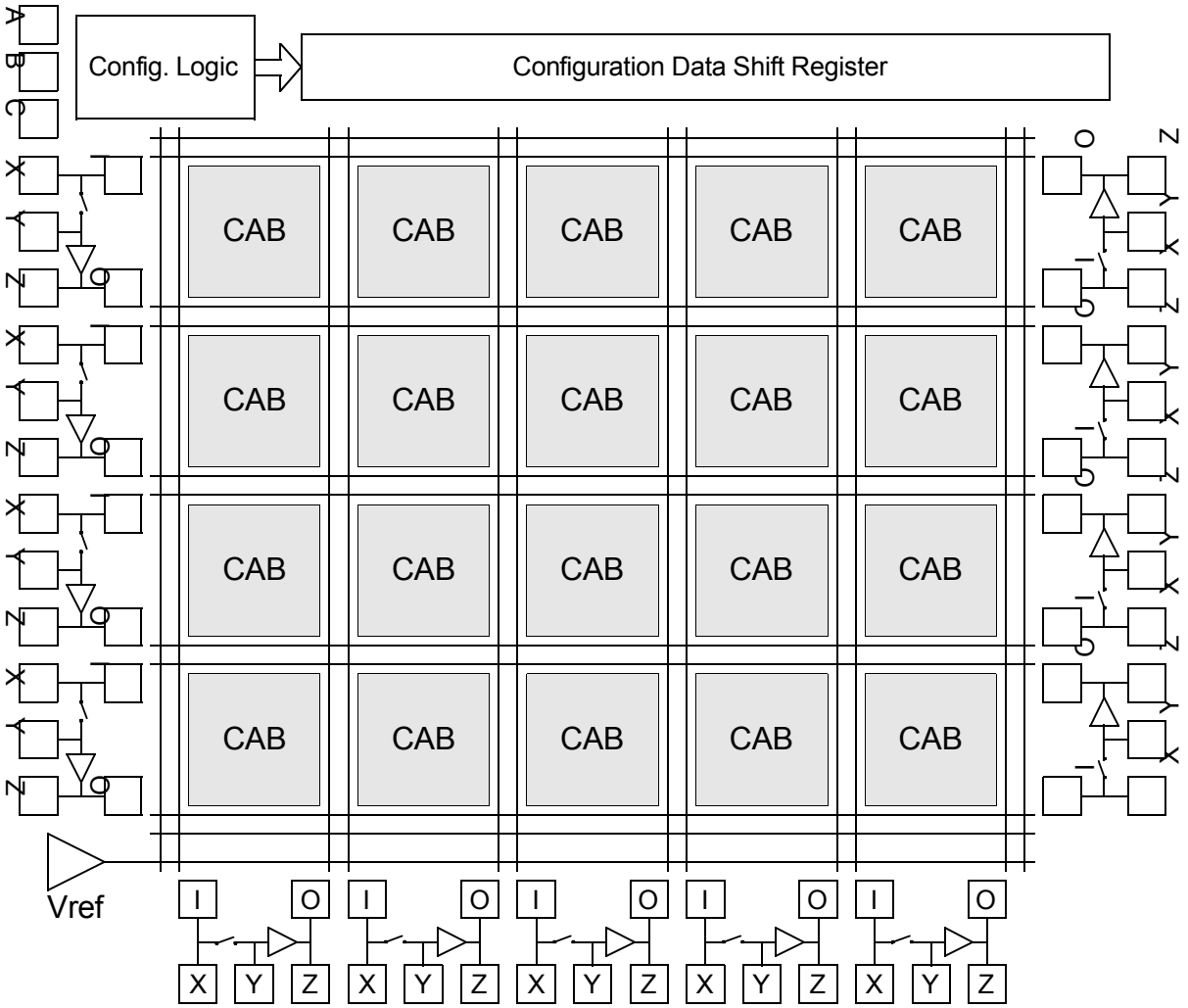


Figure 1. Block Level View of the AN10E40 array

The Configuration Logic and Shift Register work together whenever chip configuration is in process. The array of CABs is surrounded on three sides by programmable analog input/output cells, 13 in all, with two spare uncommitted op-amps. The lower region of the chip also contains a programmable reference voltage generator.

The Configurable Analog Block

The basic building block of the AN10E40 is the Configurable Analog Block. Each CAB is an op-amp surrounded by capacitor banks, local routing resources, local switching and clocking resources, and global connection points. This collection of hardware enables the CAB to perform many of the functions that could be achieved using an op-amp and conventional passive components. All analog processing is accomplished with this switched capacitor circuit.

A Quick Review of Switched Capacitor Circuits

There are many excellent texts available which dive deeply into the details of sampled systems and MOS switch capacitor circuit theory. The math gets very complex and may have kept you away from switched capacitor circuits in the past. The good news is that the AnadigmDesigner® software for Anadigm® devices shields you from all the complexities of using switched capacitor designs. Still though, it can be useful to review briefly how switched capacitor circuits operate to eliminate the fear of the unknown.

Consider the following two circuits.

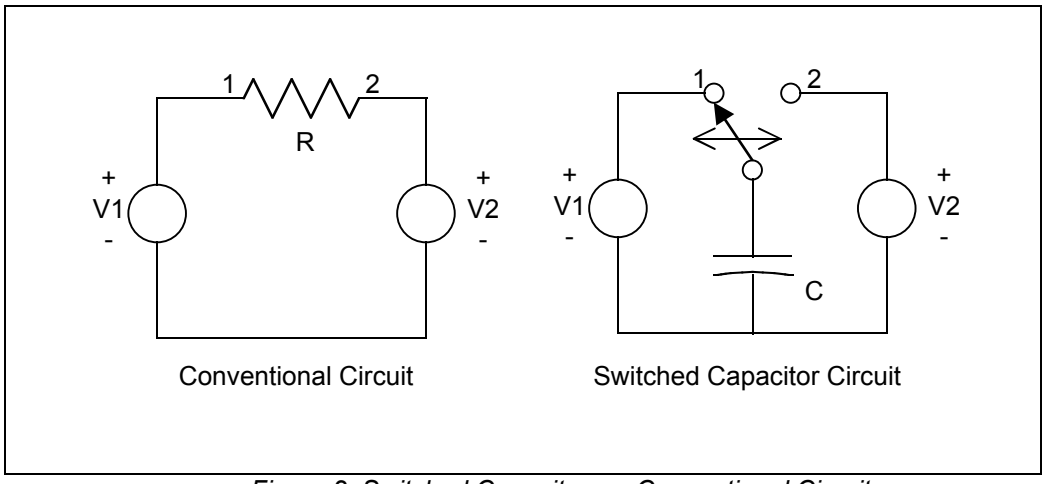


Figure 2. Switched Capacitor vs. Conventional Circuit

In the Figure 2, two circuits are shown that can both do the same job. The conventional circuit moves current around the loop through the resistor. The amount of current of course is a function of the difference between V1 and V2 and the value of R.

The switched capacitor version of the circuit does the same job, but in a different way. With the switch in position 1, charge moves from the V1 source to the capacitor C, when the switch is moved over to position 2, charge is then moved from C to V2. As the switch is thrown back and forth, recognize that charge is moving over time, in other words - current. The faster you throw the switch (and/or the bigger the capacitor is) the more current flows. Unlike the conventional circuit, simply reprogramming the switching clock rate or the size of the capacitor allows you to adjust the “resistance” between nodes 1 and 2.

Of course, since this is a sampled system you have to keep in mind the frequency of the signal that is being processed by the circuit and the frequency at which it is being sampled (or switched). For signals with frequency content constrained significantly below the sampling frequency the switched capacitor circuit works just like the conventional circuit. In all cases, the sampling rate should be at least twice as high as the highest frequency of the signal being processed.

CAB Details

The SRAM block which controls routing connections and CAB behavior is loaded during configuration time. Configuration typically occurs at power up as an automatic process but can of course be re-initiated at any time. The ability to re-configure the part at any time gives the user incredible flexibility in system design.

Programmable capacitor banks and local switching in both the input paths to the op-amp and a programmable capacitor bank in the op-amp's feedback path provide all the resources required to realize a very large number of analog processing circuits.

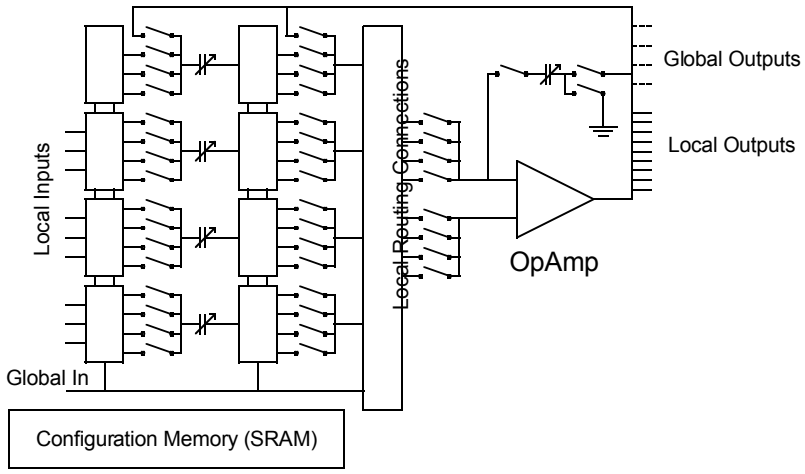


Figure 3. Block Level View of the basic CAB

Connection between other CAB's on the device and to the outside world are accomplished using the Local Inputs, Local Output, and Global routing resources.

Routing Resources

The most expedient way to gain understanding of the routing resources available on the AN10E40 is to use the associated AnadigmDesigner® design software. The routing resources and your connections to them are represented in an intuitively obvious fashion.

Local routing resources are only shown (as fly lines or rubber band lines) in the design software screen once they are used. A CAB output may be connected to an input in any of its 8 adjacent neighbors, and additionally to the CAB in the same row and to the right two locations.

Global routing resources allow you to move signals to disparate locations on the die. There are a total of 10 horizontal global routes and 12 vertical global routes within the array. A CAB's output can be connected to either of the two adjacent right or two adjacent down global routes. A CAB's input can be driven by one of the two adjacent right or adjacent down global routes (which one of these two routes alternates with location in the array).

Connections to the chip's programmable reference voltage generator are only available using Global routing resources.

Clock Generation

Recall from the discussion on switched capacitor basics that the behavior of our simple circuit was influenced by both the value of the capacitor as well as the frequency of the clock. So it is with IPmodules placed into the CABs of the AN10E40 array. IPmodule input clocks are all derived from the master CLOCK input pin. The maximum rated frequency of this input is currently specified to be 20 MHz. The master clock is split into 4 pairs of non-overlapping clocks and bussed to each of the CABs. CLOCK[3:0] are derived from the dividing the master CLOCK input down by a factor of 1 or from 2 to 62 (in increments of two). The maximum allowable clock frequency into an IPmodule is

specified to be 1 MHz. You are free to drive CLOCK into the array at up to 20 MHz, then program and use CLOCK[3:0] individually as your circuits might require.

The AN10E40 is designed such that all IPmodules along an analog signal path should use the same clock. While it is possible to mix clocks along a signal path, it should not be done without full understanding of sampled data systems, the effects of oversampling, undersampling and aliasing and careful consideration of possible unintended consequences. The edges of divided clocks are synchronized only with the master clock edges, and therefor the phase relationship of divided clocks is not guaranteed. For this reason, users are cautioned not to utilize two equal frequency divided clocks with the exception of clocks that have a divisor of one are therefor equal to the master clock.

Please note, the performance estimates for a placed IPmodule are based upon the known clock assignment and divider ratios at the time of IPmodule placement. Any change in the top level chip clock settings may of course affect your circuit behavior.

This section described the CLOCK input pin, not to be confused with the configuration clock pin CFG_CLK, discussed below in the section Configuration Clock.

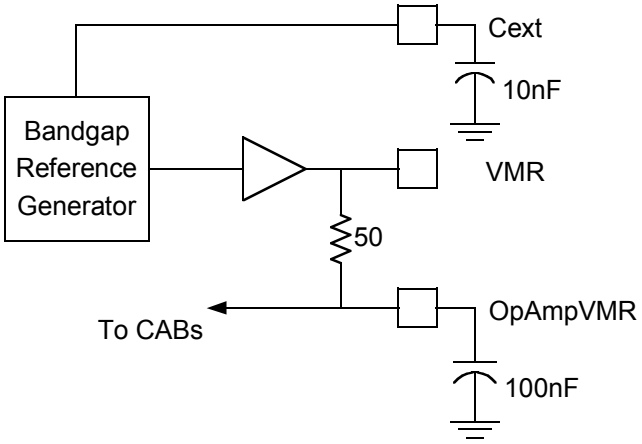
Voltage Reference

The AN10E40 provides a convenient programmable on-chip voltage reference. When your circuit requires a comparator function against a known value, this voltage reference is easily programmed and enabled.

The value programmed into the Voltage Reference is always specified relative to signal ground. On the AN10E40, signal ground is at VMR (see Voltage Mid-Rail Generator below).

Voltage Mid-Rail Generator

All analog signals within the array are referenced to Voltage Mid-Rail (VMR), typically 2.5 V with respect to AVSS. The VMR signal is generated on chip, filtered with an external capacitor then routed back into the array for use by the CABs.



The recommended connections are:

- 10 nF between CEXT and a quiet ground node
- VMR unloaded
- 100 nF between OPAMPVMR and a quiet ground node

Figure 4. Filtering OpAmpVMR

The RC network provides a simple but effective low pass filter for the on-chip OpAmpVMR signal. It is not recommended that OpAmpVMR be loaded externally with anything other than a low leakage current 100 nF capacitor.

VMR is provided as a convenience outlet for the VMR signal. The system is designed only to drive the RC filter network. If your system requires use of VMR, it is recommended that you first buffer it with a high impedance amplifier. Conversely, should your system design establish a requirement for generating signal ground (VMR)

externally, the design software allows you to disable the on-chip VMR generator and instead drive the VMR pin from off chip.

The Bandgap Reference Generator provides a nominal 2.5 V reference signal. Cext is a filtering cap used to quiet any possible switching noise from getting coupled into this important reference voltage.

Analog Input Output Cell

The AN10E40 has a flexible analog IO cell that allows you to connect directly into the core's internal circuitry, buffer input and output signals to/from the core, and using very few external components, construct a Sallen-Key filter.

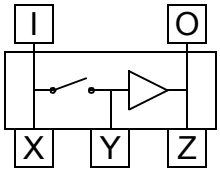


Figure 5. Analog Input Output Cell

The "I" and "O" pad designations are Input and Output; these names are relative to the IO Cell itself.

The most common configuration for use as an input is to leave the switch open and power up the buffer. Drive Y with an external signal and connect O to an IPmodule's input. X and Z should be left unloaded.

The most common configuration for use as an output is to close the switch and power up the buffer. Drive I with an IPmodule's output and connect an external load to Z. X and Y should be left unloaded.

Under certain circumstances it may be advantageous to leave the switch open and the buffer powered down. For example, a single Input Output Cell can be used to simultaneously bring a pair of signals in and out of the array. I to X is an output path from the array, and Z to O is an input path into the array. In doing so however, the external signal driving Z will be loaded with the input impedance of the IPmodule connected to. This impedance is a function of the IPmodule's clock speed and input capacitor size. Likewise, the user must stay alert to the external loading of X which can affect the driving IPmodule's performance.

Another situation which might warrant such direct connections into the array is when your design's input stage will not tolerate the non-zero offset voltage associated with an input buffer.

Sallen Key Filtering

The flexibility of the IO cell is best appreciated when considering the construction of Sallen-Key filters. Since the array is based on switched capacitor circuits, your output signal may have unwanted switching noise present. Also, since this is a sampled data system, some care should be taken to band limit input signals to avoid aliasing artifacts. Sallen-Key filters are useful for filtering such frequency components out. The AN10E40 IO cells are uniquely designed to facilitate easy construction of such filters.

The detailed derivation of the math and complete explanation of the theory of operation of these filters would be better served by another dedicated document, however we are pleased to present the general circuit diagrams for such filters and will instead refer you to Application Note 010. Also, there are quite a number of excellent analog filter design tools currently on the market. The major advantage in using such a software package is that most of them will implement the filter using standard value components, whereas the traditional cook book equation approach often results in unrealistic component values. One good example of a filter design tool is Filter Wiz LE. This effective and highly affordable PC based design tool is available on line from www.schematica.com.

For all such filters, as for all external ceramic capacitors in the signal path, only NPO or COG ceramic materials are recommended (for better voltage coefficient). X7R or similar material can add noticeable distortion to the signal.

2nd Order Sallen-Key Filter for Output Smoothing

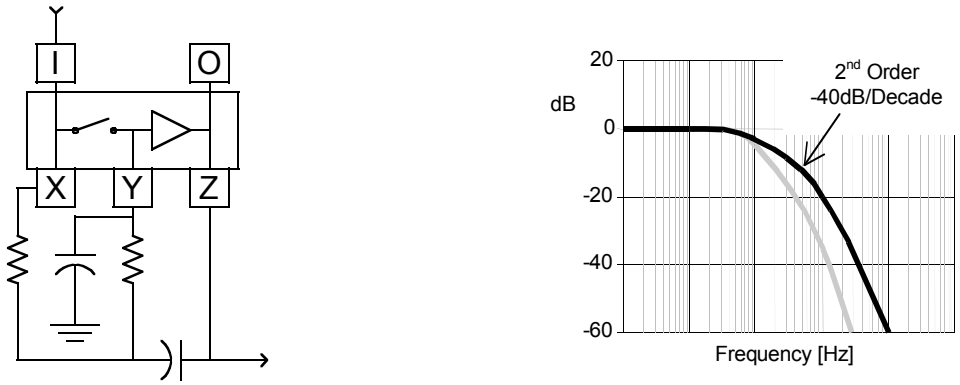


Figure 6. A 2nd Order Sallen-Key Filter for Output Smoothing

4th Order Sallen-Key Filter for Output Smoothing

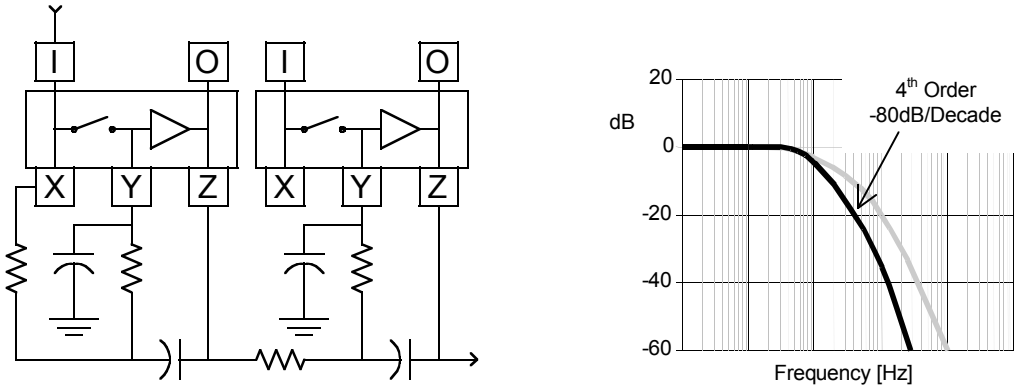


Figure 7. A 4tn Order Sallen-Key Filter for Output Smoothing

Here, the first stage of filtering is handled by an otherwise unused IO cell. It can instead be one of the two spare op-amps the AN10E40 provides. (See the Pin Out Description section for a description of pins 24, 25, 74 and 75.)

2nd Order Sallen-Key Filter for Input Anti-Aliasing

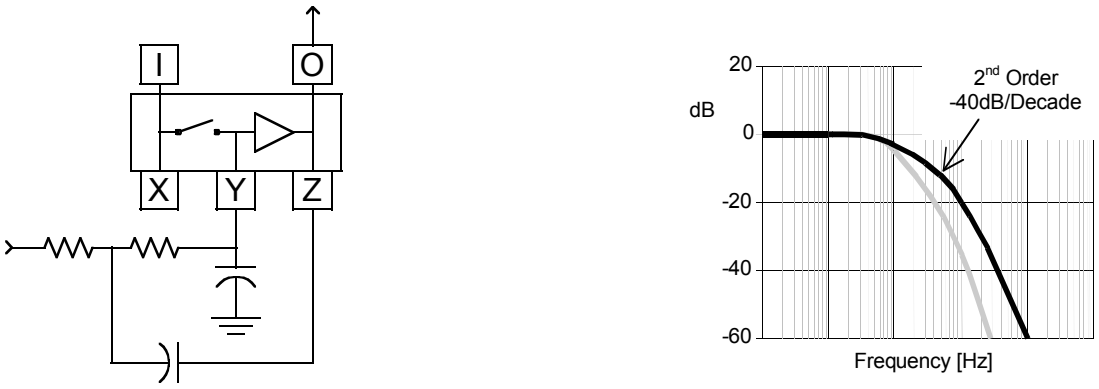


Figure 8. A 2nd Order Sallen-Key Filter for Input Anti-Aliasing

4th Order Sallen-Key Filter for Input Anti-Aliasing

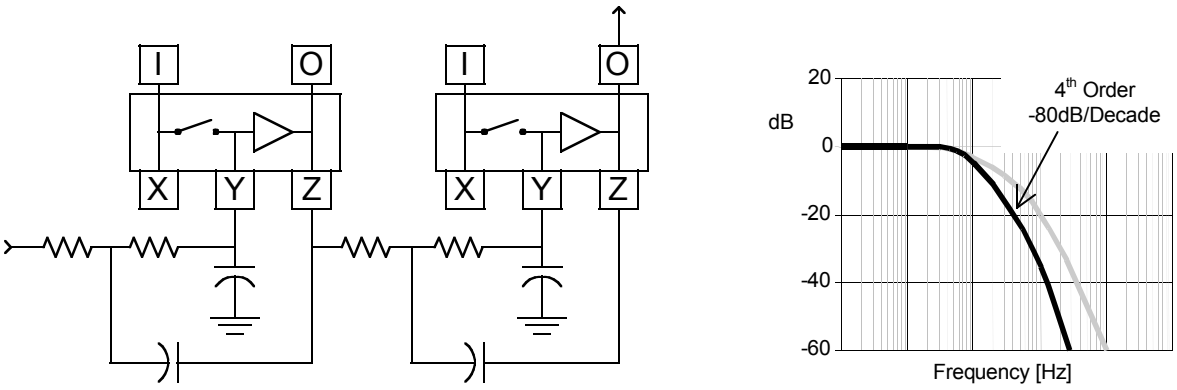


Figure 9. A 4th Order Sallen-Key Filter for Input Anti-Aliasing

Configuration Engine

The AN10E40 provides two modes of operation for loading the configuration SRAM. The simplest is Mode 1, Boot From Serial ROM. This is the most common method of booting conventional SRAM based FPGA's so consequently the cost of compatible low pin count serial PROMs has been driven way down. Some designs may however want to take advantage of the AN10E40's on the fly reprogrammability. In this case the Micro Mode (Mode 0) may be the appropriate configuration interface.

MODE Pins		
[2]	[1]	Description
x	0	**Mode 0** – Micro Mode, a conventional byte wide microprocessor interface
x	1	**Mode 1** – Boot from Serial PROM (a.k.a. Boot from ROM or BFR Mode)
0	x	AN10E40 generates its own configuration clocks (using an internal oscillator). CFG_CLK is an output.
1	x	Use an external clock for configuration. CFG_CLK is the input.

Figure 10. Mode Pin Settings for Configuration Options

The configuration SRAM for the AN10E40 contains 6864 bits. Configuration files will be slightly larger to facilitate byte alignment of data as well as address and checksum information.

The pins involved with configuration of the device are given in the following table. The F[4:0] pins change behavior based on the setting of the MODE[2:1] pins. The signal naming convention holds that active low signals are named with a "b" suffix.

Pins Common to Configuration Modes		
Pin Name	Description	
MODE[2:1]	I	Used to establish the configuration mode.
CFG_CLK	I/O	If MODE[2] is high, then configuration clock input, otherwise configuration clock output.
Pins used in Micro Mode (Mode 0)		
POR	I	Complete chip reset sequence begins on rising edge of POR. (Usually tied low.)
RESETb	I	Reset sequence begins on falling edge. Chip held in reset state as long as asserted low. Configuration re-starts on release of RESETb.
F[0] CSb	I	When low, selects the AN10E40 for a data transfer transaction
F[1] RDb	I	Assert low for a Read transaction.
F[2] WRb	I	Assert low for a Write transaction.
F[3] RS	I	Register Select. RS=0 to select Function register. RS=1 to select Data/Status register.
F[4] BUSY	O	Asserted high when the device is not ready to accept data, i.e. while device is resetting, or a data shift register to configuration SRAM transfer is taking place.
DATA[7:0]	I/O	Byte wide bi-directional data port
Pins used in BFR Mode (Mode 1)		
POR	I	Complete chip reset sequence begins on rising edge of POR. Once complete, the configuration sequence begins. (Usually tied low.)
RESETb	I	Reset sequence begins on falling edge. Chip held in reset state as long as asserted low. Configuration re-starts on release of RESETb.
F[0] BFRb	I	On falling edge of BFRb, configuration sequence occurs.
F[1] ERRb	O	Asserts low if a an error is detected in the configuration data stream. (Open Drain)
F[2] MEMCEb	O	Asserts low to select the external memory device.
F[3] PWRUP	I	Tie to VDD.
F[4] END	O	Asserts high to signify configuration has completed.
DCLK	O	Data clock to serial PROM.
DATA[0]	I	Bit wide data input.

Figure 11. Configuration Pin Functions

Mode 0 – Micro Mode (Parallel Loading)

In Micro Mode, the configuration engine of the AN10E40 presents itself as a byte wide peripheral interface, compatible with nearly any host microprocessor. In this mode, configuration data can be loaded into the device 8 times faster than the serial method presented later in Mode 1.

The Mode 0 interface is a conventional asynchronous parallel peripheral interface. Access begins when CSb is asserted, the state of the RS (Register Select), WRb (Write bar) and RDb (Read bar) control pins determine what sort of transaction will be executed. The DATA bus is used to write in commands, read out status, write and read configuration data. The RS pin selects between the only two configuration registers. When RS=0 the transaction will be with the Function register. Configuration commands are written to the Function register. When RS=1 the transaction is directed at the Data/Status register. The Data/Status register returns the current status of the configuration engine or accepts configuration write data or sources configuration read data. A more detailed description of these registers is given in Figures 14 and 15. By popular convention, RS is typically connected to the least significant bit of the processor's address bus to map the Function register to an even address and the Data/Status register to an odd address.

Figure 12 shows only those signals explicitly associated with Micro Mode configuration. Other signals including: POR, OPAM_DISABLE, CEXT, OPAMP_VMR, powers, grounds and the switched capacitor CLOCK signal must also be connected for proper operation. Please reference the Pin Out Description section for complete connection details.

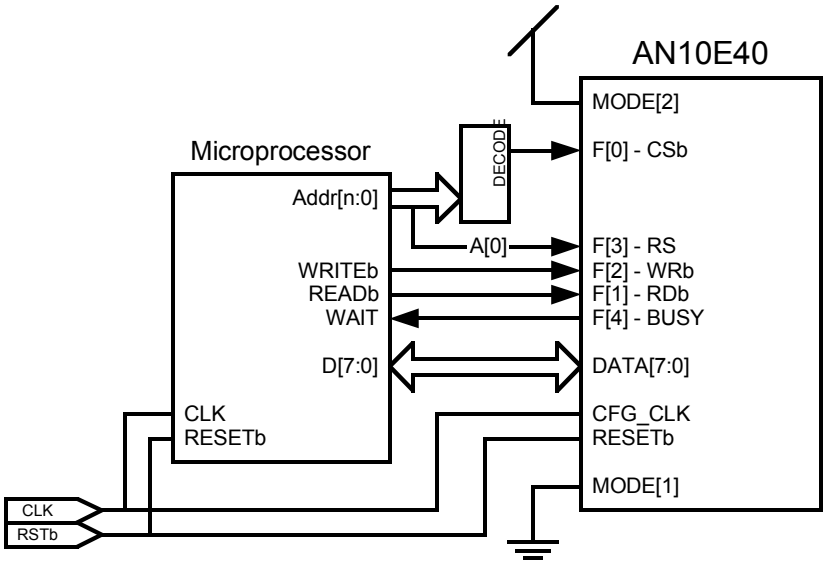
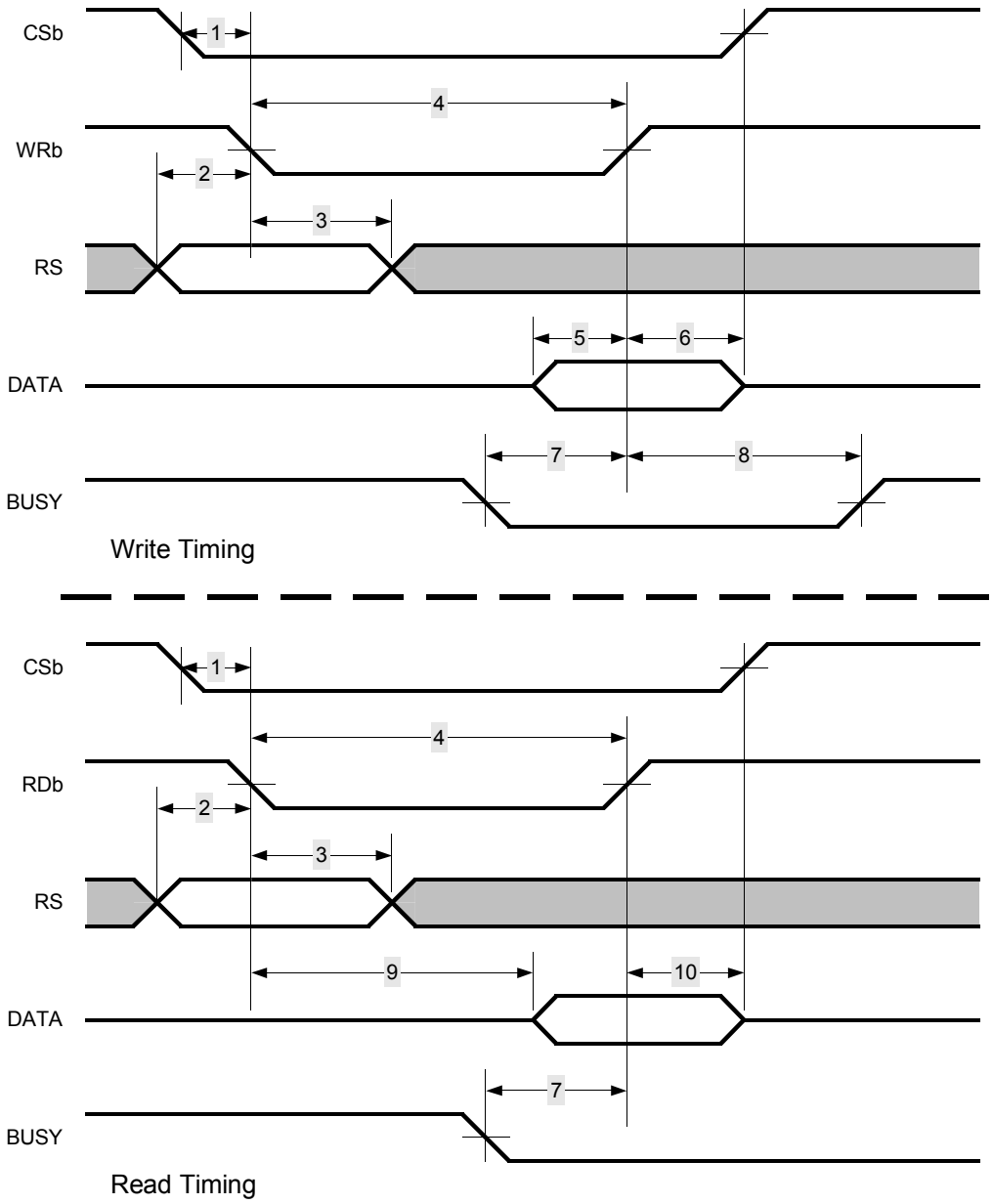


Figure 12. A conventional microprocessor interface for configuring AN10E40.

The clock for the configuration logic (CFG_CLK) must be driven in order for proper operation. The clock may be driven by a fixed clock source (50% duty cycle, not to exceed 20 MHz) or from an I/O line sourced by the host microprocessor. If using such a bit-bang approach to clock generation, the host software is required to toggle the CFG_CLK line whenever the configuration interface is being addressed, otherwise the line may be held in a steady state.

Note that when the BUSY signal is asserted, it is necessary to continue clocking CFG_CLK in order to allow the configuration engine to complete the current operation. When the BUSY signal de-asserts, CFG_CLK can be halted.

When connecting multiple AN10E40s to a single host processor, the DATA[7:0], CFG_CLK, RS, WRb, RDb pins of every FPAA device can be driven in parallel (provided fan-out specifications are not violated). Only a unique CSb line is required to address each AN10E40 in the system. FPAA devices not selected via CSb do not interfere with other transactions on the bus. All lines to the FPAA can be safely tri-stated when not in use. The timing requirements for the Micro Mode interface signals are given in Figure 13 below.



#	Characteristic	Min	Max	Unit	Notes
1	CSb Setup before RDb or WRb Falling Edge	10		ns	
2	RS Setup before RDb or WRb Falling Edge	10		ns	
3	RS Hold after RDb or WRb Falling Edge	10		ns	
4	Read or Write Pulse Width	50		ns	
5	DATA[7:0] Setup to Rising Edge of WRb	20		ns	
6	DATA[7:0] Hold after Rising Edge of WRb	10		ns	
7	BUSY Inactive before end of Read or Write	50		ns	
8	BUSY Active after Write	0	20	ns	
9	DATA[7:0] Access Time	20	40	ns	
10	DATA[7:0] Hold after Rising Edge of RDb	0	10	ns	

Figure 13. Micro Mode Write and Read Timing

Micro Mode Maximum Data Transfer Rate

The maximum Micro Mode data transfer rate is governed by the Read and Write timing diagrams shown above. The host processor must only write data when BUSY is inactive. BUSY is only asserted when data cannot be accepted at the maximum rate. The host processor can either monitor the device's BUSY output, or read the Status Register. If processor R/W cycles are faster than the timing shown, then external circuitry must be used to insert wait states.

Function Register (RS=0) and Data/Status Register (RS=1)

DATA [7:4]	DATA [3:0]	**Function Register - Behavior**
XXXX	0000	**Normal Operation** – No function performed.
XXXX	0001	**Reset Device** – Entire device configuration memory is reset. BUSY is asserted until the reset sequence is complete.
XXXX	0010	**Load Configuration** – After writing this command, a complete configuration image should be presented to the Data/Status register in 8 bit segments, starting with the configuration header block. At any time during the loading process, a read from the Data/Status register will return status. As complete rows including Error Check Bytes (ECB) are loaded, BUSY is temporarily asserted while row data is transferred from the internal data shift register to the currently addressed SRAM memory row. Once this write operation is complete, BUSY is deasserted and additional data can be written. Each time BUSY is deasserted, the Data/Status register should be checked for incorrect ID or row configuration data errors. Once an error is detected, NO further write accesses to the data shift register will be accepted until the device is reset, or another Load Configuration command is issued.
XXXX	0011	(Factory Reserved)
XXXX	0100	(Factory Reserved)
XXXX	0101	(Factory Reserved)
XXXX	0110	**Read Device ID** – 4 subsequent reads form the Data/Status register will return the device ID. The most significant ID byte is read first. The value of the device ID is 13 85 02 B7.
-	0111	(Factory Reserved)
-	1XXX	(Factory Reserved)
1XXX	XXXX	(Factory Reserved)
X1XX	XXXX	**Internal Oscillator Disable** – Normally always enabled. If internal configuration clock is selected, oscillator can not be disabled. Writing a 0 re-enables the oscillator.
XX1X	XXXX	(Factory Reserved)
XXX1	XXXX	**Analog Enable** – Powers up Analog IO Cells and CAB Op-Amps.

Figure 14. Micro Mode Function Register Behavior (RS=0)

DATA [7:0]	**Data/Status Register - Contents** (Data[7:3] are factory reserved. Their function may change without notice.)
XXXXXXX1	Incorrect Device ID detected in configuration data stream.
XXXXXX1X	Row configuration data error (ECB mismatch).
XXXXX1XX	Busy signal asserted. Allows software handshaking if hardware wait states are not to be used.
XXXX1XXX	Asserted while last internal configuration SRAM row is being written.
XXX1XXXX	Test_Count_0
XX1XXXXX	End_Test
X1XXXXXX	Last_Byte, asserted when last configuration byte is being written.
1XXXXXXX	ID_Full, asserted when the ID has been written to the device.

Figure 15. Micro Mode Data/Status Register (RS=1)

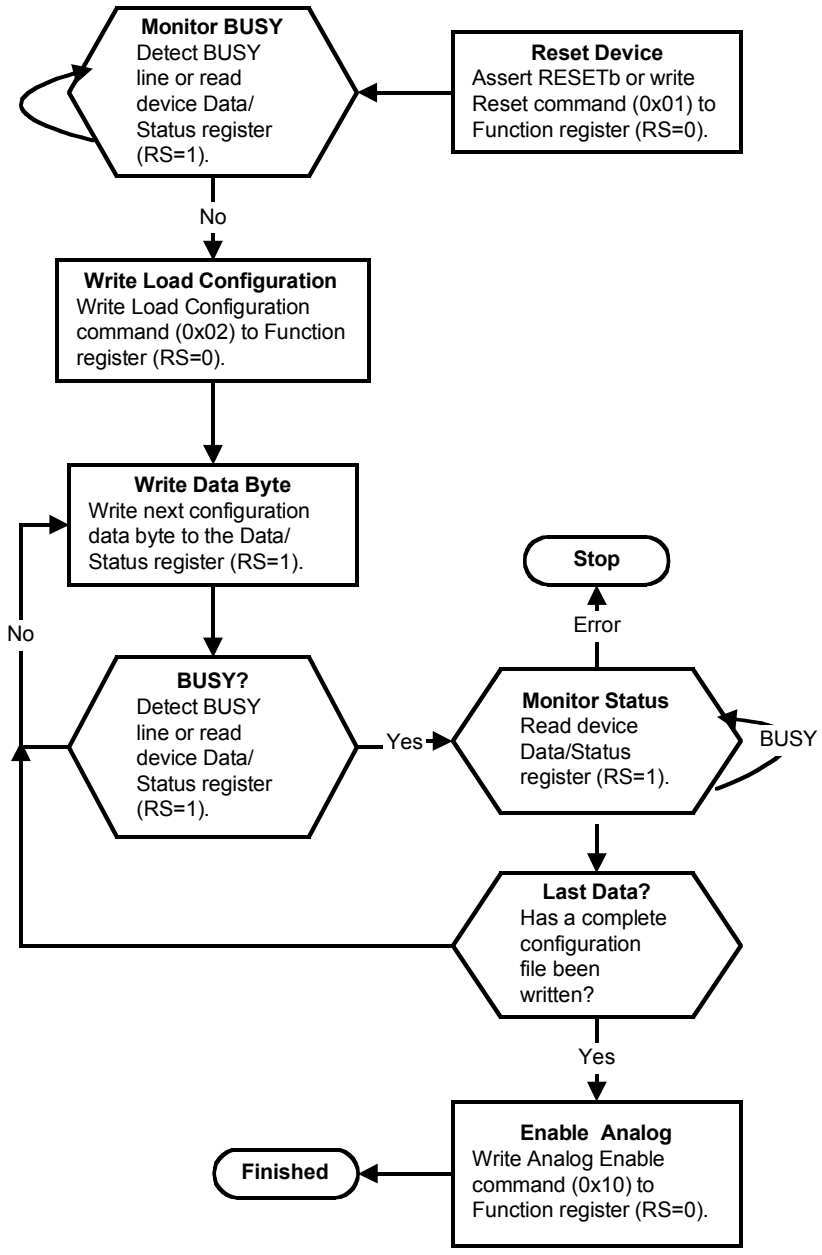
Sending the Reset Device Command

It is not always necessary to send the soft Reset Device command before sending other commands to the AN10E40. In general, it is only required the first time a host processor accesses the device to ensure a known starting condition.

Micro Mode - Configuration Sequence

Using a microprocessor to configure the FPAA enables a new type of analog system to be designed. Analog signal processing systems with multiple functions or that can adapt to changing conditions are now possible. The host processor determines which of the pre-compiled FPAA configurations are appropriate and loads that configuration image into the AN10E040.

An typical flow chart for the complete configuration process is given below.



A Mode 0 (Micro Mode) configuration sequence typically begins with assertion of device reset. This can be accomplished by either asserting RESETb or by writing the Reset Device command into the function register.

After the reset sequence completes, you have the option to specifically address a single configuration row at a time, but a more typical scenario would be to instead write the Load Configuration command into the Function register.

At this point, the device is expecting that a complete configuration image will be written to the Data/Status register (RS=1). Simplistic software might check for device busy after every byte write. Device busy will assert once a long internal shift register has been filled, and the internal configuration engine is moving the contents of the register into a single row of configuration SRAM.

After the final row is loaded, re-enable the bootstrap voltage and the analog circuitry by writing the Analog Enable command (0x10) to the Function register (RS=0).

Organization of Configuration Memory - The ASCII Hex Configuration File Format

The AnadigmDesigner® design software generates configuration files for programming serial boot PROMs, or in this case, for hosted booting. The file format that is easiest to use is ASCII Hex File format, also known as AHF. In an AHF file, a byte is represented by a pair of ASCII characters which represent the Hex value of that byte. For example "11110111" is recorded as "F7". A prototype AHF configuration file for an AN10E40 is given below. In this example, most of the configuration data has been truncated (and replaced with a comment) to facilitate concise explanation. It is not necessary to use the (bit order) reversed version of the AHF file.

```
138502B7 (4 Byte Device ID)
00 (Data Type Byte)
00AE . . . (78 configuration data bytes, plus row  0 checksum byte) . . . 0000 AF
0000 . . . (78 configuration data bytes, plus row  1 checksum byte) . . . 0000 B6
0300 . . . (78 configuration data bytes, plus row  2 checksum byte) . . . 0000 43
0021 . . . (78 configuration data bytes, plus row  3 checksum byte) . . . 0000 C3
0000 . . . (78 configuration data bytes, plus row  4 checksum byte) . . . 0000 6C
0000 . . . (78 configuration data bytes, plus row  5 checksum byte) . . . 0000 44
0E40 . . . (78 configuration data bytes, plus row  6 checksum byte) . . . 0000 D2
0022 . . . (78 configuration data bytes, plus row  7 checksum byte) . . . 0000 34
3700 . . . (78 configuration data bytes, plus row  8 checksum byte) . . . 0000 DE
00CD . . . (78 configuration data bytes, plus row  9 checksum byte) . . . 0000 52
3031 . . . (78 configuration data bytes, plus row 10 checksum byte) . . . 0000 14
```

All AHF files begin with a 4 byte device ID. All AN10E40 devices contain the `138502B7` ID code. If there is a mismatch between the device ID downloaded and the actual device ID, then the FPAA asserts an error signal and aborts the download.

Following the ID, there is one additional Data Type byte which tells the FPAA configuration engine something about all the subsequent data. Currently, the only supported data type is `00`, which designates unencrypted, uncompressed, sequential data. All white space characters in an AHF file can be ignored.

Next comes 11 rows worth of configuration data. Each row of data is 78 bytes long plus one Error Check Byte (ECB). If the ECB byte does not match the internally calculated checksum value then again (like a mismatched device ID code) the array will assert the ERRb pin, halt its configuration engine and ignore all subsequent data.

Mode 1 – Boot from ROM (BFR Mode)

In applications where the AN10E40 should boot from a serial memory device instead of a microprocessor, connect as shown below in Figure 16. In this stand alone configuration, the AN10E40 handles all the reset and configuration signaling. A standard serial EEPROM holds the configuration data. (Such serial memories are widely available as FPGA boot devices.)

Holding MODE[1] high puts the AN10E40 in BFR mode. Holding MODE[2] low instructs the AN10E40 to generate its own configuration clocks from its on-chip ring oscillator and sets CFG_CLK to be an output.

On power up, the internal power on reset sequence begins. As it concludes, the AN10E40 examines the state of the RESETb pin. If held low, it does nothing. When the host system releases RESETb, the self configuration sequence begins. Both CFG_CLK and DCLK go active and MEMCEb goes low. With MEMCEb asserted, the EEPROM presents the first data bit. With every rising DCLK edge, the AN1E40 accepts the current data bit. Also on this rising DLCK edge, the next data bit is clocked out of the serial PROM.

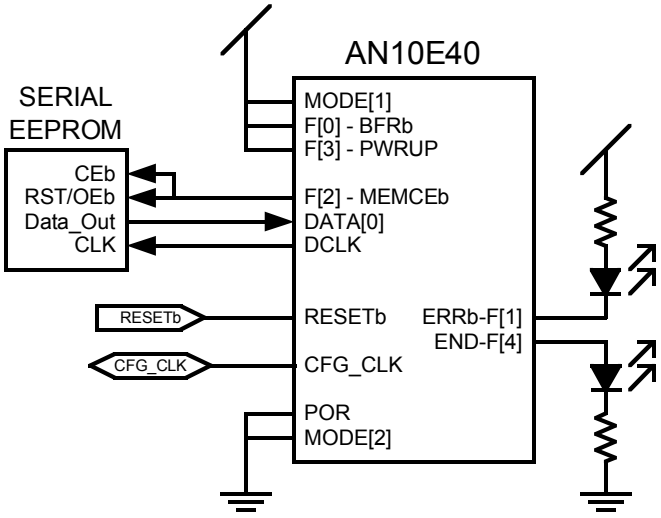


Figure 16. A typical Boot From ROM connection for the AN10E40.

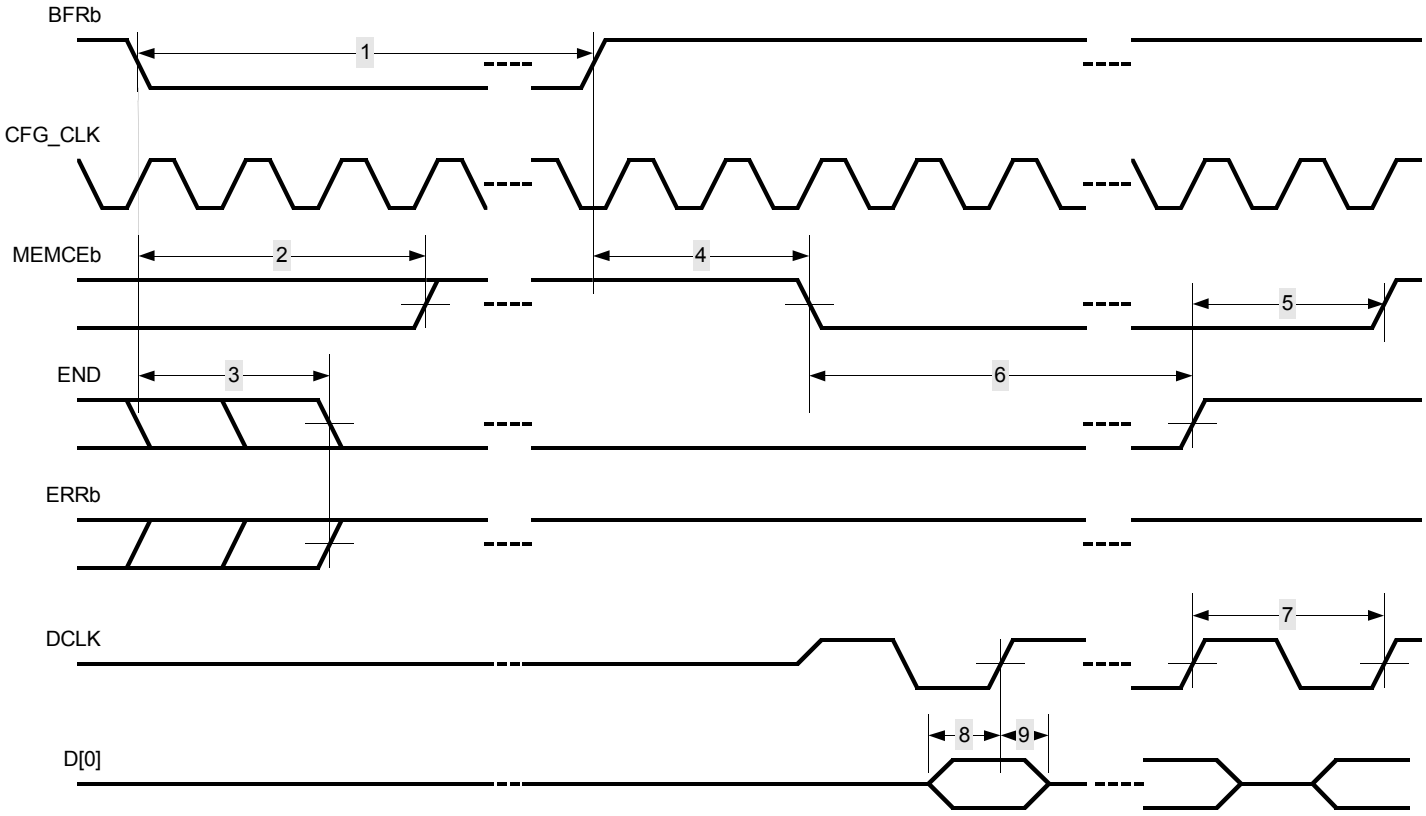
After this automatic power on configuration has completed, there are two options for repeating a configuration sequence. The first is the assertion of BFRb. On a falling edge of BFRb, the AN10E40 will repeat the complete configuration sequence. BFRb may continue to be held low for an arbitrarily long period without effecting normal operation. The second option is the assertion of RESETb. As long as RESETb is asserted low, the AN10E40 will hold idle in a reset condition. On the rising edge of RESETb, the AN10E40 will repeat the configuration sequence.

If there is an error detected in the configuration bit stream, ERRb will assert low and the configuration sequence will halt. ERRb is an open drain output. If the system has more than one FPAA on board, all the ERRb signals can be wired together to provide a single indication that some configuration error was detected.

A speed up of the configuration process is possible by supplying your own CFG_CLK. If such a speed up is desired, tie MODE[2] high and drive CFG_CLK (it is now an input) with a clock signal up to 40 MHz. DCLK will be 1/2 the frequency of CFG_CLK, so be sure to check your EEPROM specifications to be sure that it can go that fast. The following Configuration Clock section has more detail on the relationship between these two signals.

Figure 16 shows only those signals explicitly associated with BFR Mode configuration. Other signals including: OPAM_DISABLE, CEXT, OPAMP_VMR, powers, grounds and the switched capacitor CLOCK signal must also be connected for proper operation. Please reference the Pin Out Description section for complete connection details.

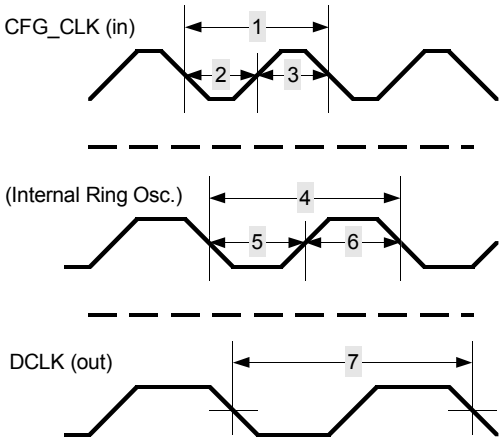
BFR Timing



#	Characteristic	Min	Max	Unit	Notes
1	BFRb Pulse Width	50		ns	
2	BFRb Assertion to MEMCEb Deassertion		3	Clk	
3	BFRb Assertion to END and ERRb Deassertion		3	Clk	
4	BFRb Release to MEMCEb Assertion		3	Clk	
5	END Assertion to MEMCEb Deassertion	2	2	Clk	
6	Configuration Time	14109	14109	Clk	
7	DCLK Period	2	2	Clk	
8	DATA[0] Set Up Time	20		ns	
9	DATA[0] Hold Time	0		ns	

Figure 17. BFR Mode Timing

Configuration Clock



#	Characteristic	Min	Typ	Max	Unit
1	CFG_CLK Period	50			ns
2	CFG_CLK Low	10			ns
3	CFG_CLK High	10			ns
4	Ring Osc Period	25	50	100	ns
5	Ring Osc Low	10	25	50	ns
6	Ring Osc High	10	25	50	ns
7	DCLK Period	Always twice the period of CFG_CLK. (If MODE[2] = 1 then CFG_CLK is an input. If MODE[2] = 0, then CFG_CLK is an output running at $^1/_8{}^{th}$ the frequency of the internal ring oscillator.)			

Figure 18. Configuration Clock Specifications

If MODE[2] is held low, a divided down version of the ring oscillator output is used as the configuration logic clock. CFG_CLK is set to be an output and reflects this clock. If instead MODE[2] is held high, CFG_CLK becomes the configuration logic clock input. For shortest possible configuration times, use CFG_CLK as an input.

In a minimal system, you may want to take advantage of the AN10E40's internal ring oscillator. The operating frequency of the ring oscillator can vary from 10MHz up to 40MHz. This variation is expected and presents no problems for the proper operation of the configuration engine. The ring oscillator is divided by 8 before use by the configuration engine.

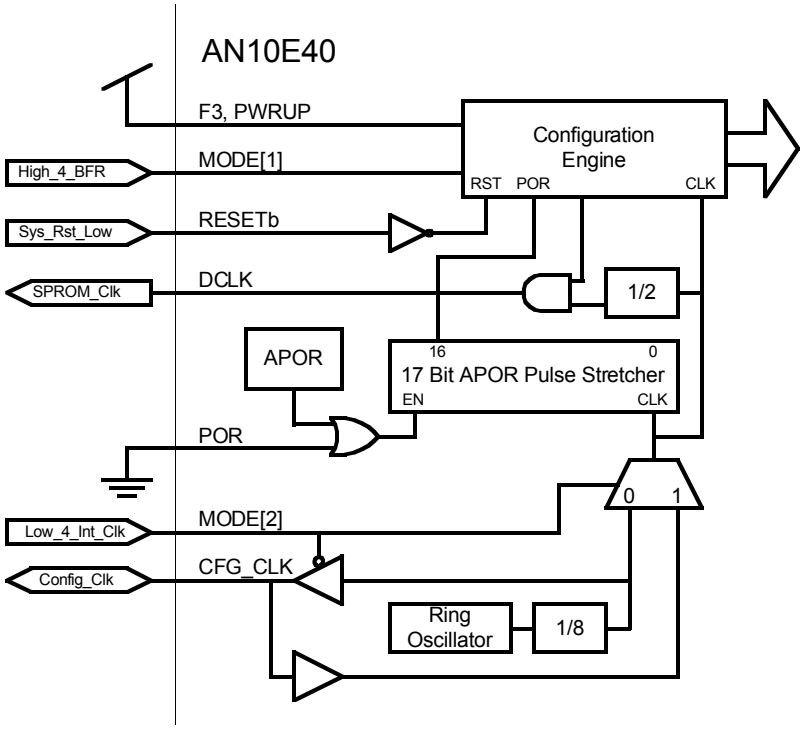


Figure 19. Block Diagram Showing Clocks and Resets

Reset Sequences

There are several sub-circuits which control the AN10E40 reset sequence and subsequent re-configuration. Each interacts with the next to ensure reliable power up and system reset behavior.

Analog Power On Reset (APOR) & Power On Reset (POR)

When coming up cold (or at the onset of a brown out condition) the APOR circuit generates a pulse. This pulse starts a companion 17 bit counter. This counter (driven by the internal configuration clock) serves as a digital APOR pulse stretcher to produce a much longer POR signal to the configuration engine.

The AN10E40 provides a POR input pin so that the internal POR signal may be manually asserted. In a typical application POR is tied to system VSS. There is otherwise rarely need for such fine control.

Internal Reset Activity

When either an external reset or internal POR reset is detected, a sequence of events transpires. First of course, the configuration engine is reset and all the analog circuitry is powered down. Next, the configuration engine continuously cycles through the SRAM configuration memory, repeatedly zeroing out the contents. This continues until the 17 bit POR timer rolls over.

The length of the APOR pulse is dependant on VDD ramp rate, and then the entire reset process may be paced by the widely varying ring oscillator. As such it is not possible to know a priori the exact length of the reset sequence, but it can be bounded as shown in the performance characteristics section.

Setting MODE[2] high, and driving CFG_CLK with a known external frequency, yields a much more deterministic configuration time. The only uncertainty is the width of the APOR pulse, but this is typically much less than half a clock cycle.

Once the POR timer rolls over, the state of the external RESETb pin is examined. If RESETb is asserted low then the configuration SRAM is cleared one more time and the chip is held in the reset state; configuration is held off until RESETb is deasserted. If RESETb is instead high as the POR timer rolls over, the configuration SRAM is cleared on more time and the configuration sequence begins. If the chip is in BFR mode, the configuration takes place automatically. If the chip is instead in Micro Mode, then the configuration engine waits for writes to the function register.

External Reset Assertion

Either POR or RESETb pins can be asserted to initiate a reset. If RESETb is not asserted, then the rising edge of POR is detected and a complete reset/configuration sequence executes. POR should be dropped before the 17 bit counter rolls over.

If instead POR is held low, a falling edge on RESETb can be detected which will clear SRAM a single time. If RESETb is held low, configuration is held off until RESETb is deasserted, otherwise configuration proceeds immediately after the SRAM clear.

In BFR mode, a falling edge of the BFRb signal is detected, and it too re-initiates a configuration sequence (but no reset sequence).

Mechanical

Package Details

The AN10E40 is currently offered in a 80 pin QFP package. This package has been characterized to have a $\_{JA}$ of 37 $^{C^\circ}/_{W}$.

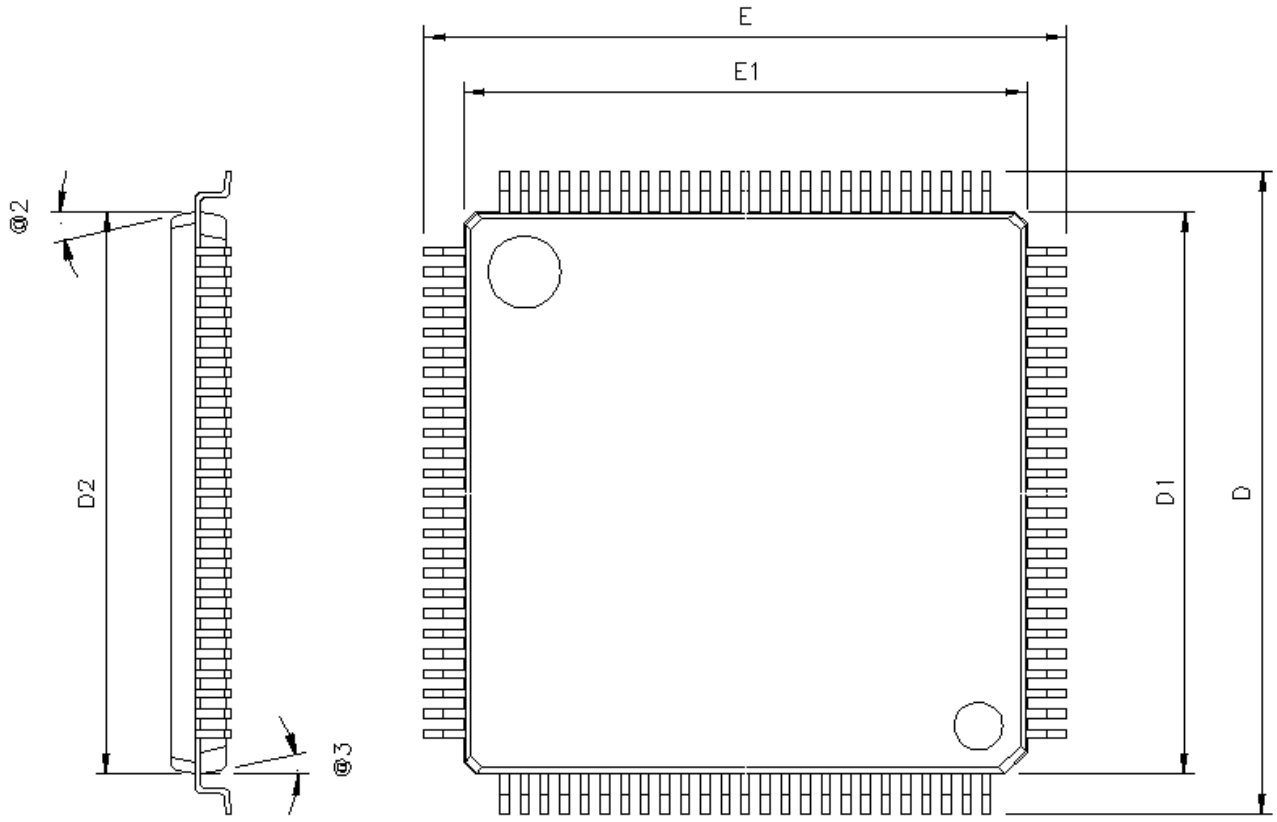
There are recommendations for dry pack handling of this device. If samples or production units are received without sealed drypack then an 8 hour, 125 ºC oven bake is recommended before wave soldering. When received in sealed drypacks, the devices should be mounted to a PCB within 48 hours of breaking the drypack seal.

Pin Out Description

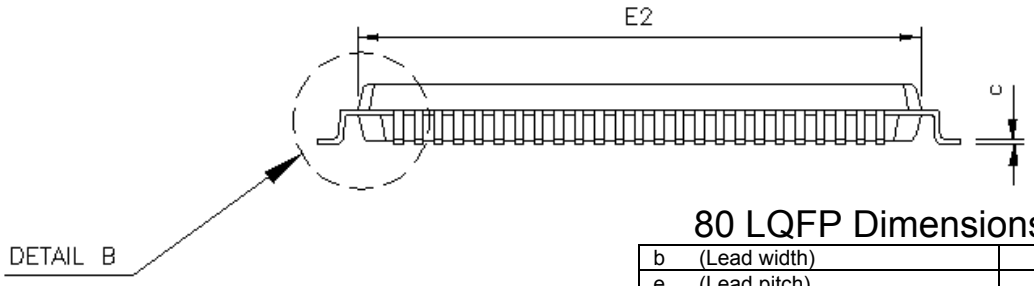
The signal naming convention holds that active low signals are named with a “b” suffix.

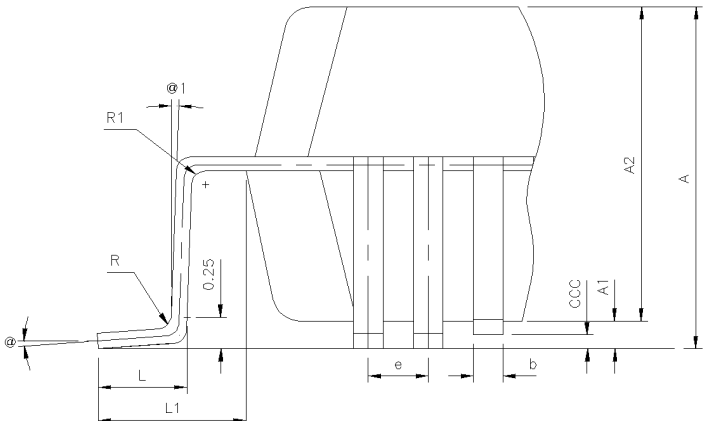
Pin	Pin name	Type	Description
1	ARRAYCLKOUT	Digital Output	Programming allows one of the 4 internal clocks to be presented here.
2	MODE[1]	Digital Input	Configuration mode control pin 0 = Micro Peripheral Interface Mode (Micro) 1 = Boot From Serial ROM (BFR)
3	MODE[2]	Digital Input	Configuration mode control pin 0 = Use Internal Clock (CFG_CLK is an output, running at 1/8 internal ring oscillator frequency.) 1 = Use External Clock (CFG_CLK is the clock input to the configuration logic.)
4	CFG_CLK	Digital I/O	Configuration logic clock Direction controlled by MODE[2]
5	DCLK	Digital Output	SPROM Configuration clock output 1/2 frequency of CFG_CLK.
6	DATA[0]	Digital I/O	Data pins used for loading configuration data and checking status. DATA[0] is used for serial BFR mode, and the entire byte width is used in Micro mode.
7	DATA[1]	Digital I/O	
8	DATA[2]	Digital I/O	
9	DATA[3]	Digital I/O	
10	DATA[4]	Digital I/O	
11	DATA[5]	Digital I/O	
12	DATA[6]	Digital I/O	
13	DATA[7]	Digital I/O	
14	F[1] (ERRb, RDb)	O.D. Out, Digital In	Configuration Function pins (BFR mode function, Micro mode function) F[1] is an Open Drain output. In multi-FPAA systems, all the ERRb lines can be tied together to provide a single error indicator.
15	F[2] (MEMCEb, WRb)	Digital Out, Digital In	
16	F[0] (BFRb, CSb)	Digital Input	
17	F[3] (PWRUP, RS)	Digital Input	
18	F[4] (END, BUSY)	Digital Output	
19	OPAMP_DISABLE	Digital Input	Op-Amp disable input (normally tied to Vss, not usually utilized in systems) Takes precedence over BFR’s PWRUP input and Micro’s Function Register Bit Position 4 (Analog Enable) 0 = Analog circuitry enabled 1 = Analog circuitry disabled
20	RESETb	Digital Input	Chip RESET Falling edge detected to start Reset
21	IOLDX	Analog Input	Unbuffered Analog input
22	IOLDY	Analog Input	Buffered Analog input
23	IOLDZ	Analog Output	Buffered Analog output
24	IOLDZ2	Analog Output	Uncommitted op-amp output
25	IOLDY2	Analog Input	Uncommitted op-amp input
26	IOLCZ	Analog Output	Buffered op-amp output
27	IOLCY	Analog Input	Buffered Analog input
28	IOLCX	Analog Input	Unbuffered Analog input
29	AVDD	Power Supply	Analog VDD, 5 Volts
30	AVSS	Power Supply	Analog VSS, 0 Volts
31	SVSS	Power Supply	Substrate VSS, 0 Volts
32	IOLBX	Analog Input	Unbuffered Analog input
33	IOLBY	Analog Input	Buffered Analog input
34	IOLBZ	Analog Output	Buffered analog output
35	IOLAZ	Analog Output	Buffered op-amp output

36	IOLAY	Analog Input	Buffered Analog input
37	IOLAX	Analog Input	Unbuffered Analog input
38	VREFOUT	Analog Output	Reference voltage
39	BVDD	Power Supply	Bandgap VDD, 5 Volts
40	BVSS	Power Supply	Bandgap VSS, 0 Volts
41	VMR	Analog Output	Signal ground, 2.5 Volts Normally left floating. Can be driven by off chip generator if the on chip VMR generator is disabled.
42	OPAMP_VMR		Signal ground, 2.5 Volts (usually loaded with 100nF to AVSS)
43	CEXT		External Reference Generator Capacitor (usually loaded with 10nF to AVSS)
44	IOD5Z	Analog Output	Buffered op-amp output
45	IOD5Y	Analog Input	Buffered Analog input
46	IOD5X	Analog Input	Unbuffered Analog input
47	IOD4Z	Analog Output	Buffered op-amp output
48	IOD4Y	Analog Input	Buffered Analog input
49	IOD4X	Analog Input	Unbuffered Analog input
50	ESD_VDD	Power Supply	ESD Structures VDD, 5 Volts
51	ESD_VSS	Power Supply	ESD Structures VSS, 0 Volts
52	IOD3Z	Analog Output	Buffered op-amp output
53	IOD3Y	Analog Input	Buffered Analog input
54	IOD3X	Analog Input	Unbuffered Analog input
55	IOD2Z	Analog Output	Buffered Analog output
56	IOD2Y	Analog Input	Buffered Analog input
57	IOD2X	Analog Input	Unbuffered Analog input
58	IOD1Z	Analog Output	Buffered Analog output
59	IOD1Y	Analog Input	Buffered Analog input
60	IOD1X	Analog Input	Unbuffered Analog input
61	IORAX	Analog Input	Unbuffered Analog input
62	IORAY	Analog Input	Buffered Analog input
63	IORAZ	Analog Output	Buffered Analog output
64	IORBZ	Analog Output	Buffered Analog output
65	IORBY	Analog Input	Buffered Analog input
66	IORBX	Analog Input	Unbuffered Analog input
67	CFG_VDD	Power Supply	Configuration (Digital) VDD ,5 Volts
68	SVSS	Power Supply	Substrate VSS, 0 Volts
69	SVDD	Power Supply	Substrate VDD, 5 Volts
70	CLOCK	Digital Input	System master clock Used by clock generator which feeds all switch capacitor analog circuitry.
71	IORCX	Analog Input	Unbuffered Analog input
72	IORCY	Analog Input	Buffered Analog Input
73	IORCZ	Analog Output	Buffered Analog output
74	IORDY2	Analog Input	Uncommitted op-amp input
75	IORDZ2	Analog Output	Uncommitted op-amp output
76	CFG_VSS	Power Supply	Configuration (Digital) VSS, 0 Volts
77	IORDZ	Analog Output	Buffered Analog output
78	IORDY	Analog Input	Buffered Analog input
79	IORDX	Analog Input	Unbuffered Analog input
80	POR	Digital Input	Power on Reset Connection to VSS is typical. This input has an active weak pull down device (capable of sinking 100 uA). If actively driving this pin, a pull up resistor may be necessary to provide additional high state current.



100 Pin Generic Drawing - Actual Device Package is 80 Pins





DETAIL "B"

80 LQFP Dimensions [mm]

b	(Lead width)	0.22-0.38
e	(Lead pitch)	0.65 Basic
ccc	(Coplanarity)	Max. 0.100
ddd	(Bent lds)	Max. 0.130
D	(Lead to lead width)	16.95 - 17.45
E	(Lead to lead length)	16.95 - 17.45
L	(Foot length)	0.73 - 1.03
L1	(Lead length)	1.60 Ref.
R	(Lead foot radius)	0.13 - 0.30
R1	(Lead shoulder radius)	Min. 0.13
A	(Overall height)	Max. 2.45
A1	(Standoff)	Max. 0.25
A2	(Package thickness)	1.80 - 2.20
c	(Lead thickness)	0.11 - 0.23
D1	(Bottom package width)	13.90 - 14.10
E1	(Bottom package length)	13.90 - 14.10
D2	(Top package width)	13.90 - 14.10
E2	(Top package length)	13.90 - 14.10
@	(Lead flat angle)	0º - 7º
@1	(Lead shoulder angle)	Min. 0º
@2	(Top package draft angle)	15º
@3	(Bottom package draft angle)	15º

Package Pin Electrical Characterization

Lead Inductance			
Lself [nH]		Lmutual [nH]	
Center	Corner	Center	Corner
4.22	5.23	1.93	2.55

Lead Capacitance			
Cself [pF]		Cmutual [pF]	
Center	Corner	Center	Corner
0.52	0.61	0.18	0.26

Lead Resistance			
Lead Resistance [mΩ]		Lead Impedance – Z_0 [Ω]	
Center	Corner	Center	Corner
1.760	2.490	90.52	92.90

Center refers to a pin to die bond wire near the center of the package (pins 10, 20, 50 and 70). Corner refers to those bond wires near the package and die corners.

Powers, Grounds and Bypassing

In order to ensure that your design benefits from the highest possible fidelity available, there are a few signals that you should pay special consideration to when designing the host circuit board.

Recommended Configuration for Power & Ground

The most common configuration ties the following pins together to a quiet +5 V power plane: AVDD, SVDD, BVDD and ESD_VDD with the shortest possible connection. The following pins should be brought down to a quiet ground plane: AVSS, SVSS, BVSS and ESD_VSS also with the shortest possible connection.

CFG_VDD and CFG_VSS can also be connected as above, but the associated digital circuitry is not as sensitive to noise, and therefor can be connected to your system's "noisier" power rails.

Bypassing recommendations vary with the design of your power planes, but it is usually sufficient to recommend the use of a parallel pair of capacitors connected between each VDD pin and its associated VSS plane. These capacitor pairs should be placed as close as possible to: AVDD, SVDD, and BVDD and connected by the shortest path possible to the associated ground plane. The recommended capacitors are .1 uF in parallel with .01 uF. Each of these should be low leakage and low ESR type capacitors. Polyester (Mylar) capacitors are optimal for the job, but the generic ceramic bypass capacitors are sufficient.

Bypassing CFG_VDD to CFG_VSS can be accomplished in a manner similar to that described above, but layout is less critical.

Bypassing ESD_VDD to ESD_VSS is not required, but can serve to optimize the performance of the ESD protection structures in the device's IO cells, in the unlikely event that such a current path is ever called upon.

AVDD and AVSS

AVDD and AVSS supply the op-amp and comparator circuits with +5 V and 0 V respectively. Obviously then, care should be taken then to ensure that the quietest possible supply and ground signals are provided.

SVDD and SVSS

The wafers used in the construction of the AN10E40 are P type, so substrate ties (SVSS) should be connected to a quiet ground potential. The N type well ties on the wafer are all connected the SVDD pin and therefor need to be biased to a quiet positive potential. Connecting SVDD to AVDD and SVSS to AVSS is a typical configuration.

BVDD and BVSS

BVDD and BVSS supply all the band-gap voltage references, VMR generator and bias current generators. Here again, the typical connection is to AVDD and AVSS.

ESD_VDD and ESD_VSS

These two signals do not normally source or sink any current to the AN10E40. In the rare event that a device pin is electrically overstressed by an ESD or EOS event (Electrostatic Discharge or Electrical Overstress), then current is sourced or sunk though these rails. These two should be connected to quiet supplies and here again AVDD and AVSS are the typical connections.

CFG_VDD and CFG_VSS

The CFG_VDD and CFG_VSS rails supply all the digital configuration circuitry, the on board ring oscillator, APOR and POR generation circuitry with +5V and 0V respectively. With the possible exception of the on board ring oscillator, any digital supply noise produced by this circuitry would not normally effect the performance of the analog portion, so no particular care need be taken with these supply signals from the chip's point of view. Your system however may have both "noisy" and "clean" power rails available. If so, CFG_Vxx may be best connected to the "noisy" rail, leaving the "clean" supply as unpolluted as possible.

OPAMVMR and CEXT

As mentioned above in the Voltage Mid-Rail Generator section, both OPAMPVMR and CEXT should be bypassed to a quiet ground node to ensure optimal performance. Generally, a good configuration consists of a Polyester (Mylar) 10nF capacitor between CEXT and AVSS. A similar bypassing connection for OPAMPVMR is also recommended. Care should be exercised in the placement of these components to minimize the signal path between the array and the bypass capacitors.

The AN10E40 in Split Supply Systems

All analog signal processing within the AN10E40 is referenced to its internal VMR node (Voltage Mid Rail, normally 2.5 V above AVSS). For those applications where a split supply (±2.5 V) is necessary, it is possible to connect the AN10E40 as shown in Figure 20.

Here the AN10E40's internal VMR generator is disabled (a feature available via AnadigmDesigner®) and the chip's VMR pin is instead driven externally by the system's ground plane.

Naturally, logic circuits which interface to the AN10E40 must also be powered off the split rail as shown.

Under some circumstances, it may be more practical to instead power the AN10E40 off a single 5 V supply and AC coupled the ground referenced input signal.

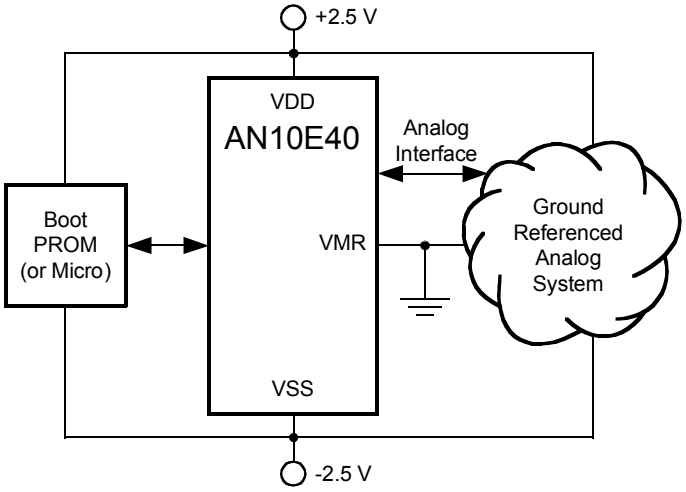


Figure 20. Connecting to a Split Rail System

Characterized Electrical Parameters

Because the AN10E40 is programmable, performance characteristics are reported for representative pieces of the device rather than for the entire device. The following sections detail these characteristics.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies (See Note1)	AVDD SVDD BVDD ESD_VDD CFG_VDD	-0.5	-	5.5	V	With respect to AVSS, SVSS, BVSS, ESD_VSS and CFG_VSS.
VD – VA	VDD - VSS	-0.5	-	0.5	V	Ideally all supplies should be at the same voltage.
Power Dissipation	Pmax, @25°C Pmax, @85°C	- -	- -	2.7 1.0	W	Still air, No heatsink, 4 layer board, 80 pins. θja = 37 °C/W
Analog and Digital Input Voltage	Vin	Vss - 0.5	-	Vdd + 0.5	V	
Ambient operating Temperature	Top	-40	-	85	°C	
Storage Temperature	Tstg	-65	-	150	°C	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies	AVDD SVDD BVDD ESD_VDD CFG_VDD	4.75	5.0	5.25	V	With respect to AVSS, SVSS, BVSS, ESD_VSS and CFG_VSS. Please refer to Spec, page21 for typical configuration
Analog Input Voltage	Vin_a	0.5	-	Vdd - 0.5	V	With respect to AVSS.

Power Consumption

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Quiescent Power (See Note2a)	Iin	-	32	42	mA	At 5.00 volts, 25°C.
Quiescent Power (See Note2b)	Iin	-	18	25	mA	At 5.00 volts, 25°C.
Nominal Power (See Note3)	Iin	-	22	31	mA	At 5.00 volts, 25°C.
Maximum Power (See Note4)	Iin	-	87 100	120	mA mA	At 5.00 volts, 25°C. At 5.25 volts, -40°C.

Notes:

1. Absolute Maximum Power Supply Rating - the failure mode is non-catastrophic for Vdd of up to 7 volts, but will cause reduced operating life time. The additional stress caused by higher local electric fields within the CMOS circuitry may induce metal migration, oxide leakage and other time/quality related weaknesses.

2a. Quiescent power consumption, 1 MHz CLOCK system master clock (pin70), before programming.

2b. Quiescent power consumption, 1 MHz CLOCK (pin 70), Device programmed, No IP Modules.

3. Nominal Power, 1 MHz CLOCK(pin 70), 4 x CAB as Inverting Amplifiers (G01), gain = 2.0, audio signal input 250 mVp-p.

4. Maximum Power Consumption, 1 MHz CLOCK (pin 70), 20 x CAB as inverting amplifiers, gain = 1.0, audio signal input 1 Vp-p, all I/O buffers active.

Digital Interface Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Comment
High Level Input Voltage threshold	VIH	0.7VDD	-	-	V	
Low Level Input Voltage threshold	VIL	-	-	0.3VDD	V	
High Level Output Voltage threshold	VOH	-	-	0.8VDD	V	
Low Level Output Voltage threshold	VOL	0.2VDD	-	-	V	
Input Leakage Current	Iin	-	0.01	1.0	uA	
Output Load	Cload	-	-	50	pF	All digital outputs except pin14.
Output Load	Rload Cload	10 -	- -	- 50	K_ pF	Pin 14, F[1] (ERRb, RDb) This is an open drain.
Configuration clock. (CFG_CLK)	Clock freq.	-	-	20	MHz	Configuration Clock, logic. Input if Pin3, Mode[2]=1.
Master Clock	Clock Freq.	-	-	1	MHz	Master clock. Used for all analog blocks.
Clock Duty Cycle	Clock duty cycle	40	-	60	%	CFG_CLK If Master clock is used with divider=1, duty cycle should be 1:1.

VMR (Voltage Mid-Rail)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
VMR Voltage	Vvmr	2.455	2.5	2.555	V	Vdd = 5 V, 25 ^{0}C, equivalent to ±2%
Voltage Drift over temp	-	-	400	800	uV/^{0}C	Ambient Temp –40^{0}C to +85^{0}C
Voltage drift over Supply range	-	-	±0.5	±1.0	%	AVDD,DVDD,BVDD = 4.75 to 5.25 volts
Output load, (VMR pin 41).	VMR Load	50	-	-	K_	Not designed to source current, this pin may be used as a voltage reference. Normally left open.
Output load, OpAmpVMR, pin 42.	VMR Load	1	10	100	nF	Not designed to source current, this pin is to be used to decouple noise.
Power Supply Rejection Ratio	PSRR	40	45	-	dB	w.r.t. AVDD, Cext=10 nF.
Narrowband VMR Noise,	-	-	65	60	dBm	Cext=10 nF Low Noise CopAmpVMR=10 nF. 50 Hz to 500 KHz bandwidth
Cext, Pin 43.	Cext	1	10	100	nF	Not designed to source current, pin is for capacitive decoupling only.

Vref (Reference Voltage)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output range	-	-2.474	0.0	2.474	V	With respect to VMR
Output range accuracy w.r.t. input setting	-	-	0.4	0.8	%	With respect to VMR, Vdd = 5.0 volts
Voltage Drift over temp	-	-	500	1000	uV/^{0}C	
Voltage drift over Supply range	-	-	0.5	2.0	%	AVDD, VDD, BVDD = 4.75 to 5.25 volts
Output load	Vref Load	50	-	-	K_	
Power Supply Rejection Ratio	PSRR	50	-55	-	dB	With respect to AVSS, Cext = 10 nF.
Vref Noise	-		55	50	dBm	Cext = 10 nF Low Noise 50 Hz to 500 KHz bandwidth

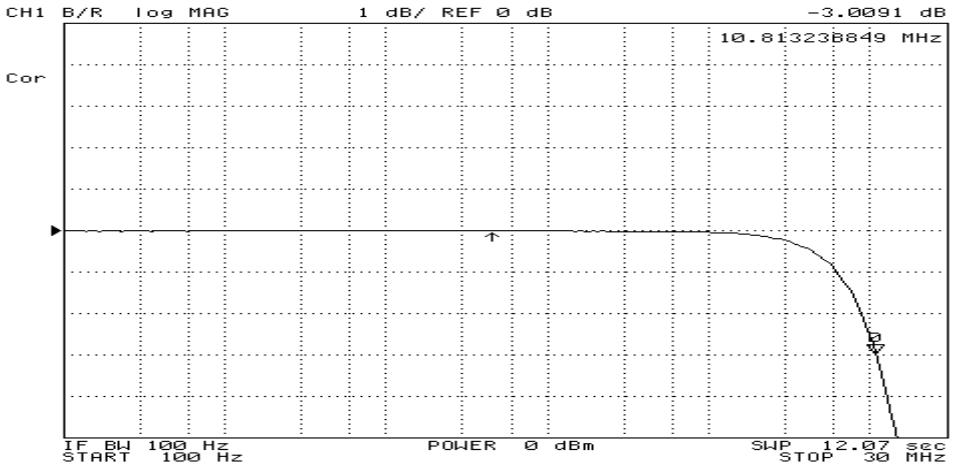
Analog Input/Output Buffer

(AVDD = SVDD = BVDD = ESD_VDD = CFG_VDD = 4.75 to 5.25 volts, Master Clock = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	Vin(z)	Vss	-	Vdd	Volts	Pins IO**Z, This pin is an input to the device core cells or an output from the I/O buffer.
Input range	Vin(x,y)	0.5	-	Vdd-0.5	Volts	Pins IO**X, IO**Y, These pins are outputs from the device core or inputs to the I/O buffer. Input range limited to I/O buffer, output range.
Output Voltage range Small signal (ss) Large signal (ls)	 Vout(ss) Vout(ls)	 0.5 0.5	 - -	 Vdd-0.5 Vdd-0.5	Volts	Pins IO**Z, Buffer output, Pins I/O**X and , IO**Y, if connected to a core cell output. ss, Cloadmax = 100 pF, Rloadmin = 1 K_. ls, Cloadmax = 100 pF, Rloadmin = 10 K_.
Slew Rate Rise	Srrise	16	18	-	V/us	VDD = 5.0 V
Slew Rate Fall	Srfall	19	21	-	V/us	VDD = 5.0 V
3dB Bandwidth	B	7.0	10.0	-	MHz	- 3 dB Point
Gain error	Gerr	-	-	-	-	The I/O buffer is configured as a unity gain buffer, Open loop gain > 80dB. Thus errors are measured as input offset.
Input Offset	Ioff	-	4	12	mV	
Input Offset Drift over temp	Ioff/dt	-	5	30	uV/^{0}C	
Input resistance	-	-	-	-	M_	Input leakage current only, There is no dc current path.
Input Leakage current	Ileak	-	0.1	10.0	uA	
Power supply rejection ratio	PSRR	55	60		dB	

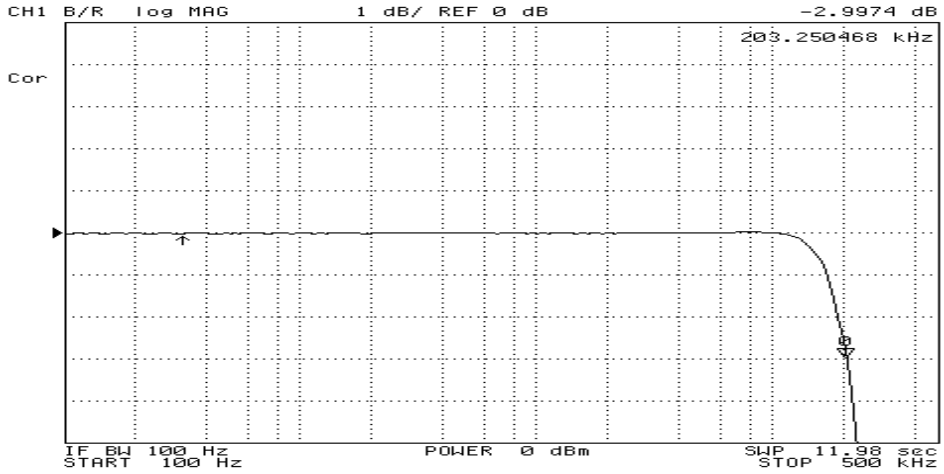
The AN10E40 Analog I/O cells are carefully designed to provide robust drive without sacrificing bandwidth. The plot below shows that the bandwidth of the I/O cells exceeds bandwidth of signals typically processed within the device (The switched capacitor architecture is switched at 1 MHz maximum clock frequency.)

I/O Cell Bandwidth (Unity gain buffer)



I/O Buffer Cell Configured as a Sallen-Key Filter

The AN10E40 Analog I/O cells are especially designed to accommodate the construction of Sallen-Key topology filters. These filters are easily constructed and are handy for input anti-aliasing or output switching noise filtering. The filter used to measure the data below was designed to roll off at 200 kHz.



The measurements shown below are repeated several times with different weighting factors.
CCIR IEC 468-3 Weighted and A-Weighted measurements are two standard Psophometric weightings common to audio and communications equipment manufacture.

Parameter	Typ.	Notes
SNR, >500 kHz Bandwidth	85 dB	1 kHz, Sine, 1.0 Vrms
SNR, 80 kHz Bandwidth	88 dB	1 kHz, Sine, 1.0 Vrms
SNR, 468-3 Weighted	87 dB	1 kHz, Sine, 1.0 Vrms
SNR, A Weighted	94 dB	1 kHz, Sine, 1.0 Vrms
Total Harmonic Distortion (THD+N)	0.015%	80 kHz

Analog Core Cell (C.A.B. Configurable Analog Block) Amplifier

(AVDD = SVDD = BVDD = ESD_VDD = CFG_VDD = 4.75 to 5.25 volts, Master Clock = 1 MHz)

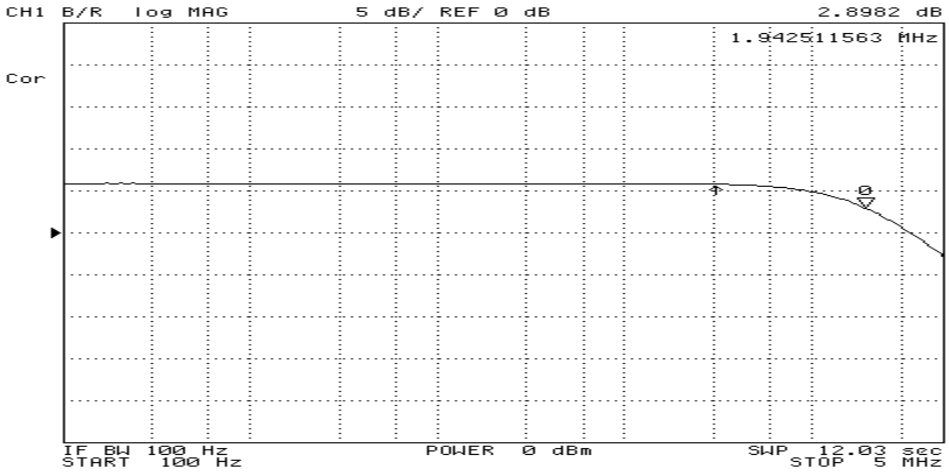
Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input range	See Analog Input/Output Buffer above.					
Input range						
Output Voltage range						
Slew Rate Rise	Srrise	16	18	-	V/us	VDD=5.0v
Slew Rate Fall	Srfall	19	21	-	V/us	VDD=5.0v
3dB Bandwidth	B	7.0	10.0	-	MHz	- 3 dB Point
Gain error	Gerr	-	0.4	-	%	Dependant upon IP module configuration.
Gain error temperature drift.	Gerr/d^{0}C	-	10	50	ppm/^{0}C	Dependant upon capacitor matching, clock and IP module, excluding Ioff,
Gain error voltage drift. (supply voltage)	Gerr/dv	-	50	250	ppm/V	Dependant upon capacitor matching, clock and IP module, excluding Ioff.
Gain error time drift. (10years).	Gerr/dt	-	10	50	ppm/yr	Dependant upon capacitor matching, clock and IP module, excluding Ioff.
Input Offset	Ioff	-	4	12	mV	
Input Offset Drift over temp	Ioff/dt	-	5.0	30.0	uV/^{0}C	
Power supply rejection ratio	PSRR	55	60		dB	

There are 20 basic CABs (Configurable Analog Block) within the AN10E40, each contains a single configurable Amplifier. The CAB architecture is designed to maximize flexibility. The AN10E40 takes advantage of switched capacitor circuit architectures and programmable switches. A good understanding of Switched Capacitor circuit operation allows the user to calculate the limits associated with the utilization of the CAB above when an IPModules is implemented using this amplifier. Around the amplifier are 5 banks of programmable capacitors which can be connected within the selected architecture and can be sized.

Typical Performance Examples

A Programmable Inverting Gain Stage

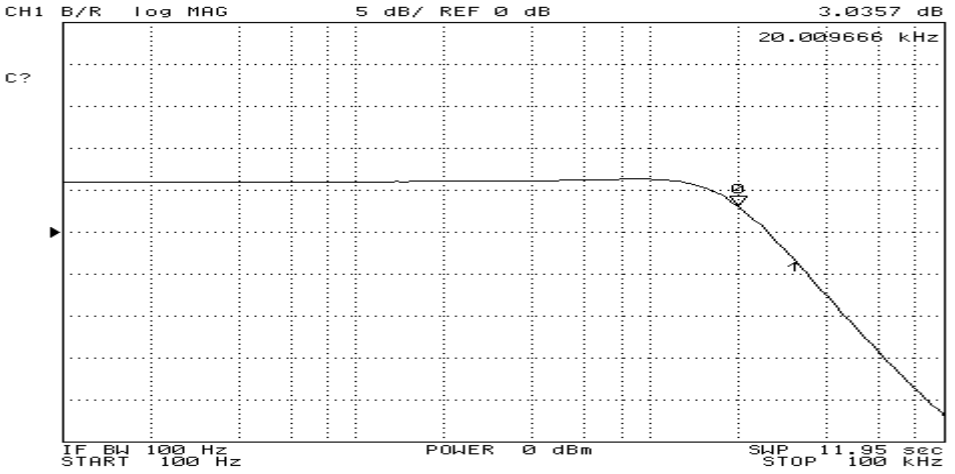
In this example, a CAB was programmed to serve as an inverting gain stage with the Gain parameter set to 2. Notice the dead flat response throughout the band swept.



	Min.	Typ.	Max.	Notes
SNR, 468-3 Weighted		77 dB		1 kHz, Sine, 0.5Vrms
SNR, A Weighted		85 dB		1 kHz, Sine, 0.5 Vrms
Total Harmonic Distortion (THD+N)		0.011%		80 kHz
Gain Set to 1.00		0.4%		Gain Set Error

A Programmable Low Pass Filter

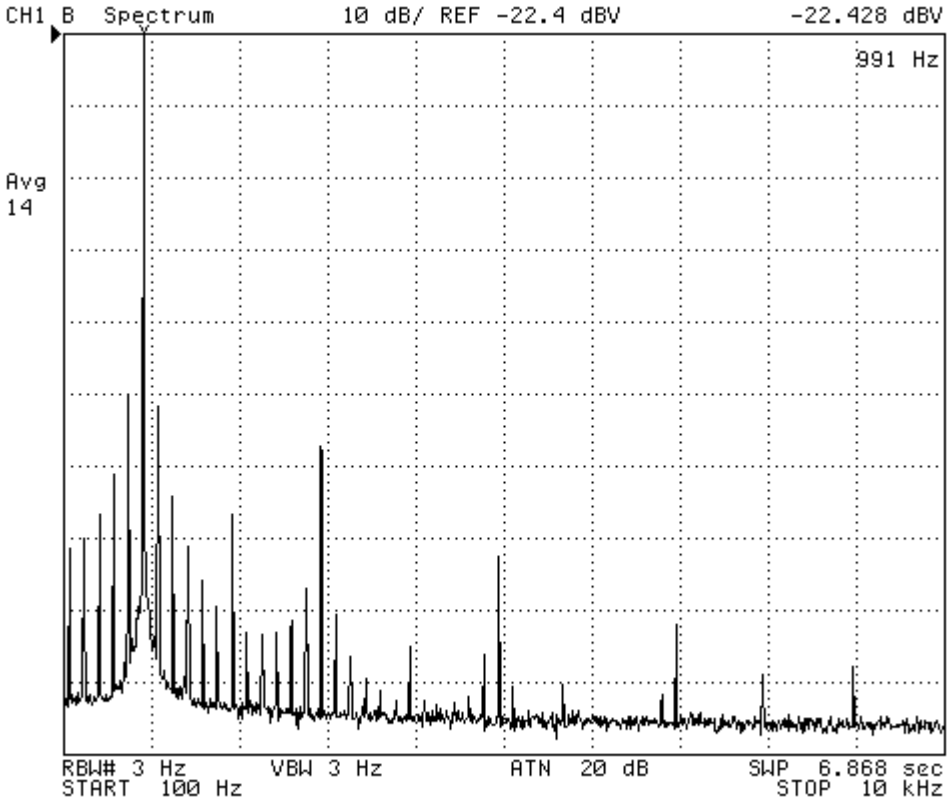
With a CAB programmed as a low pass (fc = 20 kHz), low Q (Q = 0.707) with a Gain of 2, the following performance can be expected.



	Min.	Typ.	Max.	Notes
SNR, 468-3 Weighted		70 dB		1 kHz, Sine, 0.5 Vrms
SNR, A Weighted		78 dB		1 kHz, Sine, 0.5 Vrms
Total Harmonic Distortion (THD+N)		0.05%		80 kHz
Gain Set to 1.00		0.4%		Gain Set Error
fc set to 50.0 Hz, CLK at 16.13 kHz		+0.84%		Error in -3 db Corner Frequency

Sine Wave Oscillator

The test circuit is a Sine Wave Oscillator IPmodule, programmed to generate a 1.0 V Peak, 1 kHz Sine wave. The input clock was running at 35.714 kHz. From the plot you can see that the most significant spur at 3 kHz is nearly 60 dB down from the fundamental. Other less significant spurs are noted at 2, 5, 7 and 9 kHz.



Electrostatic Discharge Characterization

The following excerpts were copied with permission from and gratitude to: The Electrostatic Discharge Association. An excellent tutorial on the subject of ESD and EOS can be found on their web site at http://www.esda.org/.

A Quick Review of ESD Basics

Electrostatic Discharge (ESD) damage results from handling the devices in uncontrolled surroundings or when poor ESD control practices are used. Generally damage is classified as either a catastrophic failure or a latent defect.

Catastrophic Failure

When an electronic device is exposed to an ESD event it may no longer function. The ESD event may have caused a metal melt, junction breakdown, or oxide failure. The device's circuitry is permanently damaged causing the device fail.

Latent Defect

A latent defect, on the other hand, is more difficult to identify. A device that is exposed to an ESD event may be partially degraded, yet continue to perform its intended function. However, the operating life of the device may be reduced.

Basic ESD Events--What Causes Electronic Devices to Fail?

ESD damage is usually caused by one of three events: direct electrostatic discharge to the device; electrostatic discharge from the device or field induced discharges.

Discharge to the Device

An ESD event can occur when any charged conductor (including the human body) discharges to an ESDS (electrostatic discharge sensitive) device. The most common cause of electrostatic damage is the direct transfer of electrostatic charge from the human body or a charged material to the electrostatic discharge sensitive (ESDS) device. When one walks across a floor, an electrostatic charge accumulates on the body. Simple contact of a finger to the leads of an ESDS device or assembly allows the body to discharge, possibly causing device damage. The model used to simulate this event is the Human Body Model (HBM).

A similar discharge can occur from a charged conductive object, such as a metallic tool or fixture. The model used to characterize this event is known as the Machine Model.

Discharge from the Device

The transfer of charge from an ESDS device is also an ESD event. The trend towards automated assembly would seem to solve the problems of HBM ESD events. However, it has been shown that components may be more sensitive to damage when assembled by automated equipment. A device may become charged, for example, from sliding down the feeder. If it then contacts the insertion head or another conductive surface, a rapid discharge occurs from the device to the metal object. This event is known as the Charged Device Model (CDM) event, and can be more destructive than the HBM for some devices. Although the duration of the discharge is very short--often less than one nanosecond--the peak current can reach several tens of amperes.

Field Induced Discharges

Another event that can directly or indirectly damage devices is termed Field Induction. As noted earlier, whenever any object becomes electrostatically charged, there is an electrostatic field associated with that charge. If an ESDS device is placed in that electrostatic field, a charge may be induced on the device. If the device is then momentarily grounded while within the electrostatic field, a transfer of charge from the device occurs.

AN10E40 ESD Classifications

Pin Type	Classifications	Notes
Digital Inputs	Class 3A Class M3 Class C6	The C6 classification is based on estimated performance based on extensive HBM characterization.
Digital Outputs	Class 3A Class M3 Class C6	The C6 classification is based on estimated performance based on extensive HBM characterization.
Digital I/0	Class 3A Class M3 Class C6	The C6 classification is based on estimated performance based on extensive HBM characterization.
Analog I/0	Class 3A Class M3 Class C6	The C6 classification is based on estimated performance based on extensive HBM characterization.
CEXT, OPAMVMR, VMR, VREF	Class 3A Class M3 Class C6	The C6 classification is based on estimated performance based on extensive HBM characterization.

Standard ESD Classifications

ESDS Component Sensitivity Classification **Human Body Model**	**ESD STM5.1-1998**
Class 0	< 250 volts
Class 1A	250 volts to < 500 volt
Class 1B	500 volts to < 1,000 volts
Class 1C	1,000 volts to < 2,000 volts
Class 2	2,000 volts to < 4,000 volts
Class 3A	4,000 volts to < 8,000 volts
Class 3B	>= 8,000 volts
ESDS Component Sensitivity Classification **Machine Model**	**ANSI/ESD-S5.2-1999**
Class M1	< 100 volts
Class M2	100 volts to < 200 volts
Class M3	200 volts to < 400 volts
Class M4	> or = 400 volts
ESDS Component Sensitivity Classification **Charged Device Model**	**EOS/ESD-DS5.3-1996**
Class C1	< 125 volts
Class C2	125 volts to < 250 volts
Class C3	250 volts to < 500 volts
Class C4	500 volts to < 1,000 volts
Class C5	1,000 volts to < 1,500 volts
Class C6	1,500 volts to < 2,000 volts
Class C7	=> 2,000 volts

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