AL4V183
AL4V185

Data Sheets

Version 2.0

Amendments

11-07-01 Preliminary Version 1.0

09-13-02
1. Revised Vp (Input Pin Voltage) in section 10.1 Absolute Maximum Ratings
2. Revised V_{IH} High Level Input Voltage in section 10.2 Recommended Operating Conditions.
3. Changed the package support from TQFP to STQFP
4. Changed data sheets version to 2.0

02-20-03 Company Contact Information updated

AL4V183/AL4V185 (1k x18, 4k x18) 16K-Bit, 64K-Bit Line FIFO

Contents:

1.0 Description

The AL4V183 and AL4V185 series memory products are high-performance, low-power 18-bit read/write FIFO (First-In-First-Out) memory chips. They are specially designed to buffer high speed streaming data for a wide range of data buffering applications, such as optical disk data caching, video line data buffering.

The 18-bit input and output ports operate independently at a maximum speed of 100MHz. The built-in address decoder and pointer managing circuits provide a straightforward bus interface to serially read/write memory that reduces inter-chip design efforts. The AL4V18x embedded memory array and high performance process technologies with extended controller functions, such as read skip, Bus-Matching and Endian Select, offer flexible memory management.

The input data is synchronous with a free-running clock (WCLK), and Write-Enable pins (/WEN). Data is written into the FIFO on every clock when enable pins are asserted. The output is synchronous with the other free-running clock (RCLK) and enables (/REN). An Output Enable pin (/OE) is provided at the read port for tri-state control of the output port.

Bus-Matching feature can flexibly configure input and output bus width. The chip can automatically convert the input data bus width to match up output data bus width by packing or unpacking the data. A Big-Endian/Little-Endian data word format is provided to invert the read-in bytes sequence for output. The AL4V18x series are operating in 3.3V power supply with 5V signal tolerant input. These chips are available as a 64-pin STQFP Package.

2.0 Features

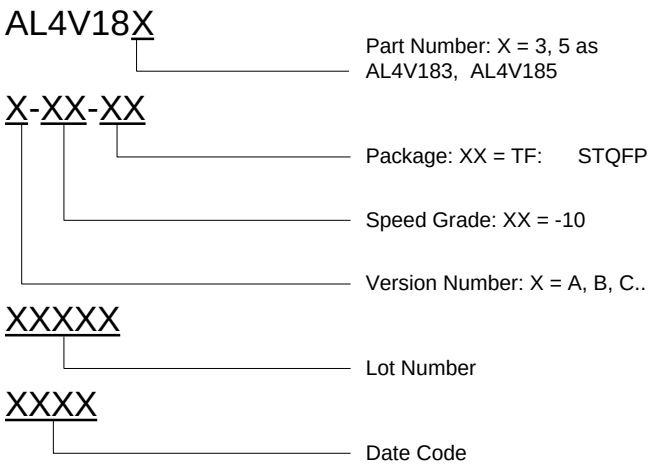
- 1,024 x18-bit cell array (AL4V183)
- 4,096 x18-bit cell array (AL4V185)
- 100 MHz Operation
- 10 ns read/write cycle time
- Independent Read and Write operations
- Output enable (data skipping)
- User selectable input and output bus width
  - x9 in to x9 out
  - x9 in to x18 out
  - x18 in to x19 out
  - x18 in to x18 out
- Big/Little Endian word format selectable
- 3.3V power supply with 5V signal tolerant input
- Available in a 64-pin Thin Quad Flat Pack (STQFP) packages

3.0 Applications

- Video line data capture
- Hard Disk cache memory
- Anti-skip audio data buffer
- Multimedia systems
- Time base correction (TBC)

4.0 Chip Information

4.1 Marking Information



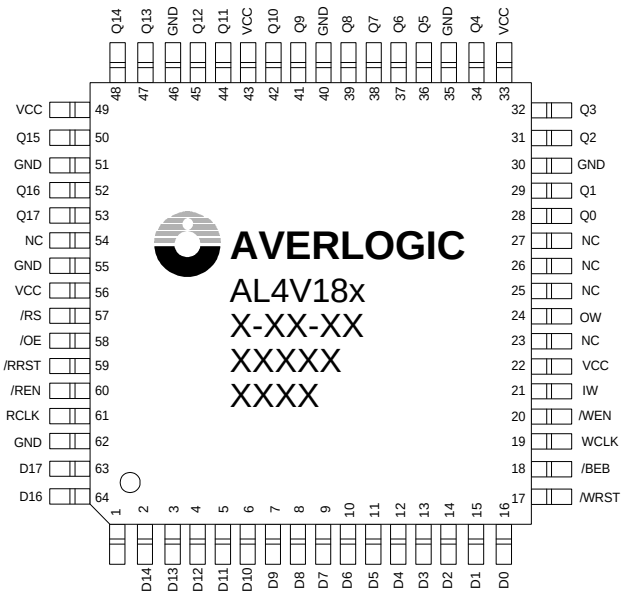
4.2 Ordering Information

The ordering information for AL4V183 and AL4V185 are:

Part number	Package	Power Supply	Status
AL4V183 (A-10-TF)	64-pin plastic STQFP (14x14mm)	+3.3V±10%	Sample in Nov., 2001
AL4V185 (A-10-TF)	64-pin plastic STQFP (14x14mm)	+3.3V±10%	Sample in Nov., 2001

5.0 Pin-out Diagram

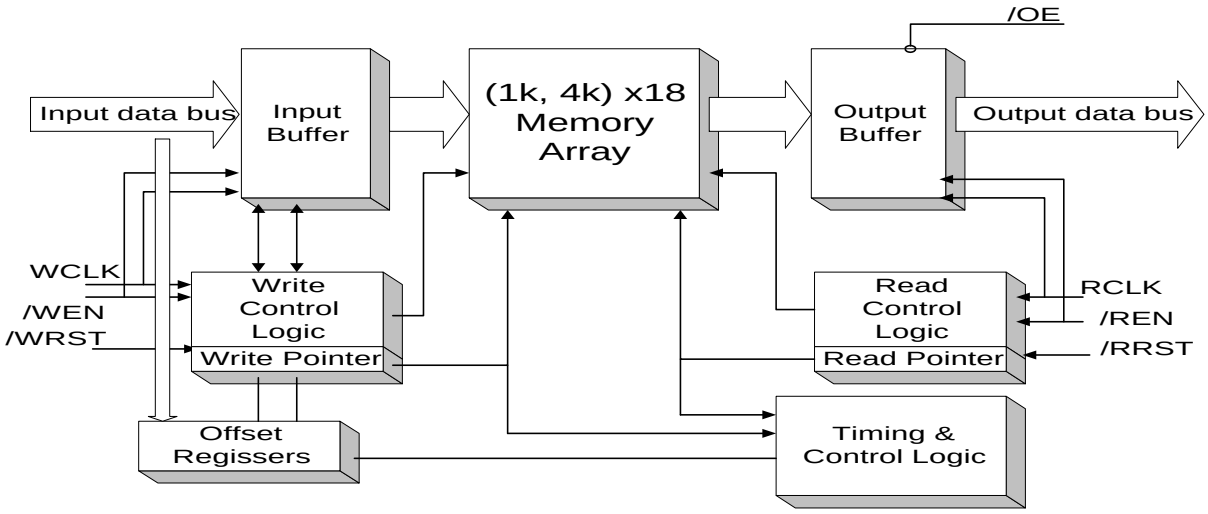
The AL4V183 and AL4V185 pin-out diagram is following:



STQFP PACKAGE TOP VIEW

Figure 1

6.0 Block Diagram



AL4V18x FIFO Block Diagram

Figure 2

The internal structure of the AL4V183 and AL4V185 consists of Input/Output buffers, Read/Write Control Logic and main (2k, 8k) x18 different configuration memory cell array and state-of-the-art logic design that takes care of addressing and controlling the read/write data.

7.0 Pin Definition and Description

The pin-out definition and function are described as following:

Write Bus Signals

Pin Symbol	Pin name	Pin number	I/O Typ	Description
D[17:0]	Data Inputs	63,64, [1:16]	I	18-bit or 9-bit Input data bus. During Reset, if IW is LOW, the Input port will be configured to 18-bit mode and D17 ~ D0 are used. If IW is HIGH, the Input port will be configured to 9-bit mode and D8 ~ D0 are used.
/WEN	Write Enable	20	I	/WEN is an input signal that controls the 18bit input data write and write pointer operation.
WCLK	Write Clock	19	I	Data is written into the FIFO on a rising edge of WCLK when the Write Enable(s) are asserted.
/WRST	Write Reset	17	I	The /WRSTB is a reset input signal that resets the write address pointer to 0.

Read Bus Signals

Pin symbol	Pin name	Pin number	I/O typ	Description
Q[17:0]	Data Outputs	53,52,50,48,47,45,44,42,41,39,38,37,36,34,32,31,29,28	O	18-bit or 9-bit Output data bus. During Reset, if OW is LOW, the Output port will be configured to 18-bit mode and Q17 ~ Q0 are used. If IW is HIGH, the Output port will be configured to 9-bit mode and Q8 ~ Q0 are used.
/REN	Read Enable	60	I	When /REN is LOW, data is read from the FIFO on every rising edge of RCLK. When /REN is HIGH, the output register holds the previous data.
/OE	Output Enable	58	I	When /OE is LOW, the data output bus is active. If /OE is HIGH, the output data bus will be in high-impedance.
RCLK	Read Clock	61	I	Data is read from the FIFO on a rising edge of RCLK when /REN is LOW.
/RRST	Read Reset	59	I	The /RRST is a reset input signal that resets the read address pointer to 0.

Miscellaneous Signals

Pin Symbol	Pin name	Pin number	I/O typ	Description

/RS	Reset	57	I	The global reset pin /RS will automatically initialize chip logic.
/BEB	Big-Endian /Little-Endian	18	I	During Reset, a LOW on /BEB will select Big-Endian operation. A HIGH on /BEB during Reset will select Little-Endian format
IW	Input Bus Width	21	I	This pin is to configure the bus width of the write port. During Reset, the write port will be configured to x18 bus width if IW is LOW and to x9 bus width if IW is HIGH.
OW	Output Bus Width	24	I	This pin is to configure the bus width of the read port. During Reset, the read port will be configured to x18 bus width if OW is LOW and to x9 bus width if OW is HIGH.

Power/Ground Signals

Pin Symbol	Pin name	Pin number	I/O typ	Description
VCC	Power	22,33,43,56	-	3.3V ± 10% power supply
GND	Ground	30,35,40,46,51,55,62	-	Ground.
NC	-	23, 25, 26, 27, 54	-	No Connect

8.0 Memory Operations

8.1 Inputs and Outputs

8.1.1 Data Input (D17 ~ D0)

D17 ~ D0 are 9-bit or 18-bit wide of input data port. During Reset, if IW is LOW, the Input port will be configured to 18-bit mode and D17 ~ D0 are used. If IW is HIGH, the Input port will be configured to 9-bit mode and D8 ~ D0 are used.

8.1.2 Data Output (Q17-Q0)

Q0-Q17 are data outputs for 18-bit wide data. During Reset, if OW is LOW, the Output port will be configured to 18-bit mode and Q17 ~ Q0 are used. If IW is HIGH, the Output port will be configured to 9-bit mode and Q8 ~ Q0 are used.

8.2 Controls

8.2.1 Reset (/RS)

Reset takes place when the Reset (/RS) input is LOW. During the system power on, a 200us negative pulse on /RS pin is required to initial internal logic after power-up. Apply a valid reset pulse to /WRSTB and /RRSTB after power-on-reset to reset read/write address pointer to zero.

8.2.2 Write Reset (/WRST) and Read Reset (/RRST)

The reset signal (/WRST or /RRST) can be given at any time to reset read or write address pointer regardless of the /WE, /RE and /OE status, however, it still need to meet the setup time and hold time requirements with reference to the clock input. When the reset signal is provided during disabled cycles, the reset operation is not executed until cycles are enabled again.

8.2.3 Write Clock (WCLK)

A write cycle is initiated on the rising edge of the Write Clock (WCLK). Data setup and hold times must be met with respect to the rising edge of WCLK. The Write and Read Clocks can be asynchronous or coincident.

8.2.4 Write Enable1 (/WEN)

When Write Enable (/WEN) is low, data can be written into the input register and memory array on the rising edge of every Write Clock (WCLK). Data is stored in the memory array sequentially and independently of any on going read operation. When Write Enable (/WEN) is HIGH, the input holds the previous data and no new data can be written into the memory array.

8.2.5 Read Clock (RCLK)

Data can be read on the outputs at the rising edge of the Read Clock (RCLK), when both Read Enable (/REN) and Output Enable (/OE) are set LOW. The Write and Read Clocks can be asynchronous or coincident.

8.2.6 Read Enable (/REN)

When Read Enables (/REN) is LOW, data is read from the memory array to the output register on the rising edge of the Read Clock (RCLK).

8.2.7 Output Enable (/OE)

When Output Enable (/OE) is enabled (LOW), the parallel output buffers receive data from the output register. When /OE is disabled (HIGH), the Q output data bus is in a high-impedance state.

8.2.8 Big-Endian/Little-Endian (/BEB)

During Reset, a LOW on /BEB will select Big-Endian operation. A HIGH on /BEB during Reset will select Little-Endian format. If Big-Endian mode is selected, the most significant byte of the word written into the FIFO will be read out of the FIFO first, followed by the least significant byte. If Little0Endian format is selected, the least significant byte of the word written into the FIFO will be read out first, followed by the most significant byte.

8.2.9 Input Bus Width (IW)

This pin is to configure the bus width of the write port. During Reset, the write port will be configured to x18 bus width if IW is LOW and to x9 bus width if IW is HIGH.

8.2.10 Output Bus Width (OW)

This pin is to configure the bus width of the read port. During Reset, the read port will be configured to x18 bus width if OW is LOW and to x9 bus width if OW is HIGH.

Table 1: Bus-Matching and Endian Support Configuration

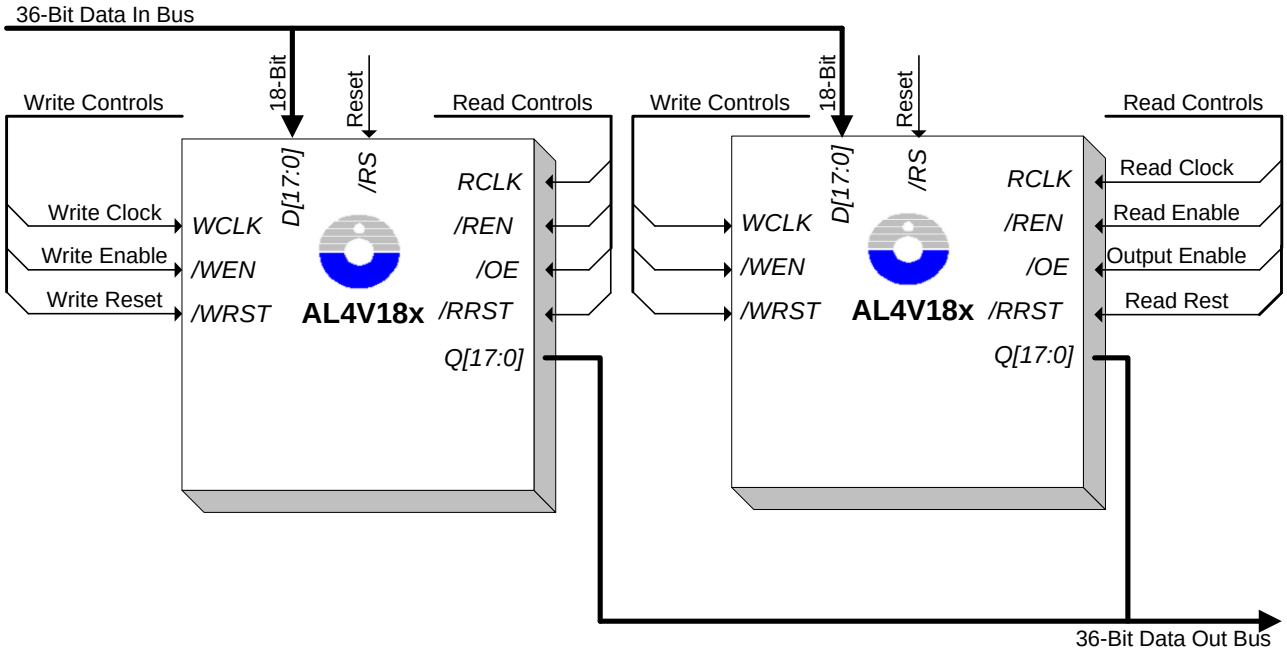
IW	OW	/BEB	Input Bus		Output		Configuration
			D17 ~ D9	D8 ~ D0	Q17 ~ Q9	Q8 ~ Q0	
L	L	L	A	B	A	B	x18 Input to x18 Output – Big Endian
L	L	H	A	B	B	A	x18 Input to x18 Output – Little Endian
L	H	L	A	B	X	A (1^{ST}) B (2^{ND})	x18 Input to x9 Output – Big Endian
L	H	H	A	B	X	B (1^{ST}) A (2^{ND})	x18 Input to x9 Output – Little Endian
H	L	L	X	A (1^{ST}) B (2^{ND})	A	B	x9 Input to x18 Output – Big Endian
H	L	H	X	A (1^{ST}) B (2^{ND})	B	A	x9 Input to x18 Output – Little Endian

Notes: In x9 in to x9 output configuration, Big-Endian/Little-Endian (/BEB) does not affect byte sequence.

9.0 Multiple Devices Bus Expansion

9.1 Width Expansion Configuration

Simply connecting the corresponding input controls signals of multiple devices may increase data bus width. Figure 3 shows an 36-bit word width data bus by using two AL4V183 or AL4V185s. Adding additional AL4V183 or AL4V185s can attain any word width expansion.



Multiple FIFO memory in bus width expansion configuration

Figure 3

10.0 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter		3.3V Rating	Unit
V_{DD}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Input Pin Voltage	-0.3 ~ + 5.5	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	°C
T_{stg}	Storage temperature	-40 ~ +125	°C

10.2 Recommended Operating Conditions

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
V_{DD}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{DD}		5.0	V
V_{IL}	Low Level Input Voltage	0		0.3 V_{DD}	V

10.3 DC Characteristics

(V_{DD} = 3.3V, Vss=0V. T_{AMB} = 0 to 70°C)

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
I_{DD}	Operating Current @20MHz	-	-	16	mA
I_{DDS}	Standby Current	-	1.8	5	mA
V_{OH}	Hi-level Output Voltage	2.4	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	V
I_{LI}	Input Leakage Current	-2	-	+2	µA
I_{LO}	Output Leakage Current	-10	-	+10	µA

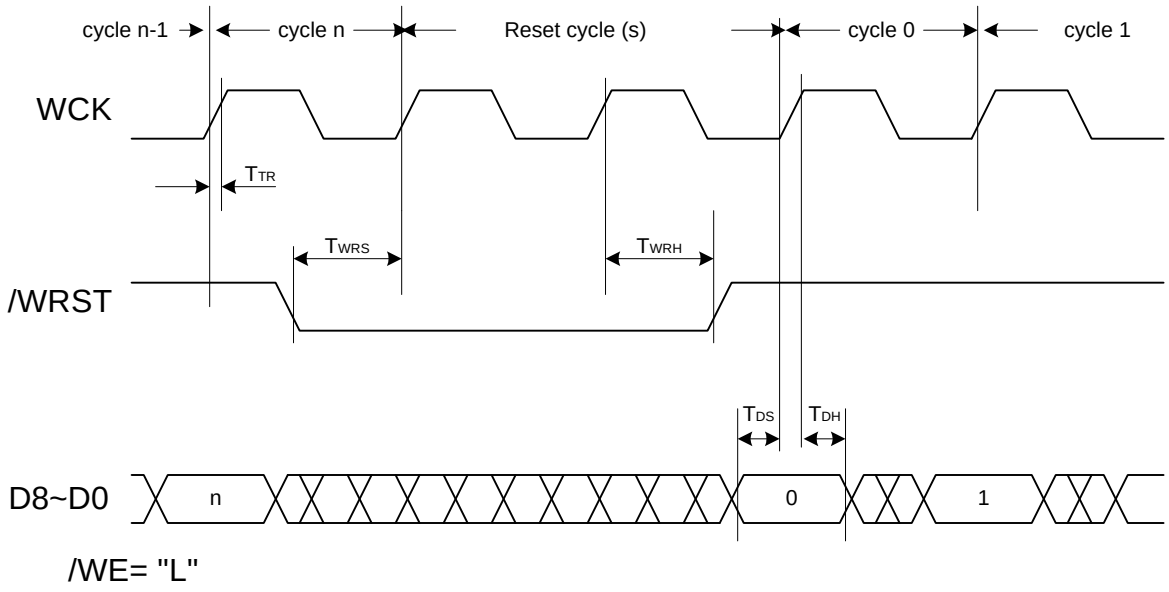
Note: The Operating Current is tested at RCLK=WCLK=20MHz and data inputs switch at 10MHz

10.4 AC Electrical Characteristics

(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

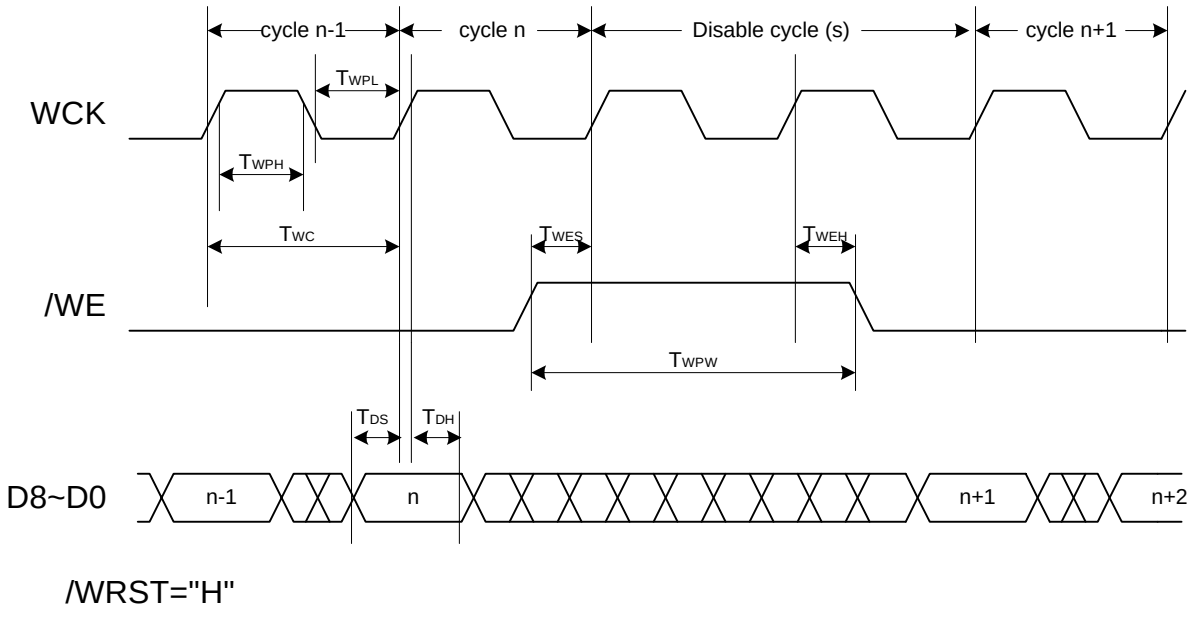
Parameter		100MHz		Unit
		Min	Max	
T_{WC}	WCK Cycle Time	10	-	ns
T_{WPH}	WCK High Pulse Width	3	-	ns
T_{WPL}	WCK Low Pulse Width	3	-	ns
T_{RC}	RCK Cycle Time	10	-	ns
T_{RPH}	RCK High Pulse Width	3	-	ns
T_{RPL}	RCK Low Pulse Width	3	-	ns
T_{AC}	Access Time	-	7.5	ns
T_{OH}	Output Hold Time	0.5	-	ns
T_{HZ}	Output High-Z Setup Time	2	-	ns
T_{LZ}	Output Low-Z Setup Time	2	-	ns
T_{WRS}	WRST Setup Time	3	-	ns
T_{WRH}	WRST Hold Time	0.5	-	ns
T_{RRS}	RRST Setup Time	3	-	ns
T_{RRH}	RRST Hold Time	0.5	-	ns
T_{DS}	Input Data Setup Time	3	-	ns
T_{DH}	Input Data Hold Time	0.5	-	ns
T_{WES}	WE Setup Time	3	-	ns
T_{WEH}	WE Hold Time	0.5	-	ns
T_{WPW}	WE Pulse Width	10	-	ns
T_{RES}	RE Setup Time	3	-	ns
T_{REH}	RE Hold Time	0.5	-	ns
T_{RPW}	RE Pulse Width	10	-	ns
T_{OES}	OE Setup Time	3	-	ns
T_{OEH}	OE Hold Time	0.5	-	ns
T_{OPW}	OE Pulse Width	10	-	ns
T_{TR}	Transition Time	2	-	ns

10.5 Timing Diagrams



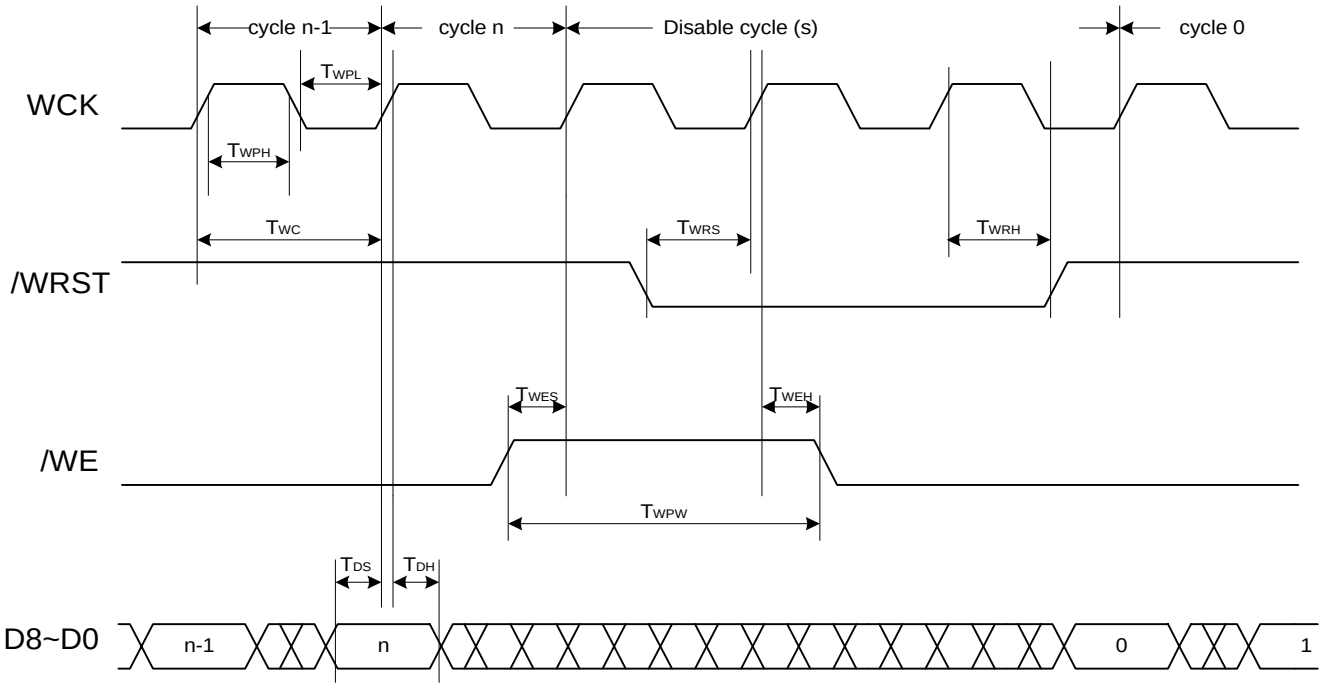
Write Cycle Timing (Write Reset)

Figure 4



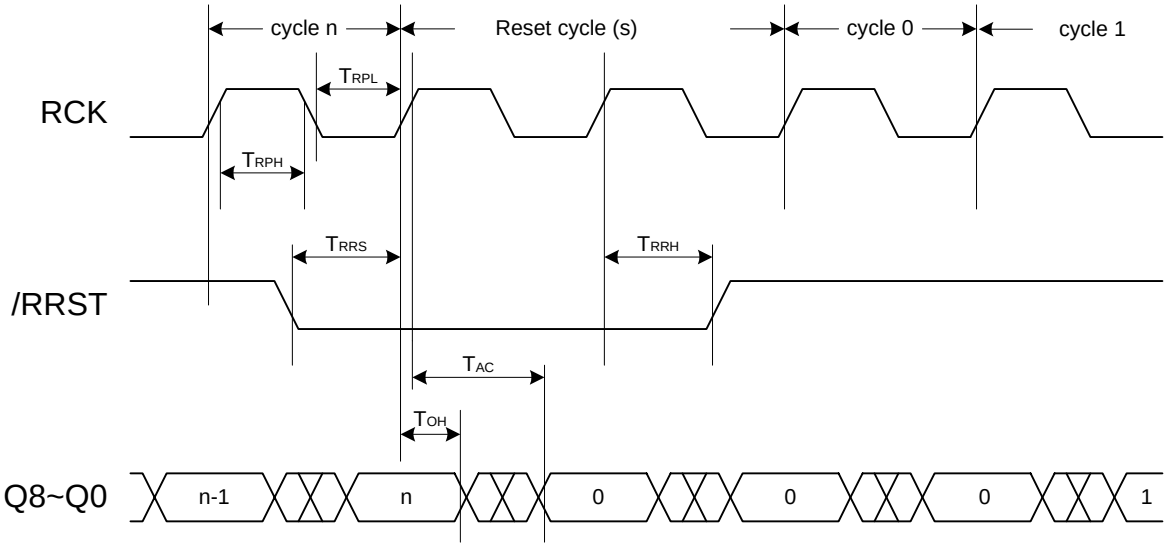
Write Cycle Timing (Write Enable)

Figure 5



Write Cycle Timing (/WE, /WRST)

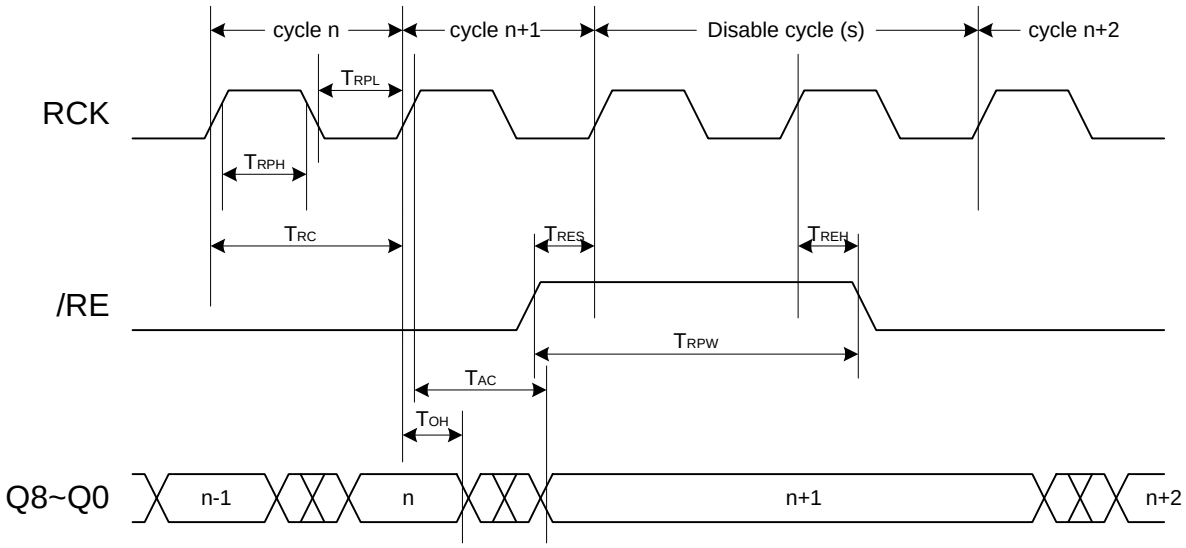
Figure 6



/RE= "L" ,/OE= "L"

Read Cycle Timing (Read Reset)

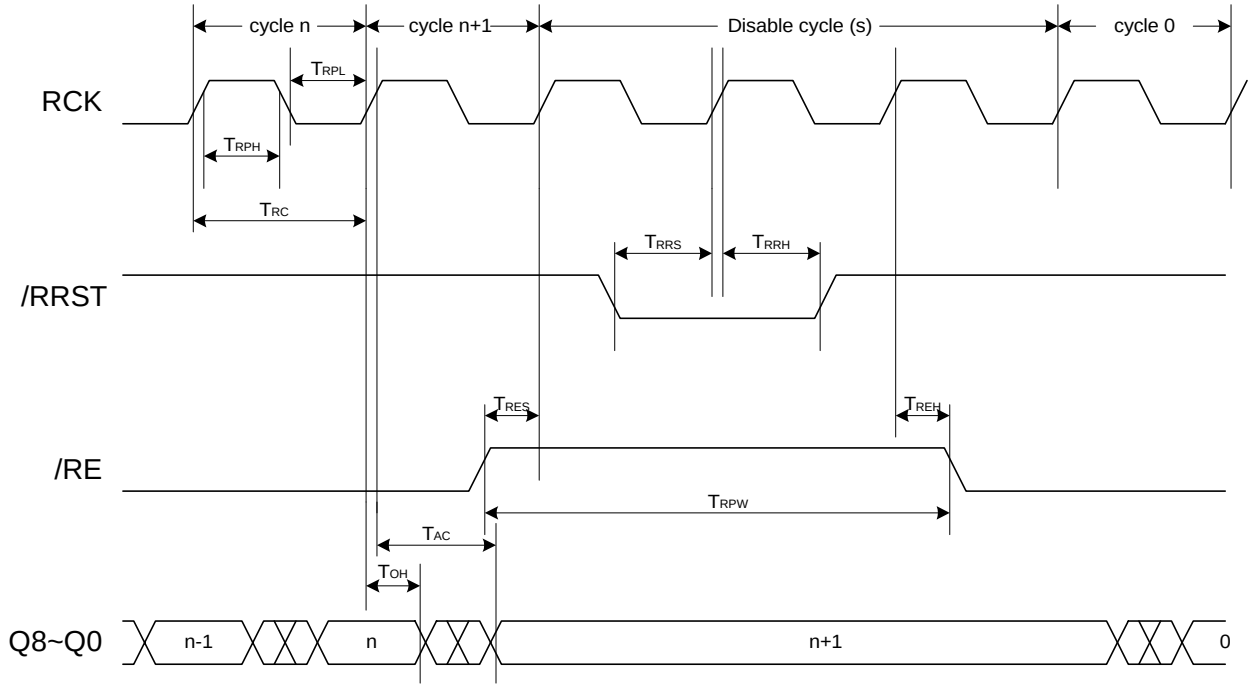
Figure 7



/OE="L" ,/RRST="H"

Read Cycle Timing (Read Enable)

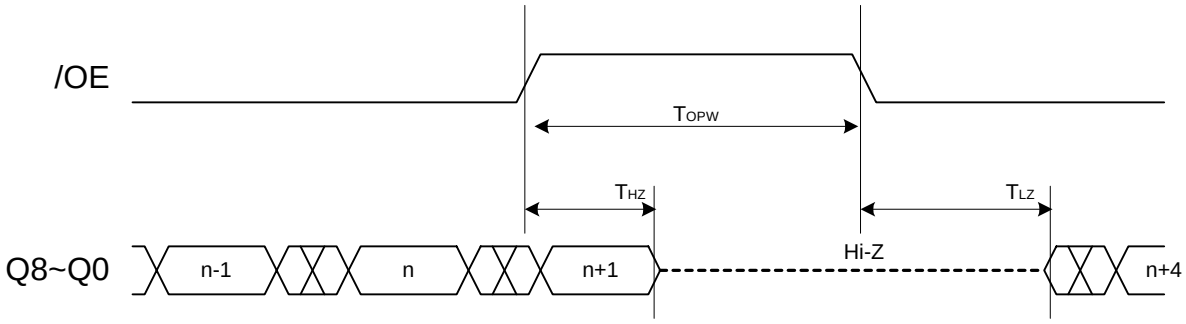
Figure 8



/OE="L"

Read Cycle Timing (/RE, /RRST)

Figure 9



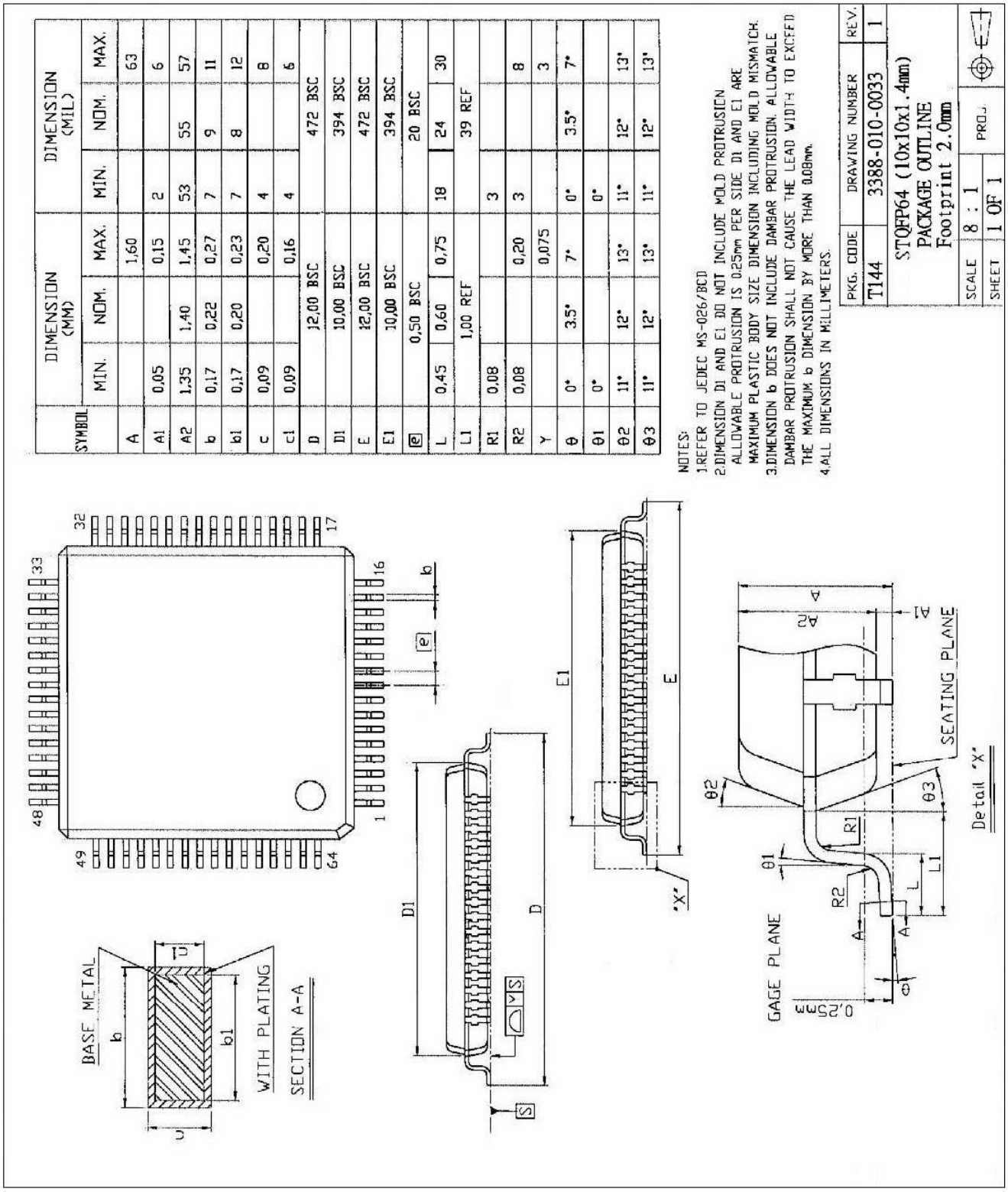
/RE="L" ,/RRST="H"

Read Cycle Timing (Output Enable)

Figure 10

11.0 Mechanical Drawing

11.1 10x10mm 64-Pin STQFP Package



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1,60			63
A1	0,05		0,15	2		6
A2	1,35	1,40	1,45	53	55	57
b	0,17	0,22	0,27	7	9	11
b1	0,17	0,20	0,23	7	8	12
c	0,09		0,20	4		8
c1	0,09		0,16	4		6
D		12,00 BSC			472 BSC	
D1		10,00 BSC			394 BSC	
E		12,00 BSC			472 BSC	
E1		10,00 BSC			394 BSC	
e		0,50 BSC			20 BSC	
L	0,45	0,60	0,75	18	24	30
L1		1,00 REF			39 REF	
R1	0,08			3		
R2	0,08		0,20	3		8
Y			0,075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTES:
1.REFER TO JEDEC MS-026/BCD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

PKG. CODE	DRAWING NUMBER	REV.
T144	3388-010-0033	1

STQFP64 (10x10x1.4mm)
PACKAGE OUTLINE
Footprint 2.0mm

SCALE 8 : 1 PROJ.
SHEET 1 OF 1

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