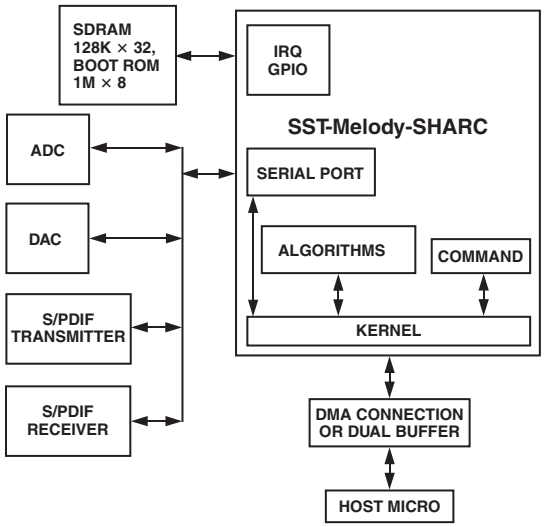
High End, Multichannel, 32-Bit Floating-Point Audio Processor

SST-Melody®-SHARC®

FEATURES

Super Harvard Architecture Computer (SHARC)
4 Independent Buses for Dual Data, Instruction, and I/O Fetch on a Single Cycle
32-Bit Fixed-Point Arithmetic; 32-Bit and 40-Bit Floating-Point Arithmetic
544 Kbits On-Chip SRAM Memory, Integrated I/O Peripheral I²S Support for 8 Simultaneous Receive and Transmit Channels
66 MIPS, 198 MFLOPS Peak, 132 MFLOPS Sustained Performance
User-Configurable 544 Kbits On-Chip SRAM Memory
2 External Port, DMA Channels and 8 Serial Port, DMA Channels
Decodes Industry Standard Formats Using a 32-Bit Floating Point Implementation for Decoding
Dolby® Digital AC-3, Dolby Digital EX Processing
Dolby Pro Logic®, 96 kHz, Dolby Pro Logic II
Dolby Headphone, Dolby 3/0
DTS® 5.1, DTS-ES®-Discreet 6.1, DTS Matrix and Matrix 3.0, DTS 96/24®, DTS NEO:6
THX® Ultra, Select, Ultra2, 5.1, 7.1, EX
SRS® Labs Circle Surround II™, Virtual Loudspeaker
MPEG AAC, MPEG2 Decode, MPEG 2-Channel Decode
PCM, PCM 96 kHz
HDCD, MLP*
Delay 7.1, 96 kHz
Bass 7.1, 96 kHz, Bass/Treble 2 Channel
ADI Surround: Club, Music, and Stadium
AAC (LC), AAC (LC) 2 Channel, AAC MP
WaveSurround 5.1 Channel to Headphone, Stereo to Headphone, Channel to Loudspeaker, Stereo to Loudspeaker
Downsampling 96 kHz to 48 kHz (2-Channel)
3-Band Equalizer, 2-Channel
Encoders: AC-3 2-Channel Consumer Encoder
Single Chip DSP-Based Implementation of Digital Audio Algorithms
I²S Compatible Ports
Interface to External SDRAM

FUNCTIONAL BLOCK DIAGRAM



Easy Interfaces to Audio Codecs
96 kHz Processing
Supports Customer Specific Post Processing
Automatic Stream Detection and Code Loading
Easy to Use Software Architecture
Optimized Library of Routines
Host Communication Using 16-Bit Parallel Port or SPI Port
Highly Flexible Serial Ports
SRAM Interface for More Delay
Supports IEC60958 For Bit Streams
8-Channel Output Using TDM Codecs

APPLICATIONS

Home Theater AVR Systems
Automotive Audio Receivers
Video Game Consoles
DVD Players
Cable and Satellite Set-Top Boxes
Multimedia Audio/Video Gateways

GENERAL DESCRIPTION

The SST-Melody-SHARC family of powerful 32-bit Audio Processors from Analog Devices provides flexible solutions and delivers a host of features across high end and high fidelity audio systems to the AV receiver and DVD markets. It includes multichannel audio decoders, encoders, and post processors for digital audio designs using DSP chipsets in home theater systems and automotive audio receivers.

(continued on page 11)

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

SST-Melody-SHARC–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS[1]

Parameter		Test Conditions	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage		3.13	3.60	3.13	3.60	V
T_{CASE}	Case Operating Temperature		–40	+100	0	+85	°C
V_{IH}	High Level Input Voltage	@ V_{DD} = max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
V_{IL1}	Low Level Input Voltage[2]	@ V_{DD} = min	–0.5	+0.8	–0.5	+0.8	V
V_{IL2}	Low Level Input Voltage[3]	@ V_{DD} = min	–0.5	+0.7	–0.5	+0.7	V

NOTES
[1]See Environmental Conditions section for information on thermal specifications.
[2]Applies to input and bidirectional pins: DATA31–0, ADDR23–0, BSEL, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG11–0, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR2–1}$, $\overline{ID2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0A, DR1A, DR0B, DR1B, TCLK0, TCLK1, RCLK0, RCLK1, $\overline{RESET}$, $\overline{TRST}$, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{SDCKE}$.
[3]Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	C and K Grades Min	C and K Grades Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DD} = min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DD} = min, I_{OL} = +4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[4]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[5, 6, 7, 8]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[5]	@ V_{DD} = max, V_{IN} = 0 V		8	µA
I_{OZLS}	Three-State Leakage Current[6]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{OZLA}	Three-State Leakage Current[9]	@ V_{DD} = max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}	Three-State Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		4	mA
I_{OZLC}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V		1.5	mA
C_{IN}	Input Capacitance[10, 11]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		8	pF

NOTES
[1]Applies to output and bidirectional pins: DATA31–0, ADDR 23–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, FLAG11–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR2–1}$, $\overline{CPA}$, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, DT0A, DT1A, DT0B, DT1B, XTAL, $\overline{BMS}$, TDO, $\overline{EMU}$, BMSTR, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10.
[2]See Output Drive Current section for typical drive current capabilities.
[3]Applies to input pins: ACK, $\overline{SBTS}$, IRQ2–0, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID1–0, BSEL, CLKIN, $\overline{RESET}$, TCK (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID1–0 = 01 and another SST-Melody-SHARC is not requesting bus mastership).
[4]Applies to input pins with internal pull-ups: DR0A, DR1A, DR0B, DR1B, $\overline{TRST}$, TMS, TDI.
[5]Applies to three-statable pins: DATA31–0, ADDR 23–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, FLAG11–0, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, TDO, $\overline{RAS}$, $\overline{CAS}$, DQM, $\overline{SDWE}$, SDCLK0, SDCLK1, $\overline{SDCKE}$, SDA10, and $\overline{EMU}$ (note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID1–0 = 01 and another SST-Melody-SHARC is not requesting bus mastership).
[6]Applies to three-statable pins with internal pull-ups: DT0A, DT1A, DT0B, DT1B, TCLK0, TCLK1, RCLK0, RCLK1.
[7]Applies to $\overline{CPA}$ pin.
[8]Applies to ACK pin when pulled up.
[9]Applies to ACK pin when keeper latch enabled.
[10]Guaranteed but not tested.
[11]Applies to all signal pins.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 130°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 seconds) . . . . . 280°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

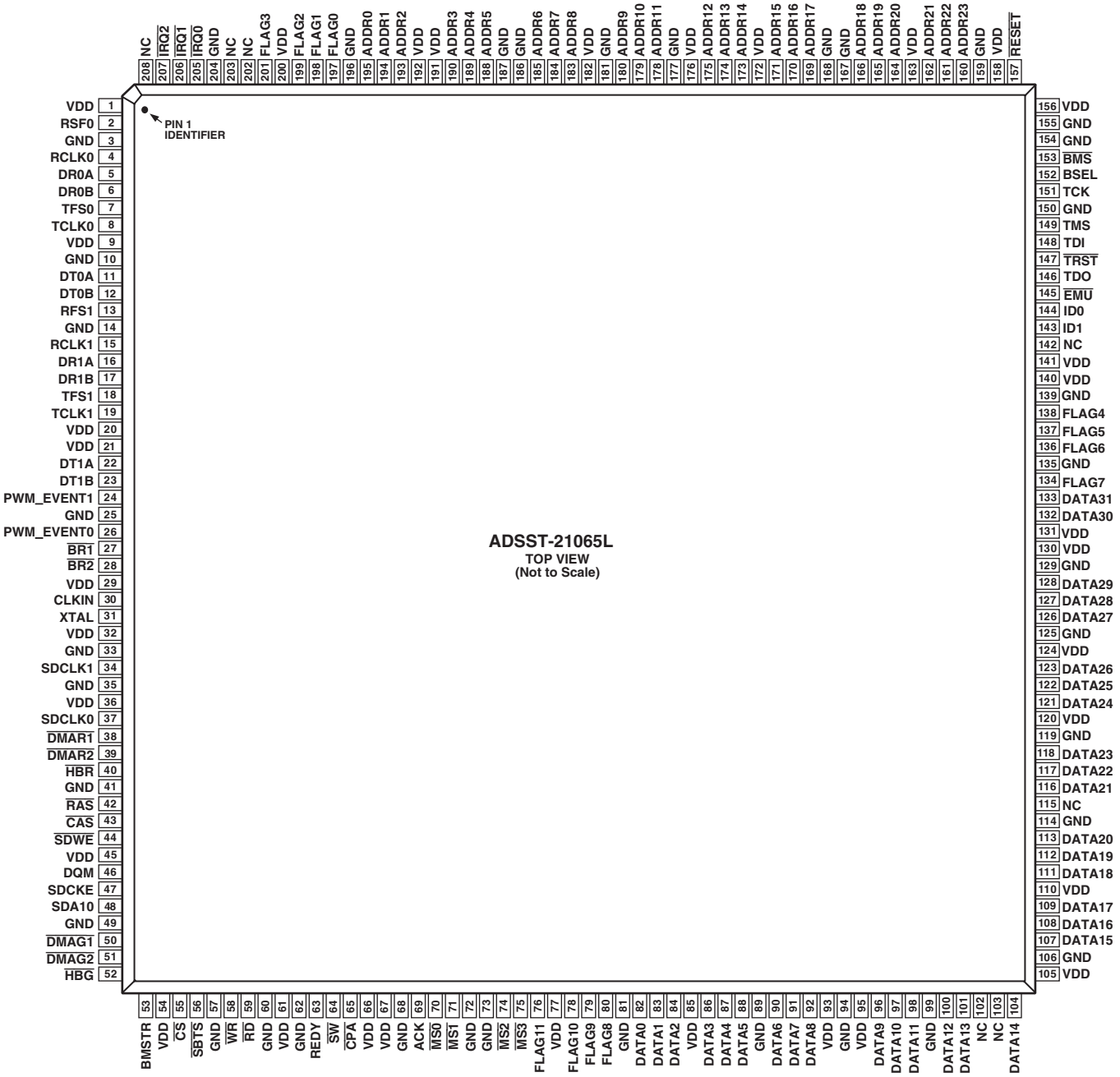
ORDERING GUIDE

Part Number	Case Temperature Range	Instruction Rate (MHz)	On-Chip SRAM (Kbit)	Operating Voltage (V)	Package Options
ADSST-21065LKS-240	0°C to 85°C	60	544	3.3	S-208-2
ADSST-21065LCS-240	–40°C to +100°C	60	544	3.3	S-208-2
ADSST-21065LKCA-240	0°C to 85°C	60	544	3.3	BC-196
ADSST-21065LKS-264	0°C to 85°C	66	544	3.3	S-208-2
ADSST-21065LKCA-264	0°C to 85°C	66	544	3.3	BC-196

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SST-Melody-SHARC features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

208-LEAD MQFP PIN CONFIGURATIONS



NC = NO CONNECT

196-BALL CSPBGA PIN CONFIGURATION

14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC7	NC8	ADDR18	ADDR17	ADDR14	ADDR11	ADDR8	ADDR7	ADDR6	ADDR3	ADDR0	FLAG2	NC2	NC1	A
TCK	GND	ADDR23	ADDR21	ADDR19	ADDR15	ADDR12	ADDR9	ADDR5	ADDR2	FLAG0	$\overline{\text{IRQ0}}$	RFS0	DR0A	B
TDO	BSEL	$\overline{\text{RESET}}$	ADDR22	ADDR20	ADDR16	ADDR13	ADDR10	ADDR4	ADDR1	FLAG3	$\overline{\text{IRQ2}}$	RCLK0	TCLK0	C
$\overline{\text{EMU}}$	$\overline{\text{TRST}}$	TMS	$\overline{\text{BMS}}$	VDD	VDD	VDD	VDD	VDD	FLAG1	$\overline{\text{IRQ1}}$	DR0B	TFS0	RCLK1	D
FLAG4	ID1	TDI	ID0	VDD	GND	GND	GND	GND	VDD	RFS1	DT0A	DT0B	TFS1	E
FLAG7	FLAG5	FLAG6	VDD	GND	GND	GND	GND	GND	GND	VDD	DR1A	DR1B	TCLK1	F
DATA29	DATA30	DATA31	VDD	GND	GND	GND	GND	GND	GND	VDD	DT1A	DT1B	PWM_ EVENT1	G
DATA26	DATA27	DATA28	VDD	GND	GND	GND	GND	GND	GND	VDD	$\overline{\text{BR2}}$	$\overline{\text{BR1}}$	PWM_ EVENT0	H
DATA23	DATA25	DATA24	VDD	GND	GND	GND	GND	GND	GND	VDD	SDCLK1	XTAL	CLKIN	J
DATA22	DATA20	DATA21	DATA19	VDD	GND	GND	GND	GND	VDD	$\overline{\text{SDWE}}$	$\overline{\text{HBR}}$	SDCLK0	$\overline{\text{DMAR1}}$	K
DATA18	DATA17	DATA16	DATA13	DATA8	VDD	VDD	VDD	VDD	VDD	$\overline{\text{DMAG2}}$	SDA10	$\overline{\text{CAS}}$	$\overline{\text{DMAR2}}$	L
DATA15	DATA14	DATA12	DATA9	DATA5	DATA2	FLAG10	ACK	$\overline{\text{CPA}}$	$\overline{\text{RD}}$	$\overline{\text{CS}}$	$\overline{\text{DMAG1}}$	SDCKE	$\overline{\text{RAS}}$	M
NC6	DATA11	DATA10	DATA7	DATA4	DATA1	FLAG11	$\overline{\text{MS1}}$	GND	REDY	$\overline{\text{SBTS}}$	BMSTR	$\overline{\text{HBG}}$	DQM	N
NC5	DATA6	DATA3	DATA0	FLAG8	FLAG9	$\overline{\text{MS3}}$	$\overline{\text{MS2}}$	$\overline{\text{MS0}}$	$\overline{\text{SW}}$	$\overline{\text{WR}}$	GND	NC4	NC3	P

208-LEAD MQFP PIN CONFIGURATION

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	V_{DD}	53	BMSTR	105	V_{DD}	157	$\overline{RESET}$
2	RFS0	54	V_{DD}	106	GND	158	V_{DD}
3	GND	55	$\overline{CS}$	107	DATA15	159	GND
4	RCLK0	56	$\overline{SBTS}$	108	DATA16	160	ADDR23
5	DR0A	57	GND	109	DATA17	161	ADDR22
6	DR0B	58	$\overline{WR}$	110	V_{DD}	162	ADDR21
7	TFS0	59	$\overline{RD}$	111	DATA18	163	V_{DD}
8	TCLK0	60	GND	112	DATA19	164	ADDR20
9	V_{DD}	61	V_{DD}	113	DATA20	165	ADDR19
10	GND	62	GND	114	GND	166	ADDR18
11	DT0A	63	REDY	115	NC	167	GND
12	DT0B	64	$\overline{SW}$	116	DATA21	168	GND
13	RFS1	65	$\overline{CPA}$	117	DATA22	169	ADDR17
14	GND	66	V_{DD}	118	DATA23	170	ADDR16
15	RCLK1	67	V_{DD}	119	GND	171	ADDR15
16	DR1A	68	GND	120	V_{DD}	172	V_{DD}
17	DR1B	69	ACK	121	DATA24	173	ADDR14
18	TFS1	70	$\overline{MS0}$	122	DATA25	174	ADDR13
19	TCLK1	71	$\overline{MS1}$	123	DATA26	175	ADDR12
20	V_{DD}	72	GND	124	V_{DD}	176	V_{DD}
21	V_{DD}	73	GND	125	GND	177	GND
22	DT1A	74	$\overline{MS2}$	126	DATA27	178	ADDR11
23	DT1B	75	$\overline{MS3}$	127	DATA28	179	ADDR10
24	PWM_EVENT1	76	FLAG11	128	DATA29	180	ADDR9
25	GND	77	V_{DD}	129	GND	181	GND
26	PWM_EVENT0	78	FLAG10	130	V_{DD}	182	V_{DD}
27	$\overline{BR1}$	79	FLAG9	131	V_{DD}	183	ADDR8
28	$\overline{BR2}$	80	FLAG8	132	DATA30	184	ADDR7
29	V_{DD}	81	GND	133	DATA31	185	ADDR6
30	CLKIN	82	DATA0	134	FLAG7	186	GND
31	XTAL	83	DATA1	135	GND	187	GND
32	V_{DD}	84	DATA2	136	FLAG6	188	ADDR5
33	GND	85	V_{DD}	137	FLAG5	189	ADDR4
34	SDCLK1	86	DATA3	138	FLAG4	190	ADDR3
35	GND	87	DATA4	139	GND	191	V_{DD}
36	V_{DD}	88	DATA5	140	V_{DD}	192	V_{DD}
37	SDCLK0	89	GND	141	V_{DD}	193	ADDR2
38	$\overline{DMAR1}$	90	DATA6	142	NC	194	ADDR1
39	$\overline{DMAR2}$	91	DATA7	143	ID1	195	ADDR0
40	$\overline{HBR}$	92	DATA8	144	ID0	196	GND
41	GND	93	V_{DD}	145	$\overline{EMU}$	197	FLAG0
42	$\overline{RAS}$	94	GND	146	TDO	198	FLAG1
43	$\overline{CAS}$	95	V_{DD}	147	$\overline{TRST}$	199	FLAG2
44	$\overline{SDWE}$	96	DATA9	148	TDI	200	V_{DD}
45	V_{DD}	97	DATA10	149	TMS	201	FLAG3
46	DQM	98	DATA11	150	GND	202	NC
47	SDCKE	99	GND	151	TCK	203	NC
48	SDA10	100	DATA12	152	BSEL	204	GND
49	GND	101	DATA13	153	$\overline{BMS}$	205	$\overline{IRQ0}$
50	$\overline{DMAG1}$	102	NC	154	GND	206	$\overline{IRQ1}$
51	$\overline{DMAG2}$	103	NC	155	GND	207	$\overline{IRQ2}$
52	$\overline{HBG}$	104	DATA14	156	V_{DD}	208	NC

196-BALL CSPBGA PIN CONFIGURATION

Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic
A1	NC1	B1	DR0A	C1	TCLK0	D1	RCLK1	E1	TFS1
A2	NC2	B2	RFS0	C2	RCLK0	D2	TFS0	E2	DT0B
A3	FLAG2	B3	$\overline{\text{IRQ0}}$	C3	$\overline{\text{IRQ2}}$	D3	DR0B	E3	DT0A
A4	ADDR0	B4	FLAG0	C4	FLAG3	D4	$\overline{\text{IRQ1}}$	E4	RFS1
A5	ADDR3	B5	ADDR2	C5	ADDR1	D5	FLAG1	E5	V_{DD}
A6	ADDR6	B6	ADDR5	C6	ADDR4	D6	V_{DD}	E6	GND
A7	ADDR7	B7	ADDR9	C7	ADDR10	D7	V_{DD}	E7	GND
A8	ADDR8	B8	ADDR12	C8	ADDR13	D8	V_{DD}	E8	GND
A9	ADDR11	B9	ADDR15	C9	ADDR16	D9	V_{DD}	E9	GND
A10	ADDR14	B10	ADDR19	C10	ADDR20	D10	V_{DD}	E10	V_{DD}
A11	ADDR17	B11	ADDR21	C11	ADDR22	D11	$\overline{\text{BMS}}$	E11	ID0
A12	ADDR18	B12	ADDR23	C12	$\overline{\text{RESET}}$	D12	TMS	E12	TDI
A13	NC8	B13	GND	C13	BSEL	D13	$\overline{\text{TRST}}$	E13	ID1
A14	NC7	B14	TCK	C14	TDO	D14	$\overline{\text{EMU}}$	E14	FLAG4
F1	TCLK1	G1	PWM_EVENT1	H1	PWM_EVENT0	J1	CLKIN	K1	$\overline{\text{DMAR1}}$
F2	DR1B	G2	DT1B	H2	$\overline{\text{BR1}}$	J2	XTAL	K2	SDCLK0
F3	DR1A	G3	DT1A	H3	$\overline{\text{BR2}}$	J3	SDCLK1	K3	$\overline{\text{HBR}}$
F4	V_{DD}	G4	V_{DD}	H4	V_{DD}	J4	V_{DD}	K4	$\overline{\text{SDWE}}$
F5	GND	G5	GND	H5	GND	J5	GND	K5	V_{DD}
F6	GND	G6	GND	H6	GND	J6	GND	K6	GND
F7	GND	G7	GND	H7	GND	J7	GND	K7	GND
F8	GND	G8	GND	H8	GND	J8	GND	K8	GND
F9	GND	G9	GND	H9	GND	J9	GND	K9	GND
F10	GND	G10	GND	H10	GND	J10	GND	K10	V_{DD}
F11	V_{DD}	G11	V_{DD}	H11	V_{DD}	J11	V_{DD}	K11	DATA19
F12	FLAG6	G12	DATA31	H12	DATA28	J12	DATA24	K12	DATA21
F13	FLAG5	G13	DATA30	H13	DATA27	J13	DATA25	K13	DATA20
F14	FLAG7	G14	DATA29	H14	DATA26	J14	DATA23	K14	DATA22
L1	$\overline{\text{DMAR2}}$	M1	$\overline{\text{RAS}}$	N1	DQM	P1	NC3		
L2	$\overline{\text{CAS}}$	M2	SDCKE	N2	$\overline{\text{HBG}}$	P2	NC4		
L3	SDA10	M3	$\overline{\text{DMAG1}}$	N3	BMSTR	P3	GND		
L4	$\overline{\text{DMAG2}}$	M4	$\overline{\text{CS}}$	N4	$\overline{\text{SBTS}}$	P4	$\overline{\text{WR}}$		
L5	V_{DD}	M5	$\overline{\text{RD}}$	N5	REDY	P5	$\overline{\text{SW}}$		
L6	V_{DD}	M6	$\overline{\text{CPA}}$	N6	GND	P6	$\overline{\text{MS0}}$		
L7	V_{DD}	M7	ACK	N7	$\overline{\text{MS1}}$	P7	$\overline{\text{MS2}}$		
L8	V_{DD}	M8	FLAG10	N8	FLAG11	P8	$\overline{\text{MS3}}$		
L9	V_{DD}	M9	DATA2	N9	DATA1	P9	FLAG9		
L10	DATA8	M10	DATA5	N10	DATA4	P10	FLAG8		
L11	DATA13	M11	DATA9	N11	DATA7	P11	DATA0		
L12	DATA16	M12	DATA12	N12	DATA10	P12	DATA3		
L13	DATA17	M13	DATA14	N13	DATA11	P13	DATA6		
L14	DATA18	M14	DATA15	N14	NC6	P14	NC5		

PIN FUNCTION DESCRIPTIONS

SST-Melody-SHARC pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR23–0, DATA31–0, FLAG11–0, SW, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTxX, DRxX, TCLKx, RCLKx, TMS, and TDI), which can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Mnemonic	Type	Function
ADDR23–0	I/O/T	External Bus Address. The SST-Melody-SHARC outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes of the IOP registers of the other SST-Melody-SHARC. The SST-Melody-SHARC inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers.
DATA31–0	I/O/T	External Bus Data. The SST-Melody-SHARC inputs and outputs data and instructions on these pins. The external databus transfers 32-bit, single-precision, floating-point data and 32-bit fixed-point data over bits 31-0. 16-Bit short word data is transferred over Bits 15-0 of the bus. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS3–0}}$	I/O/T	Memory Select Lines. These lines are asserted as chip selects for the corresponding banks of external memory. Internal $\text{ADDR}_{25–24}$ are decoded into $\overline{\text{MS3–0}}$. The $\overline{\text{MS3–0}}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{\text{MS3–0}}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. Additionally, an $\overline{\text{MS3–0}}$ line that is mapped to SDRAM may be asserted even when no SDRAM access is active. In a multiprocessor system, the $\overline{\text{MS3–0}}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	Memory Read Strobe. This pin is asserted when the SST-Melody-SHARC reads from external memory devices or from the IOP register of another SST-Melody-SHARC. External devices (including another SST-Melody-SHARC) must assert $\overline{\text{RD}}$ to read from the SST-Melody-SHARC's IOP registers. In a multiprocessor system, $\overline{\text{RD}}$ is output by the bus master and is input by another SST-Melody-SHARC.
$\overline{\text{WR}}$	I/O/T	Memory Write Strobe. This pin is asserted when the SST-Melody-SHARC writes to external memory devices or to the IOP register of another SST-Melody-SHARC. External devices must assert $\overline{\text{WR}}$ to write to the SST-Melody-SHARC's IOP registers. In a multiprocessor system, $\overline{\text{WR}}$ is output by the bus master and is input by the other SST-Melody-SHARC.
$\overline{\text{SW}}$	I/O/T	Synchronous Write Select. This signal interfaces the SST-Melody-SHARC to synchronous memory devices (including another SST-Melody-SHARC). The SST-Melody-SHARC asserts $\overline{\text{SW}}$ to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessor system, $\overline{\text{SW}}$ is output by the bus master and is input by the other SST-Melody-SHARC to determine if the multiprocessor access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output.
ACK	I/O/S	Memory Acknowledge. External devices can deassert ACK to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The SST-Melody-SHARC deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. In a multiprocessor system, a slave SST-Melody-SHARC deasserts the bus master's ACK input to add wait state(s) to an access of its IOP registers. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	Suspend Bus Three-State. External devices can assert $\overline{\text{SBTS}}$ to place the external bus address, data, selects, and strobes—but not SDRAM control pins—in a high impedance state for the following cycle. If the SST-Melody-SHARC attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not finish until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/SST-Melody-SHARC deadlock.
$\overline{\text{IRQ2–0}}$	I/A	Interrupt Request Lines. May be either edge-triggered or level-sensitive.
FLAG11–0	I/O/A	Flag Pins. Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
$\overline{\text{HBR}}$	I/A	Host Bus Request. Must be asserted by a host processor to request control of the SST-Melody-SHARC's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the SST-Melody- SHARC that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the SST-Melody-SHARC places the address, data, select, and strobe lines in a high impedance state. It does, however, continue to drive the SDRAM control pins. $\overline{\text{HBR}}$ has priority over all SST-Melody-SHARC bus requests ($\overline{\text{BR2–1}}$) in a multiprocessor system.

Mnemonic	Type	Function
$\overline{\text{HBG}}$	I/O	Host Bus Grant. Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted by the SST-Melody-SHARC until $\overline{\text{HBR}}$ is released. In a multiprocessor system, $\overline{\text{HBG}}$ is output by the SST-Melody-SHARC bus master.
$\overline{\text{CS}}$	I/A	Chip Select. Asserted by host processor to select the SST-Melody-SHARC.
REDY (O/D)	O	Host Bus Acknowledge. The SST-Melody-SHARC deasserts REDY to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{DMAR1}}$	I/A	DMA Request 1 (DMA Channel 9)
$\overline{\text{DMAR2}}$	I/A	DMA Request 2 (DMA Channel 8)
$\overline{\text{DMAG1}}$	O/T	DMA Grant 1 (DMA Channel 9)
$\overline{\text{DMAG2}}$	O/T	DMA Grant 2 (DMA Channel 8)
$\overline{\text{BR2–1}}$	I/O/S	Multiprocessing Bus Requests. Used by multiprocessing SST-Melody-SHARCs to arbitrate for bus mastership. An SST-Melody-SHARC drives its own $\overline{\text{BRx}}$ line (corresponding to the value of its ID2–0 inputs) only and monitors all others. In a uniprocessor system, tie both $\overline{\text{BRx}}$ pins to VDD.
ID1–0	I	Multiprocessing ID. Determines which multiprocessor bus request ($\overline{\text{BR1}}$ – $\overline{\text{BR2}}$) is used by SST-Melody-SHARC. ID = 01 corresponds to $\overline{\text{BR1}}$, ID = 10 corresponds to $\overline{\text{BR2}}$. ID = 00 in single-processor systems. These lines are a system configuration selection that should be hard-wired or changed only at reset.
$\overline{\text{CPA}}$ (O/D)	I/O	Core Priority Access. Asserting its $\overline{\text{CPA}}$ pin allows the core processor of an SST-Melody-SHARC bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{CPA}}$ is an open drain output that is connected to both SST-Melody-SHARCs in the system. The $\overline{\text{CPA}}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, leave the $\overline{\text{CPA}}$ pin unconnected.
DTxX	O	Data Transmit (Serial Ports 0, 1; Channels A, B). Each DTxX pin has a 50 kΩ internal pull-up resistor.
DRxX	I	Data Receive (Serial Ports 0, 1; Channels A, B). Each DRxX pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	Transmit Clock (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	Receive Clock (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pull-up resistor.
TFSx	I/O	Transmit Frame Sync (Serial Ports 0, 1)
RFSx	I/O	Receive Frame Sync (Serial Ports 0, 1)
BSEL	I	EPROM Boot Select. When BSEL is high , the SST-Melody-SHARC is configured for booting from an 8-bit EPROM. When BSEL is low, the BSEL and $\overline{\text{BMS}}$ inputs determine booting mode. See $\overline{\text{BMS}}$ for details. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMS}}$	I/O/T*	Boot Memory Select. Output: used as chip select for boot EPROM devices (when BSEL = 1). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. Input: When low, indicates that no booting will occur and that the SST-Melody-SHARC will begin executing instructions from external memory. See following table. This input is a system configuration selection that should be hardwired. BSEL BMS Booting Mode 1 Output EPROM (connect BMS to EPROM chip select). 0 1 (Input) Host processor (HBW [SYSCON] bit selects host bus width). 0 0 (Input) No booting. Processor executes from external memory.
CLKIN	I	Clock In. Used in conjunction with XTAL, configures the SST-Melody-SHARC to use either its internal clock generators or an external clock source. The external crystal should be rated at 1× frequency. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. The SST-Melody-SHARC's internal clock generator multiplies the 1× clock to generate 2× clock for its core and SDRAM. It drives 2× clock out on the SDCLKx pins for the SDRAM interface to use. See also SDCLKx. Connecting the 1× external clock to CLKIN while leaving XTAL unconnected configures the SST-Melody-SHARC to use the external clock source. The instruction cycle rate is equal to 2× CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESET}}$	I/A	Processor Reset. Resets the SST-Melody-SHARC to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted at power-up.

*Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).

PIN FUNCTION DESCRIPTIONS (continued)

Mnemonic	Type	Function
TCK	I	Test Clock (JTAG). Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the SST-Melody-SHARC. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	Emulation Status. Must be connected to the SST-Melody-SHARC EZ-ICE target board connector only.
BMSTR	O	Bus Master Output. In a multiprocessor system, indicates whether the SST-Melody-SHARC is current bus master of the shared external bus. The SST-Melody-SHARC drives BMSTR high only while it is the bus master. In a single-processor system (ID = 00), the processor drives this pin high.
$\overline{\text{CAS}}$	I/O/T	SDRAM Column Access Strobe. Provides the column address. In conjunction with $\overline{\text{RAS}}$, $\overline{\text{MSx}}$, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{RAS}}$	I/O/T	SDRAM Row Access Strobe. Provides the row address. In conjunction with $\overline{\text{CAS}}$, $\overline{\text{MSx}}$, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	I/O/T	SDRAM Write Enable. In conjunction with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{MSx}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	SDRAM Data Mask. In write mode, DQM has a latency of zero and is used to block write operations.
SDCLK1–0	I/O/S/T	SDRAM 2× Clock Output. In systems with multiple SDRAM devices connected in parallel, supports the corresponding increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	SDRAM Clock Enable. Enables and disables the CLK signal. For details, see the data sheet supplied with your SDRAM device.
SDA10	O/T	SDRAM A10 Pin. Enables applications to refresh an SDRAM in parallel with a host access.
$\overline{\text{XTAL}}$	O	Crystal Oscillator Terminal. Used in conjunction with CLKIN to enable the SST-Melody-SHARC's internal clock generator or to disable it to use an external clock source. See CLKIN.
PWM_EVENT1–0	I/O/A	PWM Output/Event Capture. In PWMOUT mode, is an output pin and functions as a timer counter. In WIDTH_CNT mode, is an input pin and functions as a pulse counter/event capture.
VDD	P	Power Supply; nominally 3.3 V dc (33 pins)
GND	G	Power Supply Return (37 pins)
NC		Do Not Connect. Reserved pins that must be left open and unconnected (7).

I = Input, S = Synchronous, P = Power Supply, (O/D) = Open Drain, O = Output, A = Asynchronous, G = Ground, (A/D) = Active Drive, T = Three-state (when $\overline{\text{SBTS}}$ is asserted, or when the SST-Melody-SHARC is a bus slave).

GENERAL DESCRIPTION *(continued from page 1)*

With 32-bit audio quality, the SST-Melody-SHARC audio processor auto-detects and decodes audio formats in real-time, enabling end users to enjoy a theater-quality audio experience in their homes.

The solutions can be customized to meet the exact requirements of the application. This audio DSP system allows designers to make value additions to product features working off the high end base functionality that they are provided with.

Evaluation boards, sample applications and all necessary software support (drivers, and so on) are available. The SST-Melody-SHARC enables OEMs to offer comprehensive and single chip solutions for advanced features in products for end users. SST-Melody-SHARC audio processors enable OEMs to produce high quality, low cost designs featuring decoder algorithms and post processors for DTS-ES Extended Surround (including both DTS-ES Discreet 6.1 and DTS-ES Matrix 6.1), DTS Neo:6, Dolby Digital, Dolby Digital EX, Dolby Pro Logic, Dolby Pro Logic II, Dolby Headphone, DDCE, THX and THX Surround EX, HDCD, MPEG1 Audio Layer 3 (also known as MP3), MPEG2 Audio, AAC, MLP, WaveSurround, SRS 3D Sound and Stereo. The audio processors also include audio encoders for DDCE, MPEG, and MP3.

The cost of development is reduced with the scalable family of code-compatible devices enabling common solutions across product lines. Field upgradeable products with programmable DSP and an optimized library of routines including Dolby and DTS suites, multichannel AAC and all others, along with the best development tools in the industry, reduce the time to market.

SST-Melody-SHARC is the comprehensive answer to the needs of the high end, high quality digital audio market. It delivers a realistic high fidelity audio experience along with a maximum number of features, across price points in the high end DVD markets.

HARDWARE ARCHITECTURE

Hardware architecture covers the interface between DSP and host microcontroller, command processing, data transfer in serial and parallel form, data buffer management, algorithm combinations, MIPS, and memory requirements that are provided.

The multichannel algorithms are implemented and tested on a demo board "PEGASUS II." This stand-alone board accepts compressed digital bit streams as serial input from LD/DVD/CD players or any stream generator and decodes in real time to generate a 2-channel or multichannel PCM stream. It has a microcontroller to scan a small keypad to give commands and select various options, and an LCD for status display.

The SST-Melody-SHARC family (SST-Melody-SHARC) hardware architecture can be broken up into four blocks:

- The Core Processor
- Dual-Ported SAAM
- External Port
- Input/Output Processor

The hardware architecture of the Melody SHARC is complex. It has four independent buses for dual data, one for instructions, and one for I/O fetch. Since the four buses are independent, multiple transactions take place in a single clock cycle. It has two external ports, DMA channels, and eight serial ports. It is a 0.35 µm technology IC operating at 3.3 V.

The SST-Melody-SHARC processor can be interfaced to external peripherals with relative ease. The communication between the SST-Melody-SHARC processor and a host microcontroller utilizes the SPI bus. The host microcontroller can be the master and the SST-Melody-SHARC processor can act as a slave. The peripherals can be controlled by the host microcontroller using the SPI bus. The communication is based on commands and parameters. Status information regarding the SST-Melody-SHARC decoding is periodically updated and made available to the host microcontroller.

The block diagram of the SST-Melody-SHARC illustrates the following architectural features:

- Computation units (ALU, multiplier, and shifter) with a shared data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- Timers with event capture modes
- On-chip, dual-ported SRAM
- External port for interfacing to off-chip memory and peripherals
- Host port and SDRAM interface
- DMA controller
- Enhanced serial ports
- JTAG test access port

We will use the Functional Block Diagram as our reference. We assume the SST-Melody-SHARC communicates with host micro using either direct DMA access or a dual buffer hardware mechanism. SST-Melody-SHARC has an on-chip memory buffer that is used for storing commands/parameters sent by the host to SST-Melody-SHARC and also status information from SST-Melody-SHARC to be sent to host micro. SST-Melody-SHARC has direct access to this memory buffer as it resides on-chip. Host micro has access to this memory using either direct DMA access or a dual buffer hardware mechanism.

There is a definite protocol for passing commands and obtaining status information. Once SST-Melody-SHARC receives a command from host micro, it will process the same and inform host micro of the status. These commands initiate actions like encoding and decoding. Encoding and decoding will result in data processing and the processed data may be delivered over the serial port. For example, while encoding, the PCM data is accepted through the serial port from peripherals like an ADC or S/PDIF receiver. The PCM data is then encoded and stored in an on-chip compressed data buffer. These compressed frames are then accessible to host micro using a high speed DMA or USB port. SST-Melody-SHARC, will prepare the compressed frames in the form of IEC 958 format so that it can be sent out using the serial port or S/PDIF transmitter. Compressed frames can be downloaded by host micro to SST-Melody-SHARC and can be decoded and the resulting PCM data can be sent on serial port transmitter. While commands and data are transferred between host micro and SST-Melody-SHARC over a dual buffer/DMA we need the help of interrupts and a few general-purpose input/output lines to provide reliable communication.

SOFTWARE ARCHITECTURE

The audio DSP chipsets from Analog Devices allows designers to make value additions to product features working off the high end base functionality that they are provided with. The SST-Melody-SHARC software has the following parts:

- Executive kernel
- Algorithm as library module

The executive kernel has the following functions:

- Power up hardware initialization
- Serial port management
- Automatic stream detect
- Automatic code load
- Command processing
- Interrupt handling
- Data buffer management
- Calling library module
- Status report

The executive kernel gets executed as soon as booting takes place. The hardware resources are initialized in the beginning. The command buffer and general-purpose programmable flag pins are initialized. Various data buffers and memory variables are initialized. Interrupts are programmed and enabled. Then, definite signatures are written "Command buffer" to inform the host that SST-Melody-SHARC is ready to receive the commands. Once commands are issued by host micro, they are executed and appropriate action takes place. Decoding is handled by issuing appropriate commands by host micro.

The kernel communicates with library module for a particular algorithm in a definite way. The details are found in the specific implementation documents. As the kernel is modular, it is easy to customize to different hardware platforms. Most of the time, the user needs to change the initialization code to suit the codec chosen.

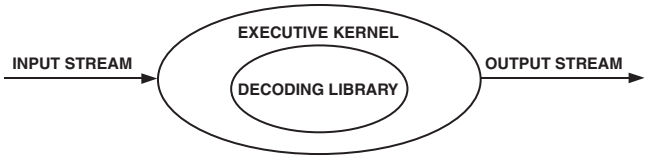


Figure 1. Software

SST-MELODY-SHARC GENERAL DESCRIPTION

The SST-Melody-SHARC is a powerful member of the SHARC family of 32-bit processors optimized for cost sensitive applications. The SHARC—Super Harvard Architecture—offers the highest levels of performance and memory integration of any 32-bit DSP in the industry—they are also the only DSPs in the industry that offer both fixed and floating-point capabilities without compromising precision or performance.

Fabricated in a high speed, low power CMOS process, 0.35 µm technology, the SST-Melody-SHARC offers the highest performance by a 32-bit DSP—66 MIPS (198 MFLOPS). With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table I lists the performance benchmarks for the SST-Melody-SHARC.

The SST-Melody-SHARC SHARC combines a floating-point DSP core with integrated, on-chip system features, including a 544 Kbit SRAM memory, host processor interface, DMA controller, SDRAM controller, and enhanced serial ports.

Table I. Performance Benchmarks

Benchmark	Timing	Cycles
Cycle Time	15.00 ns	1
1024-Pt Complex FFT (Radix 4, with Digit Reverse)	0.274 ns	18221
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	135 ns	9
[4 × 4] × [4 × 1]	240 ns	16
FIR Filter (per Tap)	15 ns	1
IIR Filter (per Biquad)	60 ns	4
Divide Y/X	90 ns	6
Inverse Square Root ($1/\sqrt{x}$)	135 ns	9
DMA Transfers	264 MBytes/sec	

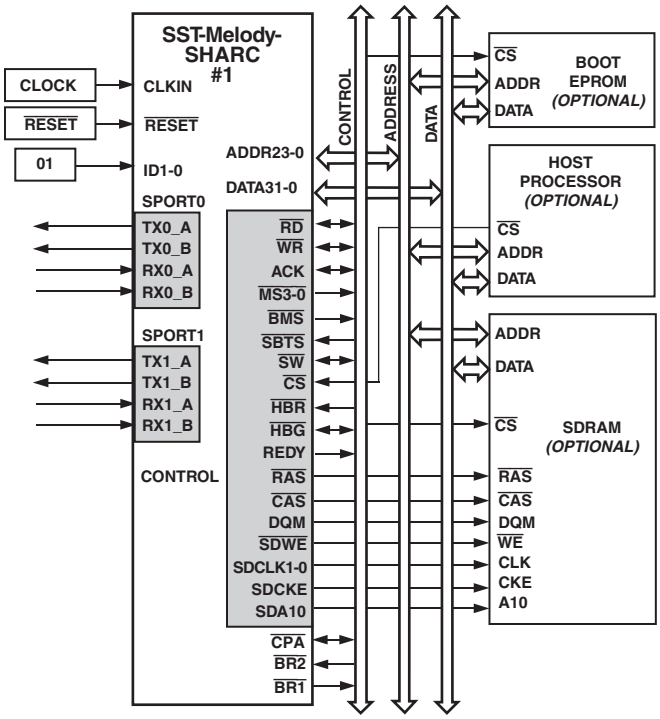


Figure 2. SST-Melody-SHARC Single-Processor System

Independent, Parallel Computation Units
The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File
A general-purpose data register file is used for transferring data between the computation units and the databuses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the SST-Melody-SHARC Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands
The SST-Melody-SHARC features an enhanced Super Harvard Architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data. With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache
The SST-Melody-SHARC includes an on-chip instruction cache that enables 3-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions that fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers
The SST-Melody-SHARC's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The SST-Melody-SHARC's two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set
The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the SST-Melody-SHARC can conditionally execute a multiply, an add, a subtract, and a branch all in a single instruction.

SST-MELODY-SHARC FEATURES

The SST-Melody-SHARC is designed to achieve the highest system throughput to enable maximum system performance. It can be clocked by either a crystal or a TTL-compatible clock signal. The SST-Melody-SHARC uses an input clock with a frequency equal to half the instruction rate—a 33 MHz input clock yields a 15 ns processor cycle (which is equivalent to 66 MHz). Interfaces on the SST-Melody-SHARC operate as shown. Hereafter in this document, 1× = input clock frequency and 2× = processor's instruction rate.

The following clock operation ratings are based on 1× = 33 MHz (instruction rate/core = 66 MHz):

SDRAM	66 MHz
External SRAM	33 MHz
Serial Ports	33 MHz
Multiprocessing	33 MHz
Host (Asynchronous)	33 MHz

SST-Melody-SHARC adds the following architectural features:

Dual-Ported On-Chip Memory
The SST-Melody-SHARC contains 544 Kbits of on-chip SRAM organized into two banks: Bank 0 has 288 Kbits, and Bank 1 has 256 Kbits. Bank 0 is configured with nine columns of 2K × 16 bits, and Bank 1 is configured with eight columns of 2K × 16 bits. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the SST-Melody-SHARC Memory Map).

On the SST-Melody-SHARC, the memory can be configured as a maximum of 16K words of 32-bit data, 34K words for 16-bit data, 10K words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 544 Kbits. All the memory can be accessed as 16-bit, 32-bit, or 48-bit.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers. Using the DM and PM buses in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the SST-Melody-SHARC's external port.

Off-Chip Memory and Peripherals Interface
The SST-Melody-SHARC's external port provides the processor's interface to off-chip memory and peripherals. The 64 M-word's, off-chip address space is included in the SST-Melody-SHARC's unified address space. The separate on-chip buses—for program memory, data memory, and I/O—are multiplexed at the external port to create an external system bus with a single 24-bit address bus, four memory selects, and a single 32-bit databus. The on-chip Super Harvard Architecture provides 3-bus performance, while the off-chip unified address space gives flexibility to the designer.

SDRAM Interface
The SDRAM interface enables the SST-Melody-SHARC to transfer data to and from synchronous DRAM (SDRAM) at 2× clock frequency. The synchronous approach coupled with 2× clock frequency supports data transfer at a high throughput—up to 220 Mbytes/sec.

The SDRAM interface provides a glueless interface with standard SDRAMs—16 Mbyte, 64 Mbyte, and 128 Mbyte—and includes options to support additional buffers between the SST-Melody-SHARC and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the SST-Melody-SHARC's four external memory banks.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The SST-Melody-SHARC supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Host Processor Interface
The SST-Melody-SHARC's host interface provides easy connection to standard microprocessor buses—8-, 16-, and 32-bit—requiring little additional hardware. Supporting asynchronous transfers at speeds up to 1× clock frequency, the host interface is accessed through the SST-Melody-SHARC's external port. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the SST-Melody-SHARC's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the IOP registers of the SST-Melody-SHARC and can access the DMA channel setup and mailbox registers. Vector interrupt support enables efficient execution of host commands.

DMA Controller
The SST-Melody-SHARC's on-chip DMA controller allows zero-overhead, nonintrusive data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the SST-Melody-SHARC's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the SST-Melody-SHARC's internal memory and its serial ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit internal words is performed during DMA transfers.

Ten channels of DMA are available on the SST-Melody-SHARC—eight via the serial ports, and two via the processor's external port (for either host processor, other SST-Melody-SHARC, memory or I/O transfers). Programs can be downloaded to the SST-Melody-SHARC using DMA transfers.

Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR1–2}}$, $\overline{\text{DMAG1–2}}$). Other DMA features include interrupt generation on completion of DMA transfers and DMA chaining for automatically linked DMA transfers.

Serial Ports
The SST-Melody-SHARC features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at 1× clock frequency, providing each with a maximum data rate of 33 Mbit/s. Each serial port has a primary and a secondary set of transmit and receive channels. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports supports three operation modes: DSP serial port mode, I^2S mode (an interface commonly used by audio codecs), and TDM (Time Division Multiplex) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with selectable word lengths of three bits to 32 bits. They offer selectable synchronization and transmit modes and optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and keymask features to enhance interprocessor communication.

Programmable Timers and General-Purpose I/O Ports
The SST-Melody-SHARC has two independent timer blocks, each of which performs two functions—Pulsewidth Generation and Pulse Count and Capture.

In Pulsewidth Generation mode, the SST-Melody-SHARC can generate a modulated waveform with an arbitrary pulsewidth within a maximum period of 71.5 secs.

In Pulse Counter mode, the SST-Melody-SHARC can measure either the high or low pulsewidth and the period of an input waveform.

The SST-Melody-SHARC also contains 12 programmable, general-purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting
The internal memory of the SST-Melody-SHARC can be booted at system power-up from an 8-bit EPROM, a host processor, or external memory. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (Boot Memory Select) and BSEL (EPROM Boot) pins. Either 8-, 16-, or 32-bit host processors can be used for booting. For details, see the descriptions of the $\overline{\text{BMS}}$ and BSEL pins in the Pin Function Descriptions section.

Multiprocessing
The SST-Melody-SHARC offers powerful features tailored to multiprocessing DSP systems. The unified address space allows direct interprocessor accesses of both SST-Melody-SHARC's IOP registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing a maximum of two SST-Melody-SHARCs and a host processor. Master processor changeover incurs only one cycle of overhead. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 132 MBytes/s over the external port.

POWER DISSIPATION

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note SHARC Power Dissipation Measurements.

Specifications are based on the following operating scenarios:

Table II. Internal Current Measurements

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate *power consumption* for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE16 \times I_{DDIDLE16} = \text{Power Consumption}$$

Table III. Internal Current Measurement Scenarios

Parameter		Test Conditions	Max	Unit
$I_{DDINPEAK}$	Supply Current (Internal)[1]	t_{CK} = 33 ns, V_{DD} = max	470	mA
		t_{CK} = 30 ns, V_{DD} = max	510	mA
$I_{DDINHIGH}$	Supply Current (Internal)[2]	t_{CK} = 33 ns, V_{DD} = max	275	mA
		t_{CK} = 30 ns, V_{DD} = max	300	mA
$I_{DDINLOW}$	Supply Current (Internal)[3]	t_{CK} = 33 ns, V_{DD} = max	240	mA
		t_{CK} = 30 ns, V_{DD} = max	260	mA
I_{DDIDLE}	Supply Current (IDLE)[4]	t_{CK} = 33 ns, V_{DD} = max	150	mA
		t_{CK} = 30 ns, V_{DD} = max	155	mA
$I_{DDIDLE16}$	Supply Current (IDLE16)[5]	V_{DD} = max	50	mA

NOTES

[1]The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2]$I_{DDINHIGH}$ is a composite average based on a range of high activity code.

[3]$I_{DDINLOW}$ is a composite average based on a range of low activity code.

[4]IDLE denotes SST-Melody-SHARC state during execution of IDLE instruction.

[5]IDLE16 denotes SST-Melody-SHARC state during execution of IDLE16 instruction.

OUTPUT DRIVE CURRENT

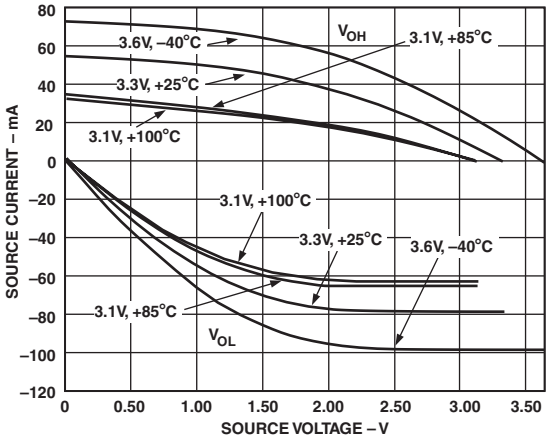


Figure 3. Typical Drive Currents

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 5. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 4. If multiple pins (such as the databus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the previous equation. Choose ΔV to be the difference between the SST-Melody-SHARC's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

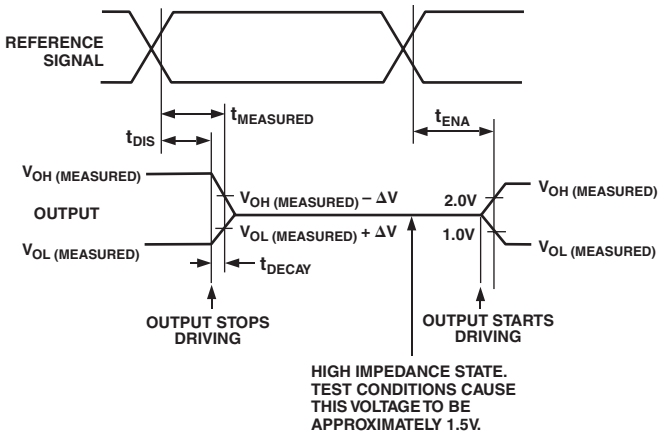


Figure 4. Output Enable

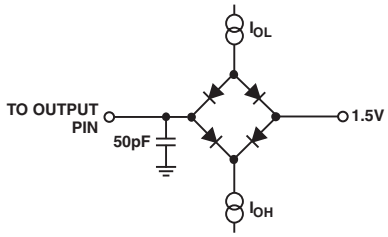


Figure 5. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 6. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins. The delay and hold specifications given should be derated by a factor of 1.8 ns/50 pF for loads other than the nominal value of 50 pF. Figure 7 and Figure 8 show how output rise time varies with capacitance. Figure 9 shows graphically how output delays and hold vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable time under Test Conditions.) The graphs of Figures 7, 8, and 9 may not be linear outside the ranges shown.

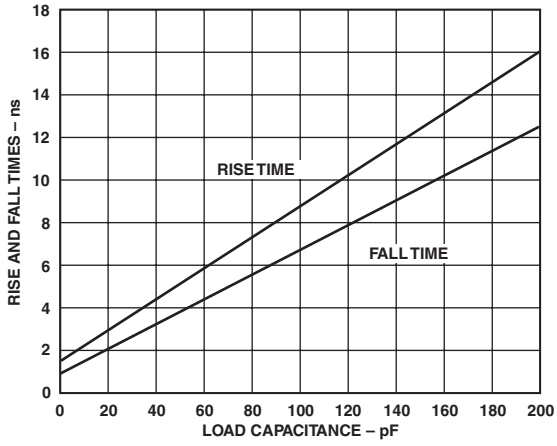


Figure 7. Typical Rise and Fall Time (10%–90% V_{DD})

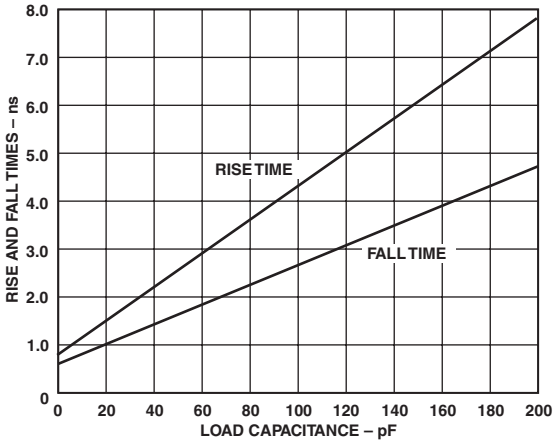


Figure 8. Typical Rise and Fall Time (0.8 V–2.0 V)

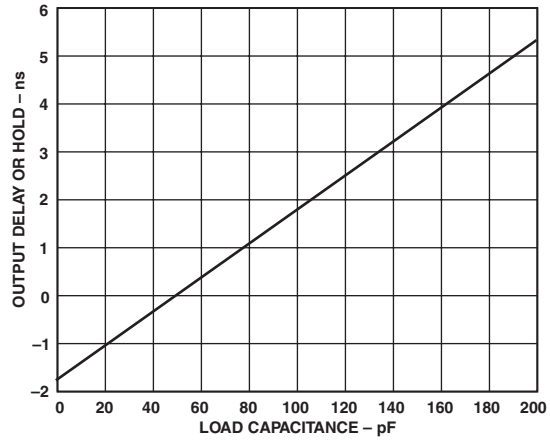


Figure 9. Typical Output Delay or Hold

Power Dissipation

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation depends on the sequence in which instructions execute and the data operands involved. See I_{DDIN} calculation in Electrical Characteristics section. Internal power dissipation is calculated this way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- Number of output pins that switch during each cycle (*O*)
- Maximum frequency at which the pins can switch (*f*)
- Load capacitance of the pins (*C*)
- Voltage swing of the pins (V_{DD})

The external component is calculated using:

$$P_{EXT} = O \times C \times V_{DD}^{2} \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The frequency *f* includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/t_{CK}$ while in SDRAM burst mode.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external memory (32-bit)
- Two 1 M × 16 SDRAM chips, each with a control signal load of 3 pF and a data signal load of 4 pF
- External data writes occur in burst mode, two every $1/t_{CK}$ cycles, a potential frequency of $1/t_{CK}$ cycles/s. Assume 50% pin switching
- The external SDRAM clock rate is 60 MHz ($2/t_{CK}$)

The P_{EXT} equation is calculated for each class of pins that can drive:

Table IV. External Power Calculations

Pin Type	No. of Pins	% Switching	×C	×f (MHz)	$\times V_{DD}^2$(V)	= P_{EXT} (W)
Address	11	50	10.7	30	10.9	0.019
$\overline{MS0}$	1	0	10.7	–	10.9	0.000
$\overline{SDWE}$	1	0	10.7	–	10.9	0.000
Data	32	50	7.7	30	10.9	0.042
SDRAM CLK	1		10.7	30	10.9	0.007
						P_{EXT} = 0.068 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation (I_{DDIN}, see calculation in Electrical Characteristics section):

$$P_{TOTAL} = P_{EXT} + \left(I_{DDIN} \times V_{DD}\right)$$

Note that the conditions causing a worst-case P_{EXT} differ from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones (1s) to all zeros (0s). Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The SST-Melody-SHARC is offered in a 208-lead MQFP and a 196-ball Mini-BGA package.

The SST-Melody-SHARC is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an air flow source may be used.

$$T_{CASE} = T_{AMB} + \left(PD \times \theta_{CA}\right)$$

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power Dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation)

θ_{JC} = 7.1°C/W for 208-lead MQFP

θ_{JC} = 5.1°C/W for 196-ball Mini-BGA

Airflow

Table V. Thermal Characteristics (208-Lead MQFP)

(Linear Ft/Min)	0	100	200	400	600
θ_{CA} (°C/W)	24	20	19	17	13

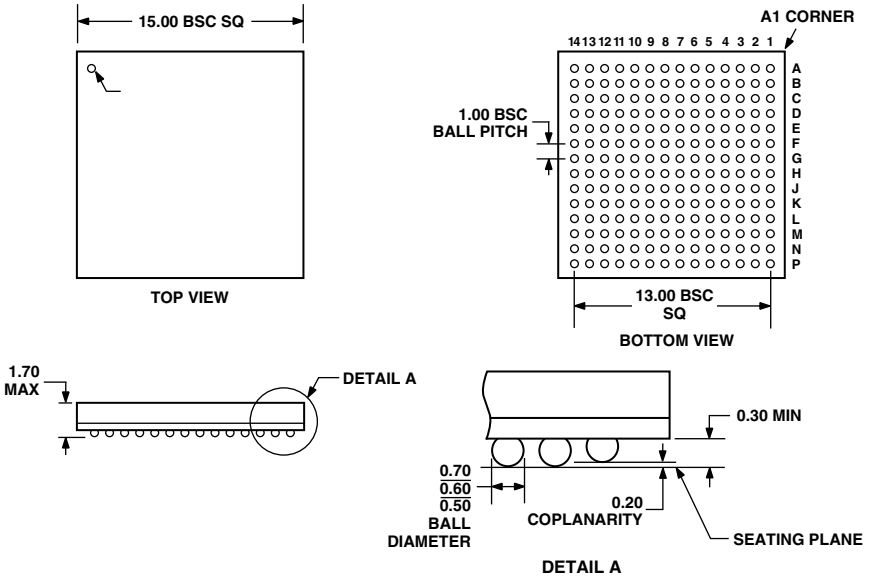
Table VI. 196-Ball Mini-BGA

(Linear Ft/Min)	0	200	400
θ_{CA} (°C/W)	38	29	23

OUTLINE DIMENSIONS

196-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-196)

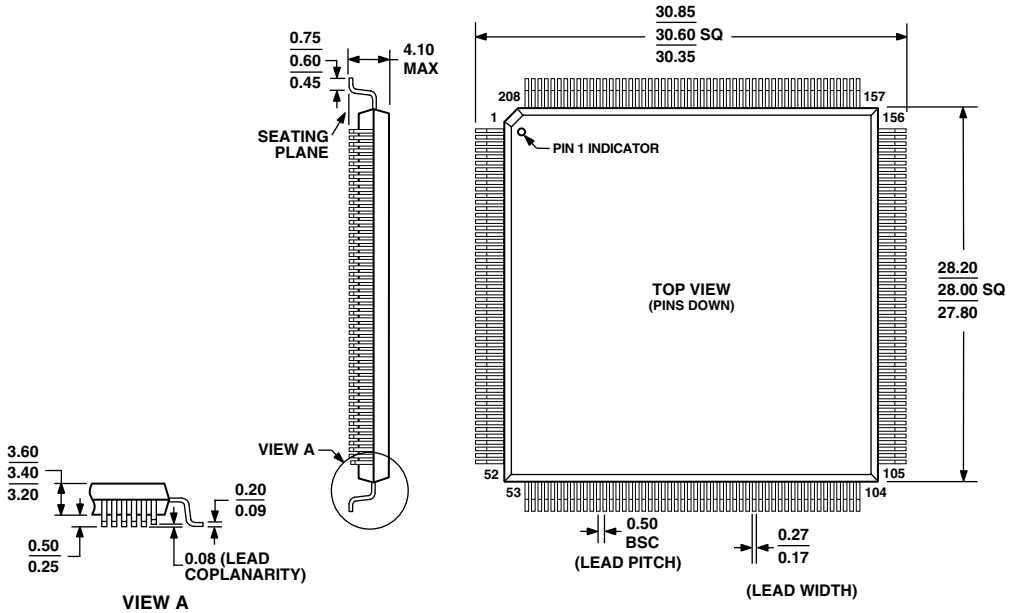
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-192AAE-1

208-Lead Plastic Quad Flatpack Package [MQFP]
(S-208-2)

Dimensions shown in millimeters



NOTES:
1. THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.
2. CENTER DIMENSIONS ARE NOMINAL.
3. DIMENSIONS ARE IN MILLIMETERS AND COMPLY WITH JEDEC STANDARD MS-029, FA-1.

C03052–0–10/02(0)

PRINTED IN U.S.A.