

## GENERAL DESCRIPTION

The AL2007LA is a Phase-Locked Loop (PLL) frequency synthesizer constructed in CMOS on single monolithic structure. The PLL macrofunctions provide frequency multiplication capabilities.

The output clock frequency  $F_{out}$  is related to the reference input clock frequency  $F_{in}$  by the following equation:

$$F_{out} = (m \cdot F_{in}) / (p \cdot 2^S)$$

Where,  $F_{out}$  is the output clock frequency.  $F_{in}$  is the reference input clock frequency.  $m, p$  and  $s$  are the values for programmable dividers. AL2007LA consists of a phase/Frequency Detector (PFD), a Charge Pump, an External Loop Filter, a Voltage Controlled Oscillator (VCO), a 6bit Pre-divider, an 8bit Main divider and 2bit Post Scaler as shown in Figure 1.

## FEATURES

- 0.35µm CMOS device technology
- 3.3 Volt Single power supply
- VCO frequency range: 60~170MHz
- Output frequency range: 20~170MHz
- Jitter  $\pm 150$ ps
- Duty ratio 40% to 60% at 170MHz
- Frequency changed by programmable divider
- Power down mode

### IMPORTANT NOTICE

Please contact SEC application engineer to confirm the proper selection of M,P,S value.

## FUNCTIONAL BLOCK DIAGRAM

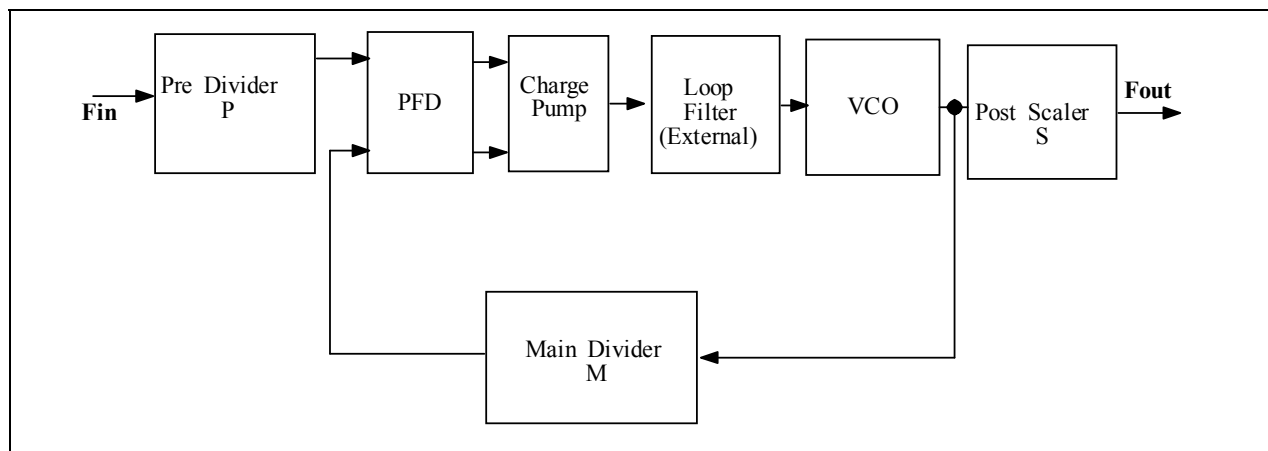


Figure 1. Phase Lockd Loop Block Diagram

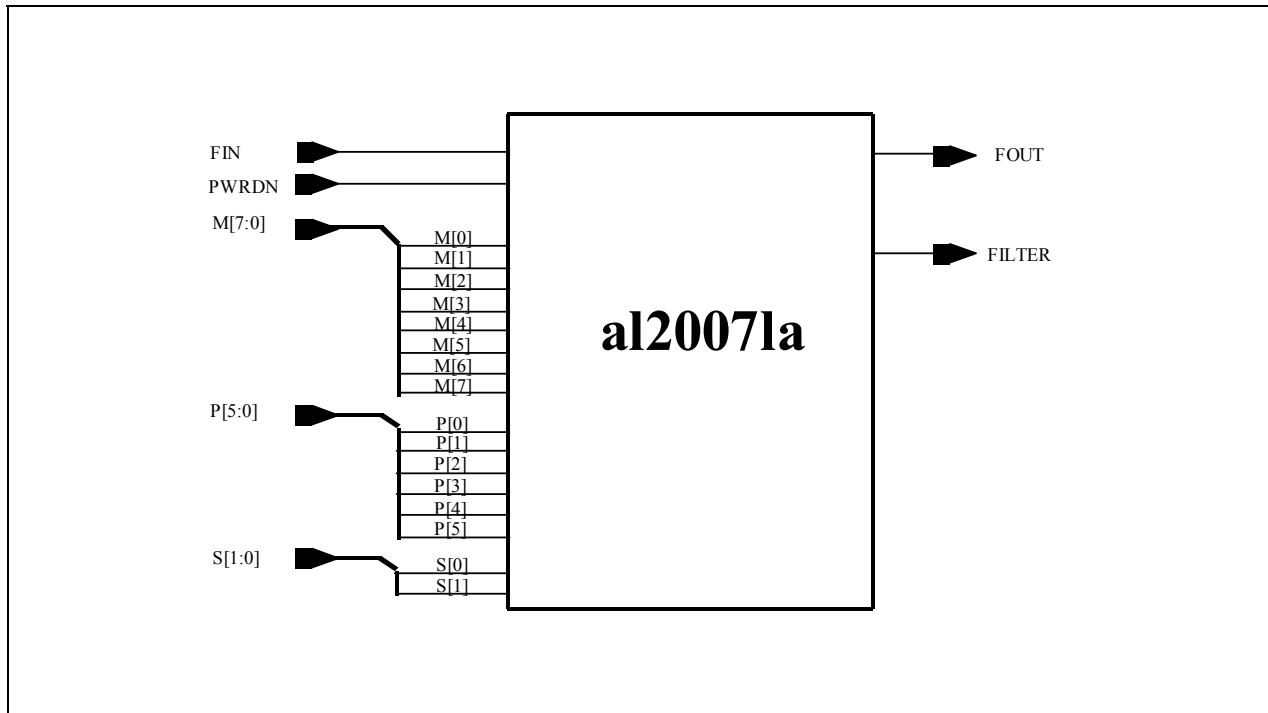
**CORE PIN DESCRIPTION**

Name	I/O Type	I/O Pad	Pin Description
VDD	DP	vddd	Digital power supply
VSS	DG	vssd	Digital ground
VDDA	AP	vdda	Analog power supply
VSSA	AG	vssa	Analog ground
VBB	AB/DB	vbba	Analog/Digital sub bias Power
FIN	DI	picc_bb	PLL clock input
FILTER	AO	poar50_bb	- Pump out is connected to Filter - A capacitor is connected between the pin and analog ground
FOUT	DO	pot12_bb	20MHz~170MHz clock output
PWRDN	DI	picc_bb	FSPLL clock power down. - PWRDN is High, PLL do not operating under this condition. - If isn't used this pin, tied to VSS.
P[5:0]	DI	picc_bb	The values for 6bit programmable pre-divider.
M[7:0]	DI	picc_bb	The values for 8bit programmable main divider.
S[1:0]	DI	picc_bb	The values for 2bit programmable post scaler.

**I/O Type Abbr.**

- AI: Analog Input
- DI: Digital Input
- AO: Analog Output
- DO: Digital Output
- AB: Analog Bidirectional
- DB: Digital Bidirectional
- AP: Analog Power
- DP: Digital Power
- AG: Analog Ground
- DG: Digital Ground

### CORE CONFIGURATION



**ABSOLUTE MAXIMUM RATINGS**

Characteristics	Symbol	Value	Unit	Applicable pin
Supply Voltage	VDD VDDA	-0.3 to 3.8	V	VDD, VDDA, VSS, VSSA
Voltage on Any Digital Pin	Vin	Vss-0.3 to Vdd+0.3	V	P[5:0], M[7:0], S[1:0] PWRDN
Storage Temperature	Tstg	-45 to 125	°C	-

**NOTES:**

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5K resistor (Human body model)

**RECOMMENDED OPERATING CONDITIONS**

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage Differential	VDD - VDDA	-0.1	0	+0.1	V
External Loop Filter Capacitance	L <sub>F</sub>		820		pF
Operating Temperature	Topr	0		70	°C

**NOTE:** It is strongly recommended that all the supply pins (VDDA, VDD) be powered from the same source to avoid power latch-up.

**DC ELECTRICAL CHARACTERISTICS**

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	VDD/VDDA	3.15	3.3	3.45	V
Digital Input Voltage High	V <sub>Ih</sub>	2.0			V
Digital Input Voltage Low	V <sub>Il</sub>			0.8	V
Dynamic Current (CORE Level without I/O Cell)	I <sub>dd</sub>			3.5	mA
Power Down Current	I <sub>pd</sub>			120	µA

**AC ELECTRICAL CHARACTERISTICS**

Characteristics	Symbol	Min	Typ	Max	Unit
Input Frequency	F <sub>IN</sub>	3	14.318	40	MHz
Output Clock Frequency	F <sub>OUT</sub>	20		170	MHz
VCO Output Clock Frequency	F <sub>VCO</sub>	20		170	MHz
Input Clock Duty Cycle	T <sub>ID</sub>	40		60	%
Output Clock Duty Cycle	T <sub>OD</sub>	40		60	%
Locking Time	T <sub>LT</sub>			150	µs
Cycle to Cycle Jitter	T <sub>JCC</sub>	-150		+150	ps

## FUNCTION DESCRIPTION

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.

In this application, it includes the following basic blocks.

- The voltage-controlled oscillator to generate the output frequency
- The divider P divides the reference frequency by p
- The divider M divides the VCO output frequency by m
- The divider S divides the VCO output frequency by s
- The phase frequency detector detects the phase difference between the reference frequency and the output frequency (after division) and controls the charge pump voltage.
- The loop filter removes high frequency components in charge pump voltage and does smooth and clean control of VCO

The m, p, s values can be programmed by 16bit digital data from the external source. So the PLL can be locked in the desired frequency.

$$F_{out} = m * F_{in} / p*s$$

If  $F_{in} = 14.318\text{MHz}$ , and  $m=M+8$ ,  $p=P+2$ ,  $s=2^S$

### Digital data format:

Main Divider	Pre Divider	Post Scaler
M7,M6,M5,M4,M3,M2,M1,M0	P5,P4,P3,P2,P1,P0	S0,S1

### NOTES:

1. S[1] - S[0]: Output Frequency Scaler
2. M[7] - M[0]: VCO Frequency Divider
3. P[5] - P[0]: Reference Frequency Input Divider

## OUTPUT FREQUENCY EQUATION & TABLE

$$\text{Frequency Equation : } F_{\text{OUT}} = \frac{(m+8)}{(p+2) \times 2^s} \times F_{\text{IN}}$$

Table 1. Example of Divider Ratio

M7	M6	M5	M4	M3	M2	M1	M0	m	M (m+8)	P6	P5	P4	P3	P2	P1	P0	p	P (p+2)	S1	S0	2'
0	1	0	1	0	1	0	1	85	93	0	1	0	1	0	1	0	42	44	0	0	1

### NOTES:

1. Don't set the P or M as zero, that is 000000 / 00000000
2. The proper range of P and M : 1<=P<=62, 1<=M<=248
3. The P and M must be selected considering stability of PLL and VCO output frequency range
4. Please consult with SEC application engineer to select the proper P, M and S values

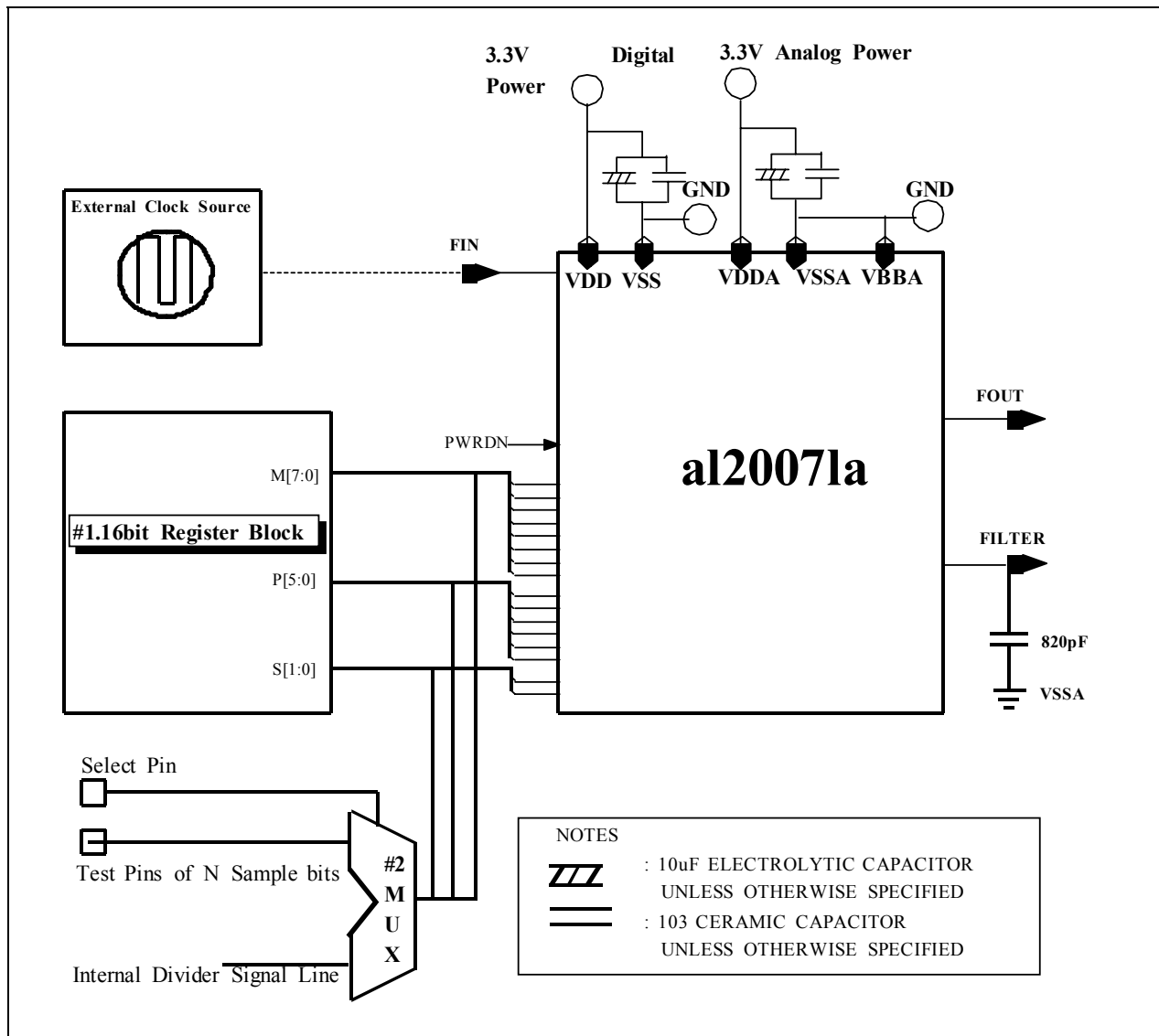
## CORE EVALUATION GUIDE

For the embedded PLL, we must consider the test circuits for the embedded PLL core in multiple applications. Hence the following requirements should be satisfied.

- The FILTER and FOUT pins must be bypassed for external test.
- For PLL test (Below 2 examples), it is needed to control the dividers - M[7:0], P[5:0] and S[1:0] - that generate multiple clocks.

Example #1. Registers can be used for easy control of divider values.

Example #2. N sample bits of 16-bit divider pins can be bypassed for test using MUX.





## CORE LAYOUT GUIDE

- The digital power(VDD,VSS) and the analog power(VDA,VSSA) must be dedicated to PLL only and seperated. If the dedicated VDD and VSS is not allowed that of the least power consuming block is shared with the PLL.
- The PIA pad is used as a FILTER pad that contains only ESD production diodes without any resistors and buffers.
- The FOUT and FILTER pins must be placed far from the internal signals in order to avoid overlapping signal lines.
- The blocks having a large digital switching current must be located away from the PLL core.
- The PLL core must be shielded by guardring.
- For the FOUT pad, you can use a custom drive buffer or POT12 buffer considering the drive current.

## WITHOUT XTAL-DRIVER USERS GUIDE

- There are two crystal driver cell (XTAL-OSC and PSOSCM2) options for the AL2007LA PLL core.
  1. If the crystal component not used , an external clock source is applied to the FIN
    - \* Please contact an SEC application engineer when using a crystal.
  2. If the crystal component not used , an external clock I/O Buffer offered from Samsung's STD90 library is recommanded for use
    - When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:
      - \* Without Xtal-driver : FIN,FILTER,FOUT,VDDA,VSSA,VDD and VSS.

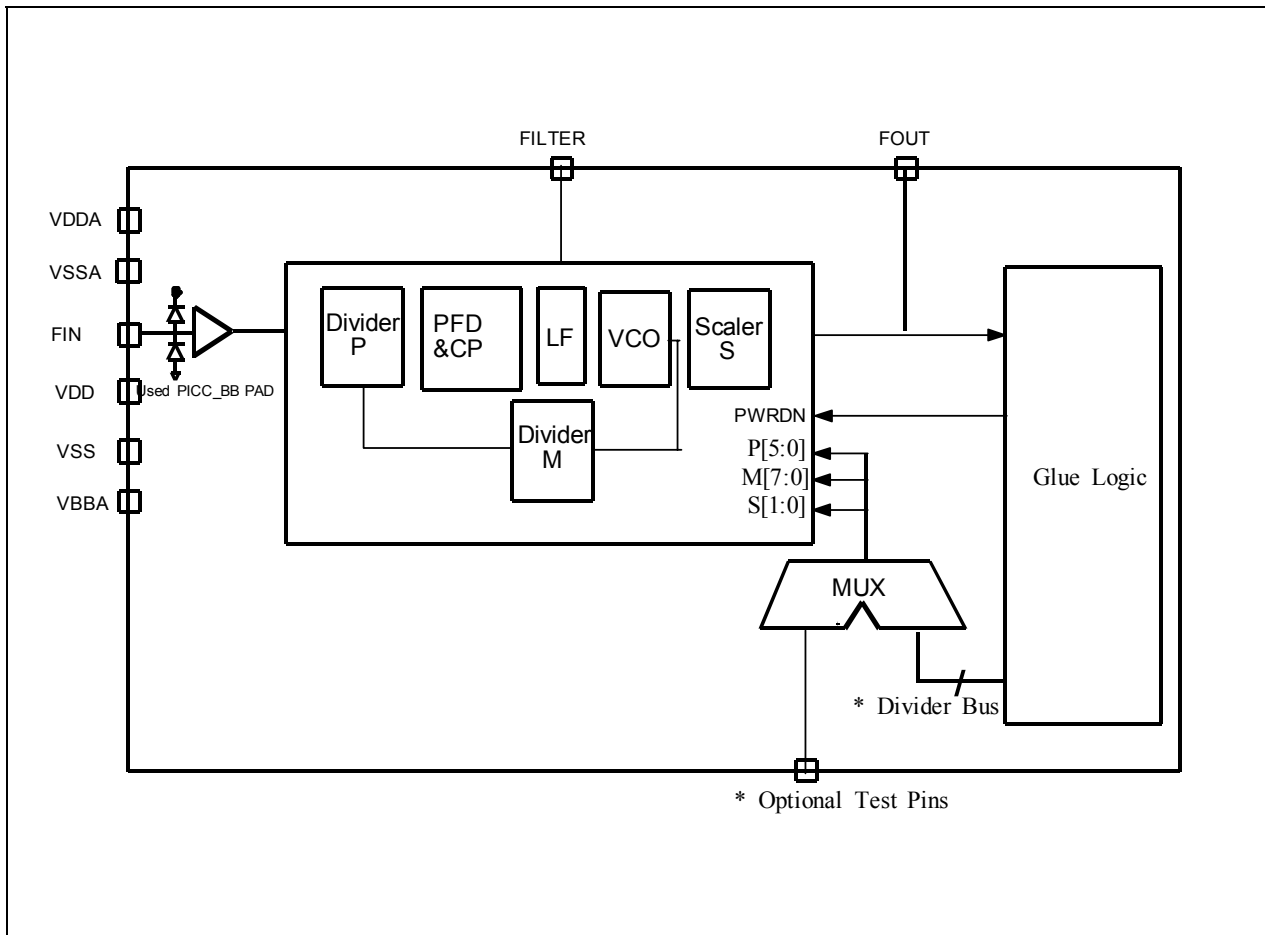
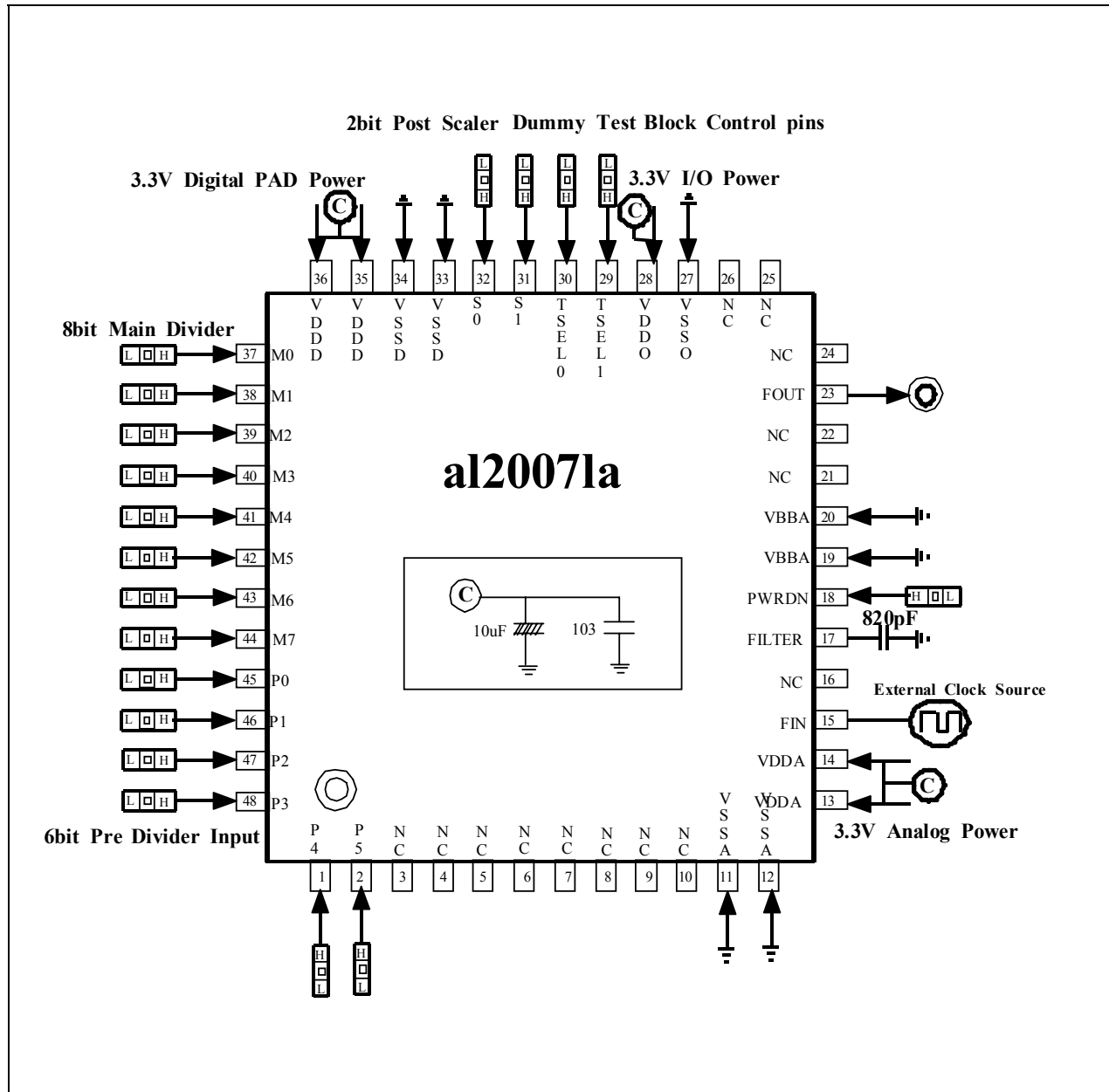


Figure 1. The example of PLL block without crystal component (Normal Case)

PACKAGE CONFIGURATION



NOTES:

1. TSEL0, TSEL1 pins are internal dummy block test pins.
2. NC is Noconnection pin

## PACKAGE PIN DESCRIPTION

Name	Pin No	I/O Type	Pin Description
VDDD	35,36	DP	Digital power supply
VSSD	33,34	DG	Digital ground
PWRDN	18	DI	FSPLL clock power down -PWRDN is High, PLL do not operating under this condition. - If isn't used this pin, tied to VSS.
P[0]~P[5]	1,2,45~48	DI	Pre-Divider Input(LSB)
VDDA	13,14	AP	Analog power supply
VSSA	11,12	AG	Analog ground
VBBA	19,20	AB/DB	Analog / Digital Sub Bias Power
FIN	15	AI	Crystal input or external F <sub>REF</sub> input
FOUT	22	DO	20MHZ~170MHz clock output
FILTER	17	AO	Pump out is connected to the FILTER. A 820pF Capacitor is connected between the pin and analog pin
TSEL0	30	DI	FOUT divide control pins. -End users used not this pins, tied to VDD or VSS
TSEL1	29	DI	FOUT divide control pins. -End users used not this pins, tied to VDD or VSS
S[0]~S[1]	31,32	DI	Post scaler input
M[0]~M[7]	37~44	DI	8bit main divider input
VDDO	28	PP	I/O PAD Power
VSSO	27	PG	I/O PAD Ground

**NOTE:** I/O TYPE PP and PG denote PAD power and PAD ground respectively.

## DESIGN CONSIDERATIONS

The following design considerations apply:

- Phase tolerance and jitter are independent of the PLL frequency.
- Jitter is affected by the noise frequency in the power(VDD/VSS,VDDA/VSSA). It increases when the noise level increases.
- A CMOS-level input reference clock is recommended for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
- The use of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
- The following apply to the noise level, which can be minimized by using good analog power and ground isolation techniques in the system:
  - Use wide PCB traces for POWER(VDD/VSS, VDDA/VSSA) connections to the PLL core. Separate the traces from the chip's VDD/VSS,VDDA/VSSA supplies.
  - Use proper VDD/VSS,VDDA/VSSA de-coupling.
  - Use good power and ground sources on the board.
  - Use Power VBB for minimize substrate noise
- The PLL core should be placed as close as possible to the dedicated loop filter and analog Power and ground pins.
- It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
- Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction

## FEEDBACK REQUEST

Thank you for having an interest in our products. Please fill out this form, especially the items which you want to request.

Parameter	Customer	SEC	Unit
Process			
Supply voltage (VDD)			
Input frequency (FIN)			
Output frequency (FOUT)			
Cycle to cycle jitter (TJCC)	100M ~ 200M		
	200M ~ 300M		
	300M ~ 400M		
	400M ~ 500M		
Period jitter (TJP)	100M ~ 200M		
	200M ~ 300M		
	300M ~ 400M		
	400M ~ 500M		
Output duty ratio (TOD)			
Lock up time (TLT)			
Dynamic current			
Stand by current			
Filter capacitor			

- How many PLLs are embedded in your system ?
- Do you need synchronization between input clock and output clock ?
- Do you need another spec of jitter ?

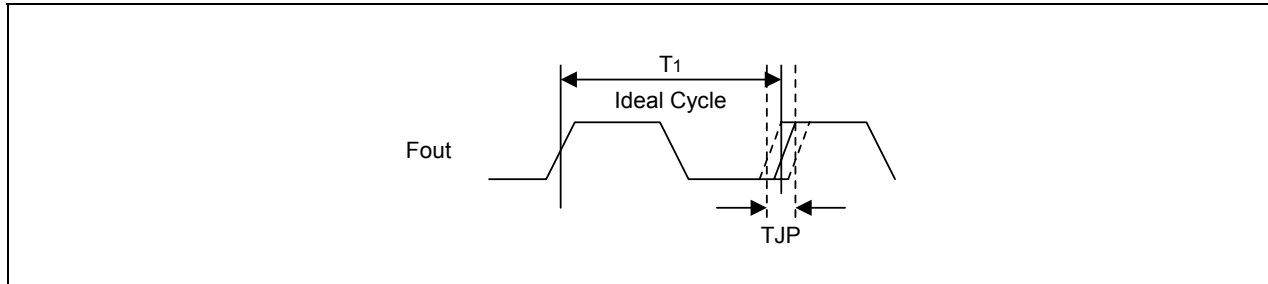
Parameter	Customer	Unit
Long-term jitter (TJLT)		psec (pk-pk)
Tracking Jitter (TJT)		psec (pk-pk)

If you have another special request, please describe below.

## JITTER DEFINITION

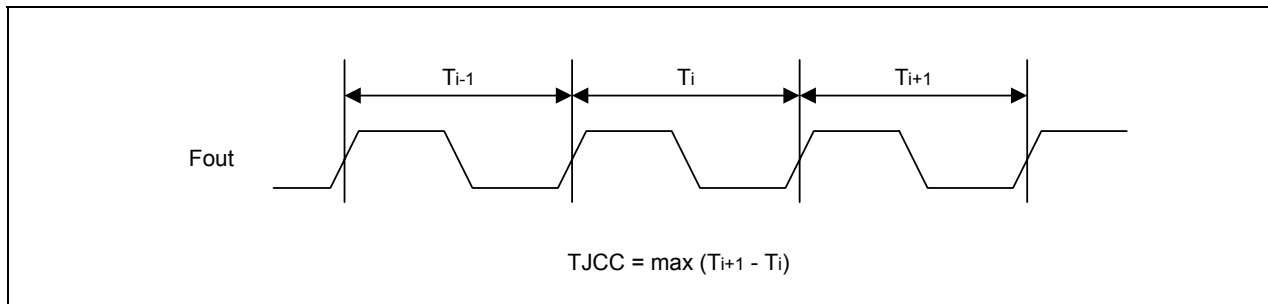
### Period Jitter

Period jitter is the maximum deviation of output clock's transition from its ideal position.



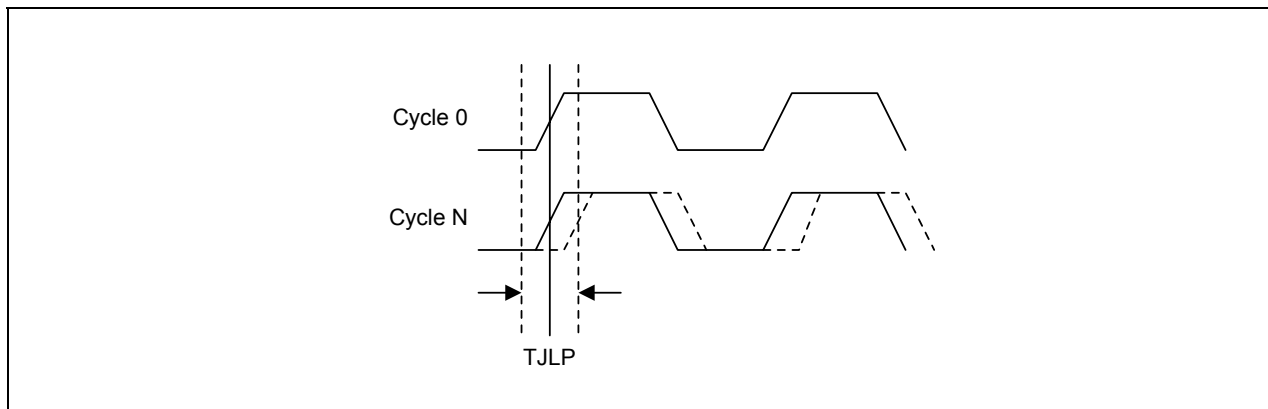
### Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the maximum deviation of output clock's transition from its corresponding position of the previous cycle.



### Long-Term Jitter

Long-term jitter is the maximum deviation of output clock' transition from its ideal position, after many cycles. The term "many" depends on the application and the frequency.



### Tracking Jitter

Tracking jitter is the maximum deviation of output clock(FOUT)'s transition from input clock (FIN) position.

