Data Sheet August 1999 File Number 2457.4

4.3A, 1000V, 3.500 Ohm, High Voltage, N-Channel Power MOSFETs

The RFP4N100 and RFP4N100SM are N-Channel enhancement mode silicon gate power field effect transistors. They are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from an integrated circuit.

Formerly developmental type TA09850.

Ordering Information

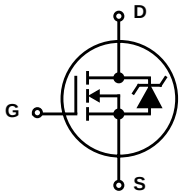
PART NUMBER	PACKAGE	BRAND
RFP4N100	TO-220AB	RFP4N100
RF1S4N100SM	TO-263AB	F1S4N100

NOTE: When ordering, use the entire part number.

Features

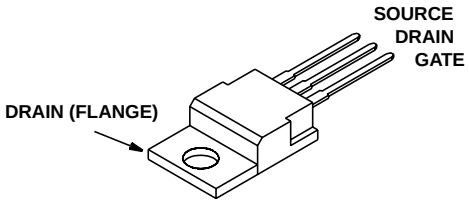
- 4.3A, 1000V
- $r_{DS(ON)} = 3.500\Omega$
- UIS Rating Curve (Single Pulse)
- $-55^{o}C$ to $150^{o}C$ Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

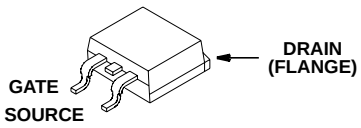


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFP4N100, RF1S4N100SM	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	1000	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	1000	V
Continuous Drain Current	I_D	4.3	A
Pulsed Drain Current (Note 3)	I_{DM}	17	A
Gate to Source Voltage	V_{GS}	±20	V
Single Pulse Avalanche Rating	E_{AS}	(See UIS SOA Curve) (Figures 4, 14, 15)	mJ
Maximum Power Dissipation	P_D	150	W
Linear Derating Factor		1.2	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from case for 10s	T_L	300	^oC
Package Body for 10s, see Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 10)	1000	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 1000V, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 800V, V_{GS} = 0V, $T_C = 150^oC$	-	-	100	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 2.5A, V_{GS} = 10V (Figures 8, 9)	-	-	3.500	Ω
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 500V, $I_D \approx$ 3.9A, R_{GS} = 9.1Ω, R_L = 120Ω)	-	-	30	ns
Rise Time	t_r		-	-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	170	ns
Fall Time	t_f		-	-	50	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 20V, I_D = 3.9A, V_{DS} = 800V (Figure 13)	-	-	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.83	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 4.3A	-	-	1.8	V
Reverse Recovery Time	t_{rr}	I_{SD} = 3.9A, dI_{SD}/dt = 100A/μs	-	-	1000	ns

NOTES:

2. Pulse test: pulse width ≤ 80μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves $T_C = 25^oC$, Unless Otherwise Specified

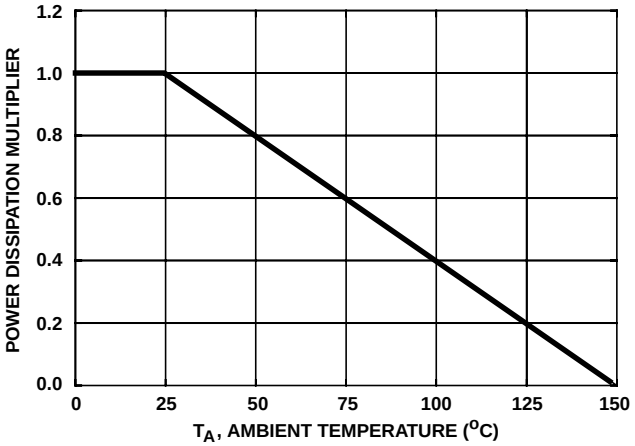


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

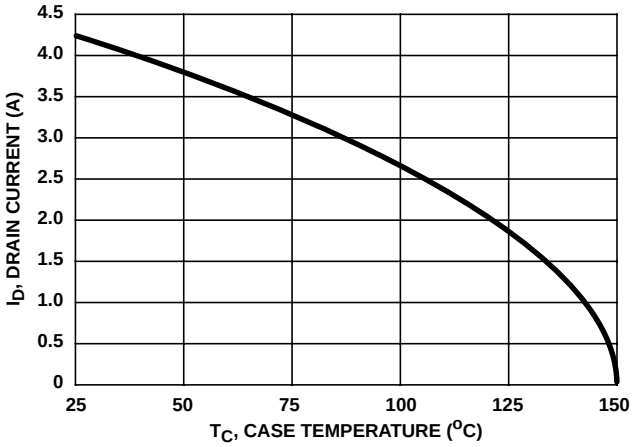


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

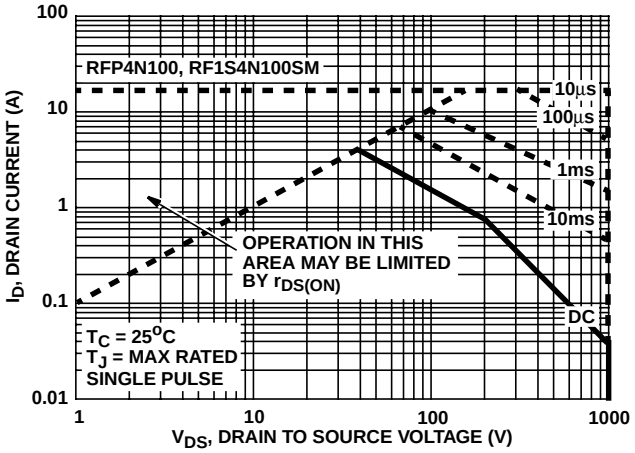


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

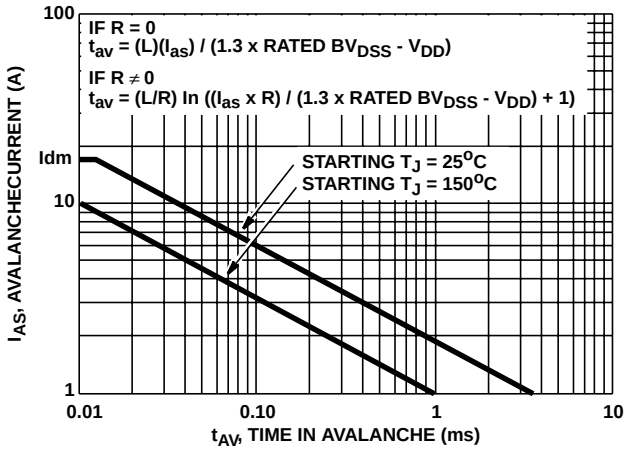


FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING SOA

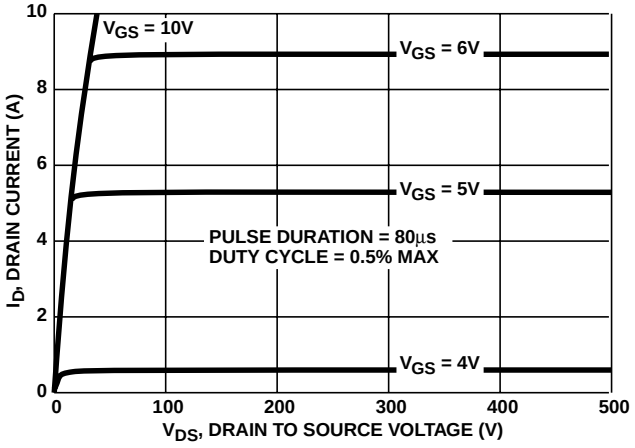


FIGURE 5. OUTPUT CHARACTERISTICS

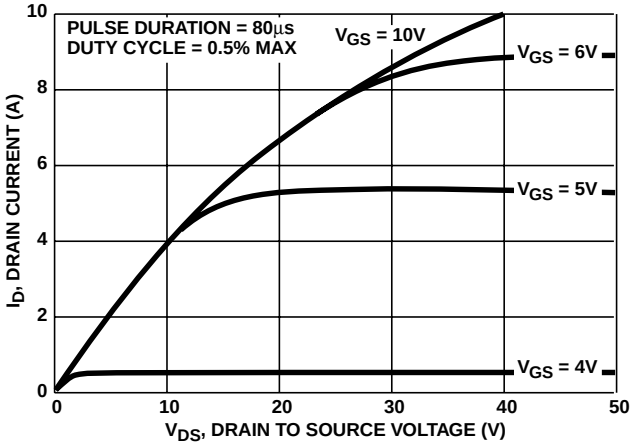


FIGURE 6. SATURATION CHARACTERISTICS

Typical Performance Curves $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

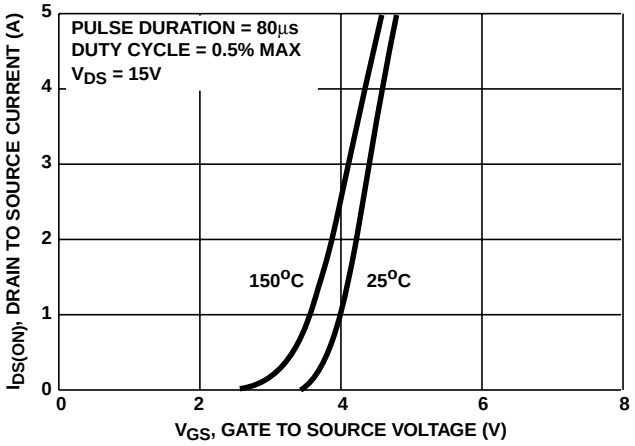


FIGURE 7. TRANSFER CHARACTERISTICS

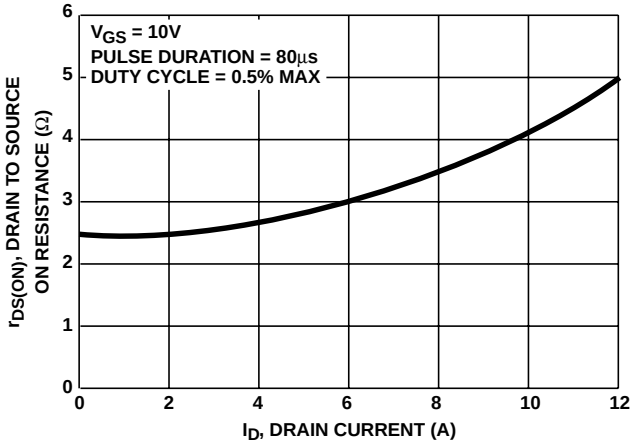


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

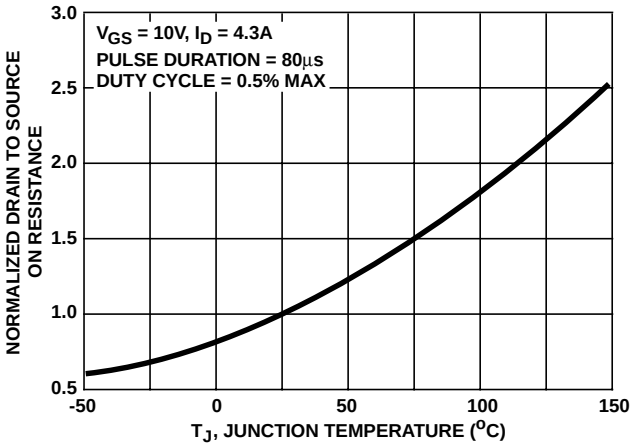


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

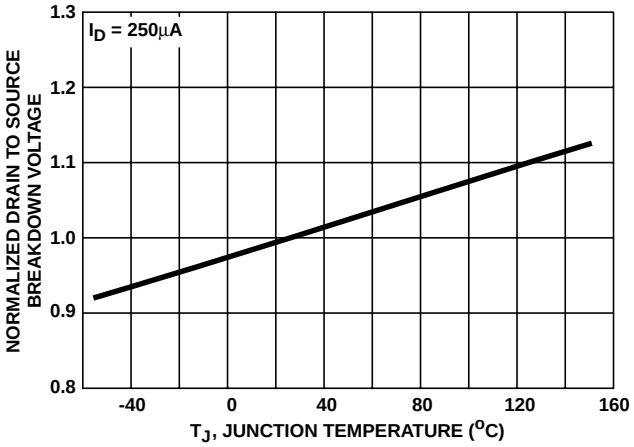


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

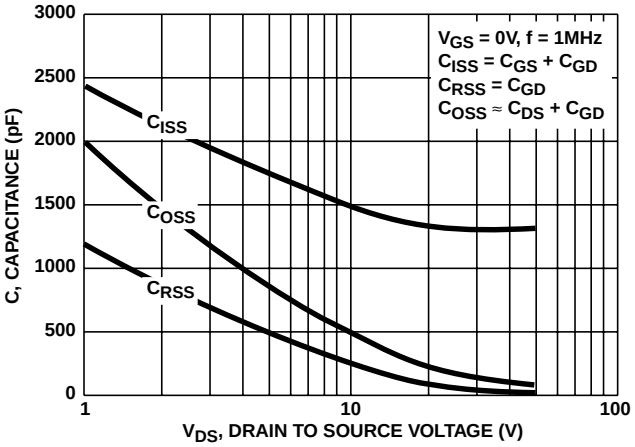


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

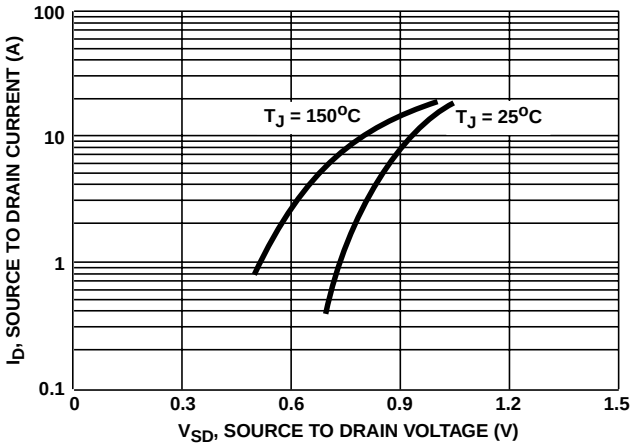


FIGURE 12. DRAIN CURRENT vs SOURCE TO DRAIN DIODE VOLTAGE

Typical Performance Curves $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

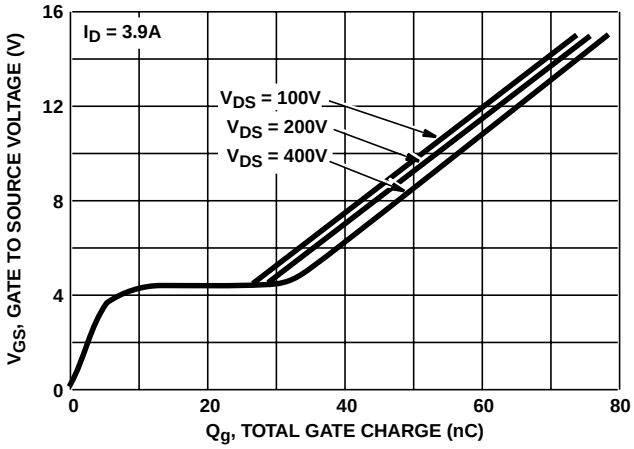


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

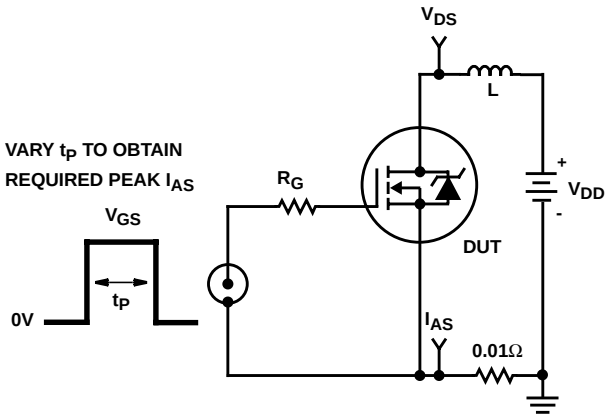


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

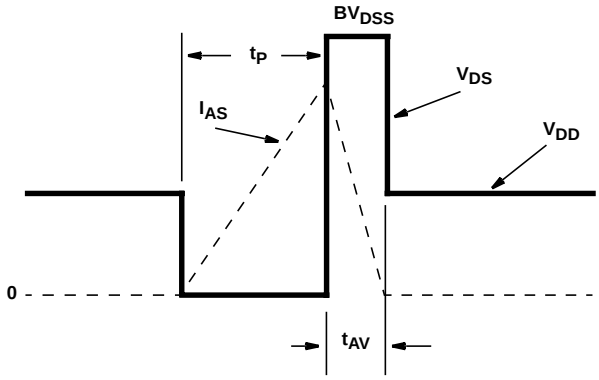


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

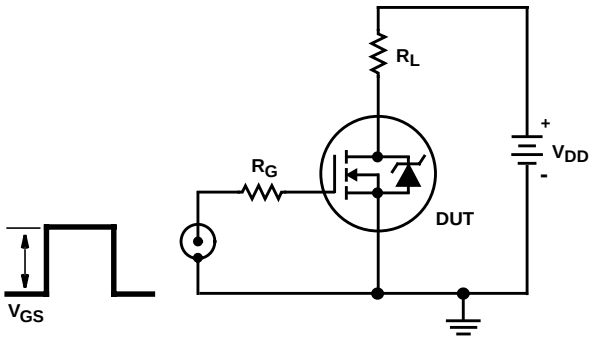


FIGURE 16. SWITCHING TIME TEST CIRCUIT

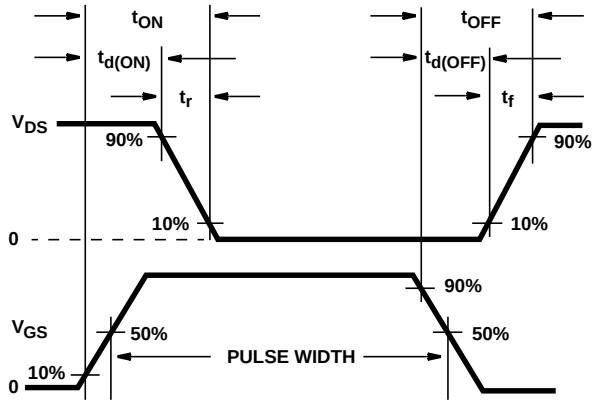


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

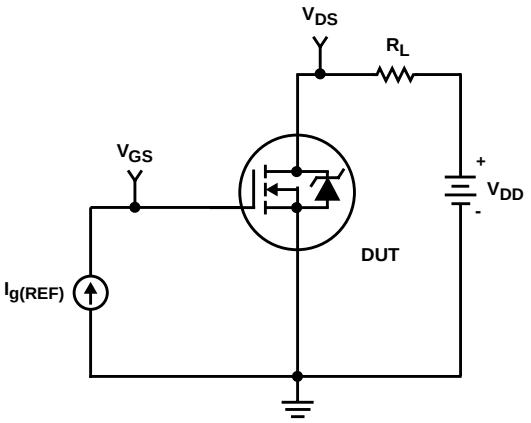


FIGURE 18. GATE CHARGE TEST CIRCUIT

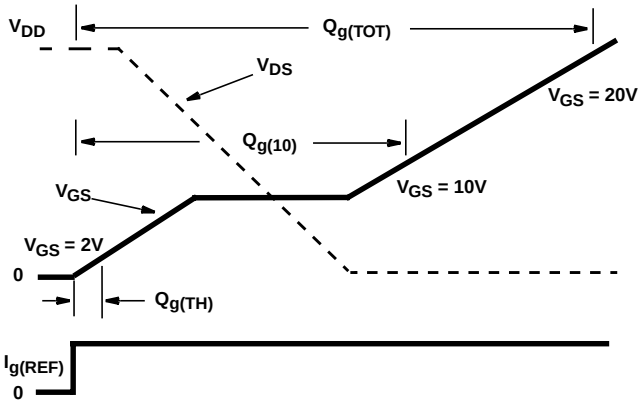


FIGURE 19. GATE CHARGE WAVEFORMS

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029