

# TMC2246A

## Image Filter

11 x 10 bit, 60 MHz

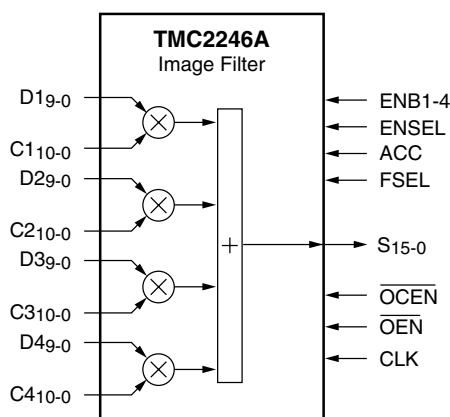
### Features

- 60 MHz computation rate
- 60 MHz data and coefficient input
- Four 11 x 10-bit multipliers
- Individual data and coefficient inputs
- 25-Bit accumulator
- Fractional and integer two's complement data formats
- Input and output data latches with user-configurable enables
- Selectable 16-bit rounded output
- Internal 1/2 LSB rounding
- Available in 120-pin CPGA, PPGA, MPGA, or MQFP

### Description

The TMC2246A is a video-speed convolutional array composed of four 11 x 10 bit registered multipliers followed by a summer and an accumulator. All eight multiplier inputs are accessible to the user and may be updated every clock cycle with integer or fractional two's complement data. A pipelined architecture, fully registered input and output ports, and asynchronous three-state output enable control simplify the design of complex systems.

### Logic Symbol



### Applications

- Fast pixel interpolation
- Fast image manipulation
- Image mixing and keying
- High-performance FIR filters
- Adaptive digital filters
- One- and two-dimensional image processing

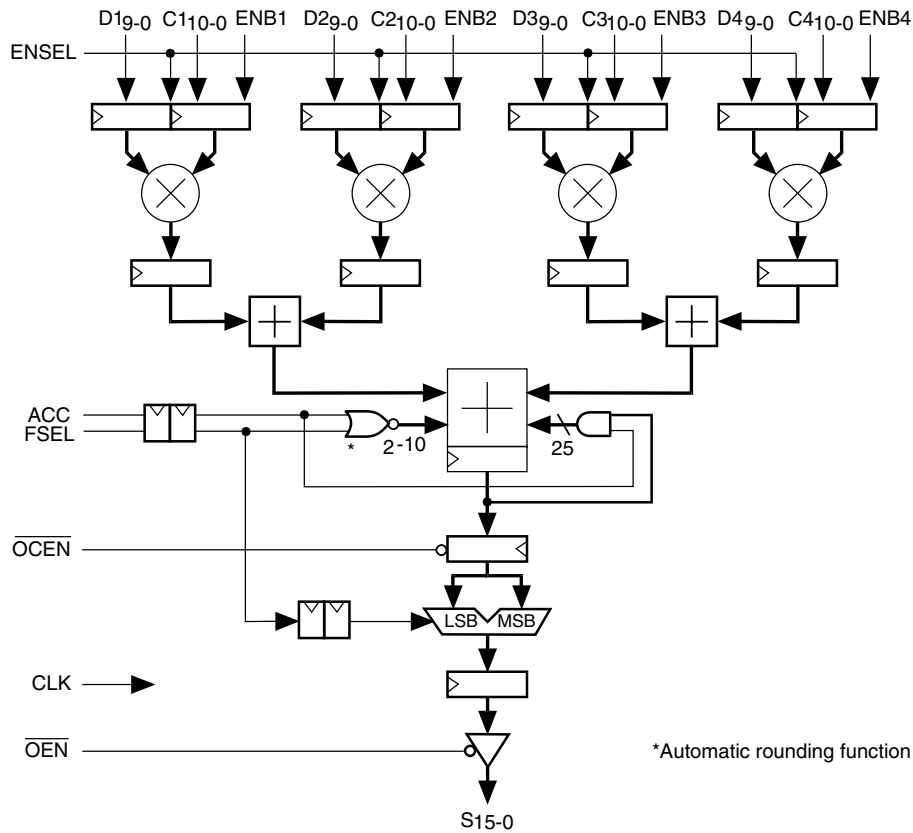
The data or coefficient inputs to the multipliers may be held over multiple clock cycles, providing storage for mixing and filtering coefficients. The 25-bit internal accumulator path allows two bits of cumulative word growth and may be internally rounded to 16 bits. Output data are updated every clock cycle, or may be held under user control. All data inputs, outputs, and controls are TTL compatible and (except for the three-state output enable) are registered on the rising edge of CLK.

The TMC2246A is uniquely suited to performing pixel interpolation in image manipulation and filtering applications. As a companion to the Fairchild Semiconductor TMC2301 and TMC2302 Image Manipulation Sequencers, the TMC2246A can execute a bilinear interpolation of an image (4-pixel kernels) at real-time video rates. Larger kernels or other, more complex, functions can be realized with no loss in performance by utilizing multiple devices.

With unrestricted access to all data and coefficient input ports, the TMC2246A offers considerable flexibility in applications performing digital filtering, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

Fabricated in a submicron CMOS process, the TMC2246A operates at a guaranteed clock rate of 60 MHz over the full temperature and supply voltage ranges. It is pin- and function-compatible with Fairchild's TMC2246, while providing higher speed operation and lower power dissipation. It is available in a 120 pin Plastic Pin Grid Array (PPGA), 120 pin Ceramic Pin Grid Array (CPGA), 120 lead MQFP to PPGA (MPGA), and a 120 lead Metric Quad FlatPack (MQFP).

## Block Diagram



## Functional Description

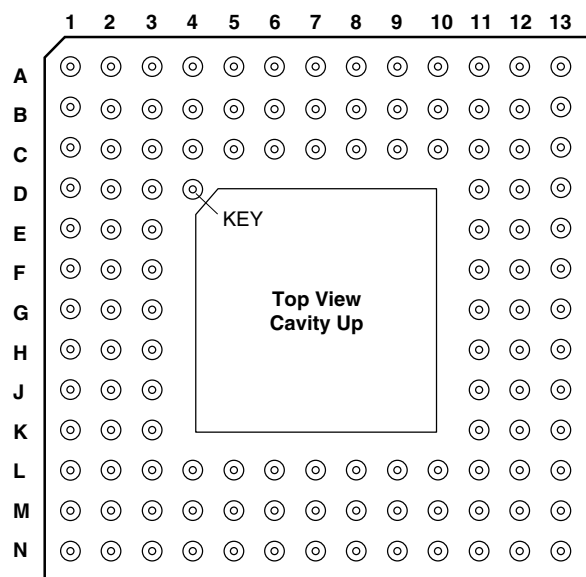
The TMC2246A Image Filter is a flexible multiplier-summer array which computes the accumulated sum of four 11x10 bit products, allowing word growth up to 25 bits.

The inputs are user-configurable, allowing latching of either the 10- or 11-bit input data. The data format is user-selectable between integer or fractional two's complement arithmetic. Total latency from input registers to output data port is 5 clocks.

The output data path is 16 bits wide, providing the lower 16 bits of the accumulator when in integer format or the upper 16 bits of the 25-bit accumulator path when fractional two's complement notation is selected. One-time rounding to 16 bits is performed automatically when accumulating fractional data, but is disabled when operating in integer format to maintain the integrity of the least-significant bits.

## Pin Assignments

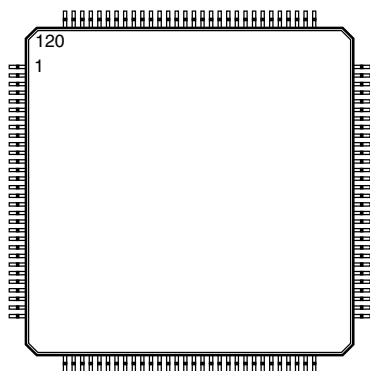
120 Pin Plastic Pin Grid Array, H5 Package, 120 Pin Ceramic Pin Grid Array, G1 Package, and 120 Pin Metric Quad FlatPack to 120 Pin Plastic Pin Array, H6 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	ENSEL	C5	D48	G11	D35	L10	C28
A2	ENB2	C6	D44	G12	D36	L11	D20
A3	ENB3	C7	GND	G13	D34	L12	D24
A4	D47	C8	VDD	H1	S6	L13	D25
A5	D45	C9	C45	H2	S5	M1	D19
A6	D42	C10	C41	H3	VDD	M2	D14
A7	D41	C11	C31	H11	GND	M3	D11
A8	C410	C12	C33	H12	D38	M4	C110
A9	C48	C13	C36	H13	D37	M5	C17
A10	C46	D1	S13	J1	S4	M6	C15
A11	C43	D2	S14	J2	S3	M7	C13
A12	C40	D3	OCEN	J3	GND	M8	C10
A13	C32	D11	C34	J11	D27	M9	C22
B1	ACC	D12	C37	J12	D29	M10	C25
B2	FSEL	D13	C39	J13	D39	M11	C29
B3	ENB4	E1	S11	K1	S2	M12	D21
B4	D49	E2	S12	K2	S1	M13	D22
B5	D46	E3	GND	K3	D18	N1	D16
B6	D43	E11	C38	K11	D23	N2	D13
B7	D40	E12	C310	K12	D26	N3	D10
B8	C49	E13	D30	K13	D28	N4	C18
B9	C47	F1	S9	L1	S0	N5	C16
B10	C44	F2	S10	L2	D17	N6	C14
B11	C42	F3	VDD	L3	D15	N7	C12
B12	C30	F11	D31	L4	D12	N8	C11
B13	C35	F12	D32	L5	C19	N9	C21
C1	S15	F13	D33	L6	GND	N10	C23
C2	OEN	G1	S7	L7	VDD	N11	C26
C3	CLK	G2	S8	L8	C20	N12	C27
C4	ENB1	G3	GND	L9	C24	N13	C210

# Pin Assignments

## 120 Lead Metric Quad Flat Pack (KE) Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	CLK	25	S <sub>1</sub>	49	C <sub>10</sub>	73	D <sub>38</sub>	97	C <sub>44</sub>
2	FSEL	26	S <sub>0</sub>	50	C <sub>20</sub>	74	D <sub>37</sub>	98	C <sub>45</sub>
3	ACC	27	D <sub>19</sub>	51	C <sub>21</sub>	75	D <sub>36</sub>	99	C <sub>46</sub>
4	OCEN	28	D <sub>18</sub>	52	C <sub>22</sub>	76	D <sub>35</sub>	100	C <sub>47</sub>
5	OEN	29	D <sub>17</sub>	53	C <sub>23</sub>	77	D <sub>34</sub>	101	C <sub>48</sub>
6	S <sub>15</sub>	30	D <sub>16</sub>	54	C <sub>24</sub>	78	D <sub>33</sub>	102	V <sub>DD</sub>
7	S <sub>14</sub>	31	D <sub>15</sub>	55	C <sub>25</sub>	79	D <sub>32</sub>	103	C <sub>49</sub>
8	GND	32	D <sub>14</sub>	56	C <sub>26</sub>	80	D <sub>31</sub>	104	C <sub>410</sub>
9	S <sub>13</sub>	33	D <sub>13</sub>	57	C <sub>27</sub>	81	D <sub>30</sub>	105	D <sub>40</sub>
10	S <sub>12</sub>	34	D <sub>12</sub>	58	C <sub>28</sub>	82	C <sub>310</sub>	106	GND
11	S <sub>11</sub>	35	D <sub>11</sub>	59	C <sub>29</sub>	83	C <sub>39</sub>	107	D <sub>41</sub>
12	V <sub>DD</sub>	36	D <sub>10</sub>	60	C <sub>210</sub>	84	C <sub>38</sub>	108	D <sub>42</sub>
13	S <sub>10</sub>	37	C <sub>110</sub>	61	D <sub>20</sub>	85	C <sub>37</sub>	109	D <sub>43</sub>
14	S <sub>9</sub>	38	C <sub>19</sub>	62	D <sub>21</sub>	86	C <sub>36</sub>	110	D <sub>44</sub>
15	S <sub>8</sub>	39	C <sub>18</sub>	63	D <sub>22</sub>	87	C <sub>35</sub>	111	D <sub>45</sub>
16	GND	40	C <sub>17</sub>	64	D <sub>23</sub>	88	C <sub>34</sub>	112	D <sub>46</sub>
17	S <sub>7</sub>	41	C <sub>16</sub>	65	D <sub>24</sub>	89	C <sub>33</sub>	113	D <sub>47</sub>
18	S <sub>6</sub>	42	GND	66	D <sub>25</sub>	90	C <sub>32</sub>	114	D <sub>48</sub>
19	S <sub>5</sub>	43	C <sub>15</sub>	67	D <sub>26</sub>	91	C <sub>31</sub>	115	D <sub>49</sub>
20	V <sub>DD</sub>	44	C <sub>14</sub>	68	D <sub>27</sub>	92	C <sub>30</sub>	116	ENB3
21	S <sub>4</sub>	45	C <sub>13</sub>	69	D <sub>28</sub>	93	C <sub>40</sub>	117	ENB2
22	S <sub>3</sub>	46	V <sub>DD</sub>	70	D <sub>29</sub>	94	C <sub>41</sub>	118	ENB1
23	S <sub>2</sub>	47	C <sub>12</sub>	71	D <sub>39</sub>	95	C <sub>42</sub>	119	ENB4
24	GND	48	C <sub>11</sub>	72	GND	96	C <sub>43</sub>	120	ENSEL

## Pin Descriptions

Pin Name	Pin Number		Pin Function Description
	CPGA/PPGA/ MPGA	MQFP	
<b>Power</b>			
V <sub>DD</sub>	F3, H3, L7, C8	12, 20, 46, 102	<b>Supply Voltage.</b> The TMC2246A operates from a single +5V supply. All power and ground pins must be connected.
GND	E3, G3, J3, L6, H11, C7	8, 16, 24, 42, 72, 106	<b>Ground.</b> The TMC2246A operates from a single +5V supply. All power and ground pins must be connected.
<b>Clock</b>			
CLK	C3	1	<b>System Clock.</b> The TMC2246A operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.
<b>Inputs</b>			
D1 <sub>9-0</sub>	M1, K3, L2, N1, L3, M2, N2, L4, M3, N3	27, 28, 29, 30, 31, 32, 33, 34, 35, 36	<b>Data Input Ports.</b> D1 through D4 are the 10-bit data input ports. The LSB is Dx <sub>0</sub> .
D2 <sub>9-0</sub>	J12, K13, J11, K12, L13, L12, K11, M13, M12, L11	70, 69, 68, 67, 66, 65, 64, 63, 62, 61	
D3 <sub>9-0</sub>	J13, H12, H13, G12, G11, G13, F13, F12, F11, E13	71, 73, 74, 75, 76, 77, 78, 79, 80, 81	
D4 <sub>9-0</sub>	B4, C5, A4, B5, A5, C6, B6, A6, A7, B7	115, 114, 113, 112, 111, 110, 109, 108, 107, 105	
C1 <sub>10-0</sub>	M4, L5, N4, M5, N5, M6, N6, M7, N7, N8, M8	37, 38, 39, 40, 41, 43, 44, 45, 47, 48, 49	<b>Coefficient Input Ports.</b> C1 through C4 are the 11-bit coefficient input ports. The LSB is Cx <sub>0</sub> .
C2 <sub>10-0</sub>	N13, M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 50	
C3 <sub>10-0</sub>	E12, D13, E11, D12, C13, B13, D11, C12, A13, C11, B12	82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92	
C4 <sub>10-0</sub>	A8, B8, A9, B9, A10, C9, B10, A11, B11, C10, A12	104, 103, 101, 100, 99, 98, 97, 96, 95, 94, 93	
<b>Outputs</b>			
S <sub>15-0</sub>	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	6, 7, 9, 10, 11, 13, 14, 15, 17, 18, 19, 21, 22, 23, 25, 26	<b>Sum Output.</b> The current 16-bit result is available at the Sum output. The LSB is S <sub>0</sub> . See the Functional Block Diagram.

## Pin Descriptions (continued)

Pin Name	Pin Number		Pin Function Description
	CPGA/PPGA/ MPGA	MQFP	
<b>Controls</b>			
FSEL	B2	2	<b>Format Select.</b> Coefficients input during the current clock are assumed to be in fractional two's complement format. Rounding to 16 bits is performed as determined by the accumulator control, ACC, and the upper 16 bits of the accumulator are output when the registered Format Select input (FSEL) is LOW. When FSEL is HIGH, two's complement integer format is assumed, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when operating in integer mode. See the Functional Block Diagram and the Applications Discussion.
ENSEL	A1	120	<b>Enable Select.</b> The registered Enable Select determines whether the data or the coefficient input registers may be held on the next rising edge of clock, in conjunction with the individual input enables ENB1–ENB4. See Table 1.
ENB1– ENB4	C4, A2, A3, B3	118, 117, 116, 119	<b>Input Enables.</b> When ENBi (i=1, 2, 3, or 4) is LOW, registers Ci and Di are both strobed by the next rising edge of CLK. When ENBi is HIGH and ENSEL is LOW, Di is strobed, but Ci is held. When ENBi and ENSEL are both HIGH, Di is held and Ci is strobed. See Table 1. Thus, either or both input registers to each multiplier are updated on each clock cycle.
ACC	B1	3	<b>Accumulate.</b> When the registered ACCumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. If operating in fractional two's complement format (FSEL = LOW), one-half LSB rounding to 16 bits is performed on the result. This allows the user to perform summations without propagating roundoff errors.  When ACC is HIGH, the internal accumulator adds the emerging products to the sum of previous products, without performing additional rounding.
$\overline{\text{OCEN}}$	D3	4	<b>Output Register Enable.</b> The output of the accumulator is latched into the output register on the next clock when the Output Register Clock Enable is LOW. When $\overline{\text{OCEN}}$ is HIGH the contents of the output register remain unchanged; however, accumulation will continue internally if ACC remains HIGH.
$\overline{\text{OEN}}$	C2	5	<b>Output Enable.</b> Data currently in the output registers is available at the output bus S <sub>15-0</sub> when the asynchronous Output Enable is LOW. When OEN is HIGH, the outputs are in the high-impedance state.
<b>No Connect</b>			
NC	D4 (Index Pin)		Not Connected. (Optional)

**Note:**

1. X denotes a "Don't Care" condition.
2. Any register not explicitly held is updated on the next rising edge of CLK.

**Table 1. Input Register Control**

ENB1-4	ENSEL	Input Register Held
1	1	Data i
1	0	Coefficient i
0	X	None

## Data Formats

### Fractional Two's Complement Format (FSEL = LOW)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
						$-2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$	$2^{-7}$	$2^{-8}$	$2^{-9}$	DATA (D1-4)
					$-2^1$	$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$	$2^{-7}$	$2^{-8}$	$2^{-9}$	COEFFICIENT (C1-4)
$-2^6$	$2^5$	$2^4$	$2^3$	$2^2$	$2^1$	$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$	$2^{-7}$	$2^{-8}$	$2^{-9}$	SUM

### Integer Two's Complement Format (FSEL = HIGH)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
						$-2^9$	$2^8$	$2^7$	$2^6$	$2^5$	$2^4$	$2^3$	$2^2$	$2^1$	$2^0$	DATA (D1-4)
					$-2^{10}$	$2^9$	$2^8$	$2^7$	$2^6$	$2^5$	$2^4$	$2^3$	$2^2$	$2^1$	$2^0$	COEFFICIENT (C1-4)
$-2^{15}$	$2^{14}$	$2^{13}$	$2^{12}$	$2^{11}$	$2^{10}$	$2^9$	$2^8$	$2^7$	$2^6$	$2^5$	$2^4$	$2^3$	$2^2$	$2^1$	$2^0$	SUM

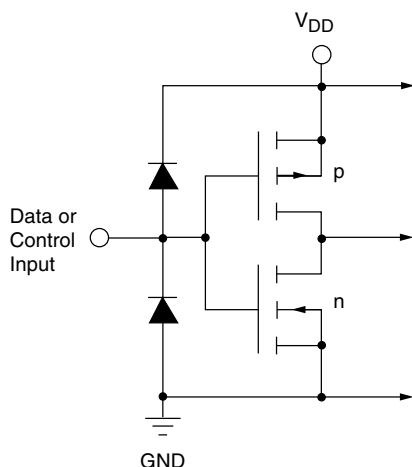
### Integer Two's Complement Data / Fractional Two's Complement Coefficient Format (FSEL = LOW)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
						$-2^9$	$2^8$	$2^7$	$2^6$	$2^5$	$2^4$	$2^3$	$2^2$	$2^1$	$2^0$	DATA (D1-4)
					$-2^1$	$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$	$2^{-7}$	$2^{-8}$	$2^{-9}$	COEFFICIENT (C1-4)
$-2^{15}$	$2^{14}$	$2^{13}$	$2^{12}$	$2^{11}$	$2^{10}$	$2^9$	$2^8$	$2^7$	$2^6$	$2^5$	$2^4$	$2^3$	$2^2$	$2^1$	$2^0$	SUM

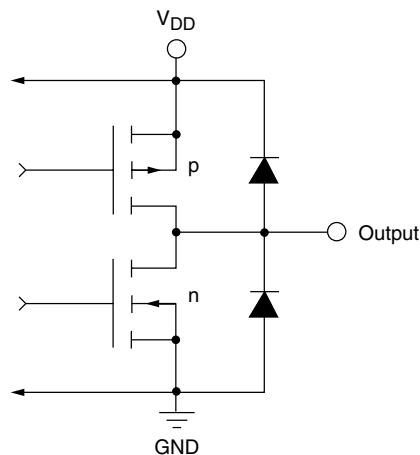
**Note:** A minus sign indicates the sign bit.

**Figure 1. Data Formats**

## Equivalent Circuits and Threshold Levels



**Figure 2. Equivalent Digital Input Circuit**



**Figure 3. Equivalent Digital Output Circuit**

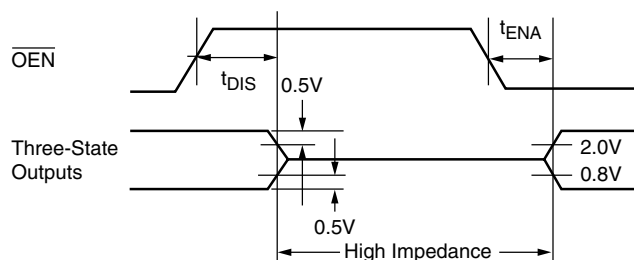


Figure 4. Threshold Levels for Three-State Measurement

**Absolute Maximum Ratings** (beyond which the device may be damaged)<sup>1</sup>

Parameter	Min	Max	Unit
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	$V_{DD} + 0.5$	V
Output, Applied Voltage <sup>2</sup>	-0.5	$V_{DD} + 0.5$	V
Output, Externally Forced Current <sup>3,4</sup>	-3.0	6.0	mA
Output, Short Circuit Duration (single output in HIGH state to ground)		1	sec
Operating, Ambient Temperature	-20	110	°C
Junction Temperature		140	°C
Storage Temperature	-65	150	°C
Lead Soldering (10 seconds)		300	°C

**Notes:**

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

**Operating Conditions**

Parameter		Min	Nom	Max	Units
$V_{DD}$	Power Supply Voltage	4.75	5.0	5.25	V
$f_{CLK}$	Clock frequency	TMC2246A		30	MHz
		TMC2246A-1		40	MHz
		TMC2246A-2		60	MHz
$t_{PWH}$	CLK pulse width, HIGH	8			ns
$t_{PWL}$	CLK pulse width, LOW	6			ns
$t_S$	Input Data Set-up Time	6			ns
$t_H$	Input Data Hold Time	1.5			ns
$V_{IH}$	Input Voltage, Logic HIGH	2.0			V
$V_{IL}$	Input Voltage, Logic LOW			0.8	V
$I_{OH}$	Output Current, Logic HIGH			-2.0	mA
$I_{OL}$	Output Current, Logic LOW			4.0	mA
$T_A$	Ambient Temperature, Still Air	0		70	°C



## Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I <sub>DD</sub>	Total Power Supply Current	V <sub>DD</sub> = Max, C <sub>LOAD</sub> = 25pF, f <sub>CLK</sub> = Max				
		TMC2246A			95	mA
		TMC2246A-1			120	mA
		TMC2246A-2			170	mA
I <sub>DDU</sub>	Power Supply Current, Unloaded	V <sub>DD</sub> = Max, $\overline{\text{OEN}}$ = HIGH, f <sub>CLK</sub> = Max				
		TMC2246A			80	mA
		TMC2246A-1			100	mA
		TMC2246A-2			140	mA
I <sub>DDQ</sub>	Power Supply Current, Quiescent	V <sub>DD</sub> = Max, CLK = LOW			5	mA
C <sub>PIN</sub>	I/O Pin Capacitance			5		pF
I <sub>IH</sub>	Input Current, HIGH	V <sub>DD</sub> = Max, V <sub>IN</sub> = V <sub>DD</sub>			±10	µA
I <sub>IL</sub>	Input Current, LOW	V <sub>DD</sub> = Max, V <sub>IN</sub> = 0 V			±10	µA
I <sub>OZH</sub>	Hi-Z Output Leakage Current, Output HIGH	V <sub>DD</sub> = Max, V <sub>IN</sub> = V <sub>DD</sub>			±10	µA
I <sub>OZL</sub>	Hi-Z Output Leakage Current, Output LOW	V <sub>DD</sub> = Max, V <sub>IN</sub> = 0 V			±10	µA
I <sub>OS</sub>	Short-Circuit Current		-20		-80	mA
V <sub>OH</sub>	Output Voltage, HIGH	S <sub>15-0</sub> , I <sub>OH</sub> = Max	2.4			V
V <sub>OL</sub>	Output Voltage, LOW	S <sub>15-0</sub> , I <sub>OL</sub> = Max			0.4	V

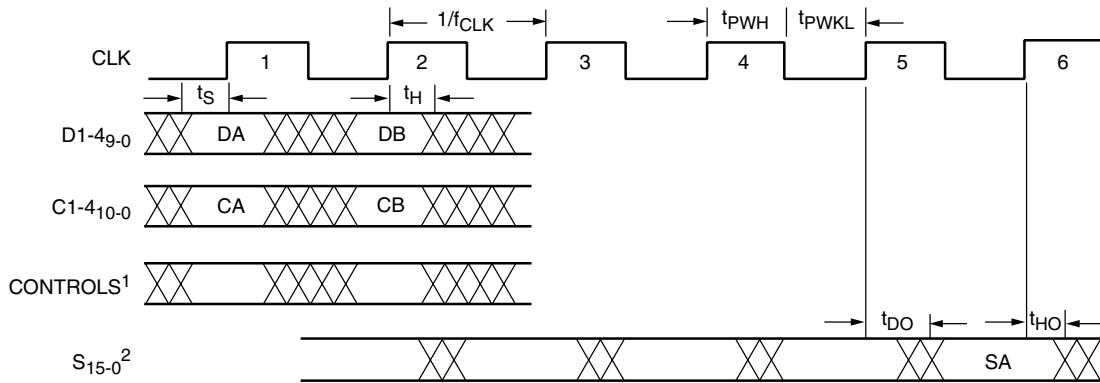
## Switching Characteristics

Parameter		Conditions <sup>1</sup>	Min	Typ	Max	Units
t <sub>DO</sub>	Output Delay Time	C <sub>LOAD</sub> = 25 pF			14	ns
t <sub>HO</sub>	Output Hold Time	C <sub>LOAD</sub> = 25 pF	4			ns
t <sub>ENA</sub>	Three-State Output Enable Delay	C <sub>LOAD</sub> = 0 pF			10	ns
t <sub>DIS</sub>	Three-State Output Disable Delay	C <sub>LOAD</sub> = 0 pF			10	ns

### Note:

1. All transitions are measured at a 1.5V level except for t<sub>ENA</sub> and t<sub>DIS</sub>.

# Timing Diagram



- Notes:**  
 1. Except  $\overline{OEN}$ .  
 2. Assumes  $\overline{OEN} = \text{LOW}$ .

## Application Notes

### Typical Operation

The versatile input clock enables and unrestricted data and coefficient inputs provided on the TMC2246A allow considerable flexibility in numerous image and signal processing architectures.

Table 2 shows a typical sequence of operations which clarifies the inherent latencies of the device and illustrates fixed coefficient storage, product accumulation, and device reconfiguration prior to beginning a new accumulation. This assumes that the device is set to fractional two's complement mode ( $FSEL = \text{LOW}$ ) with  $\overline{OCEN} = \text{LOW}$ ,  $\overline{OEN} = \text{LOW}$ , and the input registers configured to hold coefficients only ( $ENSEL = \text{LOW}$ ). X= "don't care."

### Using the TMC2246A for Pixel Interpolation

As a companion product to the TMC2301 Image Resampling Sequencer, the TMC2246A offers an excellent tool for performing high-speed pixel interpolation and image filtering.

Any pixel resampling operation with multiple-pixel kernels must utilize some parallel-processing technique, such as memory banding, to maintain high-speed image throughput rates. Memory banding utilizes adders to generate parallel offset addresses, allowing the user to access multiple pixel locations simultaneously. Using such techniques, one TMC2246A can perform bilinear interpolation (four-pixel kernel) with no loss in system performance.

Larger kernels can be realized in similar systems with additional TMC2246As. Figure 5 illustrates a basic pixel interpolation application.

**Table 2. Typical TMC2246A Operation Sequence**

CLK	D1	C1	ENB1	D2	C2	ENB2	D3	C3	ENB3	D4	C4	ENB4	ACC	Sum
0	-	-	0	-	-	0	-	-	0	-	-	0	-	-
1	D1(1)	C1(1)	1	D2(1)	C2(1)	1	D3(1)	C3(1)	1	D4(1)	C4(1)	1	0	-
2	D1(2)	X	0	D2(2)	C2(2)	0	D3(2)	X	1	D4(2)	X	1	1	-
3	D1(3)	C1(3)	0	D2(3)	C2(3)	0	D3(3)	X	0	D4(3)	X	0	1	
4	D1(4)	C1(4)	-	D2(4)	C2(4)	-	D3(4)	C3(4)	-	D4(4)	C4(4)	-	0	
5														$S(5)=D1(1)C1(1)+D2(1)C2(1)+D3(1)C3(1)+D4(1)C4(1)+2^{-10}$
6														$S(6)=S(5)+D1(2)C1(1)+D2(2)C2(1)+D3(2)C3(1)+D4(2)C4(1)$
7														$S(7)=S(6)+D1(3)C1(3)+D2(3)C2(3)+D3(3)C3(1)+D4(3)C4(1)$
8														$S(8)=D1(4)C1(4)+D2(4)C2(4)+D3(4)C3(4)+D4(4)C4(4)+2^{-10}$

Notice in this example, operating in fractional two's complement mode, that rounding is imposed on the first cycle only of an accumulation. This avoids the propagation of accumulated roundoff errors.

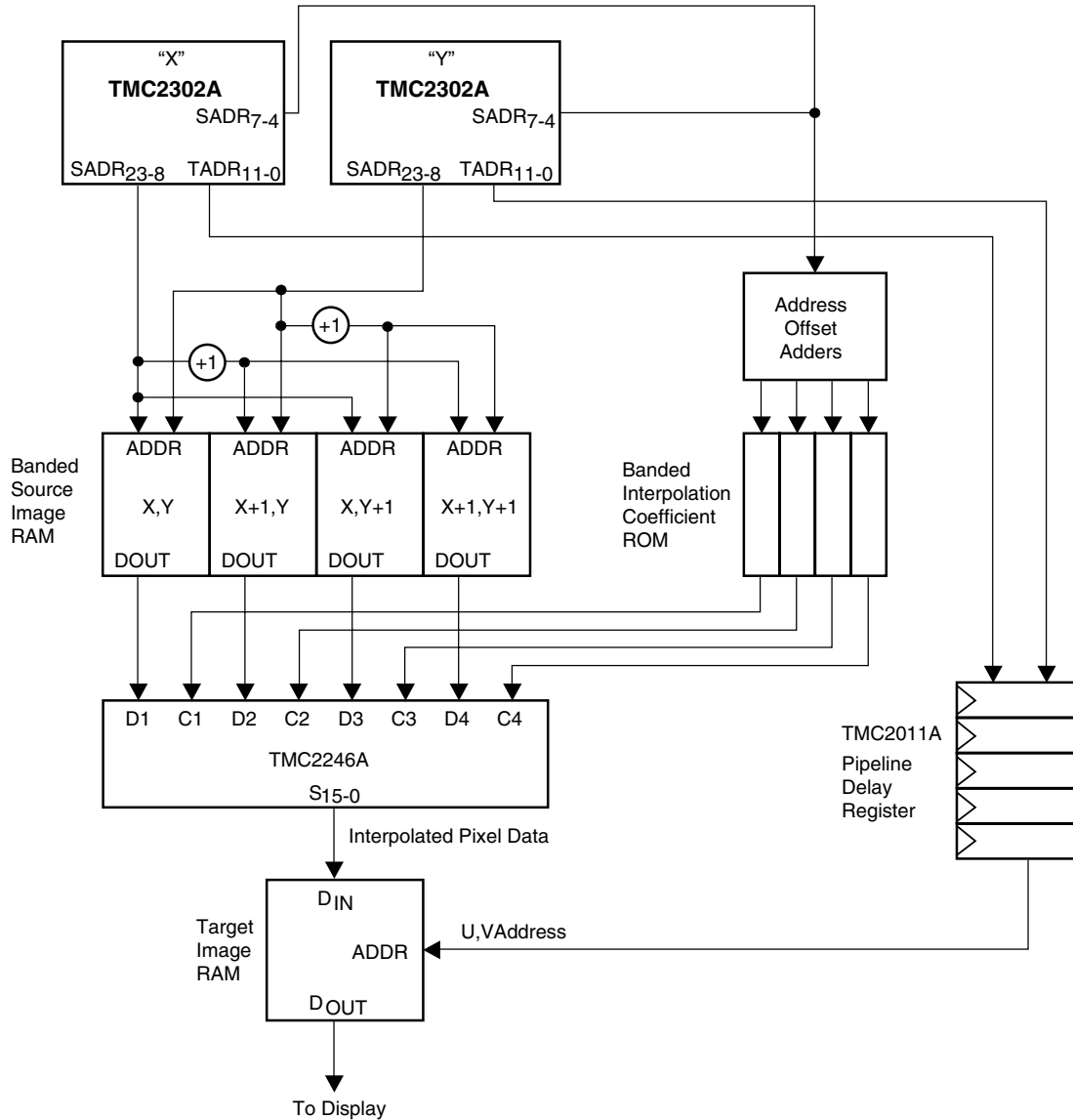


Figure 5. Bilinear Interpolation Using the TMC2246A

### TMC2246A Applications in Digital Filtering

Unrestricted access to all input ports of the TMC2246A allows the user considerable flexibility in realizing numerous digital filter architectures. Figure 6 illustrates how the device may be utilized as a flexible high-speed FIR filter with the ability to modify all of the filter coefficients dynamically or to store a fixed set if desired.

Longer filters, with more taps, are realized by including an external adder (such as the common 74381 type) to cascade multiple TMC2246As. Alternatively, two additional taps and a cascading adder are available in the Fairchild TMC2249A Digital Mixer.

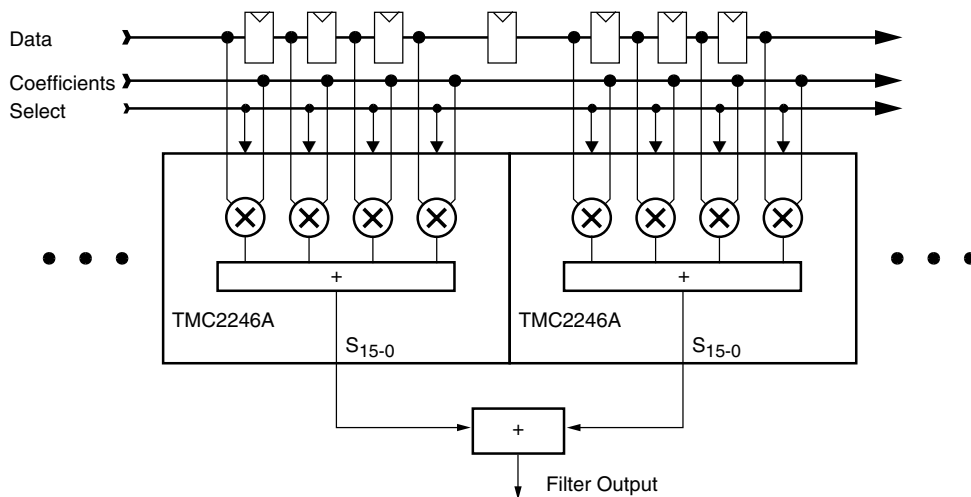


Figure 6. Using the TMC2246A For FIR Filtering

## Related Products

- TMC2301 Image Resampling Sequencer
- TMC2302A Image Manipulation Sequencer
- TMC2249A Video Mixer
- TMC2242B Half-Band Filter

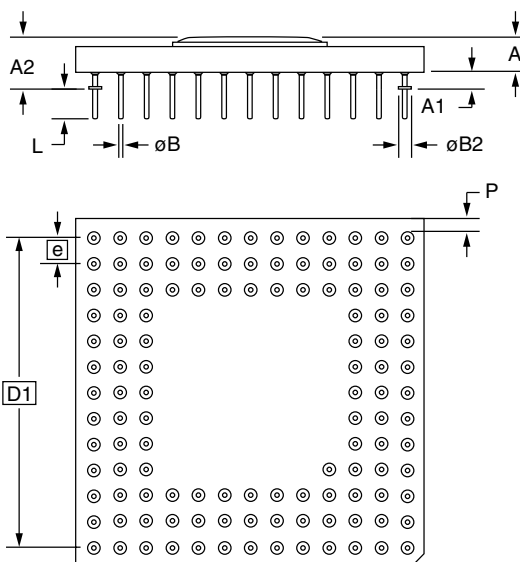
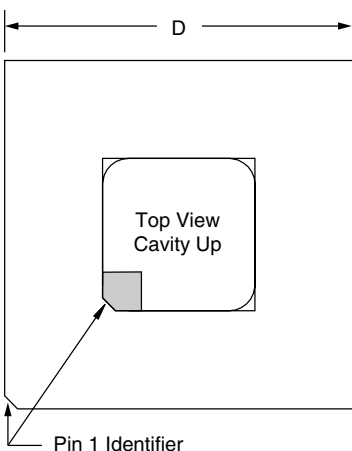
# Mechanical Dimensions

## 120-Lead CPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

**Notes:**

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



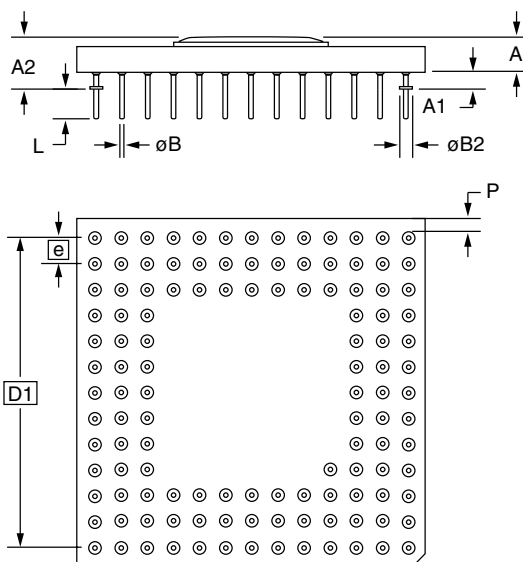
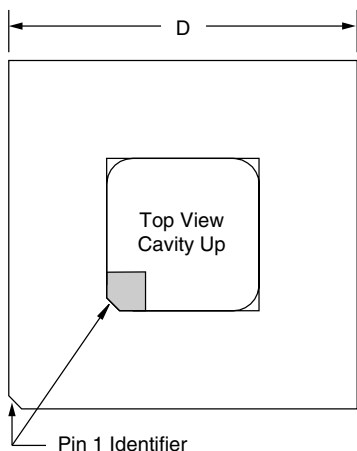
# Mechanical Dimensions

## 120-Lead PPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

**Notes:**

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



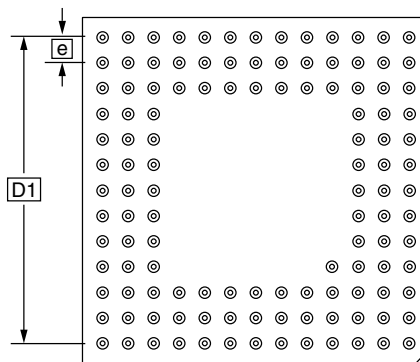
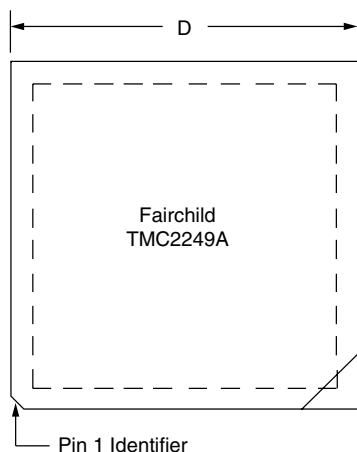
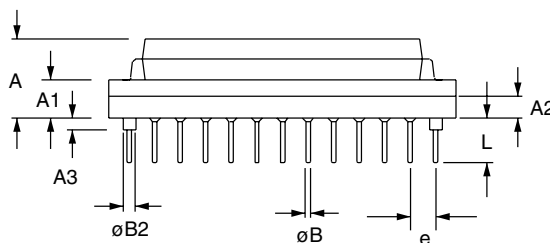
# Mechanical Dimensions

## 120-Lead Metric Quad Flat Package to Pin Grid Array Package (MPGA)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.309	.311	7.85	7.90	
A1	.145	.155	3.68	3.94	
A2	.080	.090	2.03	2.29	
A3	.050 TYP.		1.27 TYP.		
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.355	1.365	34.42	34.67	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.175	.185	4.45	4.70	
M	13		13		3
N	120		120		4

**Notes:**

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.





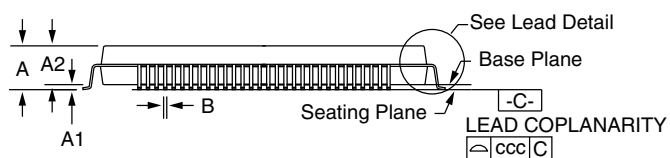
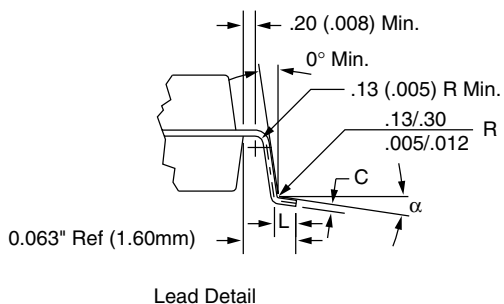
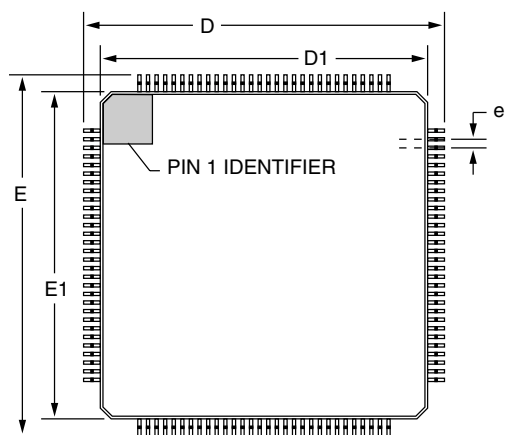
# Mechanical Dimensions

## 120-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.154	—	3.92	
A1	.010	—	.25	—	
A2	.125	.144	3.17	3.67	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.026	.037	.65	.95	4
N	120		120		
ND	30		30		
$\alpha$	0°	7°	0°	7°	
ccc	—	.004	—	.10	

**Notes:**

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.



## Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2246AG1C	0°C to 70°C	30 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2246AG1C
TMC2246AG1C1	0°C to 70°C	40 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2246AG1C1
TMC2246AG1C2	0°C to 70°C	60 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2246AG1C2
TMC2246AH5C	0°C to 70°C	30 MHz	Commercial	120 Pin Plastic Pin Grid Array	2246AH5C
TMC2246AH5C1	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2246AH5C1
TMC2246AH5C2	0°C to 70°C	60 MHz	Commercial	120 Pin Plastic Pin Grid Array	2246AH5C2
TMC2246AH6C	0°C to 70°C	30 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2246AH6C1	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2246AH6C2	0°C to 70°C	60 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2246AKEC	0°C to 70°C	30 MHz	Commercial	120 Lead Metric Quad FlatPack	2246AKEC
TMC2246AKEC1	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad FlatPack	2246AKEC1
TMC2246AKEC2	0°C to 70°C	60 MHz	Commercial	120 Lead Metric Quad FlatPack	2246AKEC2

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.