19-3882; Rev 0; 10/05

MAXIM

2.2W Stereo Audio Power Amplifier with Analog Volume Control

General Description

The MAX9787 combines a stereo, 2.2W audio power amplifier with an analog volume control in a single device. A high 90dB PSRR and low 0.01% THD+N ensures clean, low-distortion amplification of the audio signal.

The analog volume control can be driven with a potentiometer, an RC-filtered PWM source, or a DAC output. A BEEP input allows the addition of alert signals from the controller to the audio path.

Industry-leading, click-and-pop suppression eliminates audible transients during power and shutdown cycles. Other features include single-supply voltage, a shutdown mode, logic-selectable gain, thermal-overload, and output short-circuit protection.

The MAX9787 is offered in a space-saving, thermally efficient, 28-pin, thin QFN (5mm x 5mm x 0.8mm) package, and is specified over the extended -40°C to +85°C temperature range.

Applications

Notebook PCs
Flat-Panel TVs
Tablet PCs
PC Displays
Portable DVD Players
LCD Projectors
Multimedia Monitors

Features

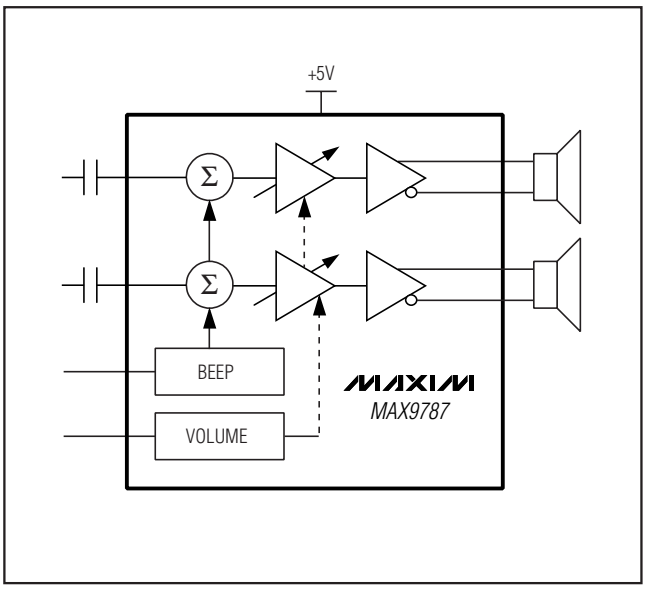
- ♦ **Class AB, 2.2W, Stereo BTL Speaker Amplifiers**
- ♦ **Analog Volume Control**
- ♦ **BEEP Input with Glitch Filter**
- ♦ **5V Single-Supply Operation**
- ♦ **High 90dB PSRR**
- ♦ **Low-Power Shutdown Mode**
- ♦ **Industry-Leading Click-and-Pop Suppression**
- ♦ **Low 0.01% THD+N at 1kHz**
- ♦ **Short-Circuit and Thermal Protection**
- ♦ **Selectable-Gain Settings**
- ♦ **Space-Saving 28-Pin TQFN (5mm x 5mm x 0.8mm)**

Ordering Information

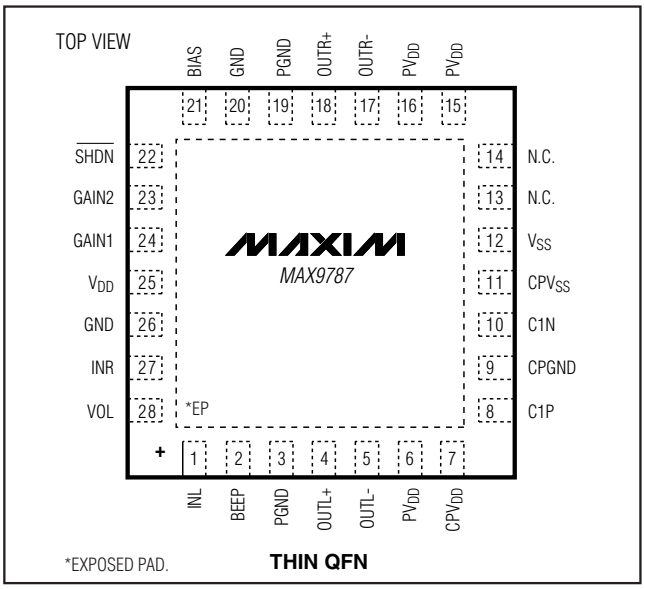
PART	PIN-PACKAGE	PKG CODE
MAX9787ETI+	28 TQFN-EP*	T2855N-1

Note: *This device is specified for -40°C to +85°C operation.*
+Denotes lead-free package.
**EP = Exposed paddle.*

Typical Operating Circuit



Pin Configuration



2.2W Stereo Audio Power Amplifier with Analog Volume Control

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD}, PV_{DD}, CPV_{DD} to GND) .....+6V
GND to PGND.....±0.3V
CPV_{SS}, C1N, V_{SS} to GND .....-6.0V to (GND + 0.3V)
Any Other Pin .....-0.3V to (V_{DD} + 0.3V)
Duration of OUT_ Short Circuit to GND or PV_{DD}.....Continuous
Duration of OUT_+ Short Circuit to OUT_- .....Continuous
Continuous Current (PV_{DD}, OUT_, PGND) 1.7A
Continuous Current (CPV_{DD}, C1N, C1P, CPV_{SS}, V_{SS}).....850mA
Continuous Input Current (all other pins) .....±20mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derate 23.8mW/°C above +70°C) 1.9W
Junction Temperature.....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = PV_{DD} = CPV_{DD} = 5V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, C_{BIAS} = 1µF, C1 = C2 = 1µF, speaker load terminated between OUT_+ and OUT_-, GAIN1 = GAIN2 = VOL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Supply Voltage Range	V_{DD}, PV_{DD}	Inferred from PSRR test		4.5		5.5	V
Quiescent Supply Current	I_{DD}				14	29	mA
Shutdown Supply Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND			0.2	5	µA
Bias Voltage	V_{BIAS}			1.7	1.8	1.9	V
Switching Time	t_{SW}	Gain or input switching			10		µs
Input Resistance	R_{IN}	Amplifier inputs (Note 2)		10	20	30	kΩ
Turn-On Time	t_{SON}				25		ms
Output Offset Voltage	V_{OS}	Measured between OUT_+ and OUT_-, T_A = +25°C			±0.4	±6	mV
Power-Supply Rejection Ratio (Note 3)	PSRR	PV_{DD} or V_{DD} = 4.5V to 5.5V (T_A = +25°C)		75	90		dB
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}			80		
		f = 10kHz, V_{RIPPLE} = 200mV_{P-P}			55		
Output Power (Note 4)	P_{OUT}	THD+N = 1%, f = 1kHz, T_A = +25°C	R_L = 8Ω	0.65	0.8		W
			R_L = 4Ω	1.2	1.5		
			R_L = 3Ω		2.2		
Total Harmonic Distortion Plus Noise	THD+N	R_L = 8Ω, P_{OUT} = 500mW, f = 1kHz			0.01		%
		R_L = 4Ω, P_{OUT} = 1W, f = 1kHz			0.02		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 5V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, C_{BIAS} = 1µF, C1 = C2 = 1µF, speaker load terminated between OUT_+ and OUT_-, GAIN1 = GAIN2 = VOL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	R_L = 8Ω, P_{OUT} = 500mW, BW = 22Hz to 22kHz		90		dB
Noise	V_n	BW = 22Hz to 22kHz, A-weighted		80		μV_{RMS}
Capacitive-Load Drive	C_L	No sustained oscillations		200		pF
Crosstalk		L to R, R to L, f = 10kHz		75		dB
Slew Rate	SR			1.4		V/µs
Gain (Maximum Volume Setting)	$A_{VMAX(SPKR)}$	GAIN1 = 0, GAIN2 = 0		6		dB
		GAIN1 = 1, GAIN2 = 0		7.5		
		GAIN1 = 0, GAIN2 = 1		9		
		GAIN1 = 1, GAIN2 = 1		10.5		
CHARGE PUMP						
Charge-Pump Frequency	f_{OSC}		500	550	600	kHz
VOLUME CONTROL						
VOL Input Impedance	R_{VOL}			100		MΩ
VOL Input Hysteresis				10		mV
Full-Mute Input Voltage		(Note 5)		4.29		V
Channel Matching		A_V = -25dB to +13.5dB		±0.2		dB
BEEP INPUT						
Beep Signal Minimum Amplitude	V_{BEEP}	R_B = 33kΩ (Note 6)	0.3			V_{P-P}
Beep Signal Minimum Frequency	f_{BEEP}		300			Hz
LOGIC INPUT ($\overline{SHDN}$, GAIN1, GAIN2, VOL)						
Logic Input High Voltage	V_{IH}		2			V
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input Current	I_{IN}				±1	µA

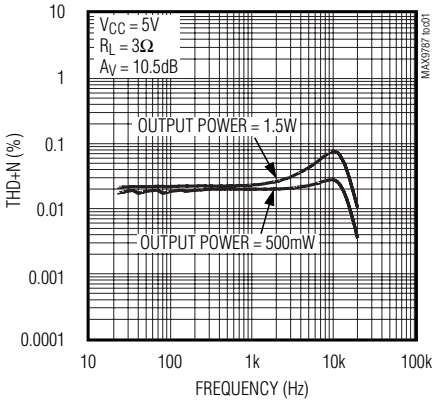
Note 1: All devices are 100% production tested at room temperature. All temperature limits are guaranteed by design.
Note 2: Guaranteed by design. Not production tested.
Note 3: PSRR is specified with the amplifier input connected to GND through C_{IN}.
Note 4: Output power levels are measured with the thin QFN's exposed paddle soldered to the ground plane.
Note 5: See Table 3 for details of the mute levels.
Note 6: The value of R_B dictates the minimum beep signal amplitude (see the *BEEP Input* section).

2.2W Stereo Audio Power Amplifier with Analog Volume Control

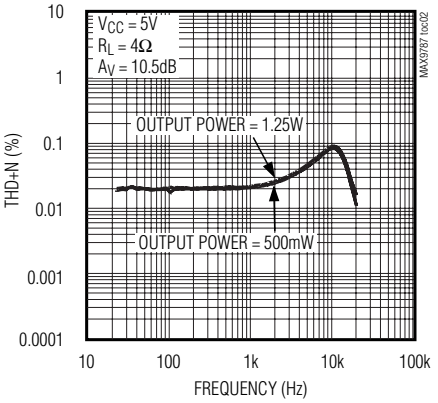
Typical Operating Characteristics

(Measurement BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

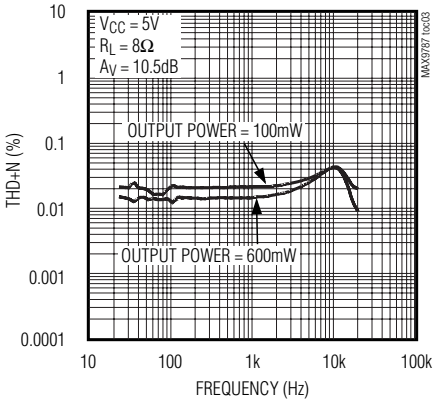
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



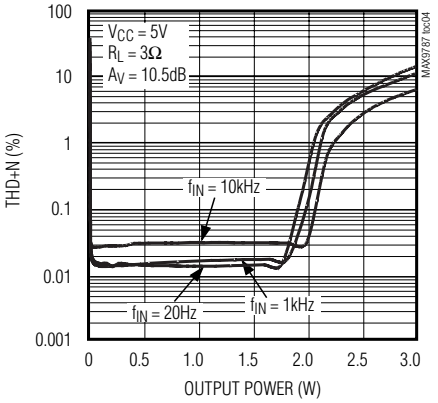
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



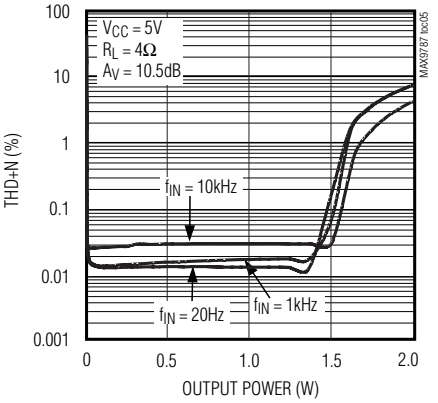
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



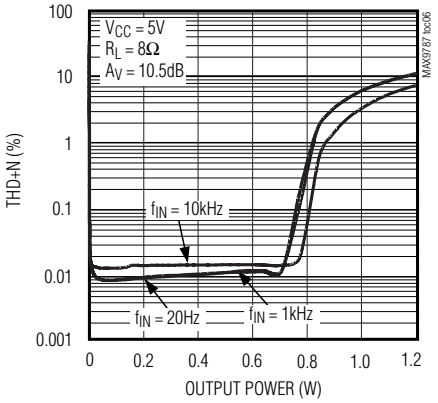
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



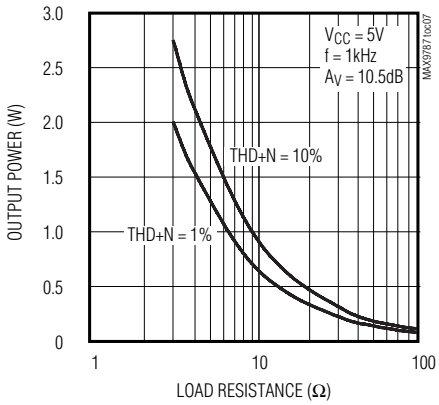
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



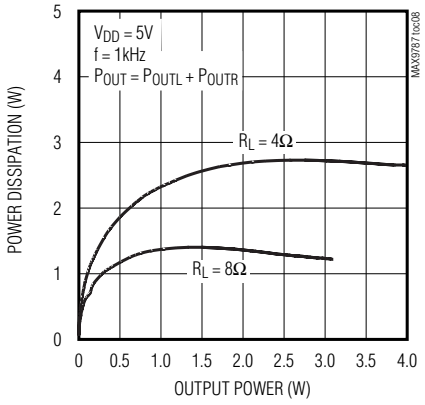
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



OUTPUT POWER vs. LOAD RESISTANCE



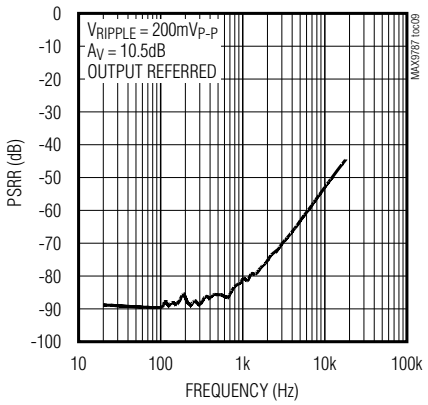
POWER DISSIPATION vs. OUTPUT POWER



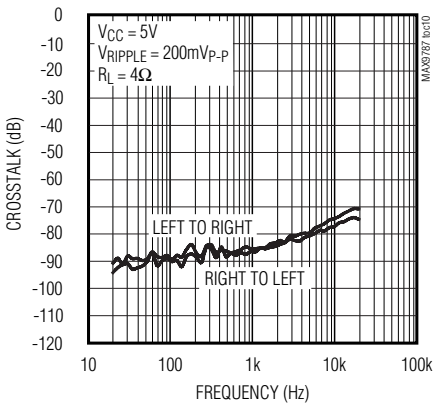
Typical Operating Characteristics (continued)

(Measurement BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

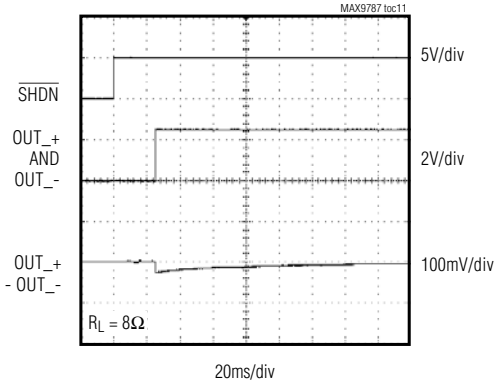
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



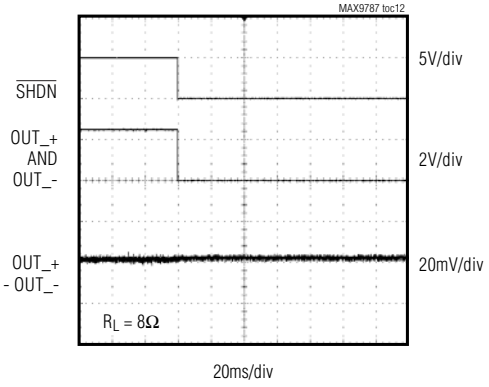
CROSSTALK vs. FREQUENCY



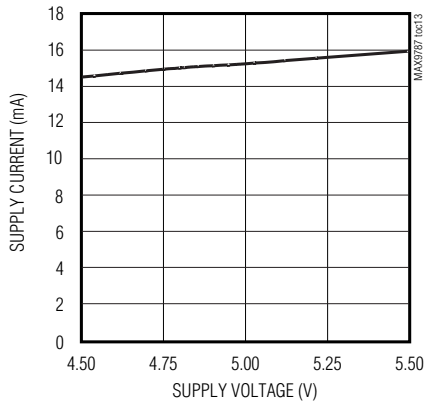
TURN-ON RESPONSE



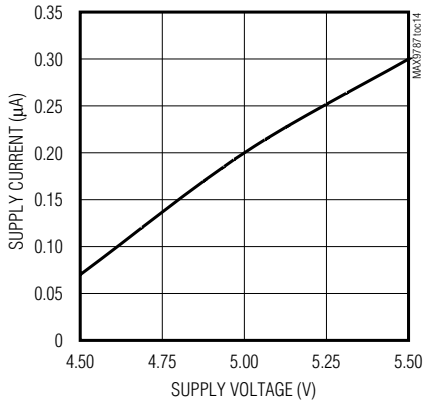
TURN-OFF RESPONSE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



2.2W Stereo Audio Power Amplifier with Analog Volume Control

Pin Description

PIN	NAME	FUNCTION
1	INL	Left-Channel Audio Input
2	BEEP	Audible Alert Beep Input
3, 19	PGND	Power Ground
4	OUTL+	Left-Channel Positive Speaker Output
5	OUTL-	Left-Channel Negative Speaker Output
6, 15, 16	PV_{DD}	Speaker Amplifier Power Supply
7	CPV_{DD}	Charge-Pump Power Supply
8	C1P	Charge-Pump Flying-Capacitor Positive Terminal
9	CPGND	Charge-Pump Ground
10	C1N	Charge-Pump Flying-Capacitor Negative Terminal
11	CPV_{SS}	Charge-Pump Output. Connect to V_{SS}.
12	V_{SS}	Amplifier Negative Power Supply
13, 14	N.C.	No Connection. Not internally connected.
17	OUTR-	Right-Channel Negative Speaker Output
18	OUTR+	Right-Channel Positive Speaker Output
20, 26	GND	Ground
21	BIAS	Common-Mode Bias Voltage. Bypass with a 1µF capacitor to GND.
22	$\overline{SHDN}$	Shutdown. Drive $\overline{SHDN}$ low to disable the device. Connect $\overline{SHDN}$ to V_{DD} for normal operation.
23	GAIN2	Gain Control Input 2
24	GAIN1	Gain Control Input 1
25	V_{DD}	Power Supply
27	INR	Right-Channel Audio Input
28	VOL	Analog Volume Control Input
EP	EP	Exposed Pad. Connect to GND.

Detailed Description

The MAX9787 combines a 2.2W bridge-tied load (BTL) speaker amplifier and an analog volume control, BEEP input, and four-level gain control. The MAX9787 features high 90dB, low 0.01% THD+N, industry-leading click-pop performance, and a low-power shutdown mode.

Each signal path consists of an input amplifier that sets the gain of the signal path, and feeds the speaker amplifier (Figure 1). The speaker amplifier uses a BTL architecture, doubling the voltage drive to the speakers and eliminating the need for DC-blocking capacitors. The output consists of two signals, identical in magnitude, but 180º out of phase.

An analog volume control varies the gain of the amplifiers based on the DC voltage applied at VOL. An undervoltage lockout prevents operation from an insufficient power supply. Click-and-pop suppression eliminates audible transients on startup and shutdown. The amplifiers include thermal-overload and short-circuit protection. An additional feature of the speaker amplifiers is that there is no phase inversion from input to output.

Charge Pump

The MAX9787 features a low-noise charge pump. The 550kHz switching frequency is well beyond the audio range, and does not interfere with the audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. Limiting the switching speed of the charge pump minimizes the di/dt noise caused by the parasitic bond wire and trace inductance. Although not typically required, additional high-frequency ripple attenuation can be achieved by increasing the size of C2 (see the *Typical Operating Circuit*).

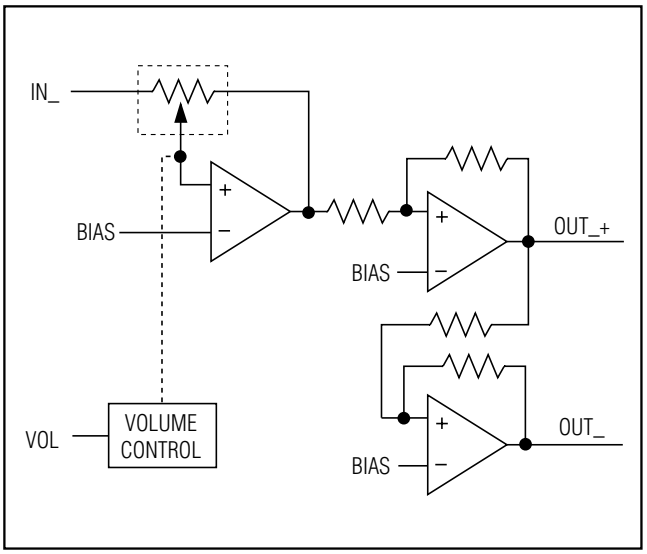


Figure 1. MAX9787 Signal Path

BIAS

The MAX9787 features an internally generated, power-supply independent, common-mode bias voltage of 1.8V referenced to GND. BIAS provides both click-and-pop suppression and sets the DC bias level for the amplifiers. Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section. No external load should be applied to BIAS. Any load lowers the BIAS voltage, affecting the overall performance of the device.

Gain Selection

The GAIN1 and GAIN2 inputs set the maximum gain of the speaker and amplifiers (Table 1). The gain of the device can vary based upon the voltage at VOL (see the *Analog Volume Control* section). However, the maximum gain cannot be exceeded.

Analog Volume Control (VOL)

An analog volume control varies the gain of the device in 31 discrete steps based upon the DC voltage applied to VOL. The input range of V_{VOL} is from 0 (full volume) to 0.858 x PV_{DD} (full mute), with example step sizes shown in Table 2. Connect the reference of the device driving VOL (Figure 2) to PV_{DD}. Since the volume control ADC is ratiometric to PV_{DD}, any changes in

Table 1. Gain Settings

GAIN2	GAIN1	SPEAKER MODE GAIN (dB)
0	0	6
0	1	7.5
1	0	9
1	1	10.5

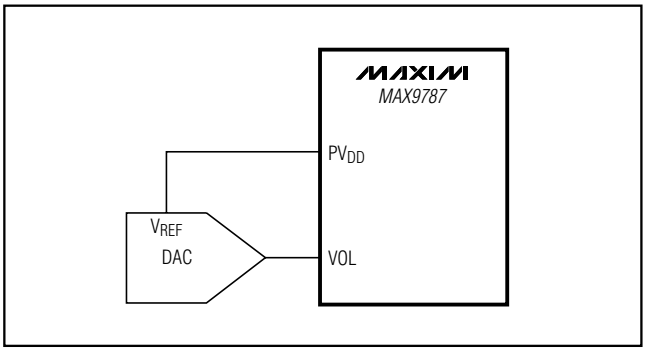


Figure 2. Volume Control Circuit

2.2W Stereo Audio Power Amplifier with Analog Volume Control

Table 2. Volume Levels

V_{VOL} (V)			SPEAKER MODE GAIN (dB)			
V_{MIN}*	V_{TYP}*	V_{MAX}*	GAIN1 = 0, GAIN2 = 0	GAIN1 = 1, GAIN2 = 0	GAIN1 = 0, GAIN2 = 1	GAIN1 = 1, GAIN2 = 1
0	0.370	0.742	6	7.5	9	10.5
0.742	0.800	0.860	5	7	8.5	10
0.860	0.915	0.977	4	6	8	9.5
0.977	1.035	1.094	3	5	7.5	9
1.094	1.150	1.211	1	4	7	8.5
1.211	1.265	1.328	-1	3	6	8
1.328	1.385	1.446	-3	1	5	7.5
1.446	1.500	1.563	-5	-1	4	7
1.563	1.620	1.680	-7	-3	3	6
1.680	1.735	1.797	-9	-5	1	5
1.797	1.855	1.914	-11	-7	-1	4
1.914	1.970	2.032	-13	-9	-3	3
2.032	2.090	2.149	-15	-11	-5	1
2.149	2.205	2.266	-17	-13	-7	-1
2.266	2.320	2.383	-19	-15	-9	-3
2.383	2.440	2.500	-21	-17	-11	-5
2.500	2.555	2.617	-23	-19	-13	-7
2.617	2.675	2.735	-25	-21	-15	-9
2.735	2.790	2.852	-27	-23	-17	-11
2.852	2.910	2.969	-29	-25	-9	-13
2.969	3.025	3.086	-31	-27	-21	-15
3.086	3.140	3.203	-33	-29	-23	-17
3.203	3.260	3.321	-35	-31	-2	-19
3.321	3.375	3.438	-37	-3	-27	-21
3.438	3.495	3.555	-41	-35	-29	-23
3.555	3.610	3.672	-45	-37	-31	-25
3.672	3.730	3.789	-48	-41	-33	-27
3.789	3.845	3.907	-53	-45	-35	-29
3.907	3.965	4.024	-57	-49	-37	-31
4.024	4.080	4.141	-61	-53	-41	-33
4.141	4.195	4.258	-65	-57	-45	-35
4.258	4.290	5.000	MUTE	MUTE	MUTE	MUTE

**Based on PV_{DD} = 5V*

PV_{DD} are negated. The gain step sizes are not constant; the step sizes are 0.5dB/step at the upper extreme, 2dB/step in the midrange, and 4dB/step at the lower extreme. Figure 3 shows the transfer function of the volume control for a 5V supply.

BEEP Input

An audible alert beep input (BEEP) accepts a mono system alert signal and mixes it into the stereo audio path. When the amplitude of $V_{BEEP(OUT)}$ exceeds 800mV_{P-P} (Figure 4) and the frequency of the beep signal is greater than 400Hz, the beep signal is mixed into the active audio path (speaker or headphone). If the signal at $V_{BEEP(OUT)}$ is either < 800mV_{P-P} or <400Hz, the BEEP signal is not mixed into the audio path. The amplitude of the BEEP signal at the device output is roughly the amplitude of $V_{BEEP(OUT)}$ times the gain of the selected signal path.

The input resistor (R_B) sets the gain of the BEEP input amplifier, and thus the amplitude of $V_{BEEP(OUT)}$. Choose R_B based on:

$$R_B \leq \frac{V_{IN} \times R_{INT}}{0.3}$$

where R_{INT} is the value of the BEEP amplifier feedback resistor (47kΩ) and V_{IN} is the BEEP input amplitude. Note that the BEEP amplifier can be set up as either an attenuator, if the original alert signal amplitude is too large, or set to gain up the alert signal if it is below 800mV_{P-P}. AC-couple the alert signal to BEEP. Choose the value of the coupling capacitor as described in the *Input Filtering* section. Multiple beep inputs can be summed (Figure 4).

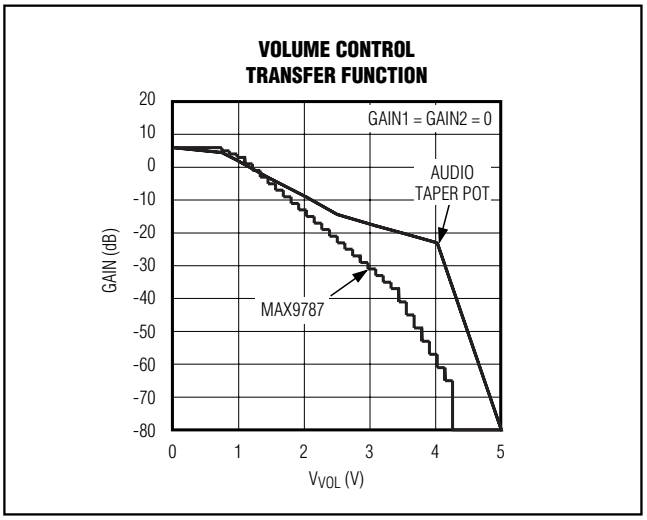


Figure 3. Volume Control Transfer Function

Shutdown

The MAX9787 features a 0.2µA, low-power shutdown mode that reduces quiescent current consumption and extends battery life. Driving $\overline{SHDN}$ low disables the drive amplifiers, bias circuitry, and charge pump, and drives BIAS and all outputs to GND. Connect $\overline{SHDN}$ to V_{DD} for normal operation.

Click-and-Pop Suppression

The MAX9787 speaker amplifiers feature Maxim's comprehensive, industry-leading click-and-pop suppression. During startup, the click-and-pop suppression circuitry eliminates any audible transient sources internal to the device. When entering shutdown, both amplifier outputs ramp to GND quickly and simultaneously.

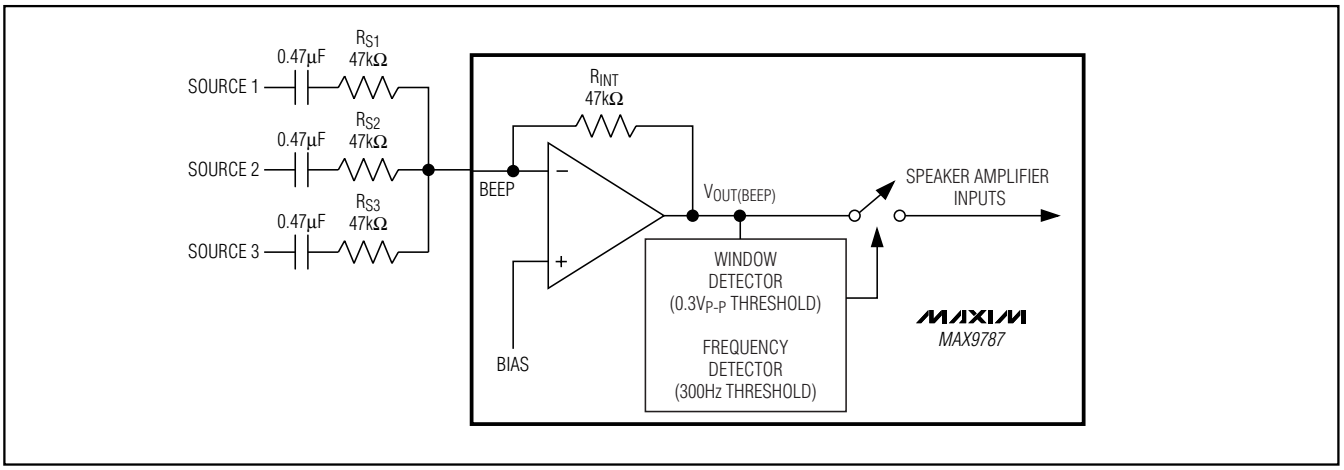


Figure 4. Beep Input

2.2W Stereo Audio Power Amplifier with Analog Volume Control

Applications Information

BTL Speaker Amplifiers

The MAX9787 features speaker amplifiers designed to drive a load differentially, a configuration referred to as bridge-tied load (BTL). The BTL configuration (Figure 5) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. Thus, the device's differential gain is twice the closed-loop gain of the input amplifier. The effective gain is given by:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

Substituting 2 X $V_{OUT(P-P)}$ into the following equation yields four times the output power due to double the output voltage:

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}}$$

$$P_{OUT} = \frac{V_{RMS}^2}{R_L}$$

Since the differential outputs are biased at midsupply, there is no net DC voltage across the load. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large and expensive, can consume board space, and can degrade low-frequency performance.

Power Dissipation and Heat Sinking

Under normal operating conditions, the MAX9787 can dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* under Continuous Power Dissipation, or can be calculated by the following equation:

$$P_{DISSPKG(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. For example, θ_{JA} of the TQFN package is +42°C/W. For optimum power dissipation, the exposed paddle of the package should be connected to the ground plane (see the *Layout and Grounding* section).

For 8Ω applications, the worst-case power dissipation occurs when the output power is 1.1W/channel, resulting in a power dissipation of about 1W. In this case, the TQFN packages can be used without violating the maximum power dissipation or exceeding the thermal protection threshold.

Output Power

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration.

If the power dissipation for a given application exceeds the maximum allowed for a given package, either reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heatsinking to the device. Large output, supply, and ground PC board traces improve the maximum power dissipation in the package.

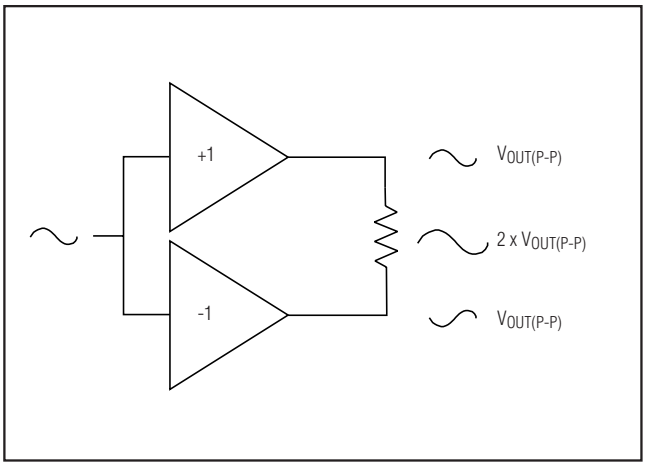


Figure 5. Bridge-Tied Load Configuration

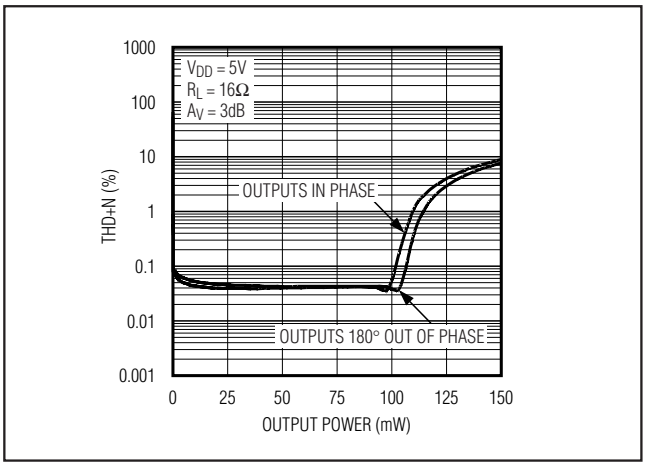


Figure 6. Total Harmonic Distortion Plus Noise vs. Output Power with Inputs In/Out of Phase

Table 3. Suggested Capacitor Manufacturers

SUPPLIER	PHONE	FAX	WEBSITE
Taiyo Yuden	800-348-2496	847-925-0899	www.t-yuden.com
TDK	807-803-6100	847-390-4405	www.component.tdk.com

Thermal-overload protection limits total power dissipation in these devices. When the junction temperature exceeds +160°C, the thermal-protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 15°C. This results in a pulsing output under continuous thermal-overload conditions as the device heats and cools.

Power Supplies

The MAX9787 speaker amplifiers are powered from PV_{DD}. PV_{DD} ranges from 4.5V to 5.5V. V_{SS} is the negative supply of the amplifiers. Connect V_{SS} to CPV_{SS}. The charge pump is powered by CPV_{DD}. CPV_{DD} should be the same potential as PV_{DD}. The charge pump inverts the voltage at CPV_{DD}, and the resulting voltage appears at CPV_{SS}. The remainder of the device is powered by V_{DD}.

Component Selection

Input Filtering

The input capacitor (C_{IN}), in conjunction with the amplifier input resistance (R_{IN}), forms a highpass filter that removes the DC bias from an incoming signal (see the *Typical Operating Circuit*). The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

R_{IN} is the amplifier's internal input resistance value given in the *Electrical Characteristics*. Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors with low-voltage coefficient dielectrics, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

BIAS Capacitor

BIAS is the output of the internally generated DC bias voltage. The BIAS bypass capacitor, C_{BIAS}, improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless, startup/shutdown DC bias waveforms for the speaker amplifiers. Bypass BIAS with a 1µF capacitor to GND.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric. Table 4 lists suggested manufacturers.

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the load regulation and output resistance of the charge pump. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics*. Above 2.2µF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Output Capacitor (C2)

The output capacitor value and ESR directly affect the ripple at CPV_{SS}. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics*.

2.2W Stereo Audio Power Amplifier with Analog Volume Control

CPV_{DD} Bypass Capacitor

The CPV_{DD} bypass capacitor (C3) lowers the output impedance of the power supply and reduces the impact of the MAX9787's charge-pump switching transients. Bypass CPV_{DD} with C3, the same value as C1, and place it physically close to the CPV_{DD} and PGND (refer to the MAX9750 Evaluation Kit for a suggested layout).

Powering Other Circuits from a Negative Supply

An additional benefit of the MAX9787 is the internally generated negative supply voltage (CPV_{SS}). CPV_{SS} provides the negative supply for the amplifiers. It can also be used to power other devices within a design. Current draw from CPV_{SS} should be limited to 5mA; exceeding this affects the operation of the amplifier. A typical application is a negative supply to adjust the contrast of LCD modules.

When considering the use of CPV_{SS} in this manner, note that the charge-pump voltage of CPV_{SS} is roughly proportional to PV_{DD} and is not a regulated voltage. The charge-pump output impedance plot appears in the *Typical Operating Characteristics*.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance, as well as route head away from the device. Good grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect CPGND, PGND, and GND together at a single point on the PC board. Route CPGND and all traces that carry switching transients away from GND, PGND, and the traces and components in the audio signal path.

Connect all components associated with the charge pump (C2 and C3) to the CPGND plane. Connect V_{SS} and CPV_{SS} together at the device. Place the charge-pump capacitors (C1, C2, and C3) as close to the device as possible. Bypass PV_{DD} with a 0.1µF capacitor to GND. Place the bypass capacitors as close to the device as possible.

Use large, low-resistance output traces. As load impedance decreases, the current drawn from the device outputs increase. At higher current, the resistance of the output traces decrease the power delivered to the load. For example, when compared to a 0Ω trace, a 100mΩ trace reduces the power delivered to a 4Ω load from 2.1W to 2W. Large output, supply, and GND traces also improve the power dissipation of the device.

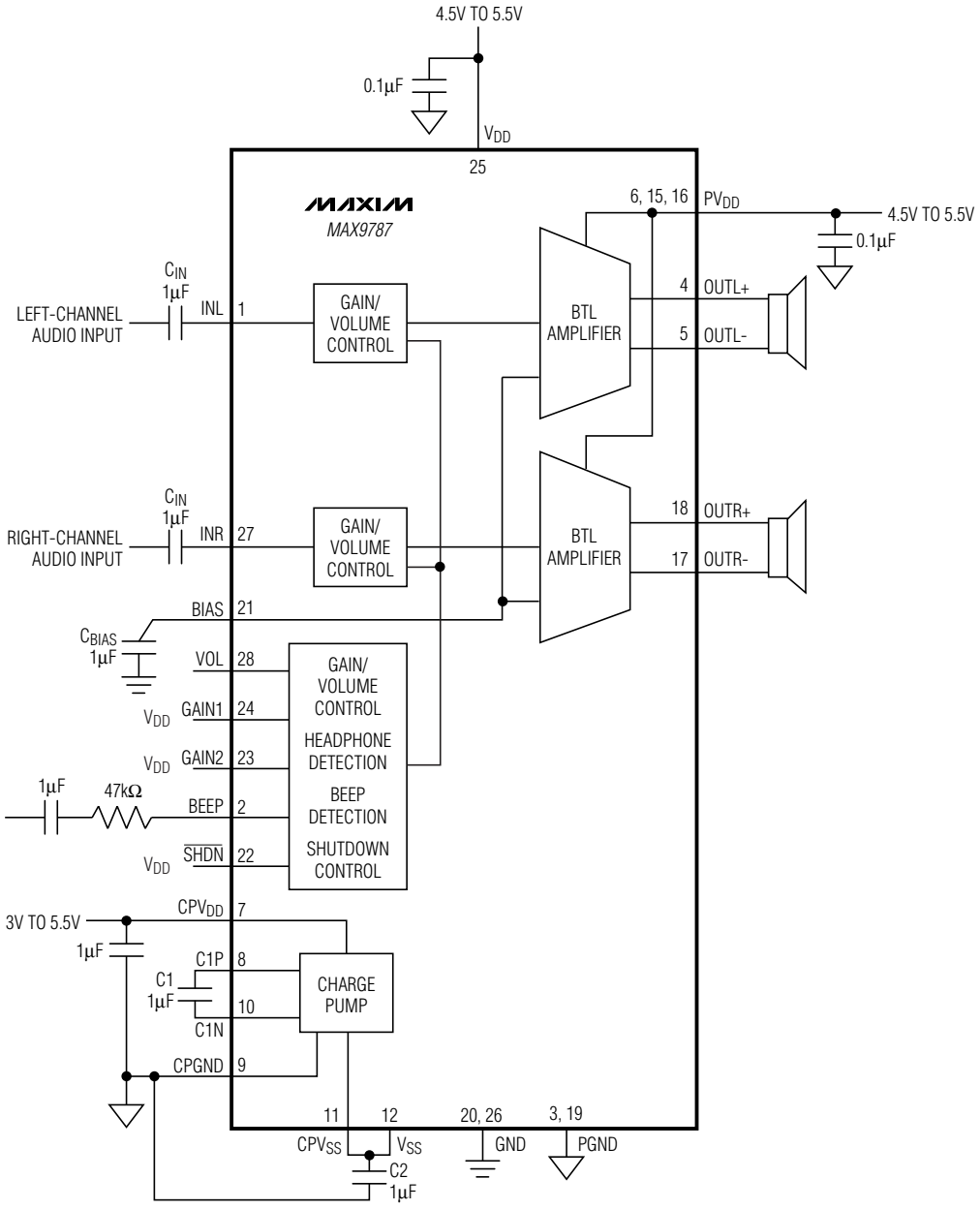
The MAX9787 thin QFN features and exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a direct heat conduction path from the die to the PC board. Connect the exposed thermal pad to GND by using a large pad and multiple vias to the GND plane.

Chip Information

TRANSISTOR COUNT: 9591

PROCESS: BiCMOS

Block Diagram

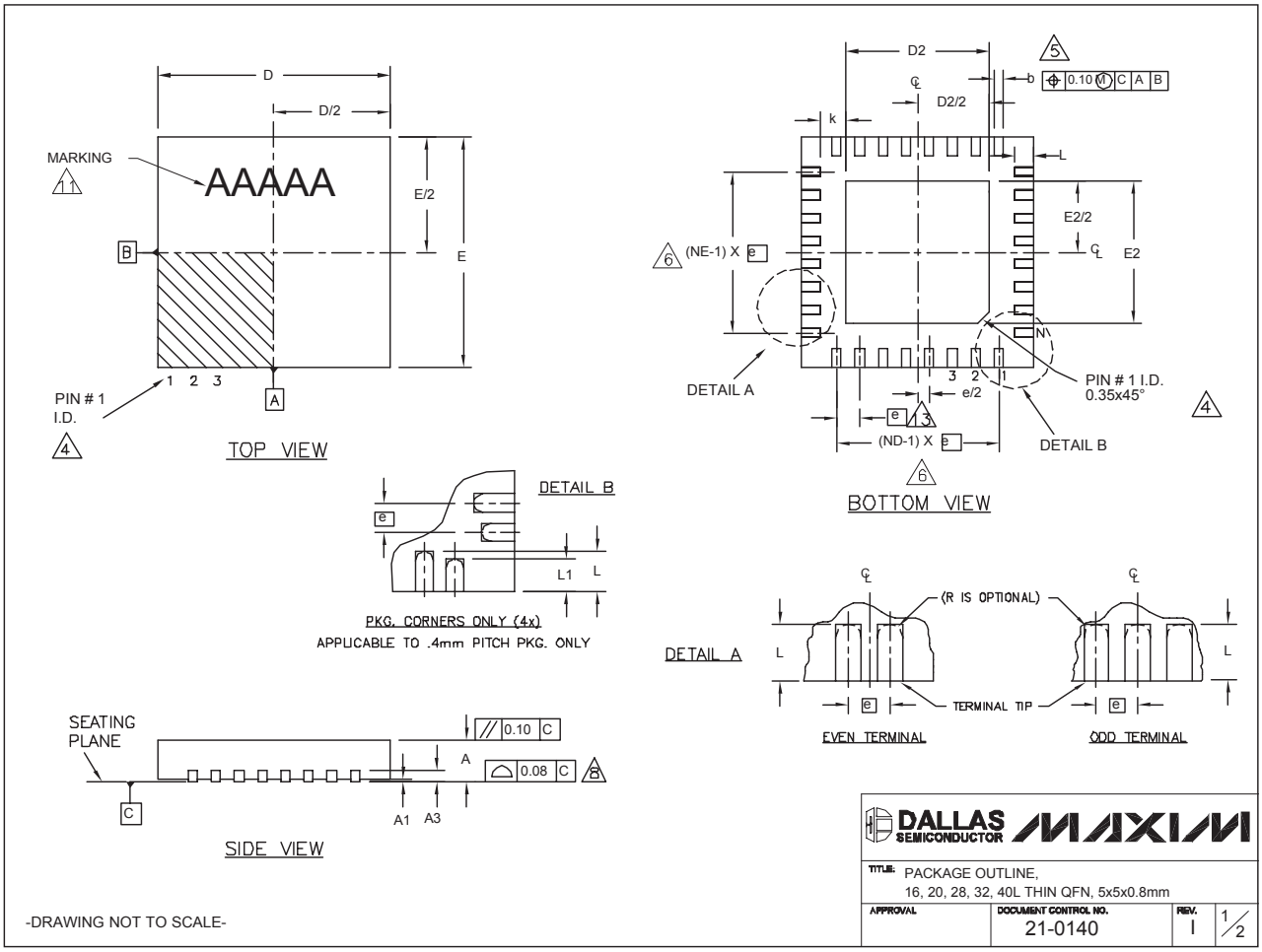


2.2W Stereo Audio Power Amplifier with Analog Volume Control

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60	
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L exceptions	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-3	3.00	3.10	3.20	**3**.00	3.10	.20	**	YES
T3255-4	3.00	3.10	3.20	**3**.00	3.10	.20	**	NO
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	I	2/2