19-1028; Rev 0; 11/07

EVALUATION KIT AVAILABLE

1.8V DirectDrive Video Filter Amplifier with Load Detection and Dual SPST Analog Switches

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General Description

The MAX9507 amplifies and filters standard-definition video signals and only consumes 5.8mW quiescent power and 11.7mW average power. The MAX9507 leverages Maxim's DirectDrive™ technology to generate a clean, internal negative supply. Combining the internal negative power supply with the external positive 1.8V supply, the MAX9507 is able to drive a 2V_{P-P} video signal into a 150Ω load.

The MAX9507 provides an I^2C interface for easy configuration and access to the load status. The MAX9507 can detect, report, and act upon the change of a video load. This feature helps reduce overall power consumption by allowing the system to turn on the video encoder and driver only when a video load is connected to the MAX9507.

With a high power-supply rejection ratio (47dB at 100kHz), the MAX9507 can be powered directly from a 1.8V digital supply. The two integrated single-pole/single-throw (SPST) analog switches are ideal for routing audio, video, or digital signals.

The input of the MAX9507 can be directly connected to the output of a video DAC. The MAX9507 also features a transparent input sync-tip clamp, allowing AC-coupling of input signals with different DC biases.

The MAX9507 has an internal fixed gain of 8. The input full-scale video signal is nominally 0.25V_{P-P}, and the output full-scale video signal is nominally 2V_{P-P}.

Features

- **1.8V or 2.5V Single-Supply Operation**
- **Low Power Consumption (5.8mW Quiescent, 11.7mW Average)**
- **Video Load Detection**
- **DirectDrive Sets Video Output Black Level Near Ground**
- **Dual SPST Analog Switches**
- **Transparent Input Sync-Tip Clamp**
- **I^2C Control**

Applications

Mobile Phones

Portable Media Players (PMP)

Ordering Information

PART	PIN-PACKAGE	PKG CODE	TOP MARK
MAX9507ATE+	16 TQFN-EP*	T1633+4	AFH

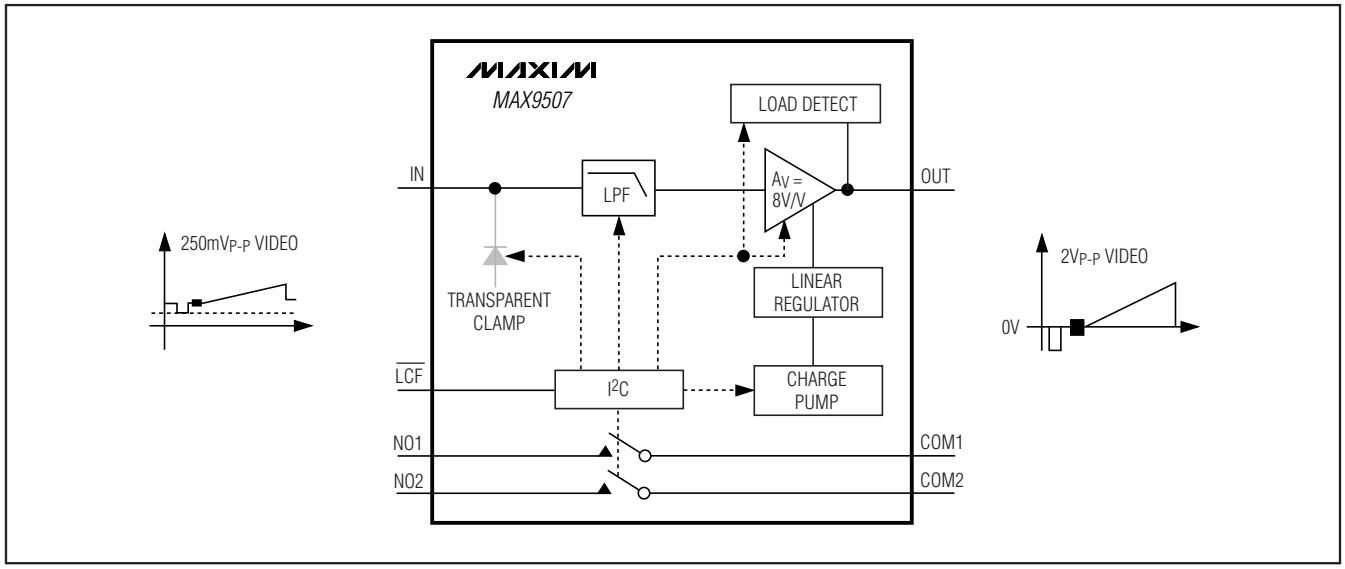
Note: *This device is specified over the -40°C to +125°C operating temperature range.*

+Denotes lead-free package.

**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to GND.)
V_{DD} .....-0.3V to +3V
CPGND .....-0.1V to +0.1V
IN .....-0.3V to (V_{DD} + 0.3V)
OUT, NO_,
COM_ .....(The greater of V_{SS} and -1V) to (V_{DD} + 0.3V)
SDA, SCL, DEV_ADDR, $\overline{LCF}$ .....-0.3V to +4V
C1P .....-0.3V to (V_{DD} + 0.3V)
C1N .....(V_{SS} - 0.3V) to +0.3V
V_{SS} .....-3V to +0.3V

Duration of OUT Short Circuit
to V_{DD}, GND, and V_{SS} .....Continuous
Continuous Current
IN, SDA, SCL, DEV_ADDR, $\overline{LCF}$ .....±20mA
NO_, COM_ .....±100mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 15.6mW/°C above +70°C) 1250mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +1.8V, GND = 0V, OUT has R_L = 150Ω connected to GND, transparent sync-tip clamp enabled, C_1 = C_2 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR		1.700		2.625	V
Supply Current	I_{DD}	No load, full operation mode	Filter enabled		3.1	5.4	mA
			Filter disabled		2.9	5.1	
Sleep-Mode Supply Current		No load			3		µA
Shutdown Supply Current	$I_{\overline{SHDN}}$				0.2	10	µA
Switch-Only Supply Current		Shutdown mode			0.2		µA
		Charge-pump-only mode			520		
Output Load Detect Threshold		R_L to GND, $V_{SYNC-TIP}$ < 13mV		200			Ω
DC-COUPLED INPUT							
Input Voltage Range		Guaranteed by output-voltage swing	1.7V ≤ V_{DD} ≤ 2.625V	0		262.5	mV
			2.375V ≤ V_{DD} ≤ 2.625V	0		325	
Input Current	I_B	IN = 130mV			2	3.2	µA
Input Resistance	R_{IN}	10mV ≤ IN ≤ 250mV			280		kΩ
Output Level		IN = 80mV		-75	+5	+75	mV
AC-COUPLED INPUT							
Sync-Tip Clamp Level	V_{CLP}	C_{IN} = 0.1µF		-8	0	+11	mV
Input-Voltage Swing		Guaranteed by output-voltage swing	1.7V ≤ V_{DD} ≤ 2.625V			252.5	mV_{P-P}
			2.375V ≤ V_{DD} ≤ 2.625V			325	
Sync Crush		Percentage reduction in sync pulse at output, R_{SOURCE} = 37.5Ω, C_{IN} = 0.1µF			1.6		%
Input Clamping Current		IN = 130mV			2	3.2	µA
Line-Time Distortion		C_{IN} = 0.1µF			0.2		%
Minimum Input Source Resistance					25		Ω
Output Level		IN = 80mV		-75	+5	+75	mV

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.8V, GND = 0V, OUT has R_L = 150Ω connected to GND, transparent sync-tip clamp enabled, C_1 = C_2 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
DC Voltage Gain	A_V	Guaranteed by output-voltage swing (Note 2)		7.84	8	8.16	V/V
Output-Voltage Swing		1.7V ≤ V_{DD} ≤ 2.625V	0V ≤ V_{IN} ≤ 262.5mV, DC-coupled input	2.058	2.1	2.142	V_{P-P}
			0V ≤ V_{IN} ≤ 252.5mV_{P-P}, AC-coupled input	1.979	2.02	2.061	
		2.375V ≤ V_{DD} ≤ 2.625V, 0V ≤ V_{IN} ≤ 325mV		2.548	2.6	2.652	
Power-Supply Rejection Ratio	PSRR	1.7V ≤ V_{DD} ≤ 2.625V, measured between 75Ω load resistors		46	60		dB
Shutdown Input Resistance		0V ≤ IN ≤ V_{DD}			2.8		MΩ
Output Resistance	R_{OUT}	OUT = 0V, -5mA ≤ I_{LOAD} ≤ +5mA			0.1		Ω
Shutdown Output Resistance		0V ≤ OUT ≤ V_{DD}			32		MΩ
Shutdown OUT Leakage Current						1	µA
Output Short-Circuit Current		Sourcing			82		mA
		Sinking			32		
AC CHARACTERISTICS (FILTER							
Standard-Definition Reconstruction Filter		OUT = 2V_{P-P}, reference frequency is 100kHz	±1dB passband		7.5		MHz
			f = 5.5MHz		0		dB
			f = 9.3MHz		-3		
			f = 27MHz		-49		
Differential Gain	DG	f = 3.58MHz			0.63		%
		f = 4.43MHz			0.93		
Differential Phase	DP	f = 3.58MHz			0.50		Degrees
		f = 4.43MHz			0.63		
2T Pulse-to-Bar K Rating		2T = 200ns, bar time is 18µs, the beginning 2.5% and the ending 2.5% of the bar time is ignored			0.1		K%
2T Pulse Response		2T = 200ns			0.3		K%
2T Bar Response		2T = 200ns, bar time is 18µs, the beginning 2.5% and the ending 2.5% of the bar time is ignored			0.2		K%
Nonlinearity		5-step staircase			0.1		%
Group-Delay Distortion		100kHz ≤ f ≤ 5MHz, OUT = 2V_{P-P}			21		ns
Peak Signal to RMS Noise		100kHz ≤ f ≤ 5MHz			65		dB
Power-Supply Rejection Ratio	PSRR	f = 100kHz, 100mV_{P-P}			47		dB
Output Impedance		f = 5MHz, IN = 80mV			7.5		Ω
Shutdown OUT-to-IN Isolation		f < 5.5MHz			102		dB
Shutdown IN-to-OUT Isolation		f < 5.5MHz			98		dB

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.8V, GND = 0V, OUT has R_L = 150Ω connected to GND, transparent sync-tip clamp enabled, C_1 = C_2 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (FILTER							
Small-Signal -3dB Bandwidth		OUT = 100mV$_{P-P}$			40.7		MHz
Large-Signal -3dB Bandwidth		OUT = 2V$_{P-P}$			9.8		MHz
Small-Signal 1dB Flatness		OUT = 100mV$_{P-P}$			32.8		MHz
Large-Signal 1dB Flatness		OUT = 2V$_{P-P}$			7.2		MHz
Slew Rate		OUT = 2V step			35		V/µs
Settling Time to 0.1%		OUT = 2V step			230		ns
Differential Gain	DG	f = 3.58MHz			0.63		%
		f = 4.43MHz			0.94		
Differential Phase	DP	f = 3.58MHz			0.50		Degrees
		f = 4.43MHz			0.64		
2T Pulse-to-Bar K Rating		2T = 200ns, bar time is 18µs, the beginning 2.5% and the ending 2.5% of the bar time is ignored			0.1		K%
2T Pulse Response		2T = 200ns			0.2		K%
2T Bar Response		2T = 200ns, bar time is 18µs, the beginning 2.5% and the ending 2.5% of the bar time is ignored			0.2		K%
Nonlinearity		5-step staircase			0.1		%
Group-Delay Distortion		100kHz ≤ f ≤ 5MHz, OUT = 2V$_{P-P}$			15		ns
Peak Signal to RMS Noise		100kHz ≤ f ≤ 5MHz			69		dB
Power-Supply Rejection Ratio	PSRR	f = 100kHz, 100mV$_{P-P}$			42		dB
Output Impedance		f = 5MHz, IN = 80mV			7.5		Ω
Shutdown OUT-to-IN Isolation		f < 5.5MHz			102		dB
Shutdown IN-to-OUT Isolation		f < 5.5MHz			98		dB
CHARGE PUMP							
Switching Frequency				325	625	1150	kHz
ANALOG SWITCHES							
On-Resistance (Note 3)	R_{ON}	$I_{COM\_}$ = 10mA, $V_{NO\_}$ = 0V	Normal range		1.2	2.2	Ω
			Extended range		1.2	2.2	
On-Resistance Flatness (Notes 3, 4)	$R_{FLAT(ON)}$	$I_{COM\_}$ = 10mA	Normal range, $V_{NO\_}$ = 0V, 1V, V_{DD}		2.3		Ω
			Extended range, $V_{NO\_}$ = -0.9V, 0V, +1.2V, V_{DD}		0.3	1.1	
NO_ Off-Leakage Current Normal Range	$I_{NO\_(OFF)N}$	V_{DD} = 2.625V, $V_{COM\_}$ = 0.3V, 2.3V; $V_{NO\_}$ = 2.3V, 0.3V; T_A = +25°C (Notes 3, 5)		-100		+100	nA
COM_ On-Leakage Current Normal Range	$I_{COM\_(ON)N}$	V_{DD} = 2.625V, $V_{NO\_}$ = high-Z, $V_{COM\_}$ = 0.3V, 2.3V; T_A = +25°C (Notes 3, 5)		-100		+100	nA
NO_ Off-Leakage Current, Extended Range	$I_{NO\_(OFF)E}$	V_{DD} = 2.625V, $V_{COM\_}$ = -0.6V, +2.3V; $V_{NO\_}$ = +2.3V, -0.6V; T_A = +25°C (Notes 3, 5)		-100		+100	nA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.8V, GND = 0V, OUT has R_L = 150Ω connected to GND, transparent sync-tip clamp enabled, C_1 = C_2 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COM_ On-Leakage Current, Extended Range	$I_{COM\_(ON)E}$	V_{DD} = 2.625V, $V_{NO\_}$ = high-Z, $V_{COM\_}$ = -0.6V, +2.3V; T_A = +25°C (Notes 3, 5)		-100		+100	nA
Turn-On Time	t_{ON}	$V_{NO\_}$ = 0.9V, R_L = 300Ω, C_L = 35pF, Figure 1 (Note 6)			310		ns
Turn-Off Time	t_{OFF}	$V_{NO\_}$ = 0.9V, R_L = 300Ω, C_L = 35pF, Figure 1 (Note 6)			372		ns
Charge Injection	Q	V_{GEN} = 0.9V, R_{GEN} = 0Ω, C_L = 1nF, Figure 2			60		pC
Off-Isolation	V_{ISO}	$V_{NO\_}$ = 1V_{P-P}, R_L = 50Ω, C_L = 5pF, Figure 1	f = 10MHz		49		dB
			f = 1MHz		69		
On-Channel -3dB Bandwidth	BW	$V_{NO\_}$ = 0dBm, R_{SOURCE} = 50Ω, R_L = 50Ω, C_L = 5pF, Figure 1			280		MHz
Total Harmonic Distortion	THD	$V_{COM\_}$ = 1V_{P-P}, R_L = 600Ω			0.037		%
Charge-Pump Noise		Extended range, R_L = 50Ω			1.2		mV_{P-P}
NO_ Off-Capacitance	C_{OFF}	f = 1MHz			21		pF
Switch On-Capacitance	C_{ON}	f = 1MHz			53		pF
CROSSTALK							
Switch to Switch		Switch 1, 2 closed; $V_{NO\_}$ = 1V_{P-P}, R_L = 50Ω, C_L = 5pF, Figure 1	f = 10MHz		-71		dB
			f = 1MHz		-88		
NO_ to OUT		Switch 1, 2 open; video circuitry enabled, $V_{NO\_}$ = 1V_{P-P}	f = 10MHz		-44		dB
			f = 1MHz		-78		
OUT to NO_		Switch 1, 2 closed; video circuitry enabled, f = 20kHz, OUT = 2V_{P-P}, R_L = 50Ω, C_L = 5pF			-94		dB
IN to COM_		Switch 1, 2 closed; video circuitry disabled, f = 20kHz, IN = 0.25V_{P-P}, R_L = 600Ω			-89		dB
OUT to COM_		Switch 1, 2 closed; video circuitry enabled, f = 20kHz, OUT = 2V_{P-P}, R_L = 50Ω, C_L = 5pF			-94		dB
CMOS DIGITAL INPUTS (SDA, SCL, DEV_ADDR)							
Input Low Voltage	V_{IL}					0.3 x V_{DD}	V
Input High Voltage	V_{IH}			0.7 x V_{DD}			V
Input Hysteresis					275		mV
Input Leakage Current	I_{IL}, I_{IH}			-10		+10	µA
Input Capacitance	C_{IN}				15		pF

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.8V, GND = 0V, OUT has R_L = 150Ω connected to GND, transparent sync-tip clamp enabled, C_1 = C_2 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (SDA, $\overline{LCF}$)							
Output Low Voltage	V_{OL}	I_{OL} = 3mA	V_{DD} > 2V			0.4	V
			V_{DD} < 2V			0.2 x V_{DD}	
Output High Leakage Current	I_{OH}	V_{OUT} = V_{DD}				1	µA
SERIAL INTERFACE TIMING (Figure 3)							
Serial Clock Frequency	f_{SCL}			0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}			1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$			0.6			µs
SCL Pulse-Width Low	t_{LOW}			1.3			µs
SCL Pulse-Width High	t_{HIGH}			0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$			0.6			µs
Data Hold Time	$t_{HD,DAT}$			0		900	ns
Data Setup Time	$t_{SU,DAT}$			100			ns
Bus Capacitance	C_B					400	pF
SDA and SCL Receiving Rise Time	t_R	(Note 7)		20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 7)		20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	(Note 7)	V_{DD} = 1.7V	20 + 0.1C_B		250	ns
			V_{DD} = 2.625V	0		250	
Setup Time for STOP Condition	$t_{SU,STO}$			0.6			µs
Pulse Width of Suppressed Spike	t_{SP}			0		50	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Voltage gain (A_V) is a two-point measurement in which the output-voltage swing is divided by the input-voltage swing.

Note 3: Normal range: charge pump disabled. Extended range: charge pump enabled. In extended range mode, the switch input can swing from -0.9V to V_{DD}.

Note 4: Flatness is defined as the difference between the maximum and minimum values of on-resistance as measured at the specified voltages.

Note 5: Not production tested, guaranteed by design.

Note 6: t_{ON} and t_{OFF} are measured from the end of the writing of register 0x00 until COM reaches 90% of the output voltage. See Figure 1.

Note 7: C_B is in picofarads.

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Test Circuits/Timing Diagrams

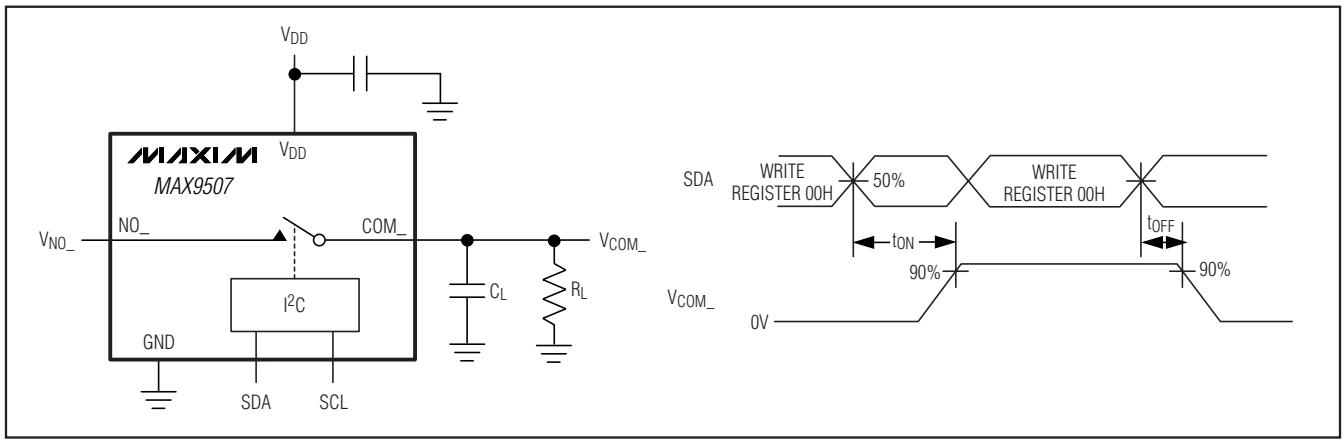

Figure 1. Analog Switch Test Circuit

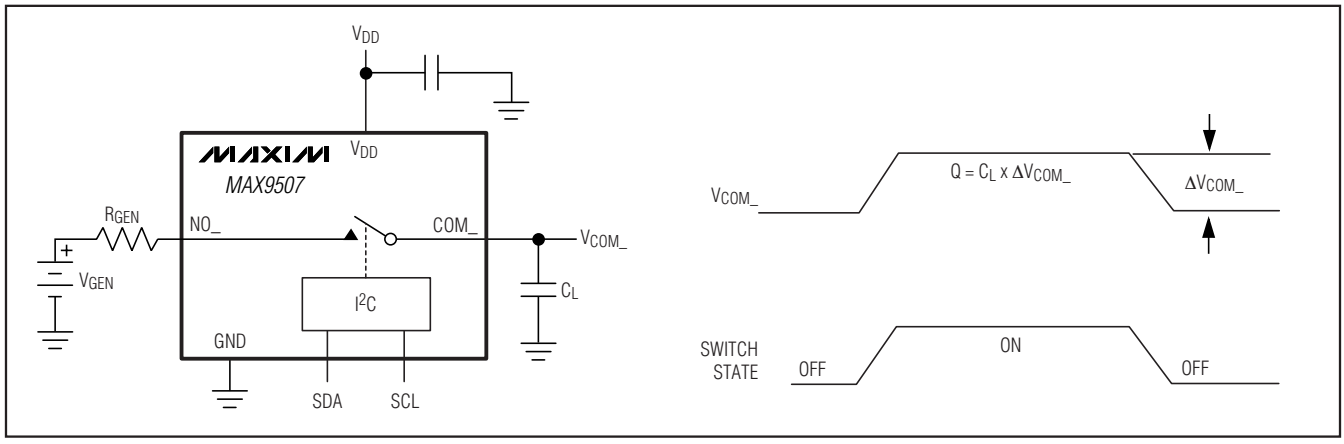

Figure 2. Analog Switch Charge Injection

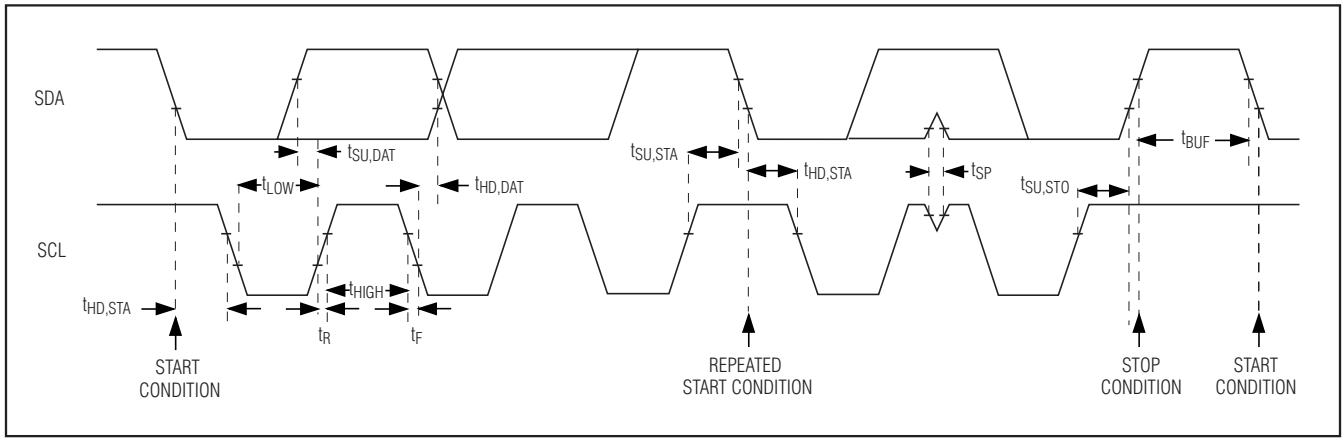

Figure 3. I²C Serial-Interface Timing Diagram

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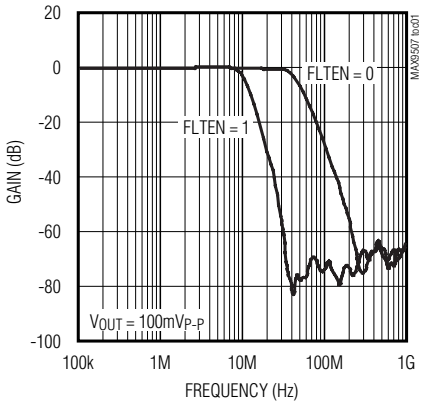
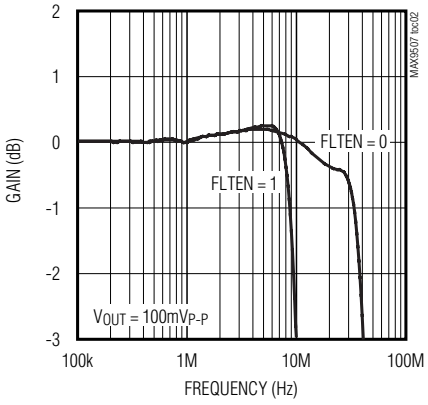
Typical Operating Characteristics

(V_{DD} = +1.8V, GND = 0V, mode 2 (Table 6), video output has R_L = 150Ω connected to GND, video filter enabled, T_A = +25°C, unless otherwise noted.)

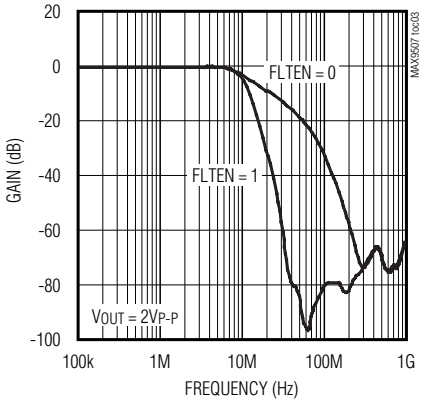
SMALL-SIGNAL GAIN vs. FREQUENCY



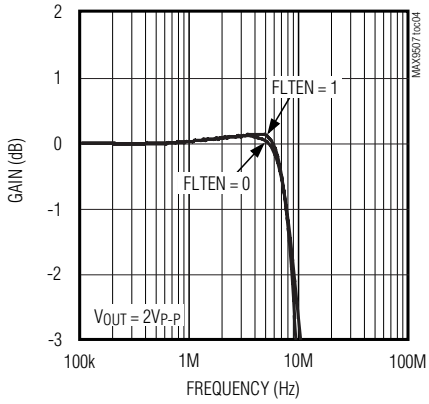
SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



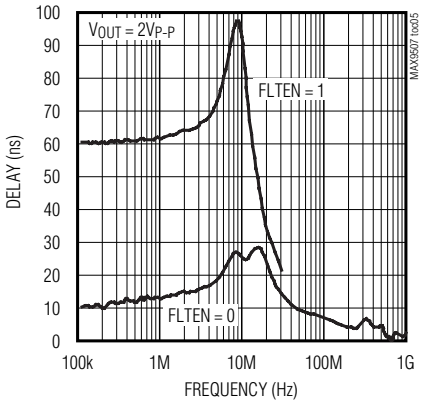
LARGE-SIGNAL GAIN vs. FREQUENCY



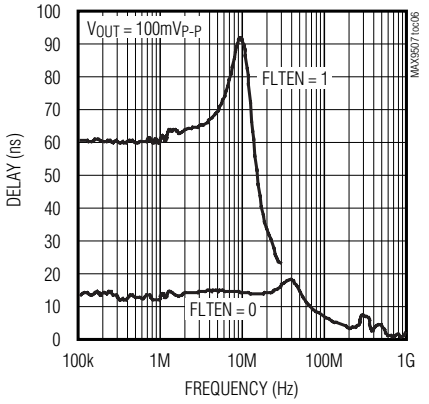
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



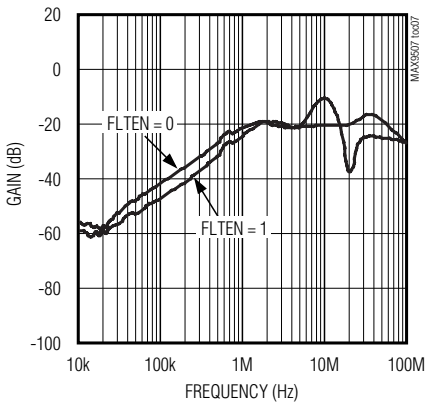
LARGE-SIGNAL GROUP DELAY vs. FREQUENCY



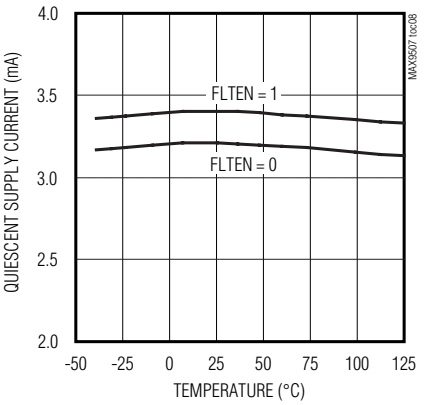
SMALL-SIGNAL GROUP DELAY vs. FREQUENCY



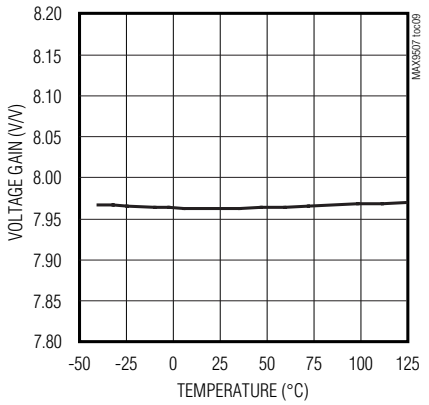
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



VOLTAGE GAIN vs. TEMPERATURE



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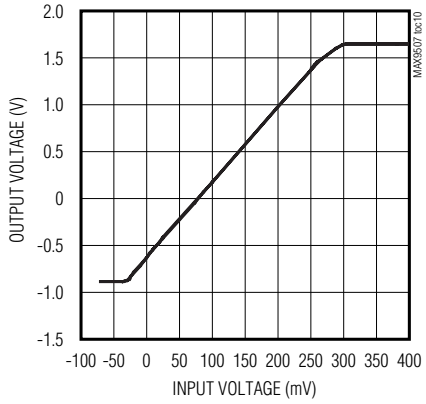
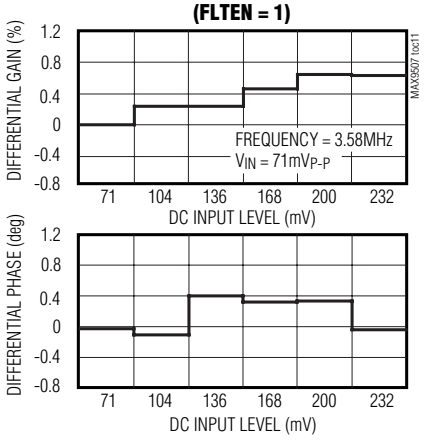
Typical Operating Characteristics (continued)

(V_{DD} = +1.8V, GND = 0V, mode 2 (Table 6), video output has R_L = 150Ω connected to GND, video filter enabled, T_A = +25°C, unless otherwise noted.)

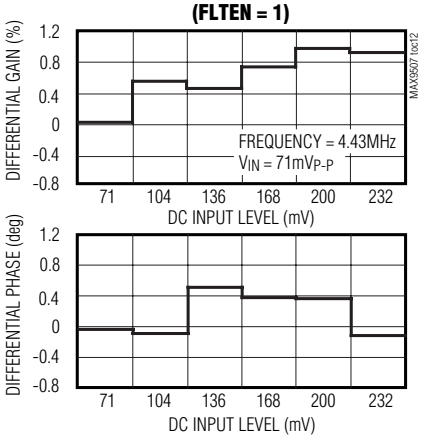
OUTPUT VOLTAGE vs. INPUT VOLTAGE



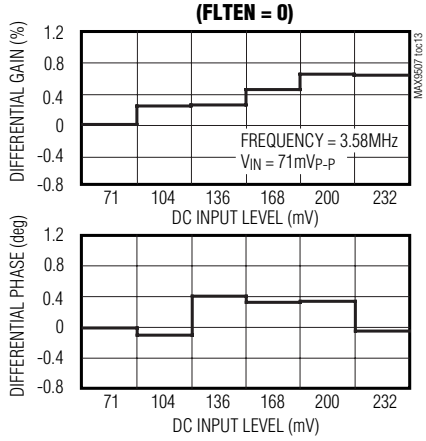
DIFFERENTIAL GAIN AND PHASE (FLTEN = 1)



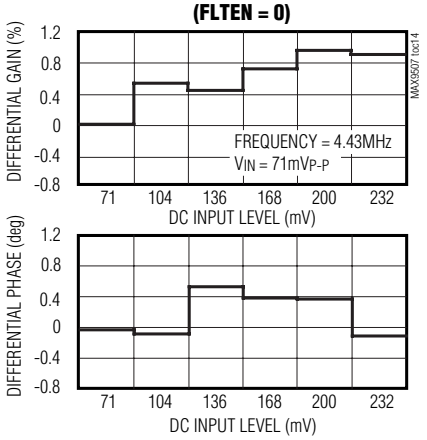
DIFFERENTIAL GAIN AND PHASE (FLTEN = 1)



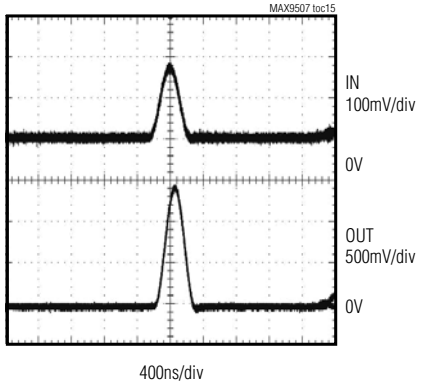
DIFFERENTIAL GAIN AND PHASE (FLTEN = 0)



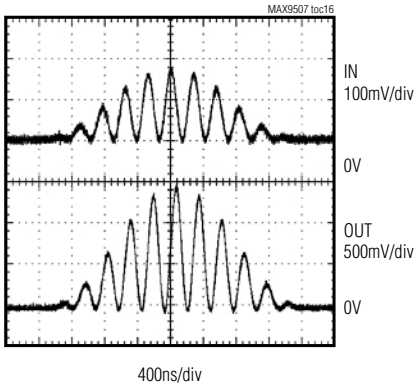
DIFFERENTIAL GAIN AND PHASE (FLTEN = 0)



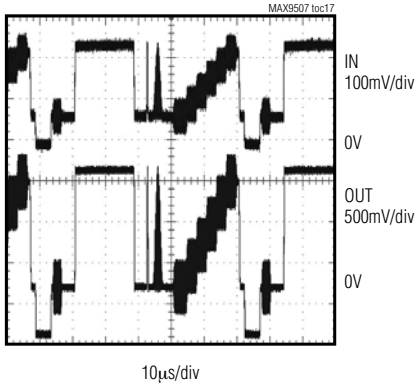
2T RESPONSE



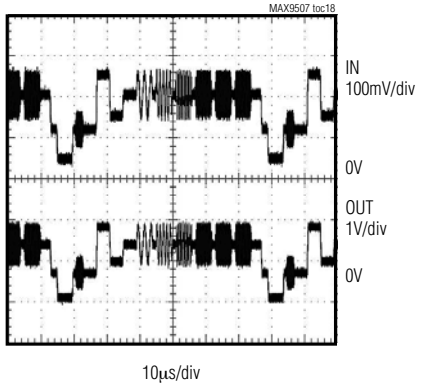
12.5T RESPONSE



NTC-7 RESPONSE



PAL MULTIBURST



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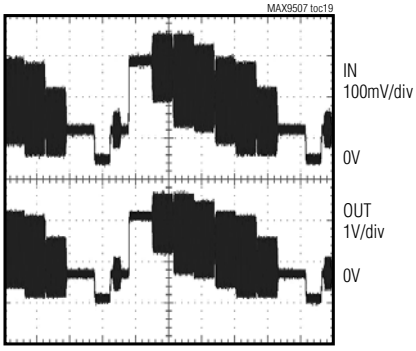
1.8V DirectDrive Video Filter Amplifier with Load Detection and Dual SPST Analog Switches

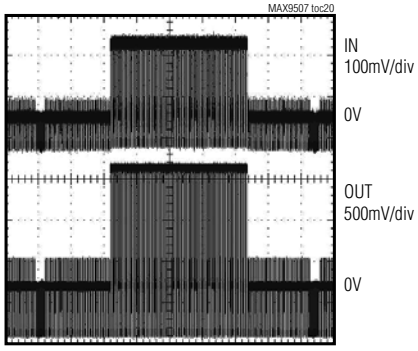
Typical Operating Characteristics (continued)

(V_{DD} = +1.8V, GND = 0V, mode 2 (Table 6), video output has R_L = 150Ω connected to GND, video filter enabled, T_A = +25°C, unless otherwise noted.)

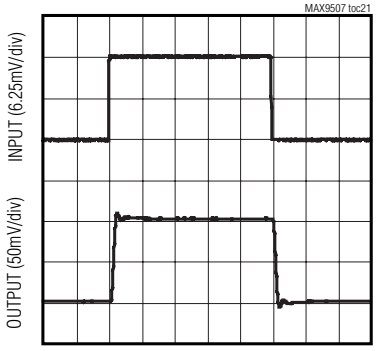
PAL COLOR BARS



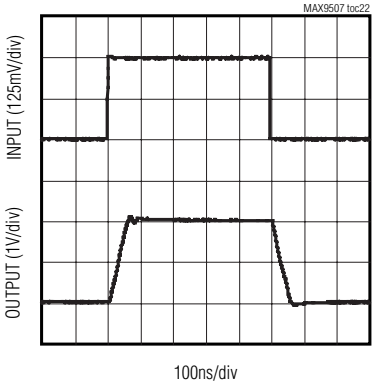
FIELD SQUARE-WAVE RESPONSE (AC-COUPLED INPUT)



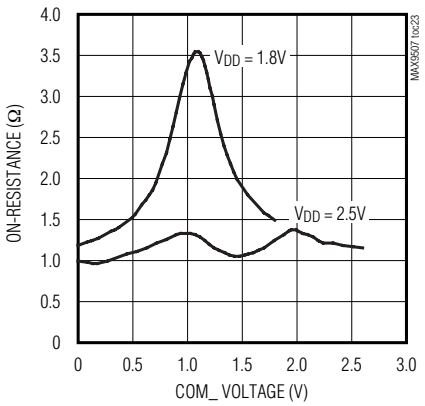
SMALL-SIGNAL PULSE RESPONSE (FLTEN = 0)



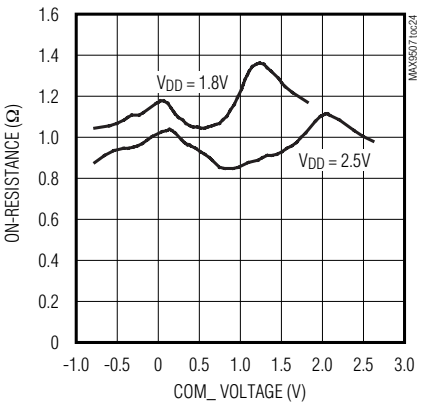
LARGE-SIGNAL PULSE RESPONSE (FLTEN = 0)



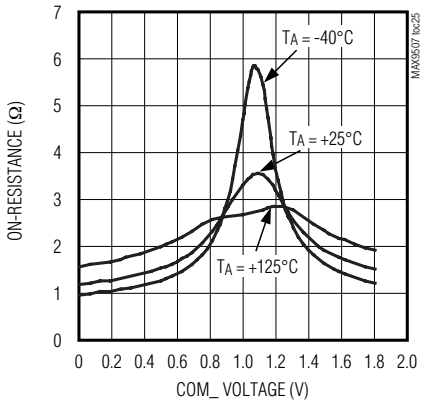
ON-RESISTANCE vs. COM_ VOLTAGE (NORMAL RANGE)



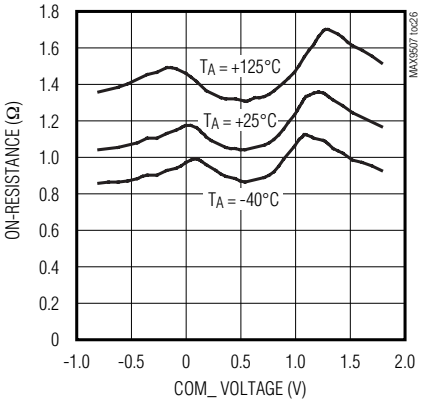
ON-RESISTANCE vs. COM_ VOLTAGE (EXTENDED RANGE)



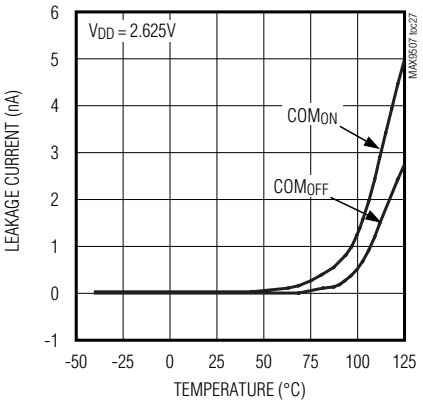
ON-RESISTANCE vs. COM_ VOLTAGE (NORMAL RANGE)



ON-RESISTANCE vs. COM_ VOLTAGE (EXTENDED RANGE)



ANALOG SWITCH LEAKAGE CURRENT vs. TEMPERATURE (NORMAL RANGE)



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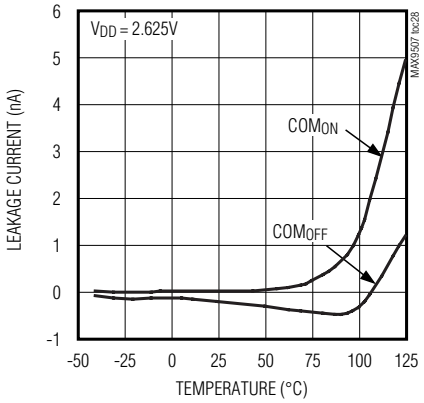
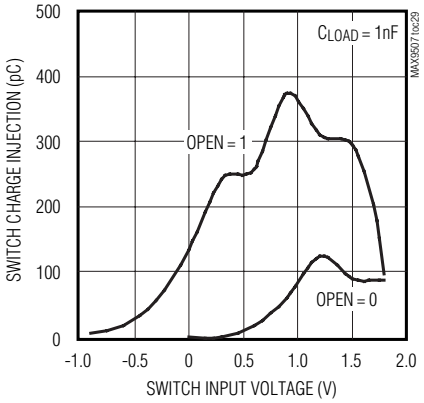
Typical Operating Characteristics (continued)

(V_{DD} = +1.8V, GND = 0V, mode 2 (Table 6), video output has R_L = 150Ω connected to GND, video filter enabled, T_A = +25°C, unless otherwise noted.)

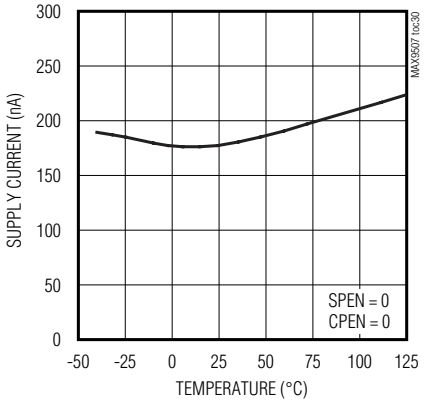
ANALOG SWITCH LEAKAGE CURRENT vs. TEMPERATURE (EXTENDED RANGE)



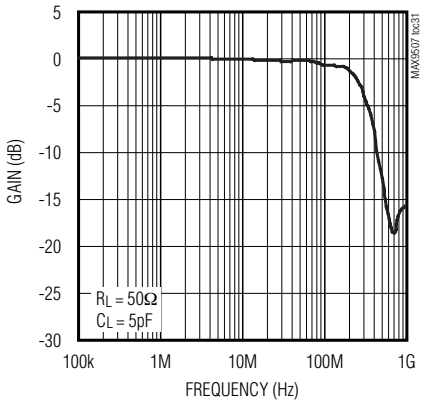
SWITCH CHARGE INJECTION vs. VOLTAGE



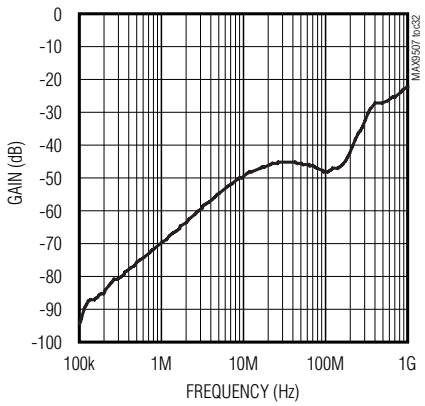
SWITCH-ONLY SUPPLY CURRENT vs. TEMPERATURE (NORMAL RANGE)



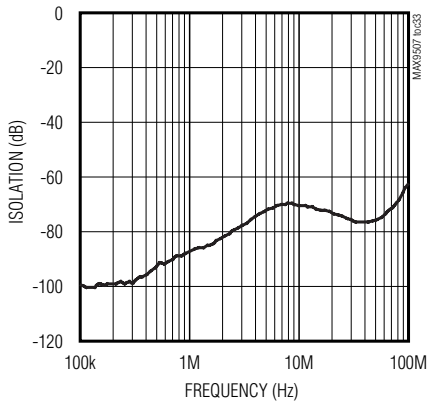
SWITCH FREQUENCY RESPONSE



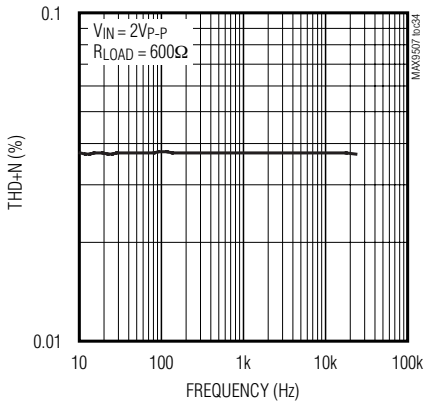
SWITCH OFF-ISOLATION vs. FREQUENCY



SWITCH-TO-SWITCH CROSSTALK vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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1.8V DirectDrive Video Filter Amplifier with Load Detection and Dual SPST Analog Switches

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Pin Description

PIN	NAME	FUNCTION
1	IN	Video Input
2	SDA	I²C-Compatible Serial-Data Input/Output
3	SCL	I²C-Compatible Serial-Clock Input
4	DEV_ADDR	I²C Device Address Input. Connect DEV_ADDR to GND, V_{DD}, SCL, or SDA. See Table 4.
5	V_{DD}	Positive Power Supply. Bypass with a 0.1µF capacitor to GND.
6	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF capacitor from C1P to C1N.
7	CPGND	Charge-Pump Ground
8	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF capacitor from C1P to C1N.
9	V_{SS}	Charge-Pump Negative Power Supply. Bypass with a 1µF capacitor to GND.
10	OUT	Video Output
11	GND	Ground
12	$\overline{LCF}$	Load Change Flag. Open-drain, active-low signal indicates when a video load change occurs.
13	NO1	Normally Open Terminal 1
14	COM1	Common Terminal 1
15	COM2	Common Terminal 2
16	NO2	Normally Open Terminal 2
—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to GND.

Detailed Description

The MAX9507 represents Maxim's second-generation of DirectDrive video amplifiers that meet the requirements of current and future portable equipment:

- 1.8V Operation: Eliminate the need for 3.3V supply in favor of lower supply voltages.
- Lower Power Consumption: The MAX9507 reduces average power consumption by up to 75% compared to the 3.3V first generation (MAX9503/MAX9505).
- Internal Fixed Gain of 8: As the supply voltages drop for system chips on deep submicron processes, the video DAC can no longer create a $1V_{P-P}$ signal at its output, and the gain of 2 found in the previous generation of video filter amplifiers is not enough.
- Load Reporting: The MAX9507 senses the presence of a video load. For portable devices, a video load is not connected most of the time, and turning off the video encoder saves power. Another benefit of load reporting is a simpler user interface, eliminating the need to browse through menus to activate the video output. Instead, the equipment will automatically enable this feature.
- Dual SPST Analog Switches: The two analog switches are ideal for routing additional audio, video, or digital signals.

DirectDrive technology is necessary for a voltage-mode amplifier to output a $2V_{P-P}$ video signal from a 1.8V supply. The integrated inverting charge pump creates a negative supply that increases the output range and gives the video amplifier enough headroom to drive a $2V_{P-P}$ video signal into a 150Ω load.

DirectDrive

Background

Integrated video filter amplifier circuits operate from a single supply. The positive power supply usually creates video output signals that are level-shifted above ground to keep the signal within the linear range of the output amplifier. For applications where the positive DC level is not acceptable, a series capacitor can be inserted in the output connection in an attempt to eliminate the positive DC level shift. The series capacitor cannot truly level shift a video signal because the average level of the video varies with picture content. The series capacitor biases the video output signal around ground, but the actual level of the video signal can vary significantly depending upon the RC time constant and the picture content.

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The series capacitor creates a highpass filter. Since the lowest frequency in video is the frame rate, which can be between 24Hz and 30Hz, the pole of the highpass filter should ideally be an order of magnitude lower in frequency than the frame rate. Therefore, the series capacitor must be very large, typically from 220µF to 3000µF. For space-constrained equipment, the series capacitor is unacceptable. Changing from a single series capacitor to a SAG network that requires two smaller capacitors can only reduce space and cost slightly.

The series capacitor in the usual output connection also prevents damage to the output amplifier if the connector is shorted to a supply or to ground. While the output connection of the MAX9507 does not have a series capacitor, the MAX9507 will not be damaged if the connector is shorted to a supply or to ground (see the *Short-Circuit Protection* section).

Video Amplifier

If the full-scale video signal from a video DAC is 250mV, the black level of the video signal created by the video DAC is around 75mV. The MAX9507 shifts the black level to near ground at the output so that the active video is above ground and the sync is below ground. The amplifier needs a negative supply for its output stage to remain in its linear region when driving sync below ground.

The MAX9507 has an integrated charge pump and linear regulator to create a low-noise negative supply from the positive supply voltage. The charge pump inverts the positive supply to create a raw negative voltage that is then fed into the linear regulator filtering out the charge-pump noise.

Comparison Between DirectDrive Output and AC-Coupled Output

The actual level of the video signal varies less with a DirectDrive output than an AC-coupled output. The average video signal level can change greatly depending upon the picture content. With an AC-coupled output, the average level will change according to the time constant formed by the series capacitor and series resistance (usually 150Ω). For example, Figure 4 shows an AC-coupled video signal alternating between a completely black screen and a completely white screen. Notice the excursion of the video signal as the screen changes.

With the DirectDrive amplifier, the black level is held at ground. The video signal is constrained between -0.3V to +0.7V. Figure 5 shows the video signal from a DirectDrive amplifier with the same input signal as the AC-coupled system.

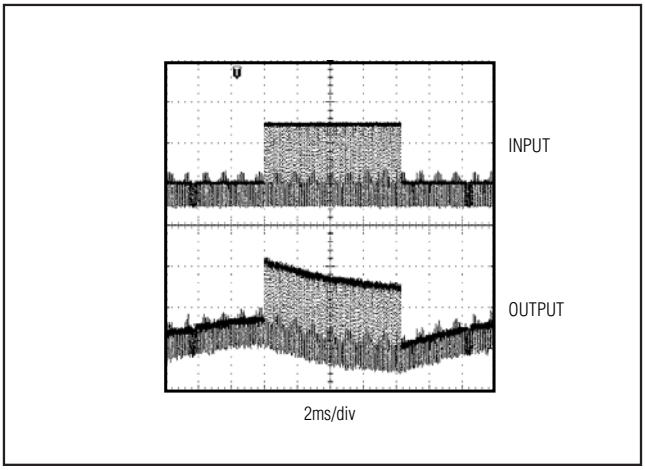

Figure 4. AC-Coupled Output

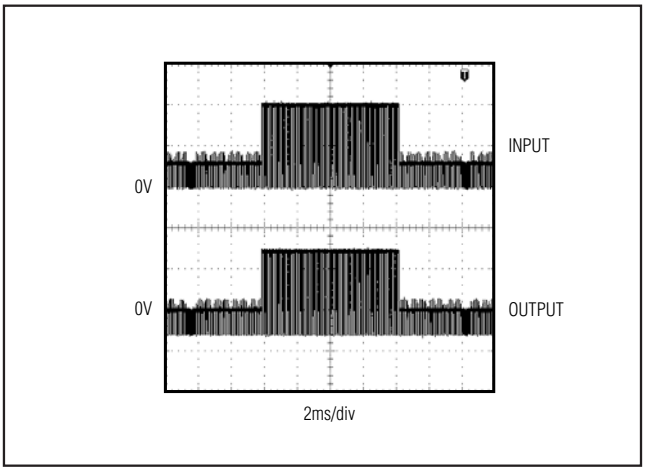

Figure 5. DirectDrive Output

Video Reconstruction Filter

The MAX9507 includes an internal five-pole, Butterworth lowpass filter to condition the video signal. The reconstruction filter smoothes the steps and reduces the spikes created whenever the DAC output changes value. In the frequency domain, the steps and spikes cause images of the video signal to appear at multiples of the sampling clock frequency. The reconstruction filter typically has ±1dB passband flatness of 7.3MHz and 48dB attenuation at 27MHz.

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1.8V DirectDrive Video Filter Amplifier with Load Detection and Dual SPST Analog Switches

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Transparent Sync-Tip Clamp

The MAX9507 contains an integrated, transparent sync-tip clamp. When using a DC-coupled input, the sync-tip clamp does not affect the input signal, as long as it remains above ground. When using an AC-coupled input, the sync-tip clamp automatically clamps the input signal to ground, preventing it from going lower. A small current of 2µA pulls down on the input to prevent an AC-coupled signal from drifting outside the input range of the device.

Using an AC-coupled input results in some additional variation of the black level at the output. Applying a voltage above ground to the input pin of the device always produces the same output voltage, regardless of whether the input is DC- or AC-coupled. However, since the sync-tip clamp level (V_{CLP}) can vary over a small range, the video black level at the output of the device when using an AC-coupled input can vary by an additional amount equal to the V_{CLP} multiplied by the DC voltage gain (A_V).

Dual SPST Analog Switches

The MAX9507 has dual SPST analog switches for routing additional audio, video, digital, and other signals. The switches are selected through the I^2C interface. SW1EN (register 0x00, bit B6) and SW2EN (register 0x00, bit B7) control the analog switches. See the *I^2C Registers and Bit Descriptions* section. The dual analog switches operate in either normal or extended range. In normal range, the part is in shutdown and the analog switches can handle signals between GND and V_{DD}. In extended range, the charge pump and linear regulator are on and the analog switches can handle signals between -0.9V and V_{DD}.

Short-Circuit Protection

The MAX9507 typical operating circuit includes a 75Ω back-termination resistor that limits short-circuit current if an external short is applied to the video output. The MAX9507 also features internal output short-circuit protection to prevent device damage in prototyping and applications where the amplifier output can be directly shorted.

Powering On/Off the MAX9507

The MAX9507 powers on in a low-power shutdown mode with the analog switches open and the video signal path, charge pump, and load detection circuitry disabled. It is good practice to configure the operating mode of the signal path before enabling it. This may include selecting the sync-tip clamp and video filter. Setting CPEN = 1 (register 0x00, bit B0) enables the charge pump. The charge pump must be fully operational before the signal path will be functional. Setting SPEN = 1 (register 0x00, bit B1) enables the signal path. Both SPEN and CPEN may be set at the same time and internal control circuitry will monitor the charge pump and enable the signal path at the appropriate time.

The analog switches can be turned on or off at any time, regardless of the state of the charge pump or signal path. However, the signal range is limited from GND to V_{DD} when the charge pump is disabled.

The MAX9507 can be placed in a low-power shutdown mode by setting SPEN = 0 and CPEN = 0.

Video Load Detection Circuitry

The MAX9507 contains video load detection circuitry at the video output, enabling efficient power consumption based on the actual presence of a video load. Setting the automatic signal path enable bit, ASPEN = 1 (register 0x01, bit B1) or the automatic charge-pump enable bit, ACPEN = 1 (register 0x01, bit B0) enables the load detection feature. The LOAD bit (register 0x01, bit B7) indicates the load status.

To enable complete, automatic control of the part, set ASPEN = ACPEN = 1 and SPEN = CPEN = 0. In this state, when an output load is connected to the amplifier, the signal path and charge pump fully turn on and stay on until the output load is disconnected. If an output load is not connected to the amplifier, then the signal path and charge pump remain in a low-power sleep mode while continuing to check if a load is connected. Setting SPEN = 1 or CPEN = 1 overrides the corresponding ASPEN or ACPEN bits, enabling the block regardless of the detected video load status.

The LOAD bit indicates the latest video load status. All changes to the video load status are debounced typically 128ms to eliminate false load-detect events.

Setting the load change flag enable bit, LCFEN = 1 (register 0x01, bit B3), and enabling the load detection feature (ASPEN = 1 or ACPEN = 1) enables the open-drain $\overline{LCF}$ output. $\overline{LCF}$ asserts low whenever the LOAD bit changes state. It remains low until the LOAD bit (register 0x01) is read. $\overline{LCF}$ can be used as an interrupt to notify the system that the load status has changed.

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Sleep Mode

If a video load is not connected to the amplifier, the MAX9507 remains in a low-power sleep mode. The load-sense circuitry checks for a load eight times per second by connecting an internal 7.5kΩ pullup resistor to the output for 1ms. If the output is pulled up, no load is present. If the output stays low, a load is connected, and the automatic control circuitry enables the appropriate blocks. When the amplifier is on, it continually checks if the load has been disconnected by detecting if the amplifier is sinking current during a horizontal line time. Therefore, a black-burst signal (or input signal < 13mV) is required to maintain the detected load status. If the load is disconnected, the device returns to the low-power sleep mode.

Common Modes of Operation

NO.	MODE	ASPEN	ACPEN	SPEN	CPEN
1	Shutdown mode. Switches in normal range. Load-detect function disabled.	0	0	0	0
2	Full operation mode. Video, charge pump, and regulator on. Switches in extended range.	X	X	1	1
3	Charge-pump-only mode. Charge pump and regulator on, video off. Switches in extended range.	X	X	0	1
4	Sleep mode. Video, charge pump, and regulator automatic. Switches in extended range only when the charge pump is on. Load-detect function enabled.	1	1	0	0
5	Charge pump and regulator on, video automatic. Switches in extended range. Load-detect function enabled.	1	0	0	1

X = Don't care.

I²C Registers and Bit Descriptions

Table 1. Register Map

REGISTER ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	POWER-ON RESET STATE
0x00	Configuration	SW2EN	SW1EN	0	STEN	FLTEN	0	SPEN	CPEN	0x00
0x01	Video Load Detect	LOAD	0	0	0	LCFEN	0	ASPEN	ACPEN	0x00

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1.8V DirectDrive Video Filter Amplifier with Load Detection and Dual SPST Analog Switches

Table 2. Configuration Register (0x00)

BIT	NAME	FUNCTION
B7	SW2EN	1 = Analog switch 2 closed. 0 = Analog switch 2 open.
B6	SW1EN	1 = Analog switch 1 closed. 0 = Analog switch 1 open.
B4	STEN	1 = Transparent sync-tip clamp enabled, the input can be DC- or AC-coupled. 0 = Transparent sync-tip clamp disabled, the input must be DC-coupled.
B3	FLTEN	1 = Video filter enabled. 0 = Video filter disabled (bypassed).
B1	SPEN	1 = Signal path enabled* (SPEN overrides the ASPEN setting). 0 = Signal path disabled.
B0	CPEN	1 = Charge pump enabled (CPEN overrides the ACPEN setting). 0 = Charge pump disabled.

**Internal control circuitry prevents the signal path from turning on until the charge pump has been enabled and has settled.*

Table 3. Video Load-Detect Register (0x01)

BIT	NAME	FUNCTION
B7	LOAD*	1 = Load detected. 0 = No load detected.
B3	LCFEN	1 = Changes to the video load will trigger $\overline{LCF}$ to pull low. 0 = Changes to the video load are not reported.
B1	ASPEN	1 = Enable automatic control of the video signal path**. 0 = Disable automatic control of the video signal path.
B0	ACPEN	1 = Enable automatic control of the charge pump***. 0 = Disable automatic control of the charge pump.

**Read-only bit indicating the load status when the video load-detect circuitry is enabled (ASPEN = 1 or ACPEN = 1). When LCFEN = 1, reading this bit will clear the $\overline{LCF}$ flag.*

***If SPEN = 0, then the signal path will be automatically enabled when a video load is detected and the charge pump has been enabled and has settled.*

****If CPEN = 0, then the charge pump will be automatically enabled when a video load is detected.*

I²C Serial Interface

The MAX9507 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9507 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the MAX9507 by transmitting a START (S) condition, the proper slave address with the R/$\overline{W}$ bit set to 0, followed by the register address and then the data word. Each transmit sequence is framed by a START (S) and a STOP (P) condition. Each word transmitted to the MAX9507 is 8 bits long and is followed by an acknowledge clock pulse. A master reads from the MAX9507 by transmitting the slave address with the R/$\overline{W}$ bit set to 0, the register address of the register to be read, a REPEATED START (Sr) condition, the slave address with the R/$\overline{W}$ bit set to 1, followed by a series of SCL pulses. The MAX9507 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, an acknowledge or a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output.

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Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9507 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I^2C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 6). A START condition from the master signals the beginning of a transmission to the MAX9507. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9507 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/$\overline{W}$) bit. Set the R/$\overline{W}$ bit to 1 to configure the MAX9507 to read mode. Set the R/$\overline{W}$ bit to 0 to configure the MAX9507 to write mode. The slave address is always the first byte of information sent to the MAX9507 after a START or a REPEATED START condition. The MAX9507 slave address is configurable with DEV_ADDR. Table 4 shows the possible slave addresses for the MAX9507.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9507 uses to handshake receipt of each byte of data when in write mode (see Figure 7). The MAX9507 pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the MAX9507 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9507, followed by a STOP condition.

Table 4. Slave Address

DEV_ADDR	B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS (hex)	READ ADDRESS (hex)
GND	1	0	0	1	1	0	0	R/$\overline{W}$	0x98	0x99
V_{DD}	1	0	0	1	1	0	1	R/$\overline{W}$	0x9A	0x9B
SCL	1	0	0	1	1	1	0	R/$\overline{W}$	0x9C	0x9D
SDA	1	0	0	1	1	1	1	R/$\overline{W}$	0x9E	0x9F

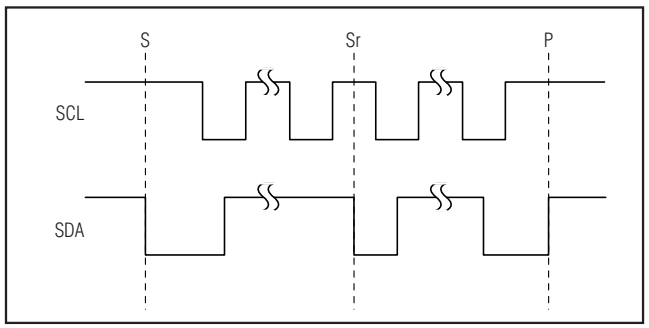

Figure 6. START, STOP, and REPEATED START Conditions

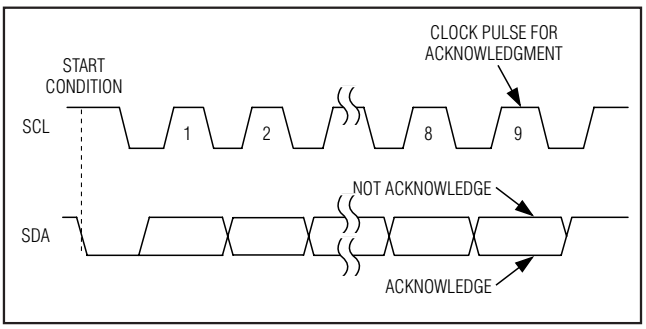

Figure 7. Acknowledge

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Write Data Format

A write to the MAX9507 consists of transmitting a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one data byte to configure the internal register address pointer, one or more data bytes, and a STOP condition. Figure 8 illustrates the proper frame format for writing one byte of data to the MAX9507. Figure 9 illustrates the frame format for writing n-bytes of data to the MAX9507.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9507. The MAX9507 acknowledges receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the MAX9507's internal register address pointer. The pointer tells the MAX9507 where to write the next byte of data. An acknowledge pulse is sent by the MAX9507 upon receipt of the address pointer data.

The third byte sent to the MAX9507 contains the data that will be written to the chosen register. An acknowledge pulse from the MAX9507 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential register address locations within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

Read Data Format

The master presets the address pointer by first sending the MAX9507's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address after a START condition. The MAX9507 acknowledges receipt of its slave address and the register address by pulling SDA low during the ninth SCL clock pulse. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9507 transmits the contents of the specified register. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first

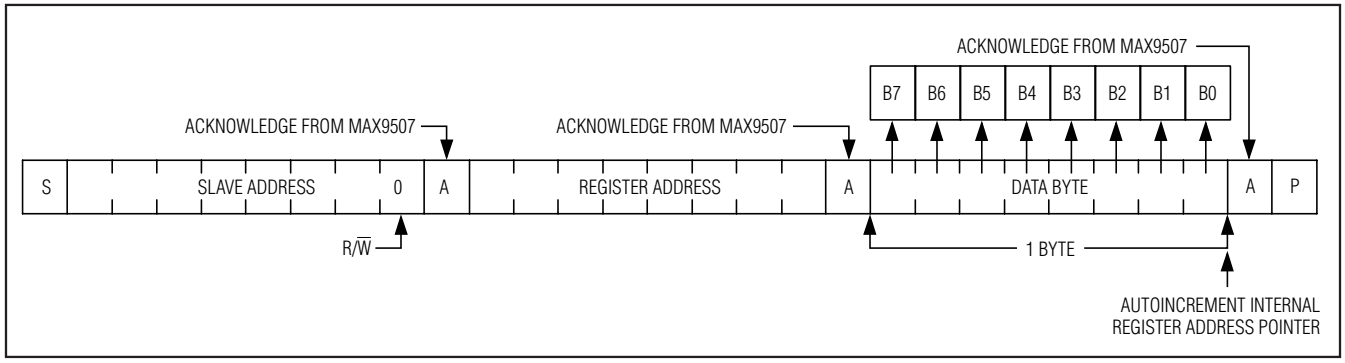

Figure 8. Writing a Byte of Data to the MAX9507

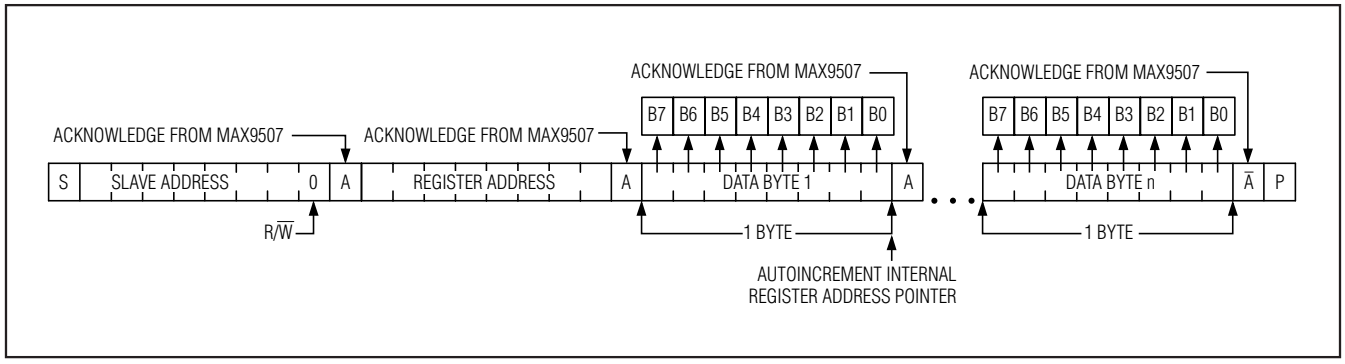

Figure 9. Writing n-Bytes of Data to the MAX9507

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data byte to be read will be from the register address location set by the previous transaction and not 0x00, and subsequent reads will autoincrement the address pointer until the next STOP condition. Attempting to read from register addresses higher than 0x01 results in repeated reads from a dummy register containing 0xFF data. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 10 and 11 illustrate the frame format for reading data from the MAX9507.

Applications Information

Power Consumption

The quiescent power consumption and average power consumption of the MAX9507 is remarkably low because of 1.8V operation and DirectDrive technology. Quiescent power consumption is defined when the MAX9507 is operating without load. In this case, the MAX9507 consumes about 5.8mW. Average power consumption, which is defined when the MAX9507 drives a 150Ω load to ground with a 50% flat field, is about 11.7mW. Table 5 shows the power consumption with different video signals. The supply voltage is 1.8V and OUT drives a 150Ω load to ground.

Notice that the two extremes in power consumption occur with a video signal that is all black and a video signal that is all white. The power consumption with 75% color bars and 50% flat field lies in between the extremes.

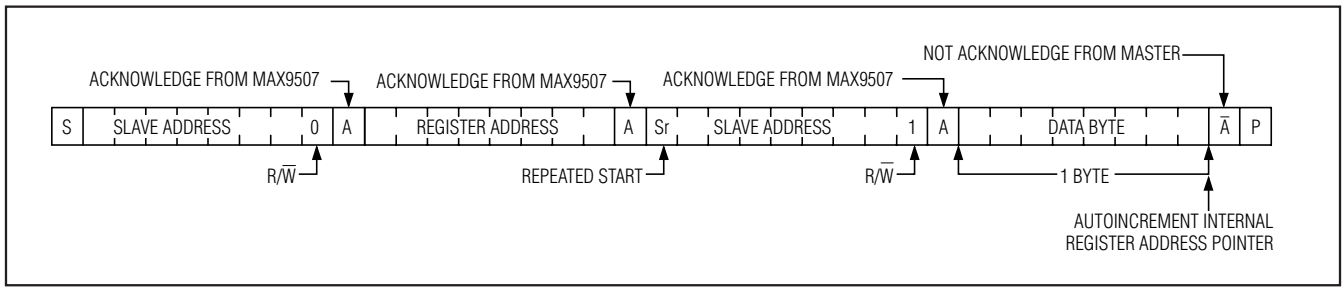

Figure 10. Reading One Indexed Byte of Data from the MAX9507

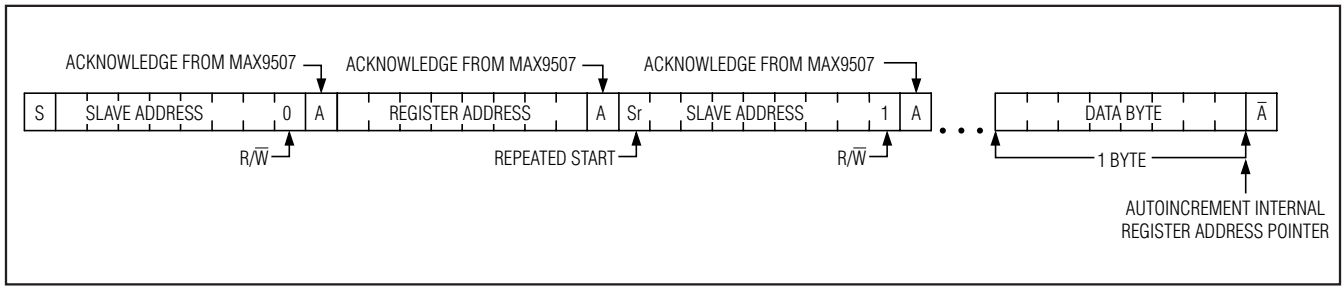

Figure 11. Reading n-Bytes of Indexed Data from the MAX9507

Table 5. MAX9507 Power Consumption with Different Video Signals

VIDEO SIGNAL	MAX9507 POWER CONSUMPTION WITH FILTER ENABLED (mW)	MAX9507 POWER CONSUMPTION WITH FILTER DISABLED (mW)
All Black Screen	6.7	6.2
All White Screen	18.2	17.9
75% Color Bars	11.6	11.0
50% Flat Field	11.7	11.3

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Interfacing to Video DACs that Produce Video Signals Larger than 0.25VP-P

Devices designed to generate 1VP-P video signals at the output of the video DAC can still work with the MAX9507. Most video DACs source current into a ground-referenced resistor, which converts the current into a voltage. Figure 12 shows a video DAC that creates a video signal from 0 to 1V across a 150Ω resistor. The following video filter amplifier has a 2V/V gain so that the output is 2VP-P.

The MAX9507 expects input signals that are 0.25VP-P nominally. The same video DAC can be made to work with the MAX9507 by scaling down the 150Ω resistor to a 37.5Ω resistor, as shown in Figure 13. The 37.5Ω resistor is one-quarter the size of the 150Ω resistor, resulting in a video signal that is one-quarter the amplitude.

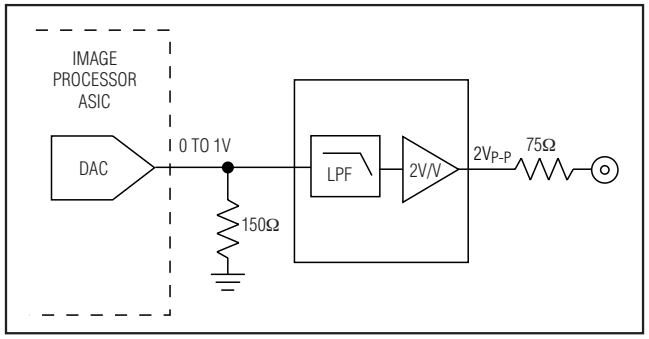

Figure 12. Video DAC Generates a 1VP-P Signal Across a 150Ω Resistor Connected to Ground

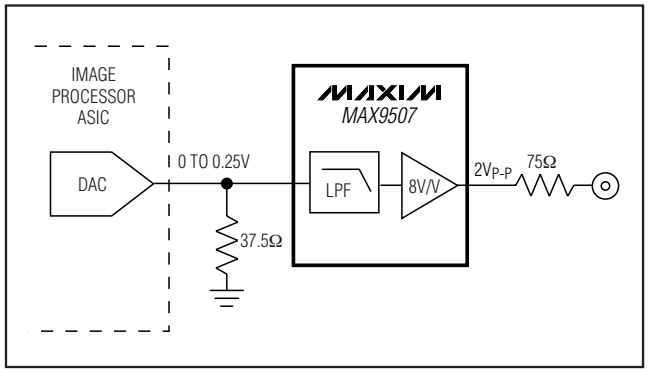

Figure 13. Video DAC Generates a 0.25VP-P Signal Across a 37.5Ω Resistor Connected to Ground

Changing Between Video Output and Microphone Input on a Single Connector

Figure 14 shows how a single pole on a mobile phone jack can be used for transmitting a video signal to a television or receiving the signal from the microphone of a headset. To transmit a video signal, open SW1 and enable the video circuitry. To receive a signal from a microphone, close SW1 and disable the video circuitry.

Switching Between Video and Digital Signals

Figure 15 shows how the dual SPST analog switches and the high-impedance output of the video amplifier enable video transmission, digital transmission, and digital reception all on a single pole of a connector. To transmit a video signal, open SW1 and SW2 and enable the video circuitry. To receive a digital signal, close SW1, open SW2, and disable the video circuitry. To transmit a digital signal, open SW1, close SW2, and disable the video circuitry.

Selecting Between Two Video Sources

The analog switches can multiplex between two video sources. For example, a mobile phone might have an application processor with an integrated video encoder and a mobile graphics processor with an integrated video encoder, each creating a composite video signal that is between 0 and 0.25V. Figure 16 shows this application in which the MAX9507 chooses between two internal video sources. The two analog switches can be used as a 2:1 multiplexer to select which video DAC output is filtered, amplified, and driven out to the connector.

If the analog switches are in extended mode, then they can also be used to select between two external video signals, as shown in Figure 17. The external video signals are usually between -2V and +2V. The resistor network divides the external signal by a factor of four, thereby reducing the signal to between -0.5V and +0.5V (see the *Anti-Alias Filter* section for an explanation on why the resistor-divider network is necessary). In extended mode, the analog switch can easily handle this bipolar input signal, even if the supply voltage is 1.8V.

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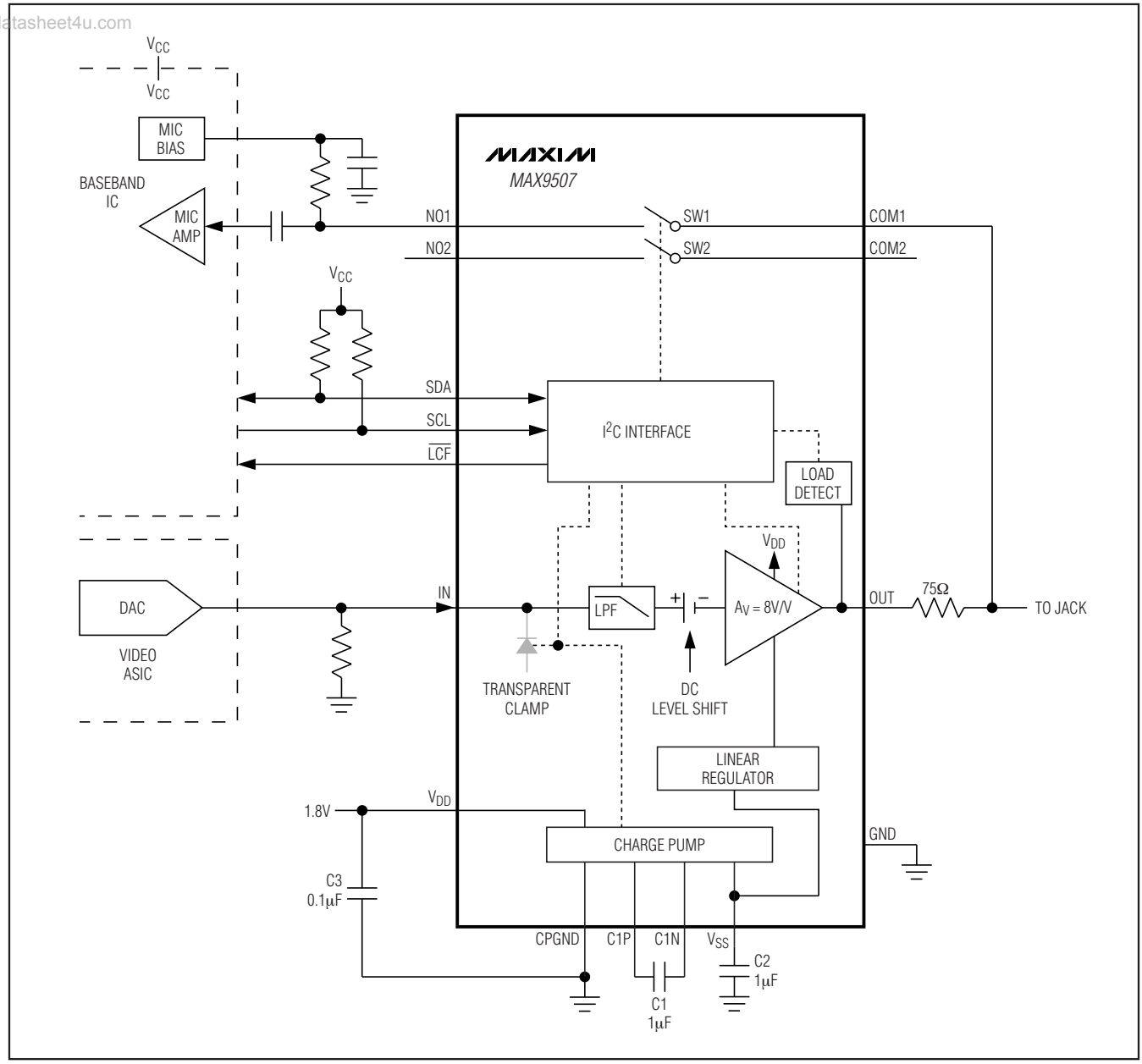

Figure 14. Video Output Configuration

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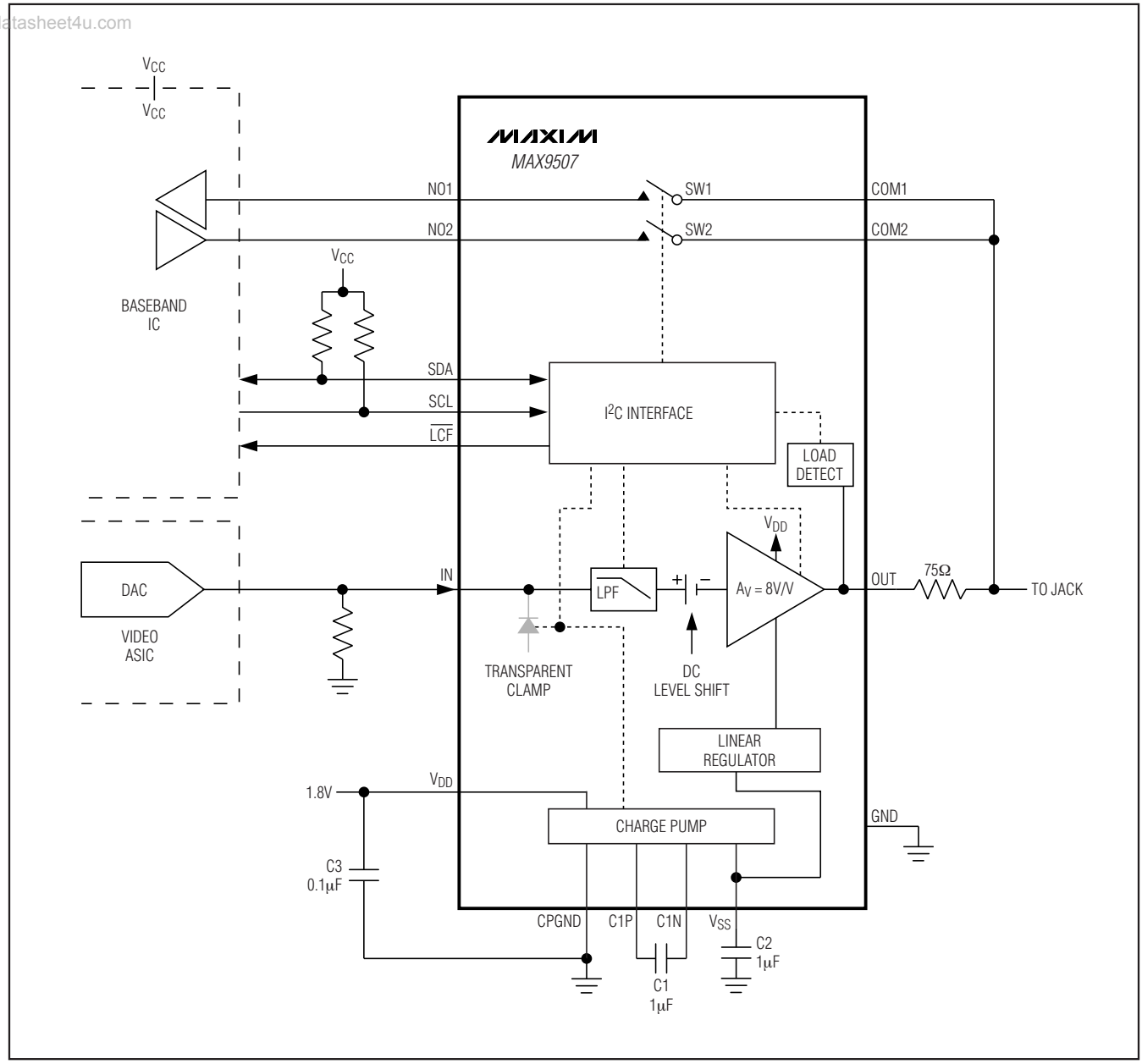

Figure 15. Video Output Configuration

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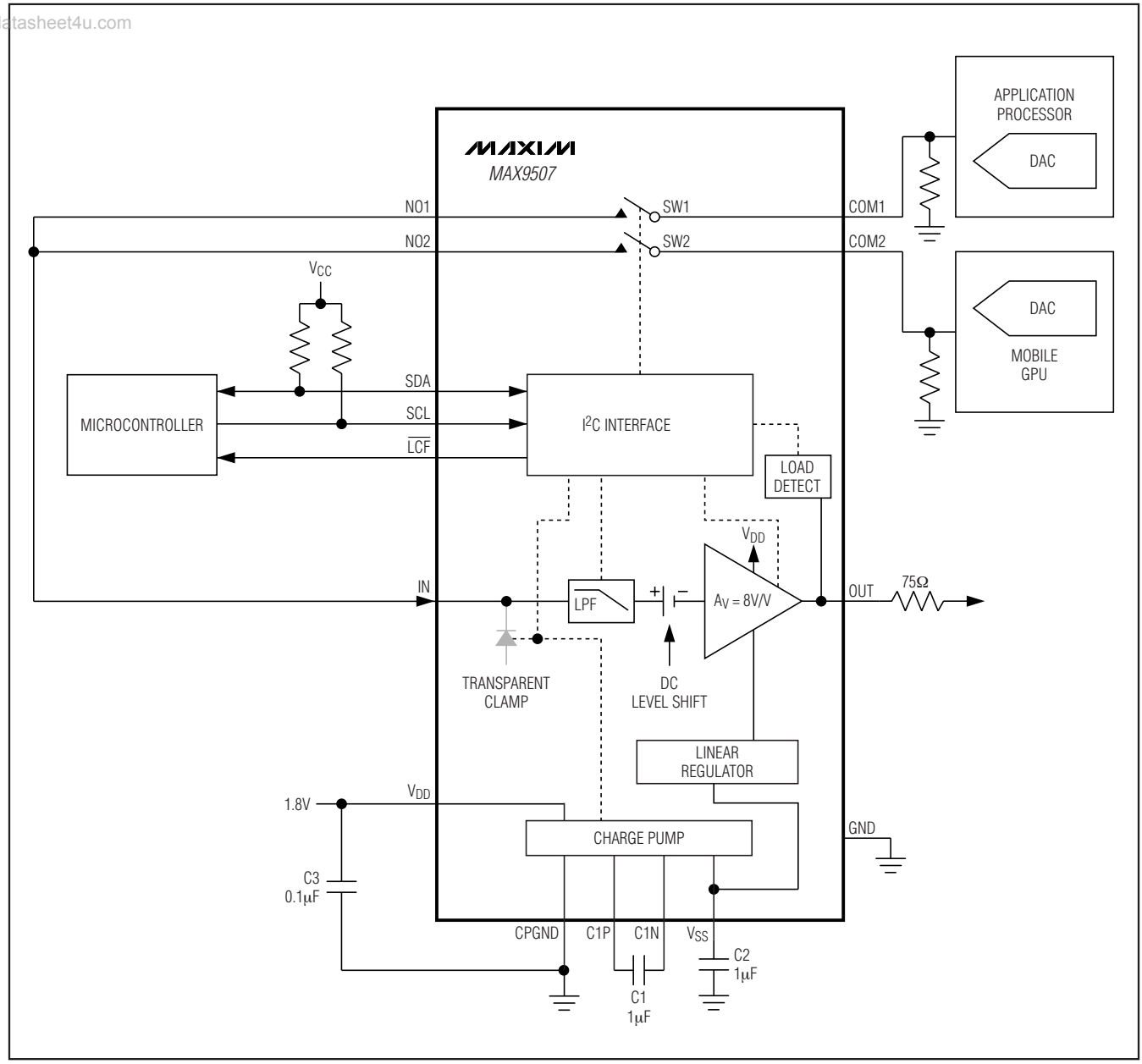

Figure 16. Selecting Between Two Internal Video Sources

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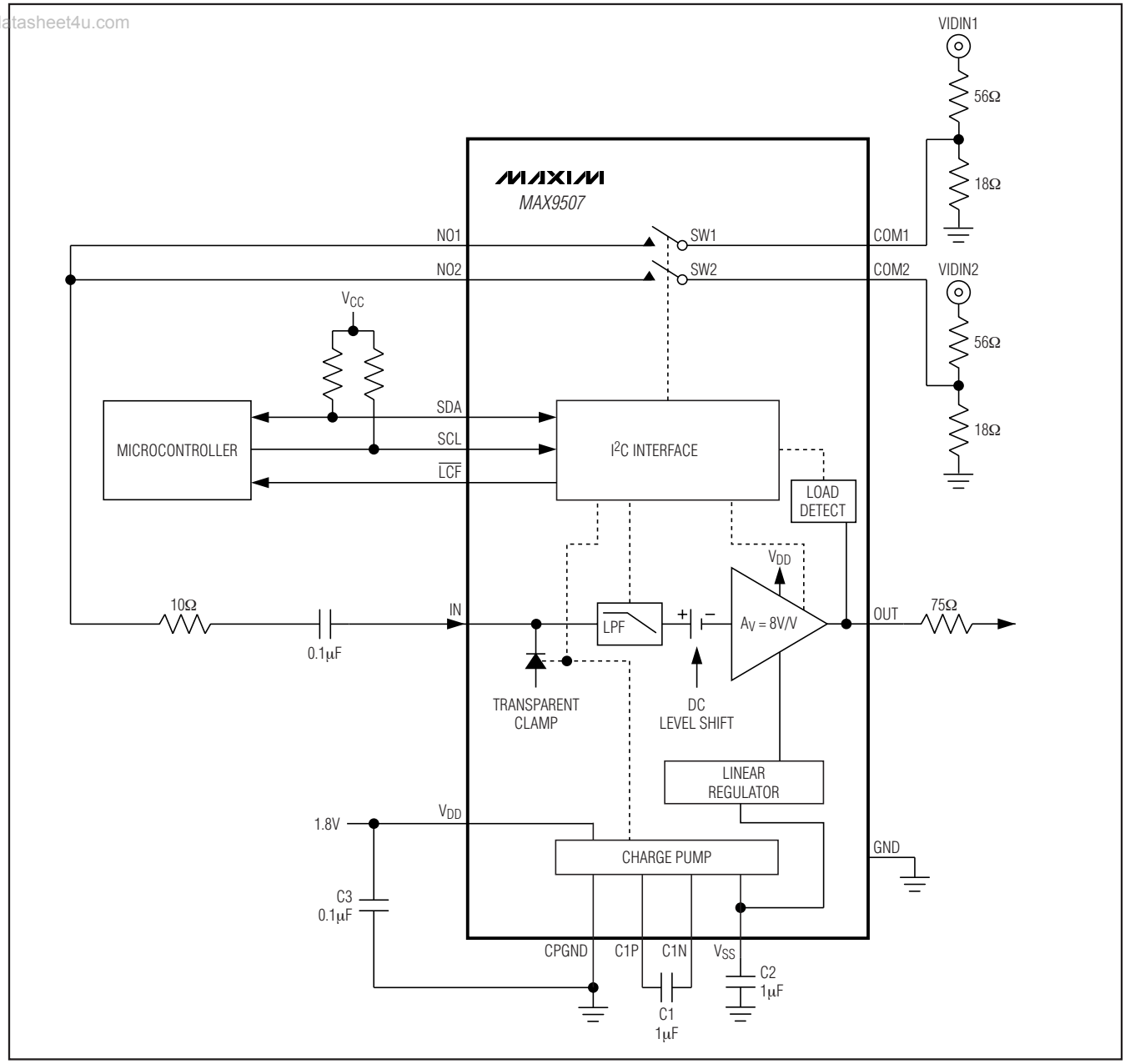

Figure 17. Selecting Between Two External Video Sources

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Anti-Alias Filter

The MAX9507 can also provide anti-alias filtering with a buffer before an analog-to-digital converter (ADC), which would be present in an NTSC/PAL video decoder, for example. Figure 18 shows the application circuit. An external composite video signal is applied to VIDIN, which is terminated with a total of 74Ω (56Ω and 18Ω resistors) to ground. The signal is attenuated by four, and then AC-coupled to IN. The normal $1V_{P-P}$ video signal must be attenuated because with a 1.8V supply, the MAX9507 can only handle a video signal of approximately $0.25V_{P-P}$ at IN. AC-couple the video signal to IN because the DC level of an external video signal is usually not well specified, although it is reasonable to expect that the signal is between -2V and +2V. The 10Ω series resistor increases the equivalent source resistance to about 25Ω, which is the minimum necessary for a video source to drive the internal sync-tip clamp.

For external video signals larger than $1V_{P-P}$, then operate the MAX9507 from a 2.5V supply so that IN can accommodate a $0.325V_{P-P}$ video signal, which is equivalent to a $1.3V_{P-P}$ video signal at VIDIN.

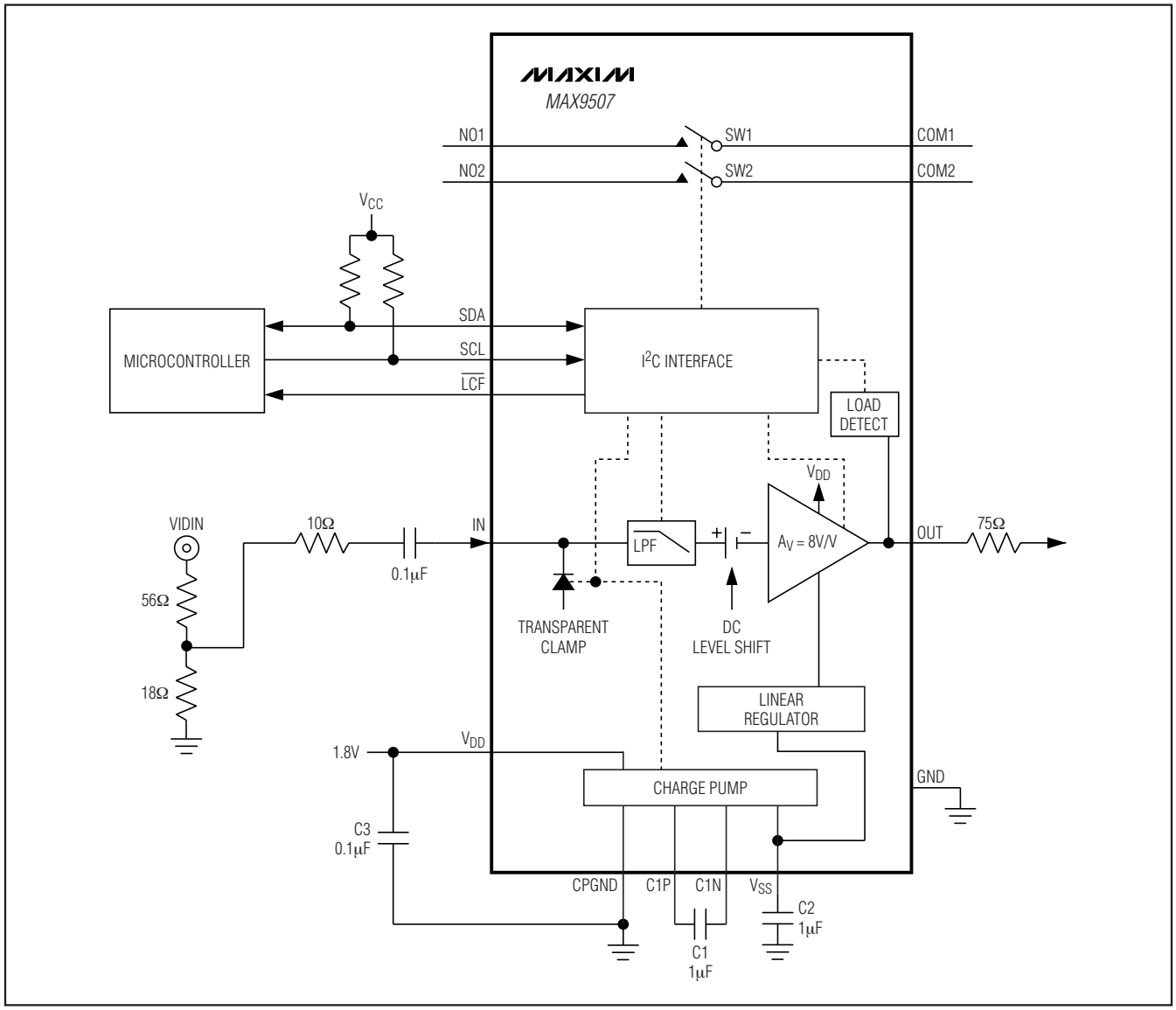

Figure 18. MAX9507 Used as an Anti-Alias Filter with Buffer

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Power-Supply Bypassing and Ground Management

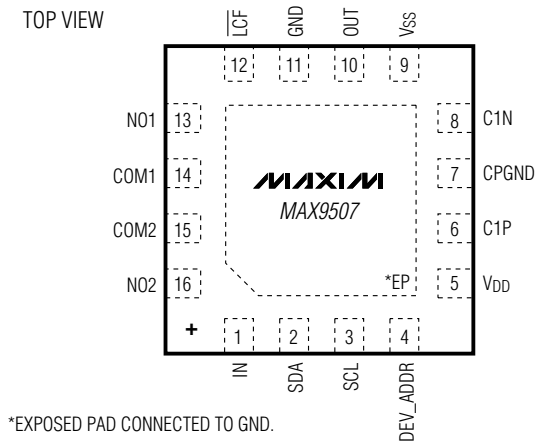
The MAX9507 operates from a 1.7V to 2.625V single supply and requires proper layout and bypassing. For the best performance, place the components as close to the device as possible.

Proper grounding improves performance and prevents any switching noise from coupling into the video signal. Bypass the analog supply (V_{DD}) with a 0.1µF capacitor to GND, placed as close to the device as possible. Bypass CPV_{SS} with a 1µF capacitor to GND as close to the device as possible. The total system bypass capacitance on V_{DD} should be at least 10µF, or ten times the capacitance between C1P and C1N.

Using a Digital Supply

The MAX9507 is designed to operate from noisy digital supplies. The high power-supply rejection ratio (47dB at 100kHz) allows the MAX9507 to reject the noise from the digital power supplies (see the *Typical Operating Characteristics*). If the digital power supply is very noisy and stripes appear on the television screen, increase the supply bypass capacitance. An additional, smaller capacitor in parallel with the main bypass capacitor can reduce digital supply noise because the smaller capacitor has lower equivalent series resistance (ESR) and equivalent series inductance (ESL).

Pin Configuration



THIN QFN (3mm x 3mm)

Chip Information

PROCESS: BiCMOS

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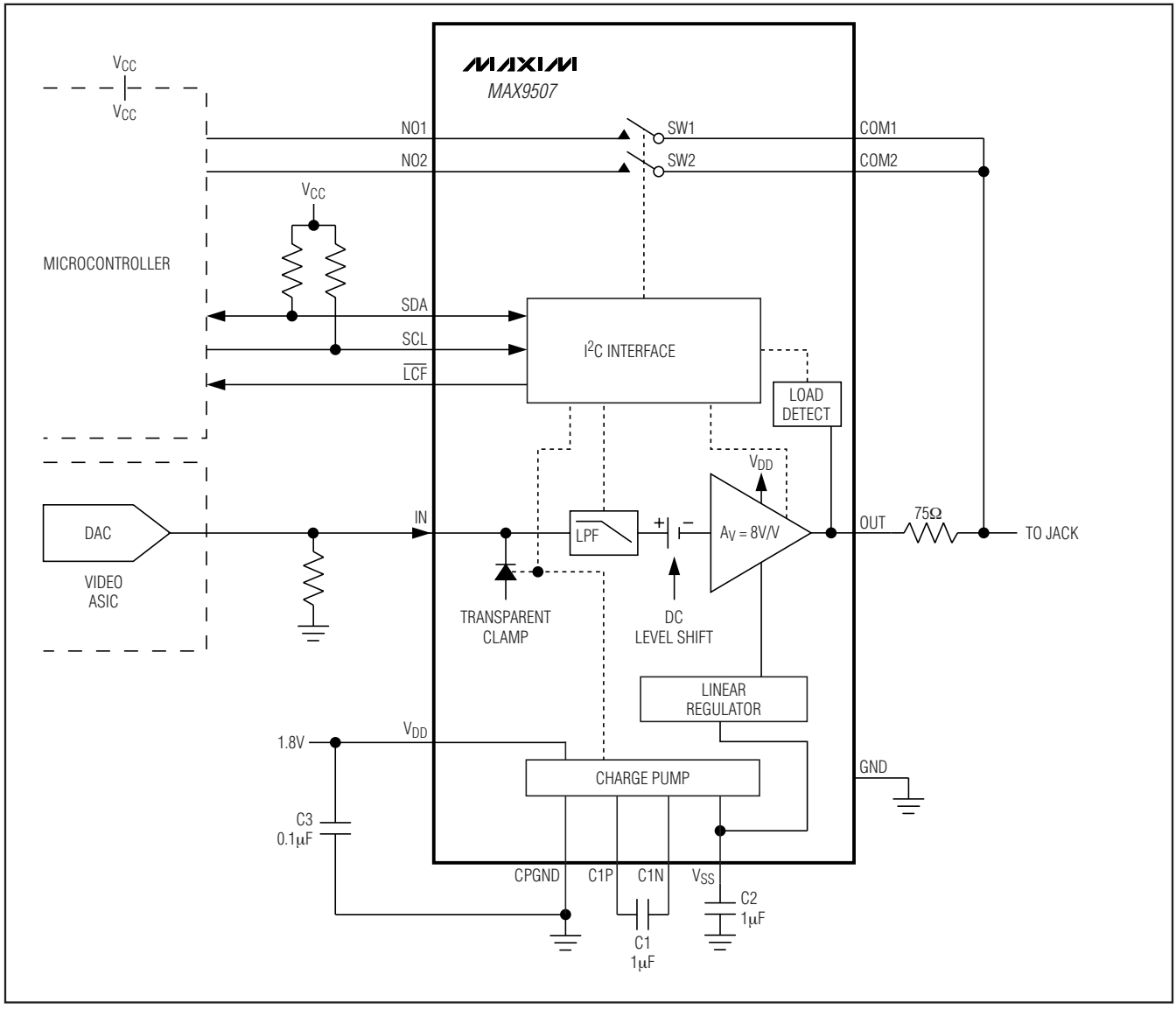
Functional Diagram/Typical Operating Circuit



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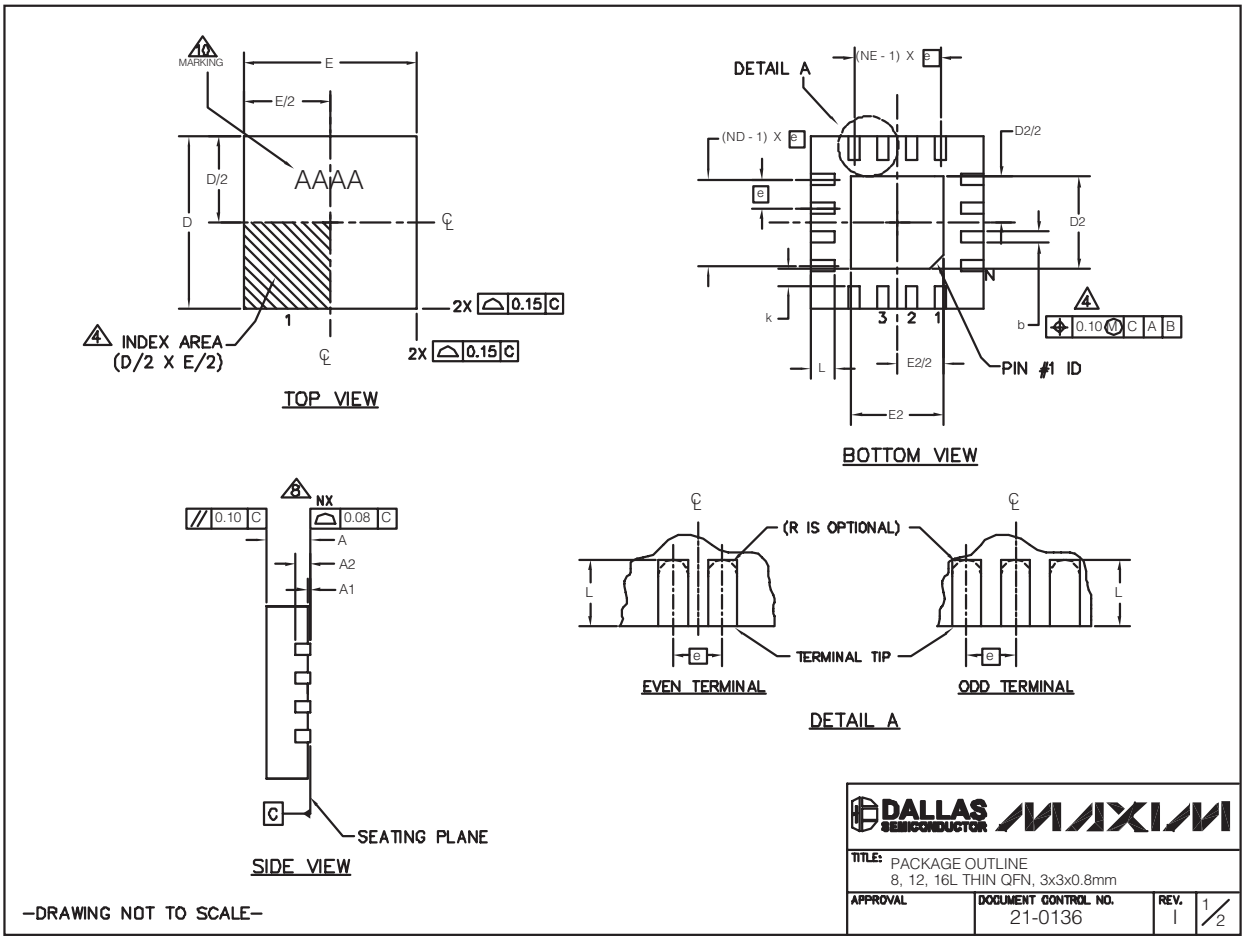
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS .
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm

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