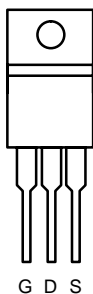


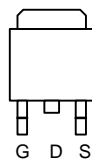
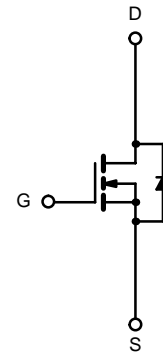
## N-Channel 60-V (D-S), 175°C MOSFET

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
60	0.008	75 <sup>a</sup>

**175°C Rated**  
Maximum Junction Temperature  
**TrenchFET®**  
Power MOSFETS

**TO-220AB**

 Top View  
SUP75N06-08

DRAIN connected to TAB

**TO-263**

 Top View  
SUB75N06-08


N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$	75 <sup>a</sup>
		$T_C = 125^\circ\text{C}$	55
Pulsed Drain Current	$I_{DM}$	240	A
Avalanche Current	$I_{AR}$	60	
Repetitive Avalanche Energy <sup>b</sup>	$E_{AR}$	L = 0.1 mH	280
Power Dissipation		$T_C = 25^\circ\text{C}$ (TO-220AB and TO-263)	250 <sup>c</sup>
		$T_A = 25^\circ\text{C}$ (TO-263) <sup>d</sup>	3.7
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient	$R_{thJA}$	PCB Mount (TO-263) <sup>d</sup>	40
		Free Air (TO-220AB)	62.5
Junction-to-Case	$R_{thJC}$	0.6	$^\circ\text{C/W}$

**Notes**

- Package limited.
- Duty cycle  $\leq 1\%$ .
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

 For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

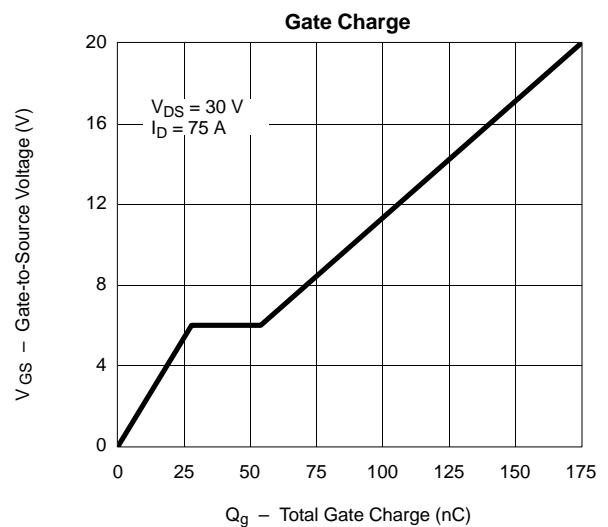
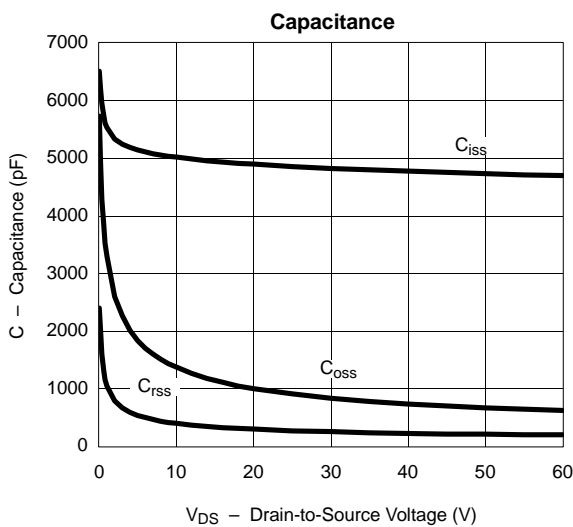
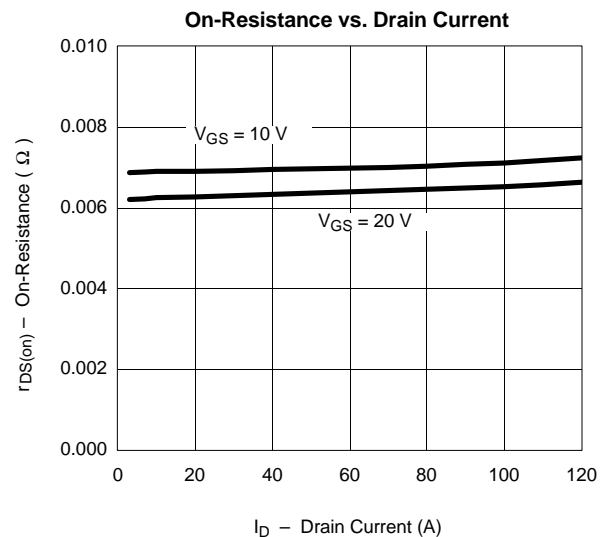
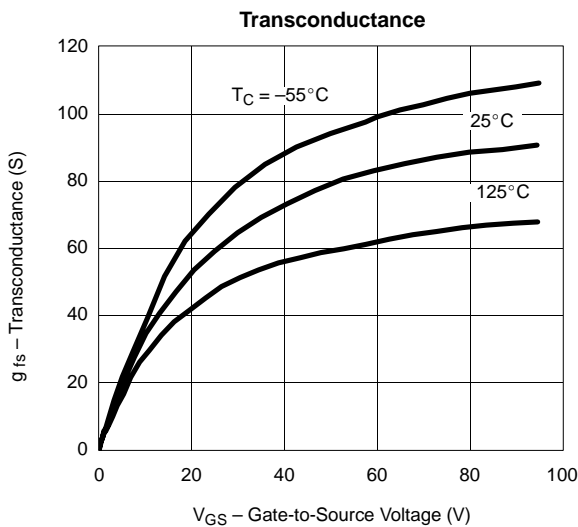
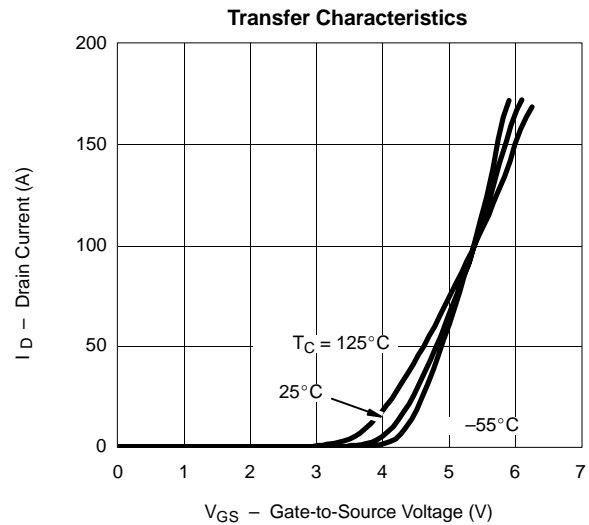
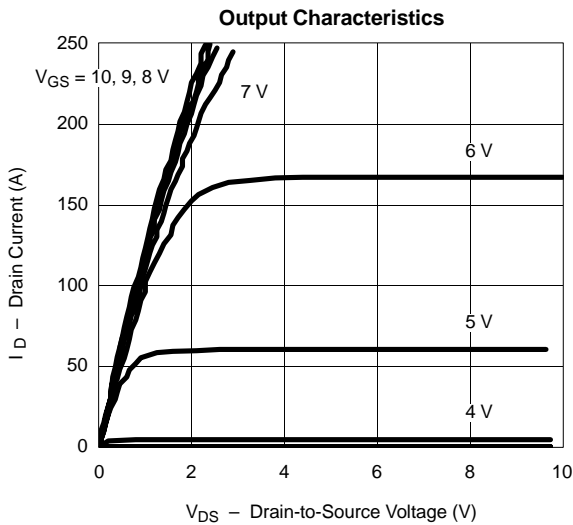


SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	3.0	4.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	120			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		0.007	0.008	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C			0.012	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C			0.016	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	30			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		4800		pF
Output Capacitance	C <sub>oss</sub>			910		
Reverse Transfer Capacitance	C <sub>rSS</sub>			270		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 75 A		85	120	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			28		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			26		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 0.47 Ω I <sub>D</sub> = 75 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 2.5 Ω		20	40	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			95	200	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			65	120	
Fall Time <sup>c</sup>	t <sub>f</sub>			20	60	
<b>Source-Drain Diode Ratings and Characteristics (T<sub>C</sub> = 25 °C)<sup>b</sup></b>						
Continuous Current	I <sub>S</sub>				75	A
Pulsed Current	I <sub>SM</sub>				240	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V		1.0	1.3	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 75 A, di/dt = 100 A/μs		67	120	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			6	8	A
Reverse Recovery Charge	Q <sub>rr</sub>			0.2	0.48	μC

Notes

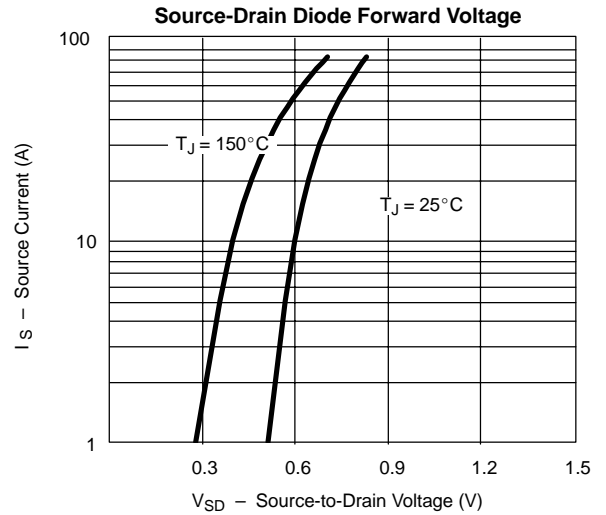
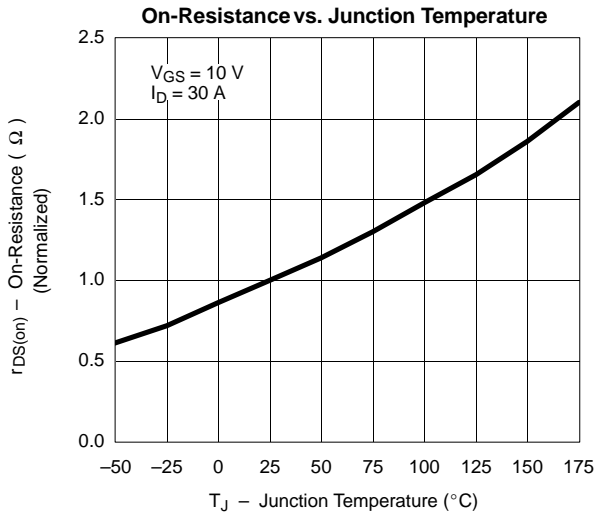
- a. Pulse test: pulse width ≤ 300 μsec, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**





**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**THERMAL RATINGS**

